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RESEARCH ARTICLE

An Adjustable Gate Driver Based on the Optimization of Switching Transient Performances

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ABSTRACT An adjustable gate driver is proposed based on the optimization of switching transient performances. The turn-on process is optimized through an adjustable charging current, while the turn-off process is optimized through an adjustable segmented drive current. The proposed gate drive circuit has the advantage of reducing switching loss, delay, and total switching time, while maintaining the switching stress and EMI noise level during both turn-on and turn-off transients. The proposed driver can be integrated into gate driver ICs, and the switching performance can be externally adjusted to match the power device for different applications. By combining the above techniques, an adjustable gate driver IC has been developed using the 0.25μm BCD process. The simulated and experimental results validate the proposed technique. Compared to the conventional gate driver, the overshoot voltage has been reduced from 15.4% to 8.3%, and the overshoot current has decreased from 20.5% to 10.2% under a 10A load condition.

INDEX TERMS Gate driver, overshoot voltage, switching transient.

I. INTRODUCTION

Power MOSFET devices play a significant role in power applications due to their high current, voltage capability. The performance and reliability of power MOSFETs are directly related to their gate drive circuits [1], [2], [3]. Many researches [4], [5], [6], [7], [8], [9], [10], [11], [12], [13], [14], [15], [16], [17], [18] have been done, mainly based on the consideration of switching speed, switching loss, overshoot current, overshoot voltage, and electromagnetic interference (EMI). Fast switching speeds produce higher current overshoot, voltage overshoot, and EMI, while slow switching speeds produce longer switching delays and higher switching losses [4]. As a result, there is a trade-off between overshoots and losses in the design of gate drivers [5].

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The conventional drive circuit employs a larger gate resistance (R_{on}) to switch the power device on, and a lower gate resistance (R_{off}) to switch the power device off [6]. This compromise method is relatively simple, and cannot meet the requirements for higher switching performance. A gate driver circuit with adjustable gate resistance is proposed in [7]. The specific optimization method involves using a large gate resistance to suppress the reverse recovery current when the external power switch current rises, and a small gate resistance to control the decline rate when the external power switch drain and source voltage drops, so as to reduce the turn-on loss. However, the method of adjusting the gate resistance is rough, and the resistance is generally only adjusted once during a single switching process, making it challenging to optimize both the switching on and switching off simultaneously. Similar gate drivers with a gate resistance adaptation to different switching stages were presented in [8], [9], [10], and [11], these methods require a complex circuit implemen-

tation and are inflexible for use in different devices. A gate driver with adjustable gate voltage based on drain voltage detection was proposed in [12]. By comparing the drain voltage of the external power device with the reference voltage, the gate drive voltage is adjusted based on the comparison voltage result to achieve the purpose of adjusting di/dt and dv/dt. However, this drain detection circuit requires a high-voltage circuit, and the detection circuit is also relatively complex. The optimizing circuits cannot be integrated on a chip;

In the existing technology, there are also many control methods based on di_C/dt and dv_{CE}/dt closed-loop detection to optimize the switching process [13], [14], [15], [16], [17], [18]. However for closed-loop control, it is challenging to control detection accuracy, and there must be a certain feedback delay. Both detection accuracy and feedback delay significantly impact the performance of the gate driver and the detection circuit, making it difficult to adjust and optimize. Furthermore, the gate driver cannot be integrated on a chip.

This paper proposes an adjustable gate driver circuit based on the transient characteristics of the gate-source voltage, which effectively solves the above problems. The optimized circuit is simple, externally adjustable, and can be integrated onto the chip to directly drive the power devices. Compared to the traditional gate drive circuit, this circuit can effectively suppress the current and voltage overshoot, reduce current and voltage peaks, improve electromagnetic interference characteristics, optimize switching characteristics, and enhance system safety.

II. ARCHITECTURE AND CIRCUIT DESIGN

This paper presents an adjustable gate driver that can be integrated on a chip. The block diagram of the adjustable gate driver IC is shown in Fig.1. The circuit mainly includes a turn-off optimizer, a turn-on optimizer, a reference circuit, an under-voltage protection circuit, a power-on reset circuit, a Schmitt circuit, a comparator circuit, and output-level series-connected NMOS transistors MN1 and MN2. The turn-on and turn-off processes are optimized using the turn-on optimizer and the turn-off optimizer, respectively. In this scheme, two NMOS transistors are used to drive external power MOSFETs, and the upper NMOS is controlled by the internal bias current in the turn-on optimizer. By adjusting the bias current and the gate-source capacitance of MN2, the turn-on performance of external power devices can be optimized. By detecting the gate drive voltage, the drive current of MN1 is controlled in two stages, enabling segmented control of the gate drive current of the external power MOSFETs. The internal drive current can be externally adjusted, making it easy to optimize the switching transient of the power MOSFETs.

A. TURN-ON OPTIMIZER

Fig.2 illustrates the circuit implementation of the turn-on optimizer, which mainly includes an operational amplifier, an adjustable bias circuit, and a current amplifier circuit.

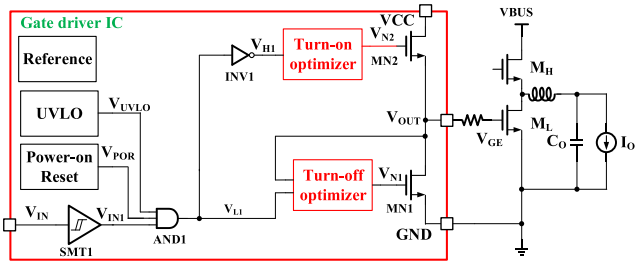

FIGURE 1. Block diagram of the proposed adjustable gate driver IC.

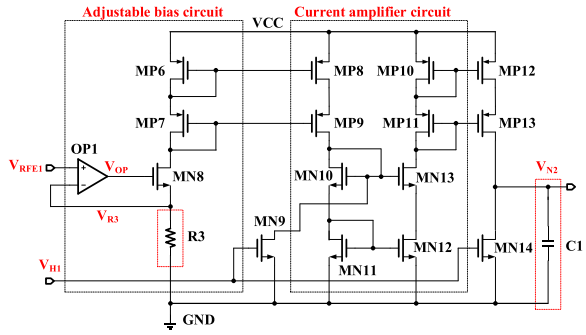

FIGURE 2. The circuit implementation of the turn-on optimizer.

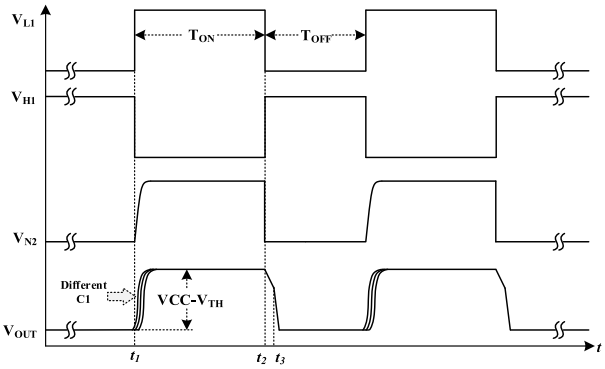

FIGURE 3. Turn-on waveform of proposed circuit.

V_{REF1} is the reference voltage inside the chip, and V_{H1} is the inverse of the input signal V_{IN}. The initial bias current I_{R3} is set through the reference voltage V_{REF1} and resistance R3, as shown in (1);

$$I_{R3} = \frac{V_{REF1}}{R_3} \tag{1}$$

After the initial bias current is amplified by the current amplifier circuit, the drive current capacity of V_{N2} is expressed as

$$I_{ON} = \frac{V_{REF1} N_2 N_3 N_4}{R_3} \tag{2}$$

where N2 represents the width-to-length ratio of MP8 to MP6; N3 represents the ratio of the width to length ratio of MN13 to MN10; and N4 represents the width-to-length ratio of MP13 to MP11.

V_{H1} controls the opening and closing of the adjustable bias circuit, and therefore the turn-on and turn-off of MN2.

The turn-on waveforms of the proposed method are shown in Fig.3. At a time just prior to t_1, V_{L1} is at a low level,

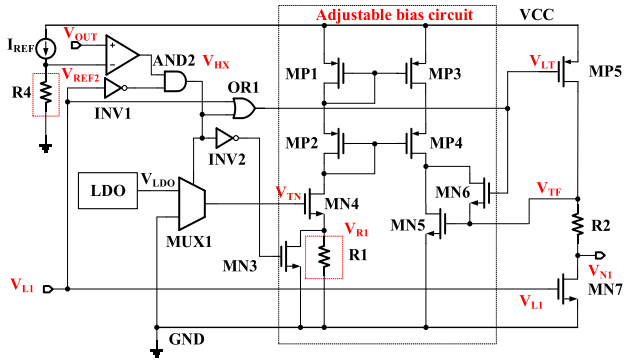

FIGURE 4. The circuit implementation of the turn-off optimizer.

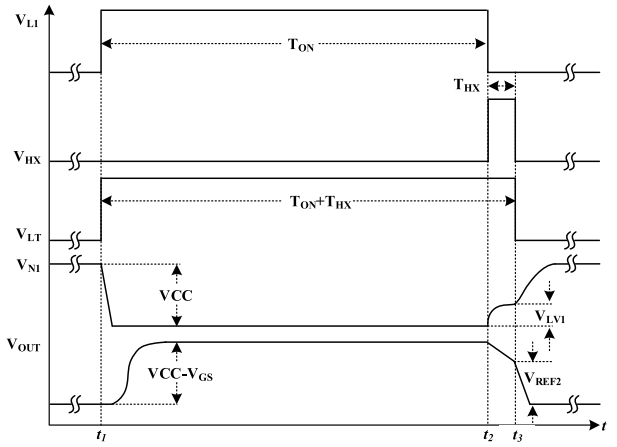

FIGURE 5. Turn-off waveform of proposed circuit.

and V_{H1} is at high level. When the adjustable bias circuit is turned off, MN14 turns on, and V_{N2} is at a low level. At time t_1 V_{L1} changes from a low level to a high level, V_{H1} changes to a low level. After time t_1, the output signal V_{N2} is increasing towards a high level, and the gate voltage of MN2 is slowly increasing towards a high value. Due to the influence of capacitor C1, V_{N2} slowly rises to a high level. Thus, the output V_{OUT} of the driver rises smoothly to the high output level, which is approximately V_{CC}-V_{TH}. The conduction speed of the internal MN2 is adjusted by changing the size of the resistance R3 and the capacitor C1. As a result, the turn-on transient of the external power MOSFETs can be optimized.

B. TURN-OFF OPTIMIZER

The turn-off optimizer is shown in the Fig.4. V_{L1} is the driving signal of the lower tube MN1, and V_{HX} is a narrow pulse signal t_{HX} which represents the short-time output V_{OUT} higher than V_{REF2} after the external MOSFET is turned off. The drive signal V_{LT} increases a narrow pulse width t_{HX} based on the V_{L1} pulse width. First, the MUX1 circuit and bias circuit are controlled by a narrow pulse signal. MUX1 outputs the LDO voltage and turns MN4 on. During the pulse time t_{HX}, the drive signal V_{N1} rises to a value V_{LV1} that is slightly higher than the threshold voltage of MN1. During

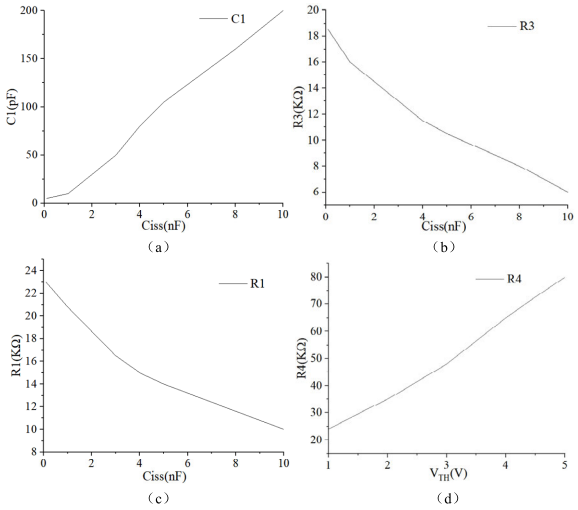

FIGURE 6. The variation of adjustable parameters with input capacitance and threshold voltage. (a) C1 versus Ciss. (b) R3 versus Ciss. (c) R1 versus Ciss. (d) R4 versus V_{TH}.

TABLE 1. Main parameters for gate driver.

Parameters	Value	Parameters	Value
Gate drive Voltage	12V	Gate resistance	5Ω
R1	14kΩ	R4	40kΩ
R3	14kΩ	V_{BUS}	48V
C1	100pF	Frequency	10KHz

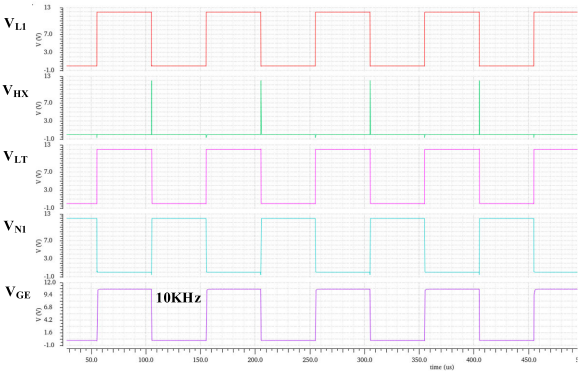

FIGURE 7. Simulated switching waveforms of proposed circuit.

the internal V_{N1} is driven by the adjustable bias circuit, and V_{OUT} decreases gradually. After the narrow pulse signal, the bias circuit is turned off, causing V_{LT} to become a low level. Subsequently, the voltage V_{N1} is rapidly raised to the VCC voltage by MP5. The external power device is powered by a higher current to enable rapid shutdown.

The turn-off optimizer regulates the turn-on drive current of the MN1 during the narrow pulse width period. Then MN1 is rapidly switched on after the internal. As a result, the circuit can reduce the overshoot voltage and EMI during turn-off transients.

The turn-off waveform of the proposed method for optimizing turn-off transient is shown in Fig.5. At the time prior to t_2, V_{L1} is at a high level and V_{N1} is at a low level. At time t_2, V_{L1} changes from a high level to a low level, V_{HX} produces

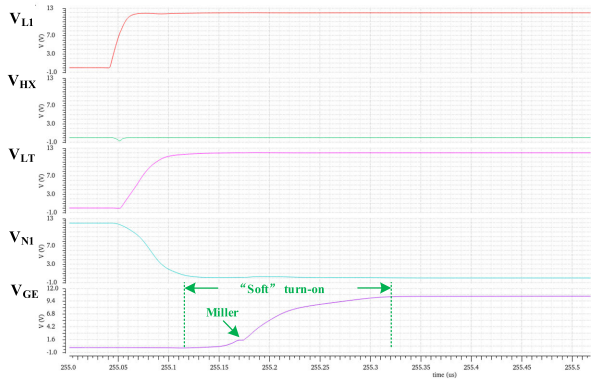

FIGURE 8. Simulated turn-on waveforms of proposed circuit.

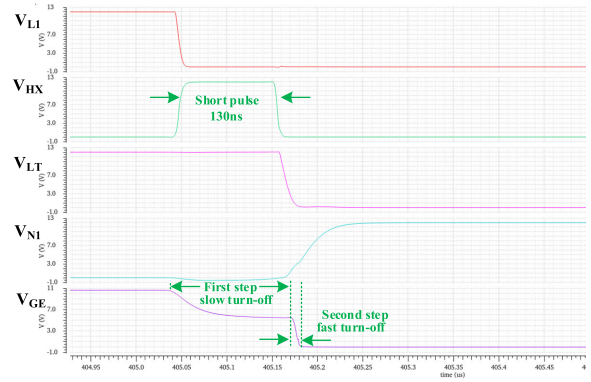

FIGURE 9. Simulated turn-off waveforms of proposed circuit.

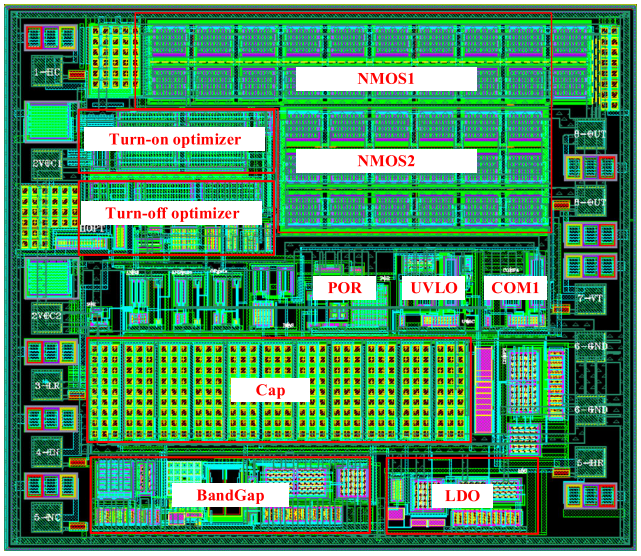

FIGURE 10. The layout of proposed circuit.

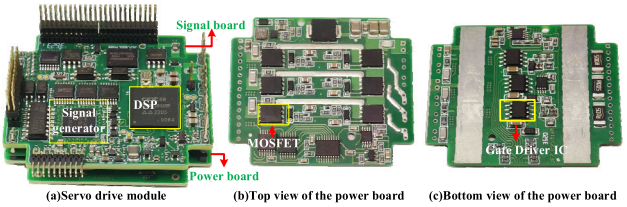

FIGURE 11. Photograph of servo drive module based on proposed gate driver.

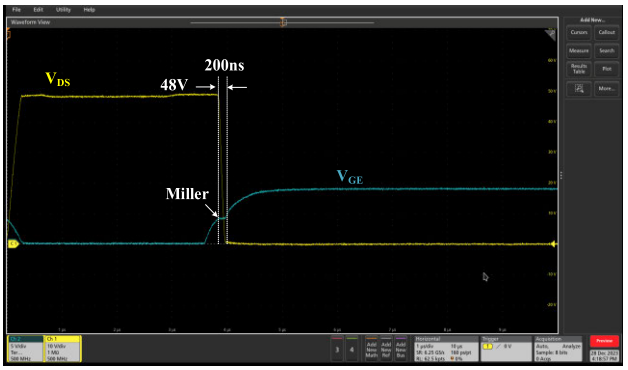

FIGURE 12. Measured turn-on waveforms of proposed gate driver.

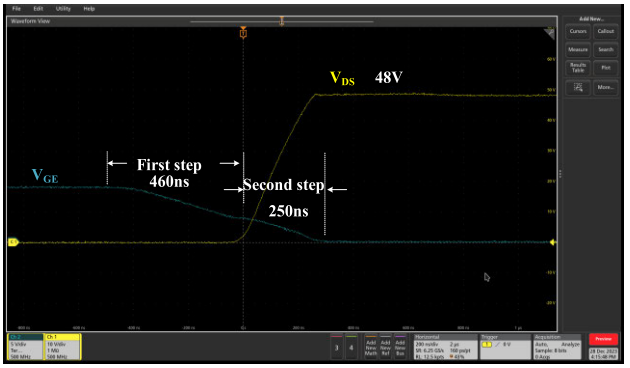

FIGURE 13. Measured turn-off waveforms of proposed gate driver.

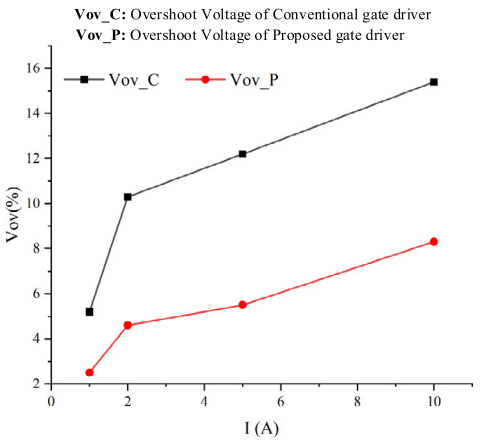

FIGURE 14. Measured overshoot voltage of proposed gate driver compared with conventional gate driver.

a narrow pulse signal with a pulse width of T_{HX}. During this pulse time, V_{N1} rises and remains at a low level voltage V_{LV1}, causing the output V_{OUT} signal of the driving circuit to drop gradually. At time t_3, the V_{HX} pulse signal becomes low and the V_{LT} signal also becomes low. As a result, V_{N1} rapidly rises to VCC, and the output signal V_{OUT} of the driver circuit rapidly declines to zero with a steeper slope. Actually, there is a delay not displayed in the figure between the driver output signal and the V_{N1} signal. This delay is caused by the response time of the internal comparator and other circuits.

Consequently, in the first stage, the external power MOSFET ML is in a slow discharge state, which effectively reduces the overshoot voltage and di/dt during the turn-off.

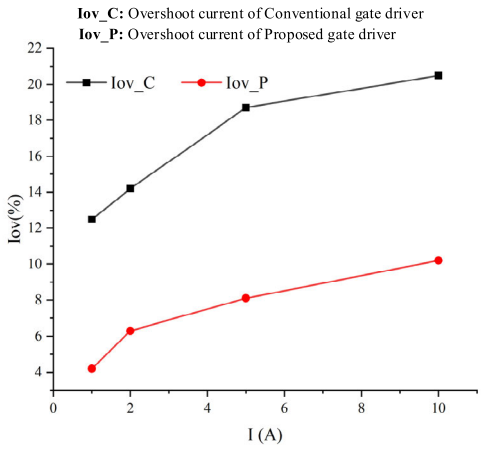

FIGURE 15. Measured overshoot current of proposed gate driver compared with conventional gate driver.

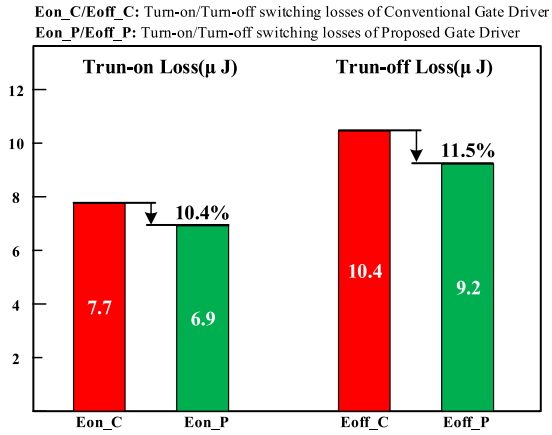

FIGURE 16. Measured switching loss of proposed gate driver compared with conventional gate driver.

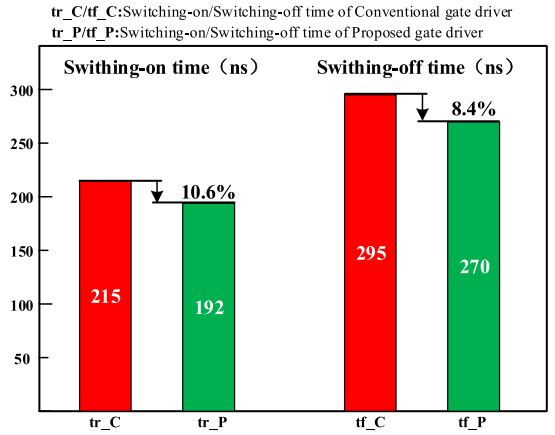

FIGURE 17. Measured switching time of proposed gate driver compared with conventional gate driver.

In the second stage, the ML is in the fast discharge state, which accelerates the turn-off process of the external MOSFETs and reduces the switching loss.

C. ANALYSIS OF ADJUSTABLE PARAMETERS

This paper proposes separate optimization processes for turn-on and turn-off operations, with the ability to externally adjust the optimization parameters. During the turn-off transient, the drive voltage of the NMOS device on the low side of the internal output stage is controlled to achieve segmented switching off current. During the turn-on transient, the optimization of the external power device's switching is achieved by controlling the gate drive current and the gate-source capacitor of the upper NMOS in the output stage.

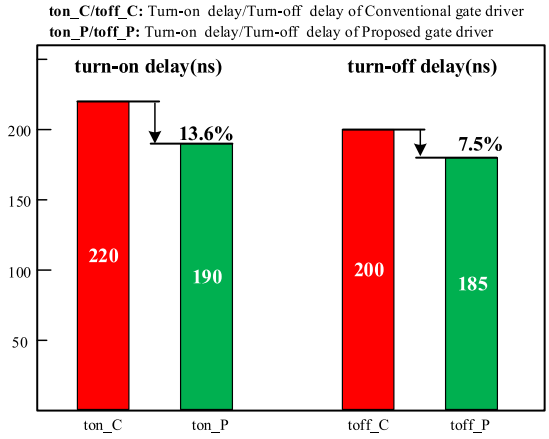

FIGURE 18. Measured propagation delay of proposed gate driver compared with conventional gate driver.

The drive current of the inner upper tube MN2 can be adjusted by changing the size of the resistance R3. In addition, the turn-on speed of the upper tube MN2 can be adjusted by changing the size of the capacitor C1. Therefore, the switching speed of the external power device is adjusted.

The narrow pulse width can be adjusted by changing the size of resistor R4 which determines the value of V_{REF2}. During the V_{HX} pulse width, the drive current of inner MN2 can be adjusted by resistor R1. Therefore, the turn-off performance of the external power device is optimized by resistors R1 and R4.

The resistors R1, R3, R4, and capacitor C1 in the circuit can be placed outside the drive ICs. By modifying these devices, the optimization circuit can adapt to different power devices. According to the requirements of the drive system for the drive speed, these parameters can be adjusted appropriately with changes in input capacitance and threshold voltage of power MOSFETs, and the corresponding reference value is shown in Fig.6. The resistors R1, R3, and capacitor C1 are mainly related to the size of the input capacitance. The resistors R4 is mainly related to the threshold voltage of the power device.

III. SIMULATION RESULTS AND MEASURED RESULTS

The proposed gate driver is implemented using the 0.25μm BCD process. The main specifications and key adjustable parameters of the driving chip are shown in Table 1.

The overall simulation waveforms are shown in Fig.7. The turn-on transient waveforms are shown in Fig.8. The turn-off transient waveforms are shown in Fig.9. The power for gate drive is 12V. The pulse width is related to the magnitude of the load. The voltage V_{GE} represents the gate-to-source voltage of external MOSFETs. The simulation waveform indicates

that the switching process of the power MOSFETs is smooth, with very low stress.

Fig.10 shows the layout of proposed gate driver IC, which is implemented on 0.25μm BCD process. The turn-on optimizer, turn-off optimizer, reference circuit, and LDO are included in the driver IC.

The driver IC is used in 48V servo drive system. The driver module based on the chip design is shown in the following Fig.11. The servo driver module is mainly composed of a power board and a signal board. The measured waveforms of the gate voltage and the drain voltage of power MOSFETs are shown in Fig.12 and Fig.13. The drive waveforms are very smooth, without any voltage oscillation.

The overshoot voltage and current compared with conventional driver ICs (IR2308) are shown in Fig.14 and Fig.15. The overshoot voltage and current decrease significantly under various load conditions. Therefore, the proposed gate driver technology significantly reduces the EMI typically created by gate drivers.

The comparisons of the switching loss and switching time of power MOSFETs under a 3A load are shown in Fig.16 and Fig.17. The comparisons of the turn-on delay and turn-off delay for a load capacitance of 1nF are shown in Fig.18. It is clearly noticeable that the switching loss, delay, and switching time are reduced in the proposed gate driver.

IV. CONCLUSION

In this paper, an adjustable gate driver that is adaptive to different power devices is proposed to optimize the turn-on and turn-off processes, respectively. The proposed gate drive circuit aims to reduce switching loss and delay while maintaining switching stress and EMI noise levels during both turn-on and turn-off transients. Based on the 0.25μm BCD process, the gate driver IC has been implemented. Compared to the conventional gate driver, the proposed gate driver has significantly lower stress and negligible EMI.

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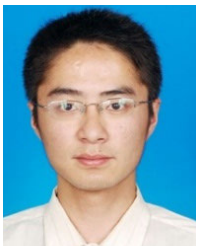

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