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RESEARCH ARTICLE

RF Performance Benchmark of Nanosheets, Nanowires, FinFETs, and TreeFETs

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ABSTRACT RF array performance of stacked nanosheets, stacked nanowires, FinFETs, and TreeFETs are optimized using double-sided gate contact, contact over active-gate, and proposed hybrid layouts. For the double-sided gate contact, gate resistance increases with the increasing active region width to decrease the maximum oscillation frequency. The gate vias on the active region of contact over active-gate can reduce gate resistance by providing vertical paths for small-signal gate current. Combining the advantages of double-sided gate contact and contact over active-gate, the hybrid can further reduce the gate resistance to improve the maximum oscillation frequency. FinFETs/TreeFETs with the vertical sections of the channel (fin/interbridge) stop the lateral small-signal gate current path to increase gate resistance and thus decrease the maximum oscillation frequency as compared to nanosheets and nanowires. Nanowires adopting the hybrid layout and gate length of 18nm can achieve the highest maximum oscillation frequency of 590GHz due to the lowest gate resistance, the highest electron concentration, and the best gate control.

INDEX TERMS RF, 5G mm-Wave, 6G, FinFET, nanosheet, nanowire, TreeFET, gate-all-around, cut-off frequency, maximum oscillation frequency.

I. INTRODUCTION

6G wireless communication with a carrier frequency range from 95GHz to 3THz needs beamforming with numerous low-noise amplifiers and power amplifiers to improve effective isotropic radiated power and reduce power consumption [1], [2], [3]. Many sets of circuits to transmit and receive signals in different frequency ranges are also necessary to support the wide carrier frequency range operations. Thus, the RF performance of transistors becomes critical for such high-frequency operation to achieve high-efficiency wireless applications. Cost-effective CMOS technology with high transistor density is suitable for beamforming applications of mobile devices. RF performance of FinFET had been investigated [4], [5], [6], [7], [8]. Double-sided gate contact (DS) was proposed to reduce gate resistance (R_g) and to boost maximum oscillation frequency (f_{MAX}) [6], [7]. FinFETs have a better f_{MAX} than the planar MOSFET [4], [5], [6], [7]. However, the cut-off frequency (f_T) of FinFET cannot outperform planar MOSFET [4], [9] due to the low electron mobility of its (110) sidewalls. Gate-all-around (GAA) FETs such as nanosheets (NS) with more (100) top and bottom surfaces than (110) sidewalls can improve f_T and f_{MAX} due to higher electron mobility [10]. Although GAA FETs including stacked NS, stacked nanowires (NW), and TreeFETs [10], [11], [12] have enhanced digital performance, RF performance should also be evaluated including back-end-of-line (BEOL) parasitics [13] and RF transistor array layouts [14], [15]. The noise analysis including the noise figure is also important for low-noise amplifier design since the noise

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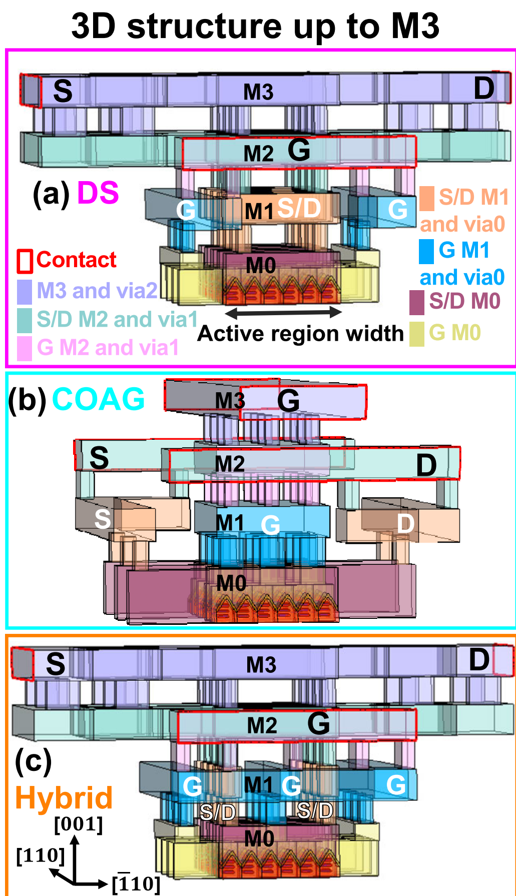

FIGURE 1. Schematics of (a) double-sided gate contact (DS), (b) contact over active-gate (COAG), and (c) proposed hybrid transistor array layouts up to the M3 level. The channel stopper, substrate, and oxides are transparent.

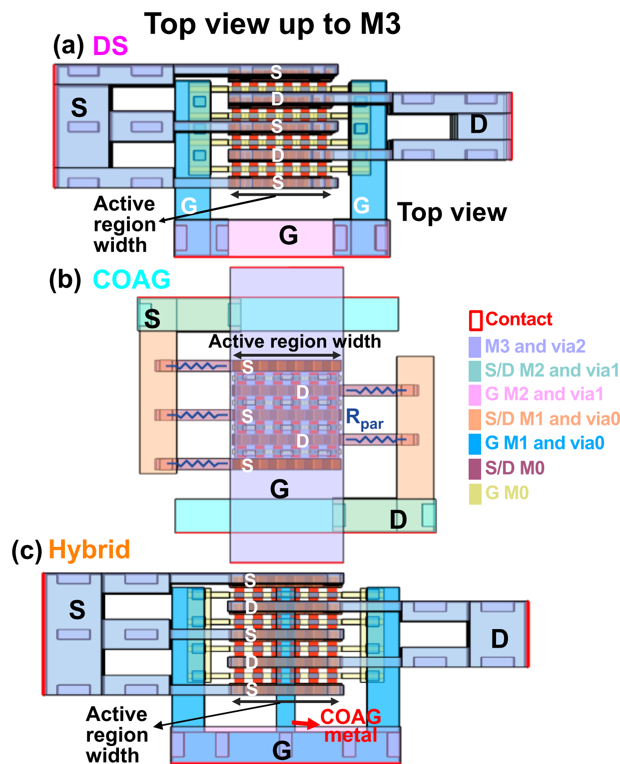

FIGURE 2. Top views of (a) DS, (b) COAG, and (c) hybrid transistor array layouts up to the M3 level. Extended S/D fingers in COAG lead to additional R_{par}.

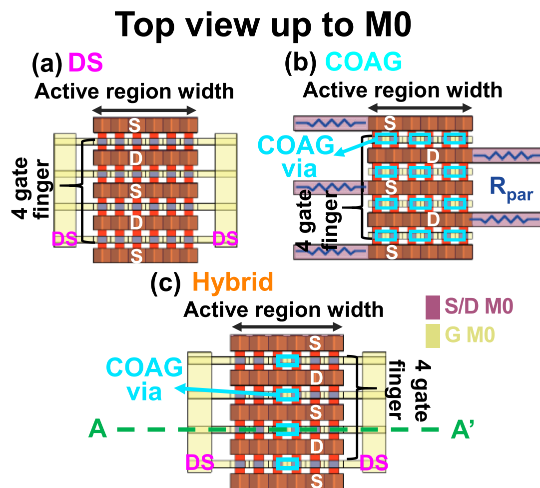

FIGURE 3. Top views of (a) DS, (b) COAG, and (c) hybrid transistor array layouts up to the M0 level. COAG vias are used on top of the gate finger for COAG and hybrid layouts to reduce gate resistance (R_g).

generated by transistors will contaminate the input signal and increase the bit error rate [16], [17]. In this work, the discussion about RF performance is mainly focused on the f_T and f_{MAX} for power amplifier (PA) applications. The DS, contact over active-gate (COAG), and proposed hybrid layouts up to the M3 level are used in TCAD [18] (Fig. 1(a)(b)(c)) to simulate f_T and f_{MAX} with the active region widths of 290 and 480nm.

Note that different active region widths are used to simulate the influence of transistor array sizes on RF performance. For DS and hybrid, the Source/Drain (S/D) metal connections are above the active region. The difference between DS and hybrid is the added COAG metal at the M1 level (Fig. 2(a)(c)). For COAG, S/D metal connections are extended at both sides of the active region (Fig. 2(b)), leading to additional parasitic resistance (R_{par}) and degrading the RF performance.

M0 gate contacts of the DS layout are located at both sides of the active region (Fig. 3(a)), while gate vias of the COAG layout are distributed evenly on the active region (Fig. 3(b)). For the hybrid layout, added COAG metal as compared to DS is used to connect COAG vias to the M1 level (Fig. 3(c)).

M0 metal lines are W, while the V0 vias and above are Cu. Device structure parameters, BEOL metal heights, and via heights are listed in Table 1. The undoped channel and [P] = 1e20cm^{-3} in S/D are used. The BEOL includes 2 drain fingers, 3 source fingers, and 4 gate fingers (Fig. 3). The device parameters such as contact gate pitch (CGP), gate length (L_g), spacer length (L_{sp}), S/D length (L_{SD}), and BEOL are the same for 4 kinds of transistors. Note that diamond-shaped S/Ds with {111} facets are used for 4 kinds of transistors. The vertical stack number (floor#) for NSs and NWs is 3. The suspension thickness (T_{SUS}) is the vertical distance between adjacent channels, and the vertical offset is

TABLE 1. Geometric parameters of RF transistor array.

Gate finger number	4	S/D length (L_{SD})	40nm
Lateral stack number (Lateral stack#)	6/10/16	Spacer length (L_{SP})	16nm
		Equivalent oxide thickness (EOT)	0.8 nm
Active region width	290/ 480nm	Vertical offset	12nm
		NS width	25nm
Contact gate pitch (CGP)	90nm	NS thickness	5nm
		NW diameter	5nm
S/D M0 height	120nm	Suspension thickness (T_{SUS}) / Interbridge height (H_{IB})	7nm
Gate M0 height (H_{gate})	80nm		
via0/via1/via2 height	65nm		
M1/M2/M3 height	70nm	Interbridge width (W_{IB})	5nm
Gate length (L_g)	18 [13] nm	Fin height	40nm
		Fin width	8nm

the distance between the bottom of the lowest channel and the top of the channel stopper. For TreeFET, the channel consists of 3 vertically stacked NS and 2 interbridges in between. To compare the structure advantages, the interbridge height (H_{IB}) is set to be the same as T_{SUS}. The {001} wafer and <110> current orientations are assumed for NS, NW, FinFET, and TreeFET.

II. CALIBRATION INCLUDING BEOL

The DS layout up to the M3 level using FinFET with the fin pitch of 48nm and fin width of 8nm was calibrated to foundry SPICE with errors <2.5% for f_T, f_{MAX}, transconductance (g_m), output conductance (g_d), total gate capacitance (C_{gg}), gate-to-drain capacitance (C_{gd}), and on current (I_{on}) in our previous work [13]. Thus, the BEOL parasitics are correctly included in our simulation. Transfer characteristics of FinFET SPICE [13], experimental NSs [19], and experimental NWs [20] are used to extract mobility (μ) considering the Masetti mobility model with doping dependence [21] in our previous works (Fig. 4(a)) [13], [14], [15]. μ_{NS}, μ_{NW}, and μ_{FinFET} are 360, 260, and 220cm^2/V/s, respectively. The order of mobilities ($\mu_{NS} > \mu_{NW} > \mu_{FinFET}$) is the same as calculated mobilities considering specular surface scattering governed by energy and parallel–momentum conservation without surface roughness scattering [22] and calculated injection velocity for short-channel devices [23]. Note that the same μ_{NS} of NS and TreeFET are used to compare the device architecture.

III. CHANNEL GEOMETRY DEPENDENCE

The COAG can reduce R_g and improve the RF performance of FinFET with $f_T = 320$GHz and $f_{MAX} = 350$GHz at the optimized fin pitch of 28nm, the active region width of 290nm, and $V_{DD} = 0.8$V (Fig. 4(b)). C_{gg} and C_{gd} are extracted by small-signal AC simulation at $V_{GS} = V_{DS} = 0.8$V. In addition, f_T and f_{MAX} are extracted from the simulated current gain and Mason's unilateral gain (G_U), respectively, at 90 GHz with −20 dB/dec extrapolations following the measurement method [24]. Note that G_U is calculated from admittance parameters [25].

The simulated electron concentrations near the centers are lower than the edges of FinFET (Fig. 5(a)), NS (Fig. 5(b)),

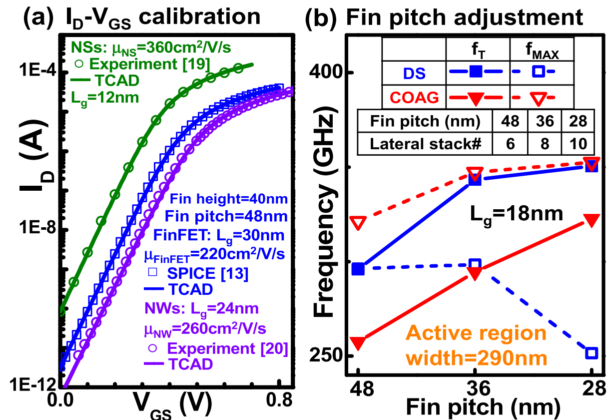

FIGURE 4. (a) Calibrated I_D-V_{GS} of FinFET, stacked NSs, and stacked NWs. (b) Fin pitch optimization with different lateral stack numbers (stack#) to improve RF performance at the similar footprint. The mobility (μ) is extracted using the Masetti mobility model [21].

and TreeFET (Fig. 5(c)). For FinFET, the high carrier density region is located at the fin top. For NS, the high carrier density regions are at both channel edges. For TreeFET, the interbridges further reduce the carrier amount in the middle of the NS channels. Thus, NW with the highest average electron concentration, 3.8X as compared to FinFET, in the channel among 4 kinds of transistors (Fig. 5(d)(e)) can achieve only 15% g_m reduction to NS (Fig. 6(a)) although NW has the lowest effective channel width ($W_{eff} = 470$nm) as compared to the FinFET/NS/TreeFET (850/1000/1050nm) at the active region width of 290nm. Note that W_{eff} is equal to the total channel peripheral width. Besides, NW with the smallest channel cross-section can achieve > 60% g_d reduction as compared to the other 3 transistor architectures due to the best gate control. Thus, TreeFET with the highest g_m in 4 kinds of transistors can improve f_T, while NW with the smallest g_d can improve f_{MAX} according to the f_T and f_{MAX} formula (Fig. 6). 3 types of BEOL have similar g_m and g_d with an active region width of 290nm (Fig. 6(a)). However, for the active region width of 480nm with a larger I_{on} than 290nm, COAG has the lowest g_m due to additional R_{par} from the extending S/D fingers outside the active region in the M0 level (Fig. 3(b)). Note that the S/D connections of DS and hybrid are above the active region without extending S/D fingers (Fig. 3(a)(c)), leading to lower R_{par} than COAG.

IV. BEOL LAYOUT COMPARISON

The gate finger cross-sections are investigated with the same active region width by adjusting lateral stack numbers (lateral stack#) (Fig. 7) with the fixed lateral spacing of 23nm (Fig. 7(a)). For DS, the gate contacts are located at both sides. Thus, the distance from gate contacts to transistors becomes larger as the lateral stack order of NS increases from 1 (left side of the active region) to 3 (the middle of the active region) in Fig. 7(a). This leads to the R_g increase from the lateral stack order of 1 (left side of the active region) to 3 (the middle of the

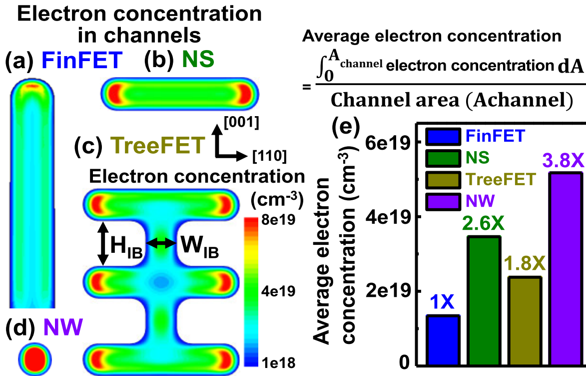

FIGURE 5. Electron concentration profile of (a) FinFET, (b) NS, (c) TreeFET, and (d) NW in channels at $V_{OV} = V_{GS} - V_T = 0.5V$. The simulated electron concentrations near the centers are lower than the edges of FinFET, NS, and TreeFET. (e) Average electron concentration comparison of NS, NW, FinFET, and TreeFET with the active region widths of 290 and 480nm. NW with the smallest channel cross-section can achieve the highest average electron concentration due to the best gate control.

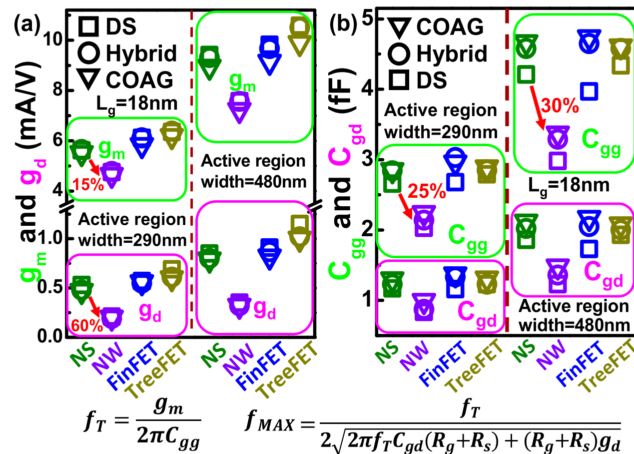

FIGURE 6. (a) Conductance and (b) capacitance comparison of NS, NW, FinFET, and TreeFET with the active region widths of 290 and 480nm. NW can achieve only a 15% g_m decrease and a 60% g_d decrease as compared to NS due to the highest average electron concentration and smallest channel cross-section in Fig. 5. NW can also achieve ≥25% C_{gg} decrease as compared to NS due to the smallest W_{eff}.

active region) in Fig. 8(a). Note that the lateral stack number (lateral stack#) of NS is 6 at the active region width of 290nm and the gate finger is symmetric. Thus, the NS lateral stack order of 6 is located at the right side of the active region at the active region width of 290nm.

As the active region width increases from 290nm to 480nm, the DS gate contacts are still located at both sides of the active region, leading to a longer distance from gate contacts to the transistor located in the middle of the active region. As a result, the increase of R_g values from transistors located at both sides to those located in the middle of the active region becomes larger at the active region width of 480nm than 290nm. Besides, FinFET and TreeFET with vertical sections of channel (fin and interbridge) stop the lateral small-signal gate current path (Fig. 7(c)(f)), leading to the larger R_g increase (Fig. 8(c)(d)(g)(h)) than NS and NW (Fig. 8(a)(b)(e)(f)) in the middle of the active region. However, gate metal between vertically stacked channels of

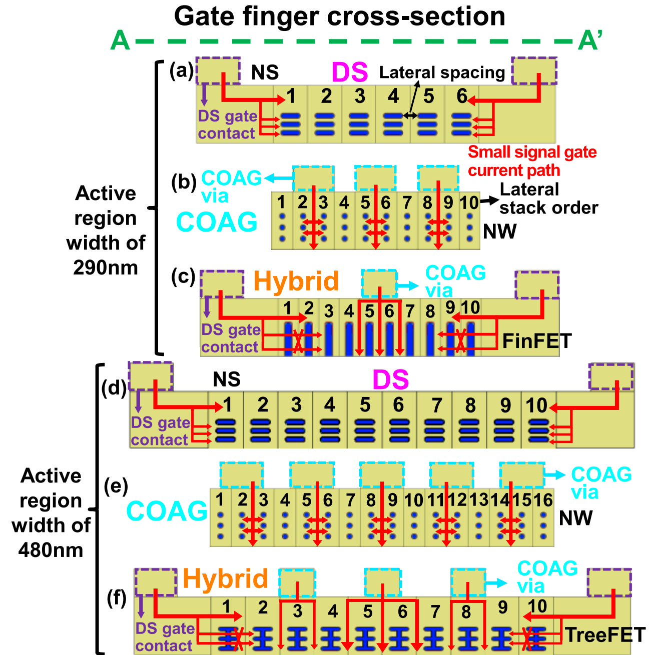

FIGURE 7. The gate finger cross-section in Fig. 3 with active region widths of (a)(b)(c) 290 and (d)(e)(f) 480nm using (a)(d) NS, (b)(e) NW, (c) FinFET, and (f) TreeFET. The same BEOL and lateral spacing are assumed. The vertical small-signal gate current can be provided by COAG vias to reduce R_g in COAG and hybrid layouts.

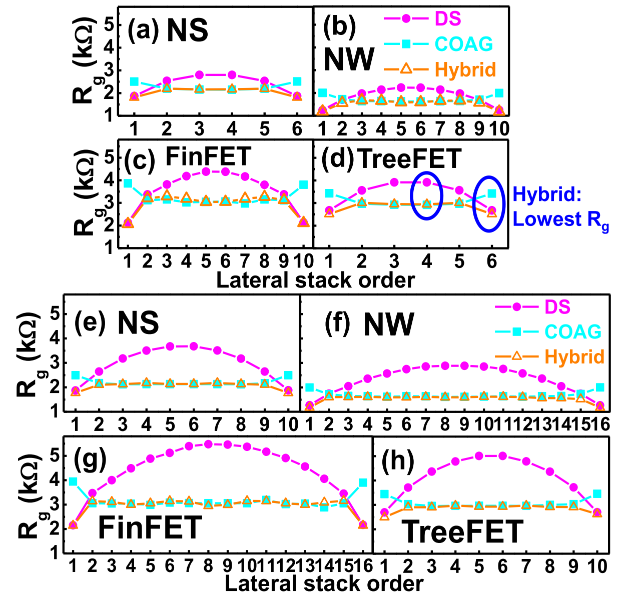

FIGURE 8. R_g distribution in different lateral stack orders with the active region widths of (a)(b)(c)(d) 290 and (e)(f)(g)(h) 480nm. The lateral stack order starts from left to right in the active region (Fig. 7). With the vertical small-signal gate current paths by COAG vias in COAG and hybrid layouts (Fig. 7(b)(c)(e)(f)), R_g in the middle of the active region decreases as compared to DS.

NS and NW (Fig. 7(a)(b)(d)(e)) can mitigate the R_g increase (Fig. 8(a)(b)(e)(f)).

For COAG, the gate contact vias are evenly distributed on the gate fingers, and the gate contacts at both sides are removed. The vertical small-signal gate current path from top COAG vias to bottom channels can reduce R_g from DS in the middle of the active region (Fig. 8), leading to R_g reduction of

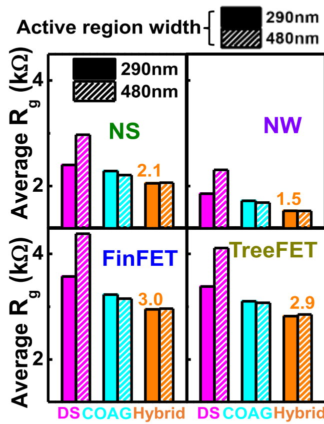

FIGURE 9. Average R_g comparison of NS, NW, FinFET, and TreeFET with the active region widths of 290 and 480nm. The average R_g value is calculated from the sum of the R_g value for each channel divided by the total channel number.

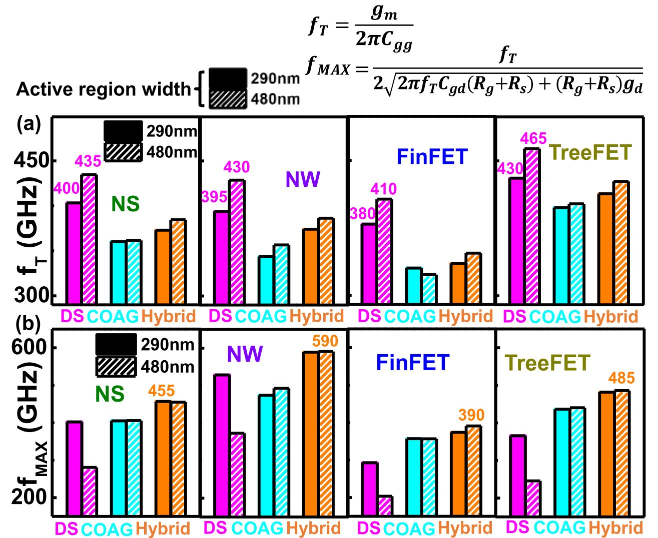

FIGURE 10. (a) f_T, and (b) f_{MAX} comparison of NS, NW, FinFET, and TreeFET with the active region widths of 290 and 480nm. The hybrid can achieve the highest f_{MAX} in 3 types of layouts. NW with the hybrid layout can achieve the highest f_{MAX} due to the lowest R_g, highest electron concentration, and best gate control.

4 kinds of transistors as compared to DS (Fig. 9), especially for active region width of 480nm. Note that 3 and 5 COAG vias are used in the COAG at the active region widths of 290nm and 480nm, respectively, to reduce the distance between gate contacts to transistors (Fig. 7(b)(e)).

Compared to the COAG, the hybrid removes 2 COAG vias and adds DS gate contacts at both sides of the active region (Fig. 7(c)(f)), leading to R_g reduction at both sides (Fig. 8). 1 COAG via and gate contacts at both sides are used in the gate finger at the active region width of 290nm. In comparison, 3 COAG vias and gate contacts at both sides are used at the active region width of 480nm. The minimum R_g values of hybrid among 3 types of BEOLs can be observed along different lateral stack orders (Fig. 8). Thus, the hybrid layout can achieve the lower average R_g of total channels than DS and COAG in 4 kinds of transistors (Fig. 9), suitable for f_{MAX} improvement. Also, similar R_g values can be achieved by adopting the hybrid layout at active region widths of 290 and 480nm, indicating that the RF performance of the larger RF transistor array will not degrade by R_g. Note that R_g is extracted by simulating the series resistance from gate contacts at the highest gate metal layer to the interface between gate M0 and gate oxide of each channel. The average R_g in Fig. 9 is from the average of R_g values in Fig. 8 with different lateral stack orders.

For capacitance comparison (Fig. 6(b)), NW with the lowest W_{eff} as compared to the FinFET/NS/TreeFET can achieve $\geq$25% C_{gg} reduction due to the lowest intrinsic gate capacitance (C_{ox}). The COAG with the most COAG vias on the gate finger increases the gate-to-S/D overlap area, leading to the highest C_{gg} and C_{gd} among the 3 types of BEOL. The DS without the COAG vias on the gate finger can achieve the lowest C_{gg} and C_{gd} among the 3 types of BEOL. The 4 kinds of transistors under the same layout have similar parasitic gate capacitance (C_{par}) with $<$5% difference (not shown in Fig.). Note that C_{gg} is equal to the sum of C_{ox} and C_{par}.

As a result, the DS has the lowest C_{gg} and highest f_T (Fig. 10(a)) due to no additional C_{par} from COAG vias. The hybrid can have higher f_T than COAG due to fewer COAG vias and less R_{par} due to no extended S/D fingers (Fig. 3(b)). For the comparison between 4 kinds of transistors under the same BEOL, TreeFET has the highest f_T due to the largest g_m in 4 kinds of transistors.

For f_{MAX} comparison, the g_d and R_g should be taken into consideration. The hybrid has the highest f_{MAX} (Fig. 10(b)) as compared to DS and COAG due to the lowest R_g (Fig. 9) at the active region width of 480nm in 4 kinds of transistors. For both hybrid and COAG, the f_{MAX} values are similar at the active region widths of 290 and 480nm due to COAG vias to avoid R_g increase in the larger active region width. For DS, f_{MAX} degrades significantly from the active region widths of 290 to 480nm, which is unsuitable for large transistor array applications. Since the NW has the smallest channel in the gate finger cross-section among 4 kinds of transistors, the R_g can be reduced due to more spacing to fill the gate metal (Fig. 7(b)(e) and Fig. 8) and the g_d can be minimized due to the best gate control (Fig. 6(a)). Consequently, the NW can achieve the highest f_{MAX} among 4 kinds of transistors (Fig. 10(b)). With the hybrid layout, L_g = 18nm, and active region width of 480nm, NW can achieve f_{MAX} = 590GHz. Note that NW still has the largest f_{MAX} if 4 kinds of transistors have the same mobility (260cm^2/V/s).

For 16nm FinFET technology adopting DS transistor array layout, the f_T and f_{MAX} are 215GHz and 251GHz, respectively at the active region width of 290nm [13]. Thus, by optimizing BEOL, FinFET with hybrid BEOL can achieve f_T = 335GHz and f_{MAX} = 375GHz, suitable for FinFET PA applications

For power amplification applications, the transistor array is large and at least has $>$40 transistors (fin number$*$ finger number). Thus, the RF performance at large transistor array size should be examined to check the benefits of BEOL

TABLE 2. RF performance comparison.

Transistor	Active region width	RF performance (f_T and f_{MAX})	TED [13] DS	EDL [14] and VLSI-TSA [15] DS / COAG	Hybrid in this work
NS Floor#=3	290nm	f_T (GHz)	340	400 / 360	375
		f_{MAX} (GHz)	370	405 / 410	455
	480nm	f_T (GHz)	-	435 / 360	400
		f_{MAX} (GHz)	-	280 / 405	455
NW Floor#=3	290nm	f_T (GHz)	-	425 / 400	375
		f_{MAX} (GHz)	-	535 / 540	590
	480nm	f_T (GHz)	-	500 / 410	405
		f_{MAX} (GHz)	-	400 / 545	590
FinFET	290nm	f_T (GHz)	280	-	335
		f_{MAX} (GHz)	280	-	375
	480nm	f_T (GHz)	-	-	350
		f_{MAX} (GHz)	-	-	390
TreeFET	290nm	f_T (GHz)	-	-	415
		f_{MAX} (GHz)	-	-	480
	480nm	f_T (GHz)	-	-	430
		f_{MAX} (GHz)	-	-	485

layout. Compared to previous work [13], [14], [15], the proposed hybrid can achieve the highest f_{MAX}(Table 2). Besides, the f_{MAX} of the hybrid does not decrease and remains the highest among the 3 types of BEOLs as the active region width increases from 290nm to 480nm. Thus, the hybrid BEOL design is suitable for PA applications since the RF performance is not degraded at large sizes of transistor arrays.

V. CONCLUSION

TreeFET with DS layout can have the highest $f_T = 465$GHz at $L_g = 18$nm and an active region width of 480nm. The hybrid layout can reduce R_g and improve f_{MAX} as compared to the DS and COAG layout at the active region width of 480nm, suitable for large transistor array applications. Stacked NW using the hybrid layout with the lowest R_g, lowest W_{eff}, lowest g_d, and highest average electron concentration can achieve the highest $f_{MAX} = 590$GHz with the active region width of 480nm. For real PA circuit design, the power gain with different input powers and carrier frequencies should be provided including matching networks. In future work, the power gain with different input powers will be simulated to check the RF device's ability of power amplification. 3 types of BEOLs combined with NS, NW, FinFET, and TreeFET will be compared in terms of power gain with the carrier frequency ranging from 24GHz to 100GHz.

REFERENCES

[1] W. Hong, Z. H. Jiang, C. Yu, D. Hou, H. Wang, C. Guo, Y. Hu, L. Kuai, Y. Yu, Z. Jiang, Z. Chen, J. Chen, Z. Yu, J. Zhai, N. Zhang, L. Tian, F. Wu, G. Yang, Z.-C. Hao, and J. Y. Zhou, ''The role of millimeter-wave technologies in 5G/6G wireless communications,'' *IEEE J. Microw.*, vol. 1, no. 1, pp. 101–122, Jan. 2021, doi: 10.1109/JMW.2020.3035541.

[2] M. Z. Chowdhury, M. Shahjalal, S. Ahmed, and Y. M. Jang, ''6G wireless communication systems: Applications, requirements, technologies, challenges, and research directions,'' *IEEE Open J. Commun. Soc.*, vol. 1, pp. 957–975, 2020, doi: 10.1109/OJCOMS.2020.3010270.

[3] G. Xu, S. Abu-Surra, W. Choi, D. Huang, N. Sharma, S. Li, and S. Dong, ''THz for 6G communications: Vision and challenges,'' in *Proc. IEEE Int. Solid-State Circuits Conf. (ISSCC)*, Feb. 2022, pp. 1–44.

[4] H.-J. Lee, S. Rami, S. Ravikumar, V. Neeli, K. Phoa, B. Sell, and Y. Zhang, ''Intel 22 nm FinFET (22FFL) process technology for RF and mm wave applications and circuit design optimization for FinFET technology,'' in *IEDM Tech. Dig.*, Dec. 2018, pp. 14.1.1–14.1.4, doi: 10.1109/IEDM.2018.8614490.

[5] H.-J. Lee, S. Morarka, S. Rami, Q. Yu, M. Weiss, G. Liu, M. Armstrong, C.-Y. Su, D. Ali, B. Sell, and Y. Zhang, ''Implementation of high power RF devices with hybrid workfunction and OxideThickness in 22 nm low-power FinFET technology,'' in *IEDM Tech. Dig.*, Dec. 2019, pp. 25.4.1–25.4.4, doi: 10.1109/IEDM19573.2019.8993647.

[6] J. Singh, and J. Ciavatti, K. Sundaram, J. S. Wong, A. Bandyopadhyay, 298 X. Zhang, S. Li, A. Bellaouar, J. Watts, J. G. Lee, and S. B. Samavedam, ''14 nm FinFET technology for analog and RF applications,'' in *Proc. Symp. VLSI Technol.*, Kyoto, Japan, Jun. 2017, pp. T140–T141, doi: 10.23919/VLSIT.2017.7998154.

[7] J. Singh, J. Ciavatti, K. Sundaram, J. S. Wong, A. Bandyopadhyay, X. Zhang, S. Li, A. Bellaouar, J. Watts, J. G. Lee, and S. B. Samavedam, ''14-nm FinFET technology for analog and RF applications,'' *IEEE Trans. Electron Devices*, vol. 65, no. 1, pp. 31–37, Jan. 2018, doi: 10.1109/TED.2017.2776838.

[8] S.-Y. Wu et al., ''An enhanced 16 nm CMOS technology featuring 2nd generation FinFET transistors and advanced Cu/low-*k* interconnect for low power and high performance applications,'' in *IEDM Tech. Dig.*, Dec. 2014, pp. 3.1.1–3.1.4, doi: 10.1109/IEDM.2014.7046970.

[9] N. Margalit, C. Xiang, S. M. Bowers, A. Bjorlin, R. Blum, and J. E. Bowers, ''Perspective on the future of silicon photonics and electronics,'' *Appl. Phys. Lett.*, vol. 118, no. 22, May 2021, Art. no. 220501, doi: 10.1063/5.0050117.

[10] N. Loubet, ''Enablement of next generation high performance nanosheet transistors,'' in *IEDM Tech. Dig.*, Dec. 2020, pp. 1–74.

[11] Y.-C. Liu, C.-T. Tu, C.-E. Tsai, Y.-R. Chen, J.-Y. Chen, S.-R. Jan, B.-W. Huang, S.-J. Chueh, C.-J. Tsen, and C. W. Liu, ''First highly stacked $Ge_{0.95}Si_{0.05}$ nGAAFETs with record I_{ON}=110 μA (4100 μA/μm) at V_{OV}=V_{DS}=0.5 V and high $G_{m,max}$=340 μS (13000 μS/μm) at V_{DS}=0.5 V by wet etching,'' in *Proc. Symp. VLSI Technol.*, Jun. 2021, pp. 1–2.

[12] C.-T. Tu, W.-H. Hsieh, B.-W. Huang, Y.-R. Chen, Y.-C. Liu, C.-E. Tsai, S.-J. Chueh, and C. W. Liu, ''Experimental demonstration of TreeFETs combining stacked nanosheets and low doping interbridges by epitaxy and wet etching,'' *IEEE Electron Device Lett.*, vol. 43, no. 5, pp. 682–685, May 2022, doi: 10.1109/LED.2022.3159268.

[13] H.-C. Lin, T. Chou, C.-C. Chung, C.-J. Tsen, B.-W. Huang, and C. W. Liu, ''RF performance of stacked Si nanosheet nFETs,'' *IEEE Trans. Electron Devices*, vol. 68, no. 10, pp. 5277–5283, Oct. 2021, doi: 10.1109/TED.2021.3106287.

[14] H.-C. Lin, T. Chou, K.-Y. Chiu, S.-R. Jan, C.-C. Chung, C.-J. Tsen, and C. W. Liu, ''RF performance of stacked Si nanosheets/nanowires,'' *IEEE Electron Device Lett.*, vol. 43, no. 7, pp. 1017–1020, Jul. 2022, doi: 10.1109/LED.2022.3179516.

[15] H.-C. Lin, K.-Y. Chiu, C.-W. Yao, T. Chou, T.-Y. Chung, and C. W. Liu, ''BEOL design and RF performance of stacked Si nanosheets and nanowires,'' in *Proc. Int. VLSI Symp. Technol., Syst. Appl. (VLSI-TSA/VLSI-DAT)*, Hsinchu, Taiwan, Apr. 2023, pp. 1–2, doi: 10.1109/VLSI-TSA/VLSI-DAT57221.2023.10134110.

[16] J.-P. Raskin, G. Pailloncy, D. Lederer, F. Danneville, G. Dambrine, S. Decoutere, A. Mercha, and B. Parvais, ''High-frequency noise performance of 60-nm gate-length FinFETs,'' *IEEE Trans. Electron Devices*, vol. 55, no. 10, pp. 2718–2727, Oct. 2008, doi: 10.1109/TED.2008.2003097.

[17] G. Crupi, A. Caddemi, D. M. M.-P. Schreurs, W. Wiatr, and A. Mercha, ''Microwave noise modeling of FinFETs,'' *Solid-State Electron.*, vol. 56, no. 1, pp. 18–22, Feb. 2011, doi: 10.1016/j.sse.2010.10.010.

[18] *TCAD Sentaurus Suite*, document Version T-2022.03, Synopsys, Mountain View, CA, USA, 2022.

[19] N. Loubet et al., ''Stacked nanosheet gate-all-around transistor to enable scaling beyond FinFET,'' in *Proc. Symp. VLSI Technol.*, Jun. 2017, pp. T230–T231, doi: 10.23919/VLSIT.2017.7998183.

[20] H. Mertens et al., ''Vertically stacked gate-all-around Si nanowire CMOS transistors with dual work function metal gates,'' in *IEDM Tech. Dig.*, Dec. 2016, pp. 19.7.1–19.7.4, doi: 10.1109/IEDM.2016.7838456.

[21] G. Masetti, M. Severi, and S. Solmi, ''Modeling of carrier mobility against carrier concentration in arsenic-, phosphorus-, and boron-doped silicon,'' *IEEE Trans. Electron Devices*, vol. ED-30, no. 7, pp. 764–769, Jul. 1983, doi: 10.1109/T-ED.1983.21207.

[22] F. M. Bufler, R. Ritzenthaler, H. Mertens, G. Eneman, A. Mocuta, and N. Horiguchi, "Performance comparison of *n*-type Si nanowires, nanosheets, and FinFETs by MC device simulation," *IEEE Electron Device Lett.*, vol. 39, no. 11, pp. 1628–1631, Nov. 2018, doi: 10.1109/LED.2018.2868379.

[23] D. Jang, D. Yakimets, G. Eneman, P. Schuddinck, M. G. Bardon, P. Raghavan, A. Spessot, D. Verkest, and A. Mocuta, "Device exploration of NanoSheet transistors for sub-7-nm technology node," *IEEE Trans. Electron Devices*, vol. 64, no. 6, pp. 2707–2713, Jun. 2017, doi: 10.1109/TED.2017.2695455.

[24] D. W. Scott, P. C. Chang, D. Sawdai, L. Dang, J. Wang, M. Barsky, W. Phan, B. Chan, B. Oyama, A. Gutierrez-Aitken, and A. Oki, "Sub-micrometer InP/InGaAs heterojunction bipolar transistors with f_T=400 GHz and f_{max} < 500 GHz," in *Proc. Int. Conf. Indium Phosph. Rel. Mater.*, May 2006, pp. 100–103, doi: 10.1109/ICIPRM.2006.1634121.

[25] M. Reisch, *High-Frequency Bipolar Transistors*. Berlin, Germany: Springer, 2003.

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