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RESEARCH ARTICLE

Realization of SVM Methods With Carrier-Based Dipolar PWM for Matrix Converters

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ABSTRACT Considering several space-vector modulation (SVM) methods, this study proposes SVM methods with carrier-based dipolar pulse width modulation (CBDPWM) for matrix converters. The switching patterns of well-known SVM methods are analyzed, and carrier-based modulation (CBM), which uses reference voltages selected from desired output voltages to generalize the PWM theory of two-level inverters, is developed for matrix converters. Moreover, the relationship between SVM and carrier-based dipolar modulation (CBDM) is revealed to generate the switching pattern of SVM methods. The experimental results confirm that arbitrary SVM methods, which require intensive calculations, can be easily realized by the CBDM by adding specified zero voltages and appropriately choosing a particular input phase as a reference.

INDEX TERMS Matrix converters, carrier-based modulation, space-vector modulation.

I. INTRODUCTION

The PWM technique with SVM for matrix converters is a popular and widely used method [1], [2], [3] because it is based on instantaneous output voltage generation and enables various switching patterns. This modulation method is an extension of the space-vector modulation of two-level inverters. In these approaches, a zero vector is chosen to define the PWM mode, while the vector sequence determines the switching sequence. Consequently, there are various techniques for selecting vectors and corresponding vector sequences [4], [5], [6], [7], [8], [9], [10], [11]. The main selection criteria consist of a low branch switching over (BSO), a unity input power factor, a maximum modulation index, a low output current ripple, a low common-mode voltage (CMV), and low switching losses.

The conventional space-vector PWM (SVPWM), as described in [4], is an indirect SVM (ISVM). In this technique, two line-to-line input voltages are chosen in each switching period to obtain the unity power factor. Moreover, this technique selects the vector sequence from vectors of middle line-to-line voltage to vectors of the maximum line-to-line voltage and a zero vector always and chooses the zero vector to give the minimum number of switchings. As a result, BSOs can be reduced from 12 BSOs to 8 BSOs, but in some sectors, simultaneous switching occurs in two phases. This result is equal to 10 BSOs. This problem can be solved by the optimized SVPWM [5] using a new technique to sequence these vectors and choosing a new zero vector to correspond to the minimum number of switchings with 8 BSOs. The zero vectors of SVPWM methods in [4] and [5] are connected to input voltages with the maximum and medium amplitude. It affects a high CMV, so the modified SVPWM [7] is proposed to utilize zero vectors with the minimum amplitude of input voltages only to reduce CMV. This method still keeps the same 8 BSOs and also decreases to only one PWM mode. Considering the vectors in [4], [5], and [7], it is found that the output voltages are generated by the maximum and medium amplitude of input voltages. These methods result in high switching losses. Therefore, the SVPWM method in [8] uses vectors of input voltages with the minimum and medium amplitude to reduce the switching losses by approximately 15 to 35%, but these vectors yield a maximum modulation index of only 0.5. Thus, the direct SVPWM [11] is proposed

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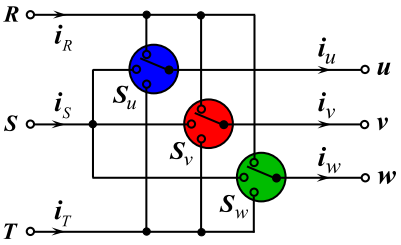

FIGURE 1. Structure of a matrix converter.

to utilize rotating vectors in the case of a modulation index greater than 0.5. As a result, the maximum modulation index can be increased to 0.866.

The SVM approach usually requires active vectors, zero vectors, and appropriate vector sequences, which depend on the input currents and output voltages at that time. The time interval of space-vector switching is obtained by calculating the duty cycle of the rectifier circuit and inverter circuit. Then, the switching signals of each circuit are gathered based on the switching status and switching time interval of the computed space vector. Thus, the SVM requires the execution of complicated duty cycle calculations, and there is no direct connection between the SVM and the desired voltage. Moreover, a look-up table is needed to select the vector for modulation, while the sector of the output voltage and the input voltage are always needed.

Recently, SVMs for direct matrix converters [12], [13], [14], [15], [16], [17], [18] have been presented. The SVM method [4] is extended to [12] and [13]. In [12], an overmodulation method based on multiorbit vector weighting to increase the maximum voltage transfer ratio was proposed, while the calculation of output harmonics for space-vector modulation based on triple Fourier series was presented in [13], and rotating vectors were expanded to SVMs in [14]. Moreover, SVMs have also been widely applied to indirect matrix converters [19], [20], [21], [22], [23], [24], [25], [26]. The aforementioned review indicated that SVMs with complicated duty cycle computations have been widely used.

These SVM methods for two- and three-level inverters can be realized by a CBM, as presented in [27], [28], [29], [30], [31], [32], [33], and [34]. For two-level inverters in [27], [28], [29], and [30], the relationship between a zero-sequence voltage and a zero vector was shown to easily create reference voltages that are equivalent to those of SVM by adding zero-sequence voltage with commanded output voltages, while a modulation method for three-level inverters was also proposed in [31], [32], [33], and [34] to generate the switching patterns of SVM methods using a CBM. These methods confirmed that the SVPWM can be easily generated by the CBM. Moreover, the CBDM for the SVM of the matrix converter was proposed in [35]. However, this approach only focused on a discontinuous PWM and one switching sequence. Similar to [31], [32], [37], [38], [39], [40], [41], [42], [43], [44], and [45], their proposed CBDM is only a technique for generating the switching signal, so it does not show the relationship between the reference signals and the desired output voltages. As a result, the behavior of the voltage construction from commanded voltages is not as easy to comprehend as is that derived from the CBM of two-level inverters.

In this study, the CBDM is proposed to realize the switching patterns of SVM methods for matrix converters. The main contributions of the study paper are as follows:

1) An analysis of switching patterns for the well-known SVM methods consists of conventional [4], optimized [5], modified [7], and direct [11] SVM methods.
2) The CBDM uses reference voltages from commanded output voltage concepts as the CBM of the two-level PWM inverters to construct the switching patterns of the SVM methods.
3) The relationships between the SVM and the CBDM with PWM modes and switching sequences are revealed.

The remainder of this paper is organized as follows. The configuration of the matrix converter is explained in Section II. In Section III, the process of the ISVM is described. Next, the direct SVM based on the ISVM is provided. In Section V, switching patterns for the well-known SVM methods are analyzed. In Section VI, the CBDM is developed to generate the switching patterns of the well-known SVM methods. Then, the relationship between the SVM and the CBDM is presented in Section VII. After, experimental results of the well-known SVM methods are shown to verify the effectiveness of the proposed method. Finally, conclusions are given in Section IX.

II. GENERAL EQUATION OF MODULATION MATRIX

The structure of the matrix converters is depicted in Fig. 1 and consists of 9 switches to control the generation of output voltages from the input voltages. The relationship between the output voltage generation is defined by (1) – (2):

$$\underbrace{\begin{bmatrix} u \\ v \\ w \end{bmatrix}}_{\boldsymbol{v}_o} = \begin{bmatrix} u* + v_Z \\ v* + v_Z \\ w* + v_Z \end{bmatrix} = \underbrace{\begin{bmatrix} m_{11} & m_{12} & m_{13} \\ m_{21} & m_{22} & m_{23} \\ m_{31} & m_{32} & m_{33} \end{bmatrix}}_{\boldsymbol{M}} \underbrace{\begin{bmatrix} R \\ S \\ T \end{bmatrix}}_{\boldsymbol{v}_i} \tag{1}$$

$$0 \leq m_{ij} \leq 1, \ \sum_{j=1}^{3} m_{ij} = 1, \ i = \{1, 2, 3\}, \ j = \{1, 2, 3\} \tag{2}$$

where the scalar values $u*$, $v*$, $w*$ and R, S, T are the commanded output voltages and the input voltages, respectively. v_z is the zero voltage, and $\mathbf{M}$ is the modulation matrix. Subscripts i and o denote the input and output quantities, respectively.

III. INDIRECT SPACE-VECTOR MODULATION

The PWM methods proposed in [4], [5], [6], [7], [8], and [9] are the ISVM for direct matrix converters. These techniques consider the matrix converter as a rectifier circuit linked to the

inverter circuit through a virtual DC bus. This system can be visualized as a 3-to-2-to-3 phase configuration, as shown in Fig. 2. The relationship between the output and input voltages can be expressed in (3):

$$\begin{bmatrix} u \\ v \\ w \end{bmatrix} = \begin{bmatrix} m_7 & m_8 \\ m_9 & m_{10} \\ m_{11} & m_{12} \end{bmatrix} \underbrace{\begin{bmatrix} m_1 & m_3 & m_5 \\ m_2 & m_4 & m_6 \end{bmatrix}}_{Rectifier\ stage} \begin{bmatrix} R \\ S \\ T \end{bmatrix}. \quad (3)$$

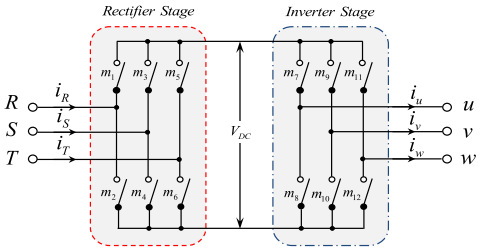

FIGURE 2. The equivalent circuit of a direct matrix converter for the ISVM viewed as two-level back-to-back (2L-BTB) capacitorless inverters.

Regarding the ISVM, there are only 21 switching states. The switching patterns of this modulation rely on vector selection and arrangement for each sector of the output voltage and input current, as shown in Fig. 3.

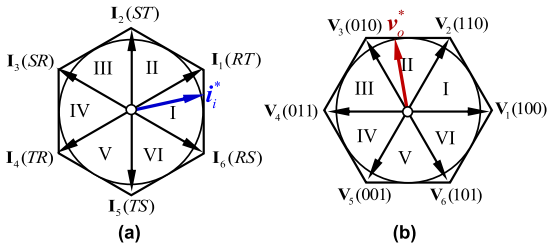

FIGURE 3. Space vectors of the input current and output voltage: (a) input rectifier hexagon and (b) output inverter hexagon.

The duty cycle calculation of the matrix converters in this modulation requires duty cycle values from the rectifier circuit, which controls the input current, and from the inverter circuit, which regulates the output voltage. Examples of the space vectors of the input current in the first sector and the output voltage in the second sector are presented in Fig. 4(a) and 4(b), respectively.

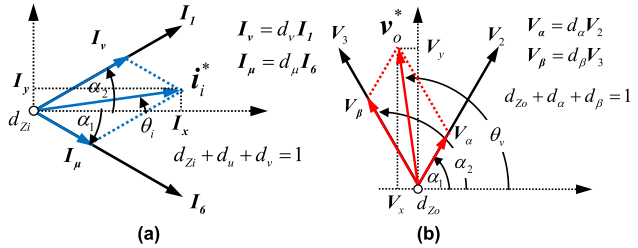

FIGURE 4. SVMs of the rectifier and inverter circuits (a) rectifier duty (b) inverter duty.

When the duty cycles d_μ, d_v, d_α, d_β of the rectifier and the inverter are combined, the relationship between the output voltage and input voltage can be written as in (4):

$$\begin{bmatrix} u \\ v \\ w \end{bmatrix} = \frac{1}{2} \begin{bmatrix} d_\alpha - d_\beta \\ d_\alpha + d_\beta \\ -(d_\alpha + d_\beta) \end{bmatrix} [(d_\mu + d_v) - d_\mu - d_v] \begin{bmatrix} R \\ S \\ T \end{bmatrix} + d_0 R. \quad (4)$$

Equation (4) can be rewritten as shown in (5), which indicates that the matrix converter generates the output voltage from two line-to-line input voltages, i.e., the RT bus and the RS bus.

$$\begin{bmatrix} u - R \\ v - R \\ w - R \end{bmatrix} = \frac{1}{2} \begin{bmatrix} d_{\alpha v} - d_{\beta v} + d_0/2 \\ d_{\alpha v} + d_{\beta v} + d_0/2 \\ -(d_{\alpha v} + d_{\beta v}) + d_0/2 \end{bmatrix} [R - T] + \frac{1}{2} \begin{bmatrix} d_{\alpha\mu} - d_{\beta\mu} + d_0/2 \\ d_{\alpha\mu} + d_{\beta\mu} + d_0/2 \\ -(d_{\alpha\mu} + d_{\beta\mu}) + d_0/2 \end{bmatrix} [R - S] \quad (5)$$

where:

$$\left.\begin{aligned} d_{\alpha\mu} &= d_\alpha d_\mu = T_{\alpha\mu}/T_s = q \sin(2\pi/3 - \theta_v) \sin(\pi/6 - \theta_i) \\ d_{\beta\mu} &= d_\beta d_\mu = T_{\beta\mu}/T_S = q \sin(\theta_v - \pi/3) \sin(\pi/6 - \theta_i) \\ d_{\alpha v} &= d_\alpha d_v = T_{\alpha v}/T_s = q \sin(2\pi/3 - \theta_v) \sin(\pi/6 + \theta_i) \\ d_{\beta v} &= d_\beta d_v = T_{\beta v}/T_s = q \sin(\theta_v - \pi/3) \sin(\pi/6 + \theta_i) \\ d_0 &= 1 - d_{\alpha\mu} - d_{\beta\mu} - d_{\alpha v} - d_{\beta v} = T_0/T_s \\ q &= q_v q_i \end{aligned}\right\}$$

where $q_v = 2\left\|\boldsymbol{v}_o^*\right\|/\sqrt{3}Vdc$ and $q_i = 2\left\|\boldsymbol{i}_i^*\right\|/\sqrt{3}I_{DC}$ are the modulation indices of the inverter circuit and the rectifier circuit, respectively.

A zero vector is chosen to define the PWM mode, while the vector sequence determines the switching sequence. Thus, the switching patterns of SVMs depend on the vector selection and sequence in each sector of the output voltage and input current, as illustrated in Fig. 3. In [4], the switching sequence $d_{\alpha\mu} \rightarrow d_{\beta\mu} \rightarrow d_{\beta v} \rightarrow d_{\alpha v} \rightarrow d_0$ is used, and a zero vector is chosen for the minimum number of switchings in each sector. When the space vector of the output voltage is in the sector II and the input current is in the sector I, the active vectors of the output voltage are $\boldsymbol{V}_\alpha = \boldsymbol{V}_2(110)$ and $\boldsymbol{V}_\beta = \boldsymbol{V}_3(010)$, and the active vectors of the input current are $\boldsymbol{I}_\mu = \boldsymbol{I}_6(RS)$ and $\boldsymbol{I}_v = \boldsymbol{I}_1(RT)$. In this case, the switching pattern will be one phase with no switching, and simultaneous switching occurs in two phases (SRS –> TRT). As a result, 10 BSOs are obtained, as shown in Fig. 5.

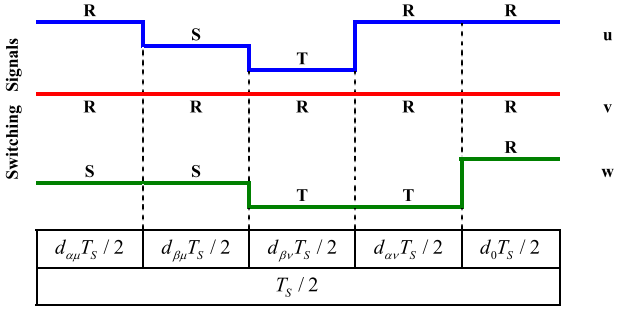

FIGURE 5. An example of the switching pattern of the ISVM in [4].

From the ISVM algorithm shown in Fig. 6, it can be seen that the corresponding modulation is very complex and

requires many calculations. Moreover, it does not show a straightforward relationship between the reference voltages and the commanded output voltages.

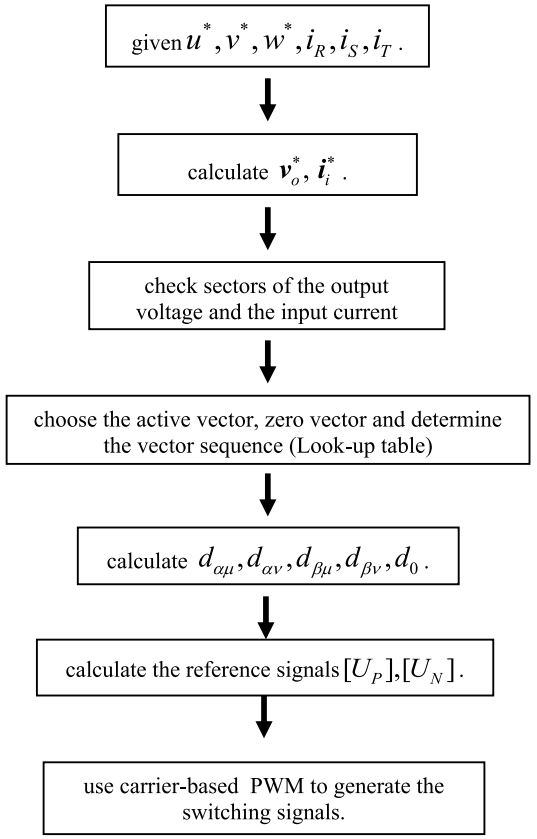

FIGURE 6. Flowchart of the ISVM algorithm.

IV. DIRECT SPACE-VECTOR MODULATION BASED ON INDIRECT SPACE-VECTOR MODULATION

The ISVM considers the direct matrix converter as a two-level back-to-back (2L-BTB) capacitorless converter. However, this viewpoint prohibits the use of rotating space vectors, which simultaneously use three-phase input voltages to generate output voltages. In fact, the direct matrix converter is fully equivalent to a three-level BTB (3L-BTB) capacitorless converter as shown in Fig. 7. This converter performs a 3-to-3-to-3 phase conversion rather than a 3-to-2-to-3 phase conversion as in the 2L-BTB converter [46]. Thus, the relationship between the output and input voltages is changed from (3) to (6), and the utilized space vectors cover all 27 switching states of the matrix converter.

$$\begin{bmatrix} u \\ v \\ w \end{bmatrix} = \begin{bmatrix} m_7 & m_{16} & m_8 \\ m_9 & m_{17} & m_{10} \\ m_{11} & m_{18} & m_{12} \end{bmatrix} \underbrace{\begin{bmatrix} m_1 & m_3 & m_5 \\ m_{13} & m_{14} & m_{15} \\ m_2 & m_4 & m_6 \end{bmatrix}}_{Rectifier\ stage} \begin{bmatrix} R \\ S \\ T \end{bmatrix}. \tag{6}$$

Although a direct SVM has space vectors to choose from rather than those of the ISVM, the technique of space vector selection and its sequence are still the same as those of the ISVM. The direct SVM in [11] is chosen from 5 of 10 vectors

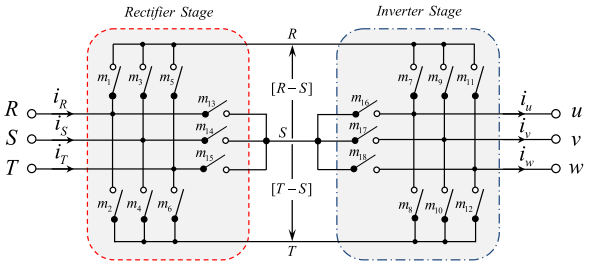

FIGURE 7. Equivalent circuit of a direct matrix converter for the direct SVM viewed as three-level BTB inverters ($R > S > T$).

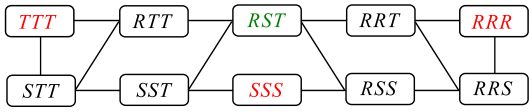

FIGURE 8. Possible switching sequence of the direct SVM in sector I.

in each sector. If the space vectors of the commanded output voltage are in sector I, the switching sequence is available, as shown in Fig. 8.

Figure 8 shows all space vectors in sector I. Notably, this modulation also has a rotating vector RST. Alternating vectors are $\boldsymbol{STT_S}$, $\boldsymbol{RSS_M}$, ***and*** $\boldsymbol{RRT_L}$ and $\boldsymbol{SST_S}$, $\boldsymbol{RRS_M}$, ***and*** $\boldsymbol{RRT_L}$. The subscripts S, M, L denote the amplitudes of the line-to-line input voltages low, medium, and high, respectively. The zero voltage in [11] is chosen by only the intermediate input voltage, e.g., $R>S>T$. The zero vector is "***SSS***". The utilized space vectors are represented as:

The duty cycles of the direct SVM can be computed in 2 ways: direct and indirect methods. However, direct computation is very complicated, such that the duty cycles of the direct SVM based on the duty cycles of the ISVM, similar to [11], are shown by the relation in Fig. 9.

TABLE 1. Space-vector utilization and sequence of the direct SVM [11].

Space-vectors	*RRS*	*RSS*	*RST*, *SSS*	*SST*	*STT*
Duty cycles	$d_1/2$	$d_2/2$	$d_3/2, d_0/2$	$d_4/2$	$d_5/2$

From Fig. 9, the relationship among space vectors can be characterized as:

$$\left.\begin{aligned} \boldsymbol{RRT} &= \boldsymbol{RRS} + \boldsymbol{SST} \\ \boldsymbol{RTT} &= \boldsymbol{RSS} + \boldsymbol{STT} \\ \boldsymbol{RST} &= \boldsymbol{SST} + \boldsymbol{RSS} = (\boldsymbol{RRT} - \boldsymbol{RRS}) + \boldsymbol{RSS} \end{aligned}\right\} \tag{7}$$

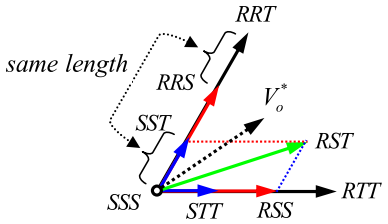

FIGURE 9. Relationship of space vectors in sector I.

The duty cycles of the ISVM $d_{\alpha\mu}, d_{\beta\mu}, d_{\beta v}, d_{\alpha v}$ in sector I are for the space vectors ***RSS***, ***RRS***, ***RRT***, ***and RTT***, while

the space vectors for the direct SVM are the ***STT***, ***SST***, ***RST***, ***RSS***, ***and RRS***; therefore, when using the relationship in (7), the duty cycles of the direct SVM d_1, d_2, d_3, d_4, d_5 can be obtained by the coefficients between (8) and (9):

$$\left.\begin{aligned} \boldsymbol{v}_o^* &= (d_{\alpha\mu})\boldsymbol{RSS} + (d_{\beta\mu})\boldsymbol{RRS} + (d_{\beta v})\boldsymbol{RRT} + (d_{\alpha v})\boldsymbol{RTT} \\ &= (d_{\alpha\mu})\boldsymbol{RSS} + (d_{\beta\mu})\boldsymbol{RRS} + (d_{\beta v})(\boldsymbol{RRS} + \boldsymbol{SST}) \\ &\quad + (d_{\alpha v})(\boldsymbol{RSS} + \boldsymbol{STT}) \\ &= (d_{\alpha v})\boldsymbol{STT} + (d_{\beta v})\boldsymbol{SST} + (d_{\alpha\mu} + d_{\alpha v})\boldsymbol{RSS} \\ &\quad + (d_{\beta\mu} + d_{\beta v})\boldsymbol{RRS} \end{aligned}\right\} \tag{8}$$

$$\left.\begin{aligned} \boldsymbol{v}_o^* &= (d_1)\boldsymbol{STT} + (d_2)\boldsymbol{SST} + (d_3)\boldsymbol{RST} + (d_4)\boldsymbol{RSS} \\ &\quad + (d_5)\boldsymbol{RRS} \\ &= (d_1)\boldsymbol{STT} + (d_2)\boldsymbol{SST} + (d_3)(\boldsymbol{SST} + \boldsymbol{RSS}) \\ &\quad + (d_4)\boldsymbol{RSS} + (d_5)\boldsymbol{RRS} \\ &= (d_1)\boldsymbol{STT} + (d_2 + d_3)\boldsymbol{SST} + (d_3 + d_4)\boldsymbol{RSS} \\ &\quad + (d_5)\boldsymbol{RRS} \end{aligned}\right\}. \tag{9}$$

From (8), (9), and the condition in (2), the duty cycles of the direct SVM based on the ISVM are derived in (10):

$$\left.\begin{aligned} d_1 &= d_{\alpha v} \\ d_2 &= 1 - (2d_{\alpha v} + d_{\alpha\mu} + d_{\beta\mu} + d_{\beta v}) \\ d_3 &= 2d_{\alpha v} + d_{\alpha\mu} + d_{\beta\mu} + 2d_{\beta v} - 1 \\ d_4 &= 1 - (d_{\alpha v} + d_{\beta\mu} + 2d_{\beta v}) \\ d_5 &= d_{\beta\mu} + d_{\beta v} \\ d_0 &= 1 - (d_1 + d_2 + d_3 + d_4 + d_5) = 0 \end{aligned}\right\}. \tag{10}$$

Although the direct SVM is more complex than the indirect SVM, the switching transition of the voltage by using the rotating vector does not change from the maximum voltage to the minimum voltage. From the space-vector utilization and sequence, this direct SVM will also yield only 8 BSOs, and will not realize simultaneous switching in any two phases, as shown in Fig. 10.

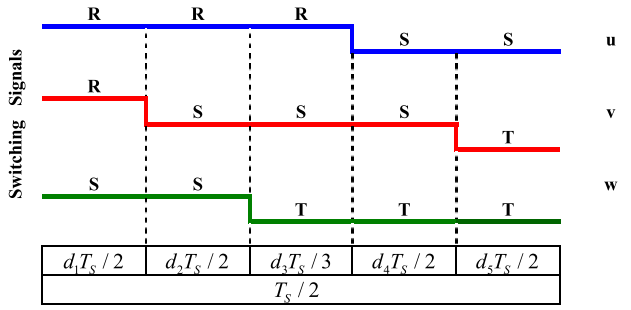

FIGURE 10. An example of the switching pattern of the direct SVM [11].

V. AN ANALYSIS OF SWITCHING PATTERNS FOR SPACE-VECTOR MODULATION METHODS

The PWM switching pattern for each output phase can be non-switching (n), unipolar (u), dipolar (d), or bipolar (b), and the symbols u, d, b, and n are used to represent the three-phase PWM mode. The numbers in front of u, d, b, and n represent the number of modulated phases in each mode. For example, <2u1d> PWM means that two phases are unipolar and another phase is dipolar. Switching sequence types A, B, and C are used instead of min-->max-->mid, max-->mid-->min, and mid-->min-->max, where max=max(R,S,T), mid=mid(R,S,T) and min=min(R,S,T), respectively. When analyzing the switching patterns in TABLE 2, 3 modes of modulation, including <2u1d>, <1n2d>, and <1b1u1d> PWM, are observed. Nevertheless, there are 2 types of switching sequences: A and C. The X symbol represents a case in which the switching sequence does not belong to A, B, or C; therefore, it cannot be constructed by the carrier-based technique.

TABLE 2. The vector sequence of modulation in the conventional SVM [4].

	Input Sectors	R>T>S	R>S>T	S>R>T	S>T>R	T>S>R	T>R>S	R>T>S
		I	II	III	IV	V	VI	
Output Sector I	Vector	RSS	RTT	STT	SRR	TRR	TSS	
		RRS	RRT	SST	SSR	TTR	TTS	
		RRT	SST	SSR	TTR	TTS	RRS	
		RTT	STT	SRR	TRR	TSS	RSS	
		TTT	TTT	RRR	RRR	SSS	SSS	
	Mode	2u1d | 1b1u1d	1n2d	2u1d | 1b1u1d	1n2d	2u1d | 1b1u1d	1n2d	
	Type	A	X | X	A	X | X	A	X | X	
Output Sector II	Vector	RRS	RRT	SST	SSR	TTR	TTS	
		SRS	TRT	TST	RSR	RTR	STS	
		TRT	TST	RSR	RTR	STS	SRS	
		RRT	SST	SSR	TTR	TTS	RRS	
		RRR	SSS	SSS	TTT	TTT	RRR	
	Mode	1n2d	2u1d | 1b1u1d	1n2d	2u1d | 1b1u1d	1n2d	2u1d | 1b1u1d	
	Type	X | X	C	X | X	C	X | X	C	

TABLE 3. The vector sequence of modulation in the optimized SVM [5].

	Input Sectors	R>T>S	R>S>T	S>R>T	S>T>R	T>S>R	T>R>S	R>T>S
		I	II	III	IV	V	VI	
Output Sector I	Vector	RSS	RRT	STT	SSR	TRR	TTS	
		RRS	RTT	SST	SRR	TTR	TSS	
		RRT	STT	SSR	TRR	TTS	RSS	
		RTT	SST	SRR	TTR	TSS	RRS	
		TTT	SSS	RRR	TTT	SSS	RRR	
	Mode	2u1d | 1b1u1d	2u1d | 1b1u1d	2u1d | 1b1u1d	2u1d | 1b1u1d	2u1d | 1b1u1d	2u1d | 1b1u1d	
	Type	A	C	A	C	A	C	
Output Sector II	Vector	SRS	RRT	TST	SSR	RTR	TTS	
		RRS	TRT	SST	RSR	TTR	STS	
		RRT	TST	SSR	RTR	TTS	SRS	
		TRT	SST	RSR	TTR	STS	RRS	
		TTT	SSS	RRR	TTT	SSS	RRR	
	Mode	2u1d | 1b1u1d	2u1d | 1b1u1d	2u1d | 1b1u1d	2u1d | 1b1u1d	2u1d | 1b1u1d	2u1d | 1b1u1d	
	Type	A	C	A	C	A	C	

Remark: The switching patterns of output voltage sectors III and V are similar to those of I, whereas the switching patterns of output voltage sectors IV and VI are similar to those of II.

According to TABLE 2, the chosen vectors and the vector sequence of [4] in some sectors comprise 10 BSOs due to simultaneous changes in the switching status in 2 phases (as shown in red in TABLE 2). To solve this problem, a reduction in switching numbers [5] is proposed by resequencing the vectors and choosing the new zero vector to be concordant with the above conditions. Then, the change in the switching status occurs in each phase separately, and the BSOs decrease by 8 times, as presented in TABLE 3. From the ISVM algorithm in Fig. 6, the simulation results of the SVM methods in [4] and [5] are exhibited in Figs. 11 and 12, respectively.

Considering the time-expanded output voltage in Fig. 11, there is only one phase of <1n2d> PWM, resulting in a higher switching number. This result affects the increase in

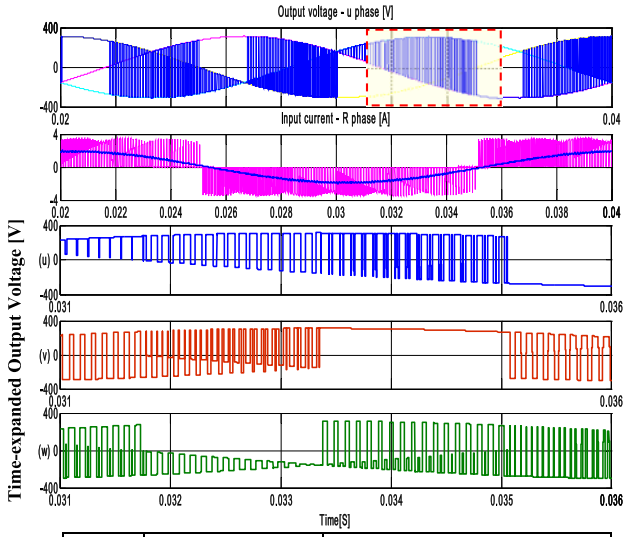

FIGURE 11. The simulation results of the SVM method [4].

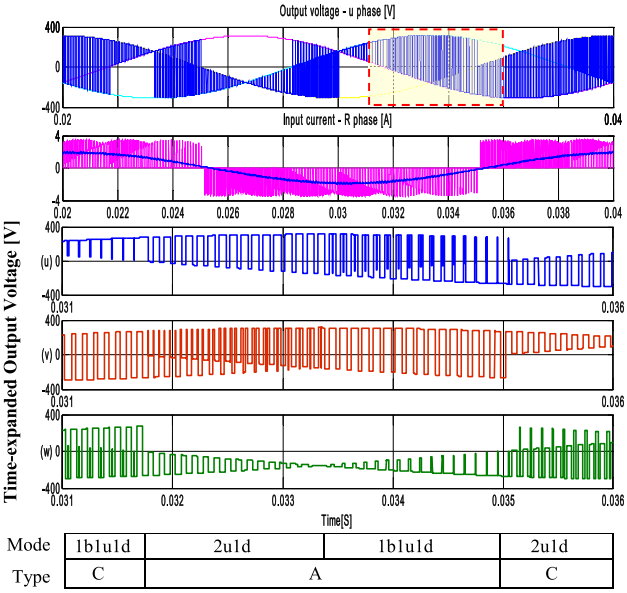

FIGURE 12. The simulation results of the SVM method [5].

BSOs by a factor of 10, which is consistent with the findings of TABLE 2. According to Fig. 12, the former period, including <1n2d> PWM in Fig. 10, turns into <1b1u1d> and <2u1d> PWM instead and is consistent with the analysis in TABLE 3.

The simultaneous change problem of switching status in 2 phases can be solved by modifying the selected vectors and resequencing the vectors, as illustrated in TABLE 4.

Additionally, due to the zero vector with absolute maximum voltage or medium voltage applied to the modulation method in [4] and [5] affecting the high CMV, [7] suggested utilizing the zero vector with absolute minimum voltage instead, as indicated in TABLE 5. The analysis of this vector reveals the <2u1d> PWM with switching sequence type A or C, as represented in TABLE 5.

TABLE 4. The modified vector sequence of modulation in [4] without simultaneous changes in the switching status in two phases.

	Input Sectors	R>T>S	R>S>T	S>R>T	S>T>R	T>S>R	T>R>S	R>T>S
		I	II	III	IV	V	VI	
Output Sector I	Vector	RSS	RRT	STT	SSR	TRR	TTS	
		RRS	RST	SST	STR	TTR	TRS	
		RRT	SST	SSR	TTR	TTS	RRS	
		RTT	STT	SRR	TRR	TSS	RSS	
		TTT	TTT	RRR	RRR	SSS	SSS	
	Mode	2u1d 1b1u1d	1n2d	2u1d 1b1u1d	1n2d	2u1d 1b1u1d	1n2d	
	Type	A	B A	A	B A	A	B A	
Output Sector II	Vector	RRR	RRT	SSS	SSR	TTT	TTS	
		RRT	TRT	SSR	RSR	TTS	STS	
		RRS	TST	SST	RTR	TTR	SRS	
		TRS	SST	RST	TTR	STR	RRS	
		SRS	SSS	TST	TTT	RTR	RRR	
	Mode	1n2d	2u1d 1b1u1d	1n2d	2u1d 1b1u1d	1n2d	2u1d 1b1u1d	
	Type	B C	C	B C	C	B C	C	

TABLE 5. The vector sequence of modulation in the modified SVM [7].

	Input Sectors	R>T>S		R>S>T		S>R>T		S>T>R		T>S>R		T>R>S		R>T>S
		I		II		III		IV		V		VI		
Output Sector I	Vector	RSS	SSS	RRT	RRR	STT	TTT	SSR	SSS	TRR	RRR	TTS	TTT	
		RRS	RSS	RTT	RRT	SST	STT	SRR	SSR	TTR	TRR	TSS	TTS	
		RRT	RRS	STT	RTT	SSR	SST	TRR	SRR	TTS	TTR	RSS	TSS	
		RTT	RRT	SST	STT	SRR	SSR	TTR	TRR	TSS	TTS	RRS	RSS	
		TTT	RTT	SSS	SST	RRR	SRR	TTT	TTR	SSS	TSS	RRR	RRS	
	Mode	2u1d												
	Type	A		C		A		C		A		C		
Output Sector II	Vector	SRS	SSS	RRT	RRR	TST	TTT	SSR	SSS	RTR	RRR	TTS	TTT	
		RRS	SRS	TRT	RRT	SST	TST	RSR	SSR	TTR	RTR	STS	TTS	
		RRT	RRS	TST	TRT	SSR	SST	RTR	RSR	TTS	TTR	SRS	STS	
		TRT	RRT	SST	TST	RSR	SSR	TTR	RTR	STS	TTS	RRS	SRS	
		TTT	TRT	SSS	SST	RRR	RSR	TTT	TTR	SSS	STS	RRR	RRS	
	Mode	2u1d												
	Type	A		C		A		C		A		C		

TABLE 6. The vector sequence of modulation in the direct SVM [11].

	Input Sectors	R>T>S	R>S>T	S>R>T	S>T>R	T>S>R	T>R>S	R>T>S
		I	II	III	IV	V	VI	
Output Sector I	Vector	TSS	RRS	RTT	SST	SRR	TTR	TSS
		TTS	RSS	RRT	STT	SSR	TRR	TTS
		TTT,RTS	SSS,RST	RRR,SRT	TTT,STR	SSS,TSR	RRR,TRS	TTT,RTS
		RTT	SST	SRR	TTR	TSS	RRS	RTT
		RRT	STT	SSR	TRR	TTS	RSS	RRT
	Mode	2u1d						
	Type	B						
Output Sector II	Vector	STS	RRS	TRT	SST	RSR	TTR	STS
		TTS	SRS	RRT	TST	SSR	RTR	TTS
		TTT,TRS	SSS,SRT	RRR,RST	TTT,TSR	SSS,STR	RRR,RTS	TTT,TRS
		TRT	SST	RSR	TTR	STS	RRS	TRT
		RRT	TST	SSR	RTR	TTS	SRS	RRT
	Mode	2u1d						
	Type	B						

According to TABLES 2, 3, and 5, these methods choose vectors that utilize two line-to-line input voltages with maximum and medium amplitude voltages to generate output voltages. This technique results in choosing vectors that obtain high switching losses. The PWM method [8] uses minimum and medium line-to-line voltages. This method can reduce the switching losses by 15%-35%, but the maximum modulation index is limited to 0.5. The direct SVM method [11] uses the rotating vector to turn into a zero vector when the modulation index is greater than 0.5; this approach increases the maximum modulation index to 0.866. The vector sequence is shown in TABLE 6.

According to the switching sequence from TABLE 6, switching sequence types A and C turn into switching sequence type B. Thus, this PWM method is used only for one PWM mode and one switching sequence type.

VI. DEVELOPMENT OF CARRIER-BASED PWM FOR MATRIX CONVERTERS

A. CARRIER-BASED MODULATION FOR TWO-LEVEL INVERTERS

In addition to SVMs, CBMs are another commonly used approach for two-level inverters. This method can generate switching signals by comparing reference signals to the triangular carrier wave. Generally, the size of the carrier wave equals one unit. However, the maximum and minimum values of the carrier wave used to explain the modulation concept depend on the input voltage or DC bus voltages (V_{DC}). In addition, the reference signals are equal to the generated output voltage, as shown in Fig. 13.

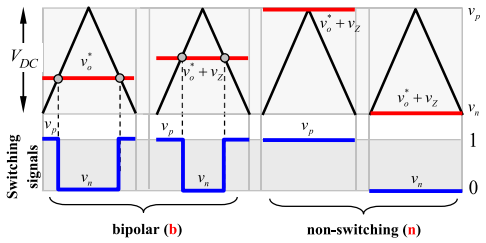

FIGURE 13. CBM for two-level inverters.

B. CARRIER-BASED DIPOLAR MODULATION FOR THREE-LEVEL INVERTERS

Although the CBDM method in [36] has been extensively used by many researchers to generate the switching signals for three-level inverters, normally, CBDM is only the technique or tool for generating the PWM signal, so it cannot show the behavior of the voltage construction, and there is no simple relationship between the reference signals and the desired output voltages [31], [32], [37], [38], [39], [40], [41], [42], [43], [44]. Therefore, this study develops the concept of CBDPWM, which involves constructing positive and negative reference voltages u_P, u_N from the commanded output voltage and adding two zero voltages v_{ZP}, v_{ZN}, as given in (11)-(13) and Fig. 14.

$$v_{o0}^* = v_o^* - v_0 \triangleq u_P^* + u_N^* \tag{11}$$

$$v_{Z0} = v_Z - v_0 \triangleq v_{ZP} + v_{ZN} \tag{12}$$

$$v_{o0} = v_{o0}^* + v_{Z0} \triangleq \underbrace{\left(u_P^* + v_{ZP}\right)}_{u_P} + \underbrace{\left(u_N^* + v_{ZN}\right)}_{u_N} \tag{13}$$

where v_{o0}^*, v_{Z0}, v_{o0} are the commanded output voltage, zero voltage, and output voltage, respectively, and these voltages are referred to as the neutral point voltage ($v_0 = 0$).

C. CARRIER-BASED DIPOLAR MODULATION FOR MATRIX CONVERTERS

From Fig. 1, the three input voltages of the matrix converters are variable, and their instantaneous values are different from those of three-level inverters. Consequently, the maximum and minimum values of the double-carrier wave corresponding to the middle-phase voltage "S" for the matrix converters are not constant, as shown in Fig. 15. In this case, the reference voltages u_P, u_N from the commanded output voltage and

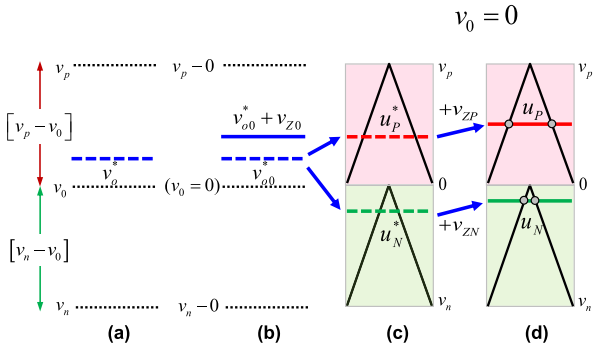

FIGURE 14. The reference voltage generation from the commanded output voltage for three-level inverters: (a) commanded voltage, (b) commanded voltage referring to the neutral point voltage, (c) positive and negative commanded voltages, and (d) positive and negative reference voltages.

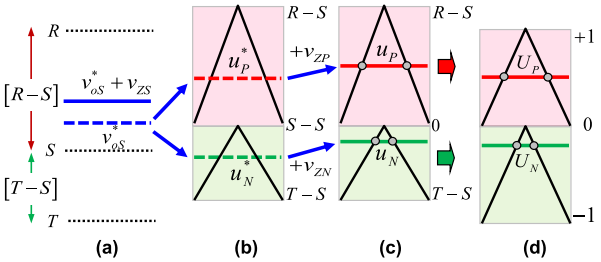

FIGURE 15. The reference voltage generation from the commanded output voltage for matrix converters: (a) commanded voltage referred to as the "S" phase, (b) positive and negative commanded voltages, (c) positive and negative reference voltages, and (d) reference signals.

the addition of two zero voltages v_{ZP}, v_{ZN} for the CBDM are changed from (11)-(13) to (14)-(16):

$$v_{oS}^* = v_o^* - S \triangleq u_P^* + u_N^* \tag{14}$$

$$v_{ZS} = v_Z - S \triangleq v_{ZP} + v_{ZN} \tag{15}$$

$$v_{oS} = v_o - S = v_{oS}^* + v_{ZS} \triangleq \underbrace{\left(u_P^* + v_{ZP}\right)}_{u_P} + \underbrace{\left(u_N^* + v_{ZN}\right)}_{u_N} \tag{16}$$

where v_{oS}^*, v_{ZS}, v_{oS} are the commanded output voltage, zero voltage, and output voltage, respectively, and these voltages are referred to as the middle-phase voltage "S".

Figure 15 depicts the reference voltages generated from the commanded output voltage for the CBDM, which are briefly described as follows. First, the commanded output voltage v_o^* is shown in Fig. 15(a). Next, when referring to "S", the phase (v_{oS}^*) is divided into 2 parts: a positive commanded output voltage u_P^* derived from the positive [R-S] bus and a negative commanded output voltage u_N^* obtained from the negative [T-S] bus, as represented in Fig. 15(b). After, when adding appropriate zero voltages referred to as the "S" phase v_{ZP} andv_{ZN}, as demonstrated in Fig. 15(c), the reference voltages u_P, u_N increase or decrease at the desired positions. Furthermore, the total voltage of both values ($u_P + u_N$) will reflect the addition of zero voltage and commanded output voltage ($v_{oS}^* + v_{ZS}$) similar to the modulation scheme of two-level inverters. Finally, when the two reference voltages u_P, u_N are applied as normalized values, the resulting double-reference signal $[U_P]$ $[U_N]$ given as is and used for comparison to the

one-unit double-carrier wave, as shown in Fig. 15(d). The reference voltages u_P, u_N can also originate from equivalent SVM modulations in Tables 2 to 6, as shown in Fig. 16.

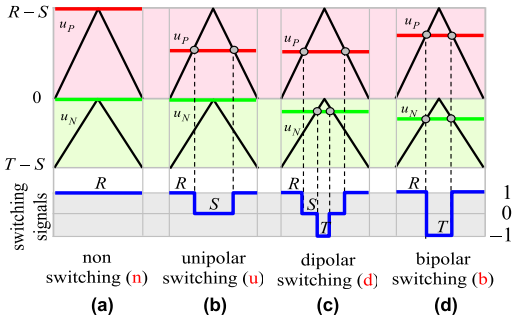

FIGURE 16. CBDM for generating all switching types of SVM methods.

As shown in Fig. 16, the given CBDM extends the modulation theory of two-level inverters, which applies the concept of the reference voltage generated from the commanded output voltage and the addition of the zero voltage. This feature reflects the voltage conversion behavior and the direct relationship between the commanded output voltages and reference voltages. From Fig. 16(c), dipolar switching, in which all the input voltages (R,S,T) are used to produce the output voltage in each switching period, is between those of unipolar and bipolar switching when the output voltage is decreased, and the system changes to unipolar switching, as shown in Fig. 16(b). As the output voltage is increased, the system changes to bipolar switching, as shown in Fig. 16(d). As a result, unipolar and bipolar modulations are a subset of dipolar modulations. Additionally, the proposed CBDM is a very powerful approach for generating PWM signals. This approach can enable all possible switching types of matrix converters.

VII. RELATIONSHIP BETWEEN SPACE-VECTOR MODU-LATION AND CARRIER-BASED DIPOLAR MODULATION

A. ZERO VOLTAGE SELECTION

In the CBDM concept, as shown in Fig. 15, the commanded positive and negative voltages for the three phases are obtained as:

$$\boldsymbol{u}_P^* = \frac{R\,[R-S]}{R^2+S^2+T^2}\underbrace{\begin{bmatrix} u* \\ v* \\ w* \end{bmatrix}}_{\boldsymbol{v}_o^*}, \quad \boldsymbol{u}_N^* = -\frac{T\,[S-T]}{R^2+S^2+T^2}\underbrace{\begin{bmatrix} u* \\ v* \\ w* \end{bmatrix}}_{\boldsymbol{v}_o^*}. \tag{17}$$

Equation (17) is simple because it shows that the commanded output voltages $\boldsymbol{v}_o^*$ can be divided into commanded reference voltages $\boldsymbol{u}_P^*, \boldsymbol{u}_N^*$ for carrier-based dipolar modulation depending on the proportion of the $R[R-S]$ and $T[T-S]$ terms. Thus, it is easy to understand the behavior of the output voltage construction.

By adding the zero voltages v_{ZP} and v_{ZN}, the reference voltages $\boldsymbol{u}_P^*, \boldsymbol{u}_N^*$ can be moved up or down within the respective bands of the upper and lower carrier waves. This trend leads to different PWM modes, as exhibited in Fig. 17.

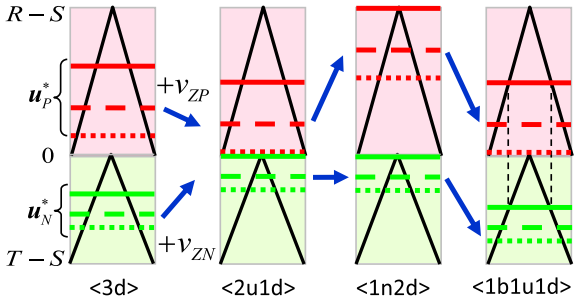

FIGURE 17. PWM modes with two different zero voltages.

From Fig. 17, the two zero voltages v_{ZP} and v_{ZN} are utilized to realize the SVM methods as (18)-(20):

1) *<2u1d> PWM*: For the zero voltages of (18), the <2u1d> PWM can also be realized. This modulation gives the dipolar PWM for the middle phase and the other phases in the unipolar PWM:

$$v_{ZP} = -\min\left(\boldsymbol{u}_P^*\right), \; v_{ZN} = -\max\left(\boldsymbol{u}_N^*\right) \tag{18}$$

2) *<1n2d> PWM*: The <1n2d> PWM clamps the maximum or minimum input phase to that of the output phase depending on the absolute values of the input voltages to avoid overmodulation. The corresponding two zero voltages that shift the reference signals up or down to <1n2d> PWM are given by (19):

$$\underbrace{\begin{aligned} v_{ZP} &= [R-S] - \max\left(\boldsymbol{u}_P^*\right), \\ v_{ZN} &= -\max\left(\boldsymbol{u}_N^*\right) \end{aligned}}_{if\ S \le 0} \quad \text{or} \quad \underbrace{\begin{aligned} v_{ZP} &= -\min\left(\boldsymbol{u}_P^*\right), \\ v_{ZN} &= [T-S] - \min\left(\boldsymbol{u}_N^*\right) \end{aligned}}_{if\ S > 0} \tag{19}$$

3) *<1b1u1d> PWM*: The zero voltages can be chosen according to (20):

$$\left.\begin{aligned} v_{ZP} &= -\min\left(\boldsymbol{u}_P^*\right), \\ v_{ZN} &= -\min\left([R-S] - \max(\boldsymbol{u}_P^*) + \boldsymbol{u}_P^*\right) \\ &\quad - \max\left(\boldsymbol{u}_N^*\right) \end{aligned}\right\} \quad if\ S \le 0\ or$$

$$\left.\begin{aligned} v_{ZP} &= -\max\left([T-S] - \min(\boldsymbol{u}_N^*) + \boldsymbol{u}_N^*\right) \\ &\quad - \min\left(\boldsymbol{u}_P^*\right), \\ v_{ZN} &= -\max\left(\boldsymbol{u}_N^*\right) \end{aligned}\right\} \quad if\ S > 0. \tag{20}$$

From (17), the reference voltages $\boldsymbol{u}_P, \boldsymbol{u}_N$ from the commanded output voltages $\boldsymbol{u}_P^*, \boldsymbol{u}_N^*$ for carrier-based dipolar modulation can be expressed as:

$$\begin{aligned} \boldsymbol{u}_P &= \underbrace{\frac{R\,[R-S]}{R^2+S^2+T^2}\begin{bmatrix} u* \\ v* \\ w* \end{bmatrix}}_{\boldsymbol{u}_P^*} + \begin{bmatrix} v_{ZP} \\ v_{ZP} \\ v_{ZP} \end{bmatrix}, \\ \boldsymbol{u}_N &= \underbrace{-\frac{T\,[S-T]}{R^2+S^2+T^2}\begin{bmatrix} u* \\ v* \\ w* \end{bmatrix}}_{\boldsymbol{u}_N^*} + \begin{bmatrix} v_{ZN} \\ v_{ZN} \\ v_{ZN} \end{bmatrix}. \end{aligned} \tag{21}$$

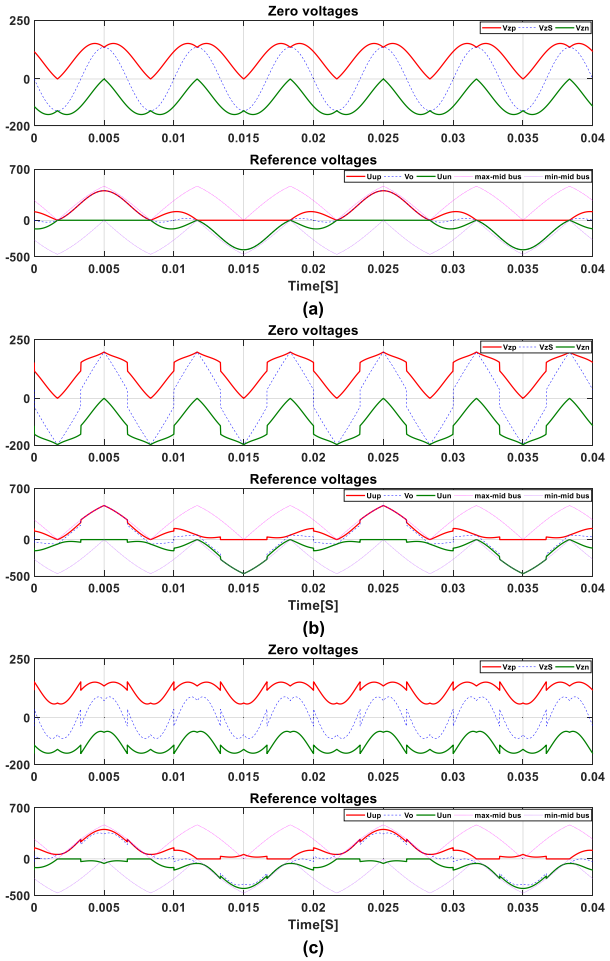

FIGURE 18. Zero voltages and reference voltages of the "u" phase in CBDM (a) <2u1d> PWM (b) <1n2d> PWM and (c) <1b1u1d> PWM.

Equations (18)-(20) show that the condition of the input phase voltage must always be checked for <1n2d> PWM and <1b1u1d> PWM; in contrast, <2u1d> PWM is unnecessary. The zero voltages and reference voltages of these PWMs are compared in Fig. 18.

Figure 18 shows that the reference voltages can be produced by using the commanded output voltage and zero voltages, which are similar to the modulation method for two-level inverters.

B. SELECTION OF THE INPUT PHASE AS A REFERENCE

In general, the switching sequence arrangement in CBM obstructs the realization of SVM methods for matrix converters. This occurs because changing the switching sequence by adjusting the carrier wave is not easy. However, in this study, the switching sequence arrangement for matrix converters can easily be achieved by choosing only the input phase voltage as a reference.

From (21) and Fig. 17, the modulation matrix in (1) can be characterized as:

$$\boldsymbol{M} = [m_{ij}] = \begin{bmatrix} m_{11} & m_{12} = 1 - m_{11} - m_{13} & m_{13} \\ m_{21} & m_{22} = 1 - m_{21} - m_{23} & m_{23} \\ m_{31} & m_{32} = 1 - m_{31} - m_{33} & m_{33} \end{bmatrix} \quad (22)$$

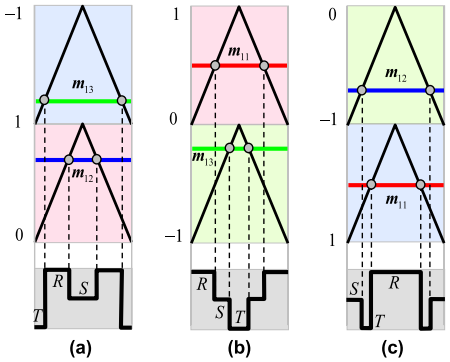

FIGURE 19. The switching sequence for the u-phase when choosing different input phases as a reference: (a) type A, (b) type B and (c) type C.

where:

$$[m_{i1}] = [\boldsymbol{u}_P]/[R-S], \quad [m_{i3}] = [\boldsymbol{u}_N]/[T-S].$$

A detailed selection of the input phase as a different reference (central value of carrier signal) for the CBDM can be found in [47]. From Fig. 15(d), the three various types of switching sequences—A, B, and C—for only the u-phase are presented in Fig. 19, while the three-phase reference signals $[U_P]$ and $[U_N]$ compared with the double-carrier wave causing A, B, and C switching sequences are described in (24), (26), and (28), respectively.

1) Type A: For type A in TABLES 2 to 5, the switching sequence is used by the minimum-phase voltage to the maximum-phase voltage and then to the middle-phase voltage (min --> max --> mid). This type of switching can be realized by CBDM, as shown in Fig. 19(a). From (1), the output voltages referred to as the "R" phase or the maximum-phase voltage can be expressed as:

$$\begin{bmatrix} u-R \\ v-R \\ w-R \end{bmatrix} \triangleq \begin{bmatrix} m_{13} \\ m_{23} \\ m_{33} \end{bmatrix} [T-R] + \begin{bmatrix} m_{12} \\ m_{22} \\ m_{32} \end{bmatrix} [S-R]. \quad (23)$$

Equation (23) shows that the output voltages $\boldsymbol{u}_P, \boldsymbol{u}_N$ are generated from the [T-R] and [S-R] bus voltages, which are the same as in (5). The PWM switching signals can be created by dipolar modulation. Equation (23) is normalized by the [T-R] and [R-S] bus voltages. The upper and lower reference signals $[U_P]$, $[U_N]$ for the double-carrier wave are obtained by:

$$[U_P] = \begin{bmatrix} m_{13} \\ m_{23} \\ m_{33} \end{bmatrix} \geq 0, \quad [U_N] = -\begin{bmatrix} m_{12} \\ m_{22} \\ m_{32} \end{bmatrix} \leq 0 \quad (24)$$

2) Type B: The switching sequence type B in TABLES 4 and 6 can be realized using a mid-phase reference. This switching sequence will exhibit a switching transition from max to mid and then to min (R-->S-->T), as shown in Fig. 19(b) and as characterized in (25) and (26):

$$\begin{bmatrix} u-S \\ v-S \\ w-S \end{bmatrix} \triangleq \begin{bmatrix} m_{11} \\ m_{21} \\ m_{31} \end{bmatrix} [R-S] + \begin{bmatrix} m_{13} \\ m_{23} \\ m_{33} \end{bmatrix} [T-S] \quad (25)$$

$$[U_P] = \begin{bmatrix} m_{11} \\ m_{21} \\ m_{31} \end{bmatrix} \geq 0, \quad [U_N] = -\begin{bmatrix} m_{13} \\ m_{23} \\ m_{33} \end{bmatrix} \leq 0 \quad (26)$$

3) Type C: From the selection of the min-phase as a reference, switching sequence type C in TABLES 2 to 5 can be generated. In this case, a switching transition occurs from S-->T-->R, and there is a direct transition from the minimum-phase voltage to the maximum-phase voltage or vice versa, as shown in Fig. 19(c). As a result, the dv/dt of the output voltages is as high as that of type A:

$$\begin{bmatrix} u-T \\ v-T \\ w-T \end{bmatrix} \triangleq \begin{bmatrix} m_{12} \\ m_{22} \\ m_{32} \end{bmatrix} [S-T] + \begin{bmatrix} m_{11} \\ m_{21} \\ m_{31} \end{bmatrix} [R-T] \quad (27)$$

$$[U_P] = \begin{bmatrix} m_{12} \\ m_{22} \\ m_{32} \end{bmatrix} \geq 0, \quad [U_N] = -\begin{bmatrix} m_{11} \\ m_{21} \\ m_{31} \end{bmatrix} \leq 0. \quad (28)$$

Equations (24), (26), and (28) indicate that the switching sequence in the proposed CBDM method can easily be changed. The reference signals $[U_P]$, $[U_N]$ are changed from the proper columns of the modulation matrix. For example, the reference signals $[U_P]$, $[U_N]$ come from Columns 3 and 2 of the modulation matrix for switching sequence type A, or for switching sequence type B, the reference signals $[U_P]$, $[U_N]$ are derived from Columns 1 and 3 of the modulation matrix. Consequently, this method is not changed by the carrier wave with phase opposition disposition (POD) to the switching sequence arrangement, as reported in [41], [42], [43], [44], and [45].

After using the different input phases as a reference, the switching sequence and space-vector utilization for <2u1d>, <1n2d>, and <1b1u1d> PWM are listed in TABLE 7.

TABLE 7. Switching sequence and space-vector utilization when R>S>T, the output voltage in sector 1, and the modulation index 0 ≤ q ≤ 0.866.

PWM modes	<2u1d>			<1n2d>			<1b1u1d>		
Phase Ref.	R	S	T	R	S	T	R	S	T
Space vectors	RTT	RRS	SSS	RTT	RRR	RSS	TTT	RRS	TSS
	RRT	RSS	RSS	RRT	RRS	RTS	RTT	RRT	TTS
	RRS	SSS,RST	RTS	RRR	RRT	RTT	RRT	RST	TTT
	RSS	SST	RTT	RRS	RST	RRT	RRS	RTT	RTT
	SSS	STT	RRT	RSS	RTT	RRR	RSS	TTT	RRT

According to the procedures of the CBDM, the three simple steps to generate the required switching patterns of the SVM are defined in Fig. 20.

Compared with Fig. 6, it is clear that the switching patterns of the SVM can be simply realized by using the CBDM, which requires fewer calculations and procedures than the same two-level inverters with CBM.

VIII. EXPERIMENTAL RESULTS

To verify the effectiveness of the proposed PWM algorithm, a CBDPWM realization of the SVM methods is implemented by a DSP (TMSLF2407) with two PWM peripherals for dipolar modulation and a field-programmable gate array (FPGA) board (Discovery-III XC3S200F), as shown in Figs. 21 to 22.

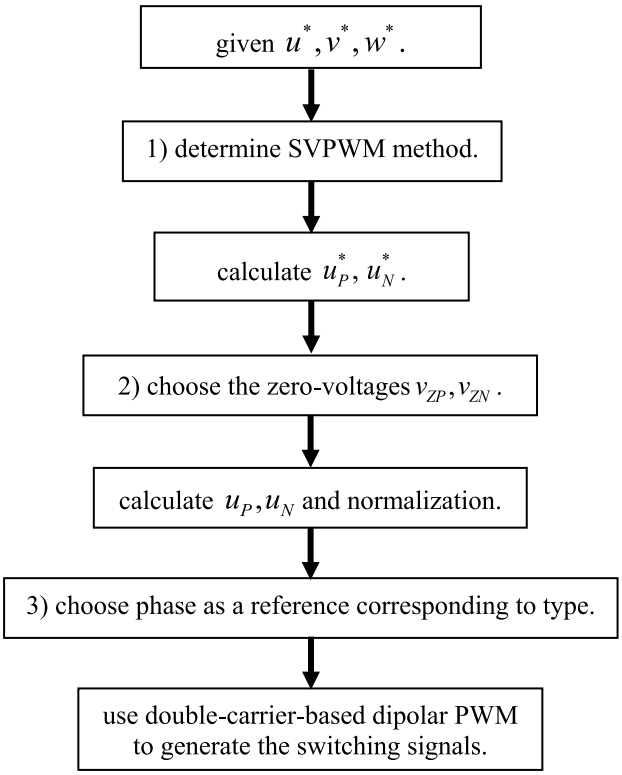

FIGURE 20. Flowchart of the CBPWM algorithm to realize the SVM methods.

TABLE 8. Experimental conditions.

input voltage: 200 V 50 Hz	modulation index q=0.8
output voltage: q*200 V 100 Hz	switching frequency 10 kHz
input filter: $L_f = 3.3mH, C_f = 10uF$(Y)	load: $R_L = 50\Omega$, $L = 34mH$

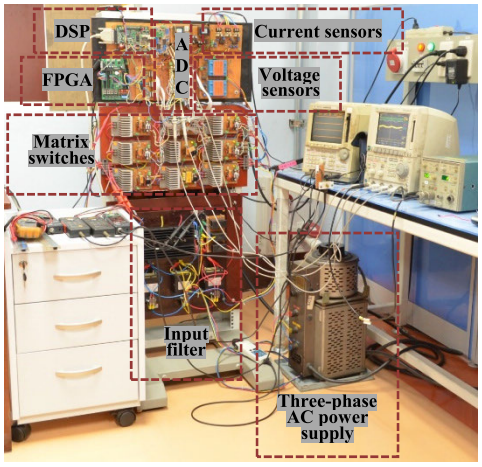

FIGURE 21. Experimental setup of the matrix converter.

As shown in Fig. 23, the process of producing the switching signals for 18 matrix switches is briefly described as follows. First, the 6 PWM signals are generated by the DSP board using the information of the commanded output voltages, and input voltages. After, these PWM signals are sent to the FPGA board to create switching signals for 18 IGBTs with appropriate dead time adjustments. Moreover, the FPGA

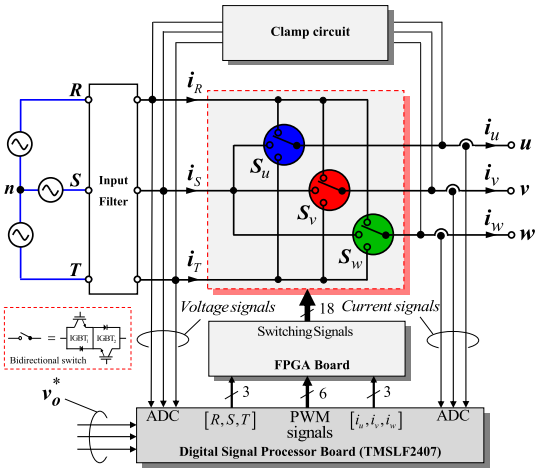

FIGURE 22. Simplified block diagram of the hardware in Fig. 21.

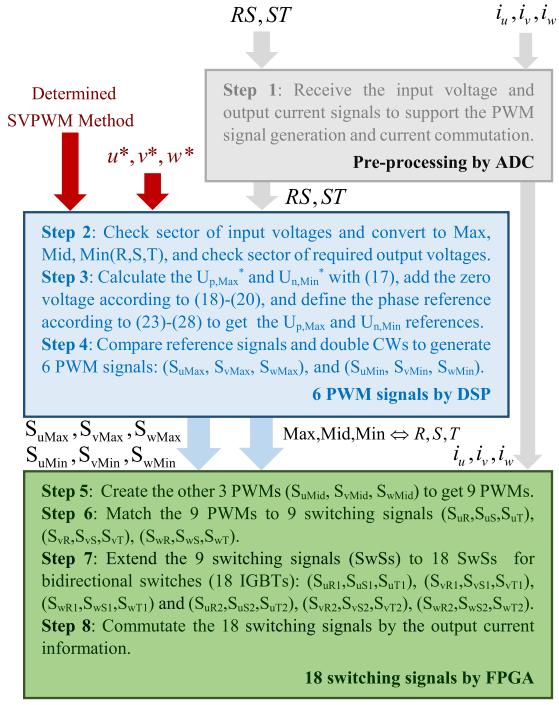

FIGURE 23. Flowchart of the implementation.

board is also used to realize the current commutation among the matrix switches.

The experimental results are shown in Figs. 24 to 29 to confirm the effectiveness of the proposed modulation algorithm with the CBDPWM in creating switching patterns equivalent to those of well-known SVM methods. The experimental conditions are listed in TABLE 8, wherein a unity input PF is assumed for all SVM methods. Regarding the results presented in Fig. 24, the obtained switching patterns are consistent with the optimized SVM in TABLE 3 and similar to the simulation results in Fig. 12. Additionally, the results in Fig. 25 demonstrate that the switching patterns are consistent with those of the conventional SVM in TABLE 4 and similar to the simulation results in Fig. 11. The <1n2d> PWM is modified to reduce the number of switches by 8 BSOs.

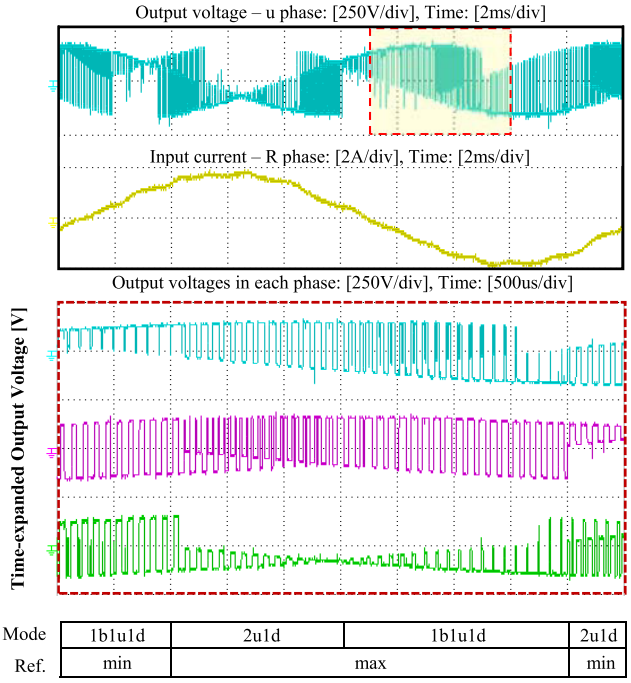

FIGURE 24. Experimental results: mixed both PWM modes and references in dipolar PWM (equivalent to the optimized SVM method in [5]).

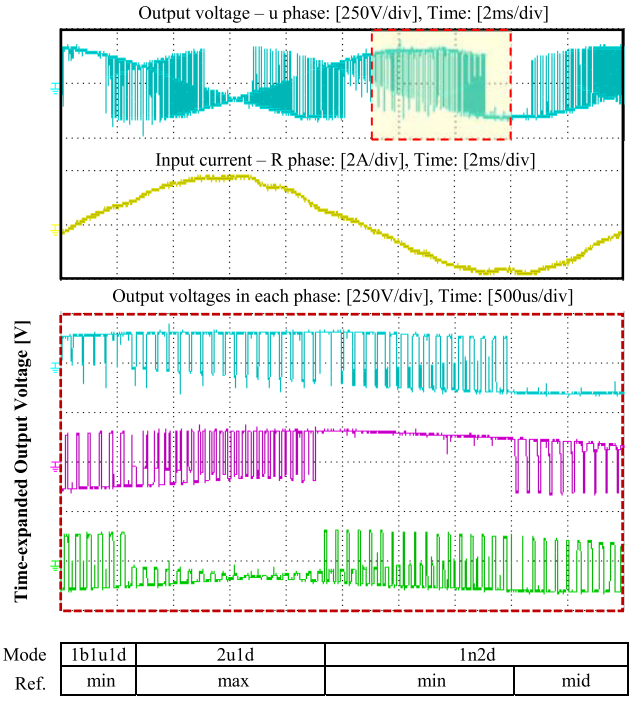

FIGURE 25. Experimental results: mixed both PWM modes and references in dipolar PWM (improved version of the conventional SVM method in [4]).

The switching patterns of the SVM methods in both cases, as shown in Figs. 24 to 25, are mixed PWM modes depending on the input currents and the output voltages at that time. Therefore, the CBDM is used to generate switching patterns that are equivalent to those of the SVM methods. It is also necessary to realize the generation of input currents and proper output voltages to provide suitable switching patterns.

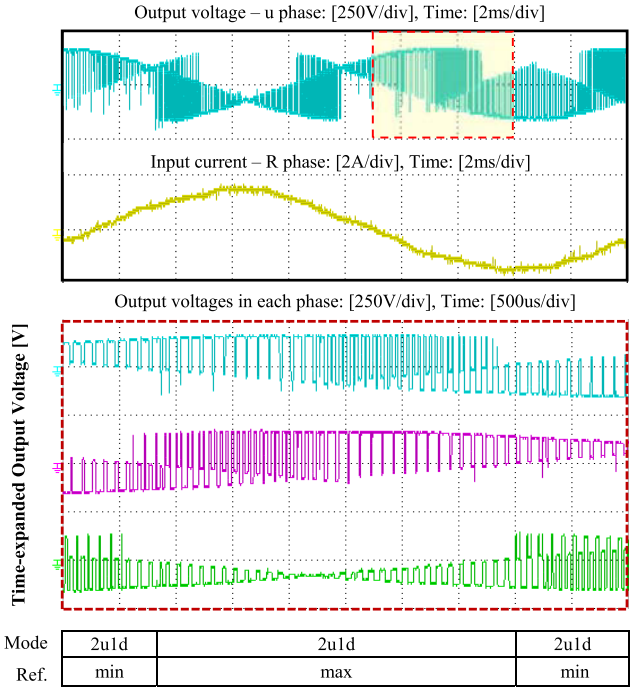

FIGURE 26. Experimental results: one PWM mode and mixed references in dipolar PWM (equivalent to the modified SVM method in [7]).

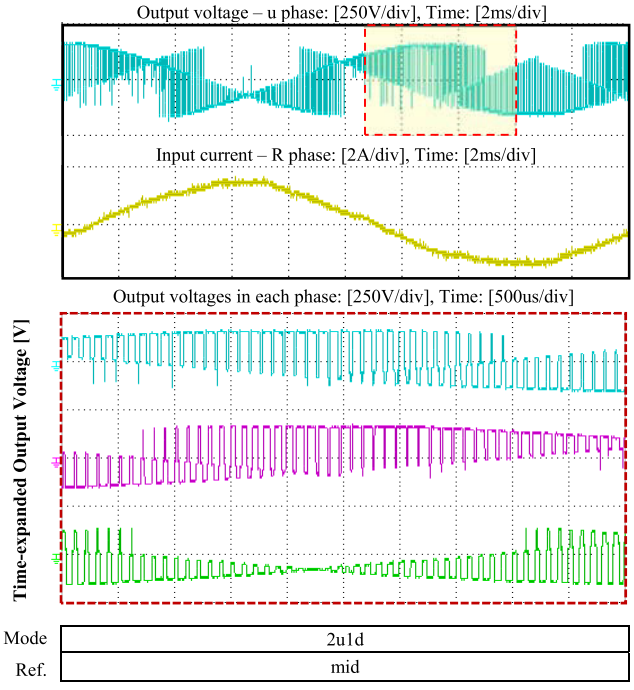

FIGURE 27. Experimental results: one PWM mode and one reference in dipolar PWM (equivalent to the direct SVM method in [11]).

However, in the case of only one PWM mode, as shown in TABLES 5 and 6, the <2uld> PWM mode is utilized. In this case, the data on the sector of input currents and output voltages for the CBDM are unnecessary; only the zero voltages following (18) are selected. Thus, this approach can reduce the modulation process and facilitate modulation. The experimental results are equivalent to the PWM modes of the modified and direct SVM methods in Tables 5 and 6, as demonstrated in Figs. 26 and 27, respectively.

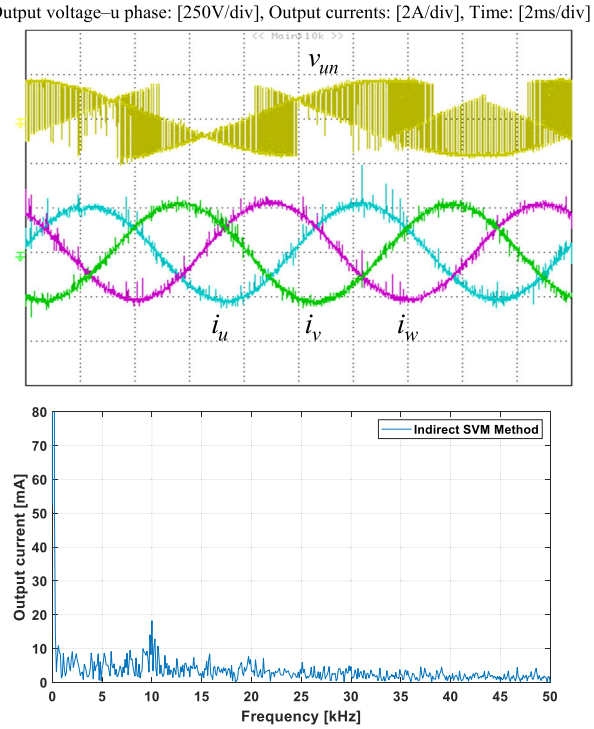

FIGURE 28. Experimental results of the output currents with the indirect SVM method in [7].

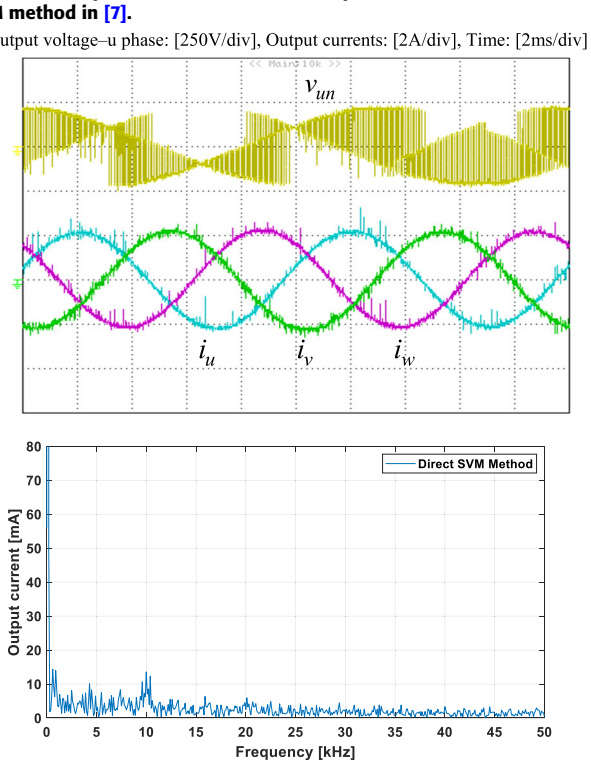

FIGURE 29. Experimental results of the output currents with the direct SVM method in [11].

To compare the output current ripple of the well-known and extensively used indirect and direct SVM methods for matrix converters, Figs. 28 to 29 show the experimental results of the output currents. The output current ripple of the direct SVM method by the <2u1d> PWM with only the mid-phase reference, as shown in Fig. 29, is lower than those of the

TABLE 9. Relationship between SVM methods and the proposed CBDM.

SVPWM Methods	PWM modes	Types	Eq. relation with CBDM		Mod. index
			Zero Volt.	Phase Ref.	
Borojevic[4] [12], [13]	<2u1d>	A	(18)	(24)	≤ 0.866
	<1b1u1d>	C	(20)	(28)	
	<1n2d>	X	(19)	NA	
Nielsen[5]	<2u1d>	A, C	(18)	(24), (28)	≤ 0.866
	<1b1u1d>	A, C	(20)	(24), (28)	
Enjeti[7]	<2u1d>	A, C	(18)	(24), (28)	≤ 0.866
Helle[8], [10]	<2u1d>	B	(18)	(26)	≤ 0.5
Sato[11]	<2u1d>	B	(18)	(26)	≤ 0.866
[14], [24]	<1n2d>	NA	(19)	NA	≤ 0.866

modified ISVM method, as shown in Fig. 28. This occurs because the output voltage using the mid-phase phase as a reference has no direct switching transition of the voltage from the maximum phase to the minimum phase and it can be confirmed by the spectrum of the output current. Thus, it can be concluded that the direct SVM method or <2u1d> PWM with mid-phase reference not only has good performance but is also easiest to implement for the CBDM algorithm with only one PWM mode and only one phase reference. This switching pattern is the same as that of commercial matrix converters, which were presented by Yaskawa Electric [48].

The experimental results demonstrate that SVM methods, which are otherwise complex and require intensive numerical solutions, can be easily realized using the CBDM. This result is the same as that of the CBM for two-level inverters [27], [28], [29], [30]. The relationships between certain space-vector PWM methods and the proposed CBDM are listed in TABLE 9.

IX. CONCLUSION

This study achieves a CBDPWM realization of SVM for matrix converters by analyzing the PWM mode and the switching sequence stemming from the well-known SVM methods. Corresponding development of the CBM is considered a generalization of the PWM theory of two-level inverters. Moreover, this study also shows that the addition of zero voltages can generate the required PWM modes, including the selection of the input phase as a suitable reference for CBDM to generate the switching sequence of the required SVM methods. In addition, the obstruction in utilizing rotating space-vectors from the viewpoint of ISVM methods leads to the fact that the direct matrix converter is equivalent to the 3L-BTB capacitorless inverter. The results reveal that the arbitrary SVM methods can be realized very easily by the proposed CBDPWM, and the calculation and procedure of the mentioned method are much easier than those of the SVM, especially the direct SVM method by the <2u1d> PWM with the mid-phase reference is optimal to generate by CBDPWM.

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