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RESEARCH ARTICLE

Mitigating Camera Interference Arising From RF High Transmit Power: The Role of Common Mode Filters and Receiver Compensation Techniques

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ABSTRACT This paper investigates the challenges and solutions related to Radio Frequency Interference (RFI) in mobile devices equipped with high-resolution cameras, focusing on the Mobile Industry Processor Interface (MIPI) C-PHY interface. The compact design of modern mobile devices makes them susceptible to RFI, which can degrade signal quality and cause visual anomalies. Through simulation-based analysis, we explore the effectiveness of Common Mode Filters (CMFs) in mitigating RFI, highlighting the significance of CMF placement near the Board-to-Board (BTB) connector for enhanced RF immunity and signal integrity. Additionally, we examine receiver compensation techniques to further protect C-PHY signals against RFI. These techniques address the issue of signal imbalances, which can lead to differential-mode interference. The study proposes fine-tuning signal path delays at the CPU receiver end as a strategy to minimize noise, demonstrating improvements in eye diagram metrics. Our findings offer valuable insights into optimizing the placement of CMFs and implementing receiver compensation techniques, contributing to the enhancement of signal integrity and noise reduction in high-speed digital interfaces, thereby ensuring the reliability and performance of camera systems in mobile devices within the RF/EMC/SIPI domain.

INDEX TERMS MIPI C-PHY, radio frequency interference (RFI), common mode filters (CMFs), receiver compensation techniques.

I. INTRODUCTION

The evolution of mobile phone technology has led to the integration of cameras with higher resolutions, necessitating the adoption of advanced Mobile Industry Processor Interface (MIPI) C-PHY [1], [2], [3] interface technologies to facilitate data transmission between central processing units (CPUs) and camera modules. However, the compact structural design of contemporary devices often imposes stack-up constraints that can exacerbate the coupling of high-power Radio Frequency (RF) emissions from the device's antennas into the camera module, Flexible Printed Circuitry (FPC), or Board-to-Board (BTB) connectors, as depicted in Figure 1.

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Such coupling may result in Radio Frequency Interference (RFI) with the camera's high-speed signal transmission. The confluence of RF energy with MIPI C-PHY signals has the potential to introduce decoding errors. Notably, the susceptibility of MIPI C-PHY technology to RF disturbances—emanating from the mobile phone's RF transmission—can manifest in visual anomalies such as display flickering and freezing. These issues can markedly impair the overall user experience.

Figure 2 presents the magnitude of the S-parameters, where S220 represents the S-parameter result of the RF transmit antenna, corresponding to the antenna (indicated by the blue dashed line) in Figure 1. The nine curves, labeled S1,220-S9,220, depict the isolation results between the RF transmit antenna and the nine high-speed C-PHY signals

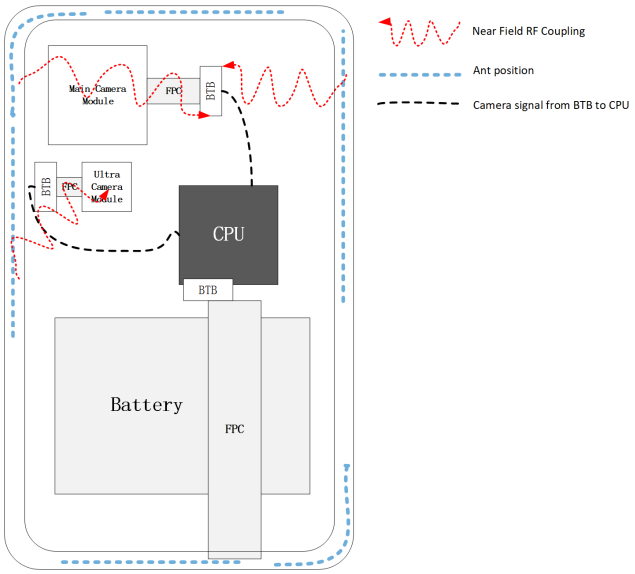

FIGURE 1. Block diagram of smart phone with camera MIPI C-PHY Interface.

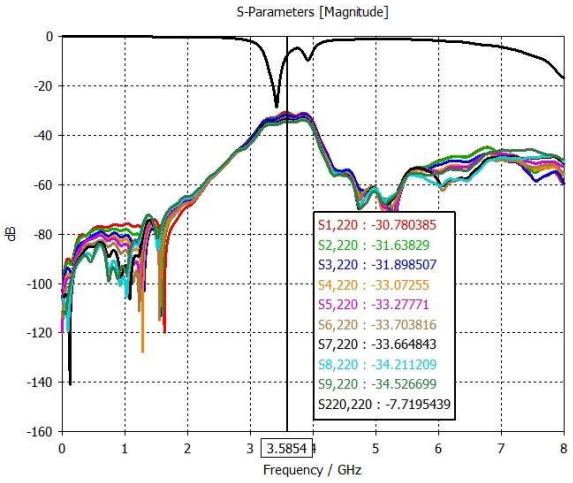

FIGURE 2. Isolation between smart phone antenna and MIPI C-PHY signals.

(3 lanes × 3 trio traces) of the Camera Module. As illustrated in Figure 1, the coupling path between the RF transmit antenna and the Camera Module C-PHY signal is denoted by the red dashed line with arrows, indicating the Near Field RF coupling. The RF energy from the antenna couples into the camera module, FPC, and BTB connectors. The isolation results reveal that the variation in isolation among C-PHY intra-lane signals is minimal, with differences not exceeding 1 dB. Consequently, the interference from the RF transmitter to the C-PHY signal can be approximated as common-mode noise interference. It may seem intuitive to employ Common Mode Filters (CMFs) to attenuate RF transmit interference that manifests as common-mode noise. CMFs have been widely employed in high-speed (HS) systems [4] to suppress common-mode noise emissions. These emissions can originate from the HS differential signals themselves or from the coupling of Double Data Rate (DDR) noise within the CPU. Previous studies [5] and [6] have demonstrated that CMFs can effectively attenuate common-mode noise generated by USB 3.0 interfaces, achieving a suppression of more than 10 dB in the corresponding RF bands. Furthermore, the design methodology for CMFs targeting the mitigation of common-mode radiated noise from PCIe Gen3/4 signals has been discussed in [7]. However, the effectiveness of CMFs in enhancing RF immunity for MIPI C-PHY is not universal; in some cases, the use of CMFs may not only fail to provide the desired immunity but could potentially exacerbate the issue. To address the challenges posed by RFI in high-resolution camera systems integrated into modern mobile devices, a comprehensive analysis is essential.

II. ISSUE ANALYSIS WITH RFI SIMULATION

This study employs simulation-based techniques to investigate the effectiveness of CMFs in mitigating RFI and to explore the impact of CMF placement on signal integrity and RF immunity. The simulations are utilizing Computer Simulation Technology (CST) [8], ANSYS High Frequency Structure Simulator (HFSS), and Keysight Advanced Design System (ADS) [9]. The aim is to provide insights into the optimization of CMF implementation strategies.

In the following section, a detailed examination of the radiated RFI issue is presented through simulation-based analysis. The simulation setup and methodology are described, and the key findings are discussed. The analysis focuses on the role of CMFs in enhancing RF immunity and the significance of CMF placement in relation to the noise source. The results obtained from this analysis contribute to the development of effective RFI mitigation techniques and design guidelines for high-speed digital interfaces in mobile devices.

A. MIPI C-PHY RADIATED RFI SIMULATION SETUP WITH CMF

The simulation model, depicted in Figure 3, is developed by integrating CST 3D, HFSS 3D layout, and ADS. CST 3D is utilized to determine the coupling between the smartphone antenna and the C-PHY signals of the camera module, while HFSS 3D layout is employed to extract the S-parameters of the C-PHY traces routing on the main Printed Circuit Board (PCB). The S-parameters obtained from these two simulations, along with the S-parameters of the CMF, are then incorporated into ADS to perform a comprehensive end-to-end simulation. This simulation model emulates the real-world camera RFI scenario in a smartphone, where RF energy is emitted from the antenna, couples to the MIPI C-PHY signal through near-field coupling, and ultimately reaches the CPU receiving end.

The camera sensor MIPI high-speed interface is modeled using an IBIS (I/O Input-Output Buffer Information Specification) model, which generates a MIPI C-PHY signal employing a three-wire signaling configuration. This signal is connected to the camera module part, where it becomes vulnerable to RF common-mode interference noise, primarily

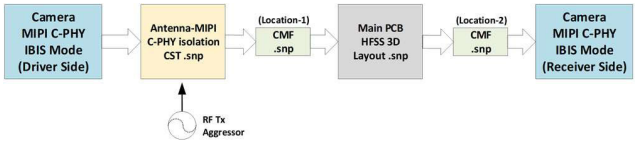

FIGURE 3. MIPI C-PHY radiated RFI simulation with CMF added.

induced by the antenna's near-field coupling through radiation. The desired MIPI C-PHY signal, along with the coupled unwanted RF transmit interference, propagates through the main PCB and finally arrives at the receiver's CPU IBIS model. The placement of the CMF plays a vital role in evaluating its effectiveness in enhancing camera RF immunity. Two potential locations are investigated: near the Camera BTB (Location-1 in Figure 3) and adjacent to the CPU (Location-2 in Figure 3). By observing key parameters of the high-speed [10], [11] interface signal at the CPU side, such as eye diagram (eye height and eye width), and the magnitude of the noise signal and phase difference between the noise signals, this setup enables an investigation into how the CMF contributes to resolving camera RF immunity issues.

B. CMF IMPACT WITHOUT RADIATED RFI

In the MIPI C-PHY link, the inclusion of a CMF in series is inevitably going to introduce additional signal attenuation. Furthermore, as mentioned in Section A, the placement of the CMF in the circuit can also affect the camera's immunity to RFI. Given this situation, we will first analyze the impact of the CMF on the MIPI C-PHY link in the absence of RF transmission interference. Based on the simulation model in Figure 3, we will analyze the effects of several typical manufacturer CMF models available on the market.

Figure 4 displays the eye diagram information with an eye probe output at the CPU Die, comparing the following three scenarios: without a CMF, with three commercial CMF models M/I/P placed near the BTB (Location-1) and near the end of the CPU chip (Location-2). The eye height and eye width information extracted from the eye diagrams in Figure 4 are exemplified in Table 1. From the table, it can be observed that placing the CMF near Location-1, which is close to the BTB, results in a more severe deterioration of the C-PHY EH(eye height) and EW(eye width) compared to placing it near the end of the CPU chip.

A detailed analysis will be conducted by examining the variations in Differential Mode (DM) impedance and Common Mode (CM) impedance across the entire C-PHY transmission link [12]. The simulation model, as illustrated in Figure 1, is modified by replacing the sensor IBIS model with a TDR source and the CPU IBIS model with a matching termination. This configuration allows for the observation of impedance changes from the sensor output port to the CPU input port. Figure 5 depicts the setup for the simulation, while Figure 6 presents the corresponding Time Domain Reflectometry (TDR) [13] results. By analyzing the TDR results, the impact of CMF placement at two distinct locations on its performance attributes can be elucidated.

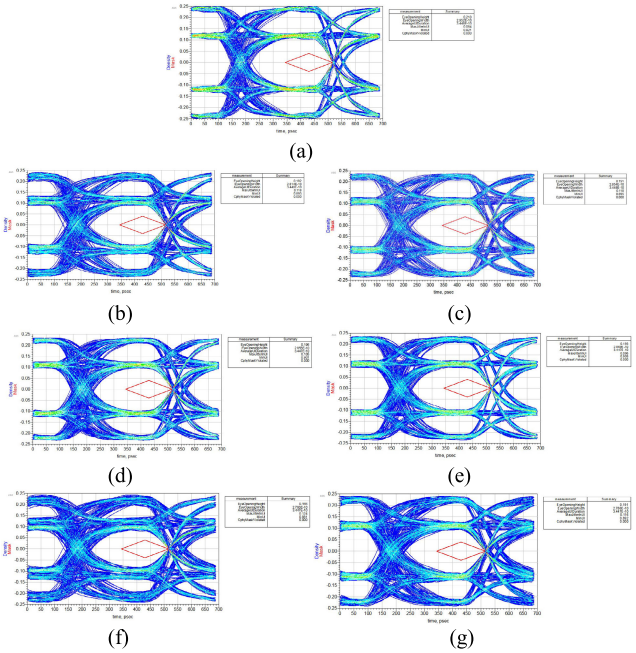

FIGURE 4. Eye Diagram at CPU Die (a) Without CMF (b) M-Model at Location-1 (c) M-Model at Location-2 (d) I-Model at Location-1 (e) I-Model at Location-2 (f) P-Model at Location-1 (g) P-Model at Location-2.

TABLE 1. EH and EW comparison.

CMF Model	EH/EW at Location-1	EH/EW at Location-2
Without CMF	EH:218mV, EW:295ps	
M-Model	EH:182mV, EW:282ps	EH:191mV, EW:283ps
I-Model	EH:196mV, EW:285ps	EH:193mV, EW:287ps
P-Model	EH:166mV, EW:279ps	EH:191mV, EW:279ps

Figure 6 illustrates the impedance profile variations as measured by TDR along the transmission path, extending from the output of the camera sensor to the input of the CPU. This comparison is made when three distinct models of CMFs are serially integrated at different locations within the circuit. The impedance contribution of the CMFs is indicated by the hatched regions in the Figure 6. TDR analysis across the link reveals that the differential impedance for both the camera's FPC and the mainboard is maintained at 90 Ω. In contrast, the BTB connector, due to its specialized structural connection mechanism—namely the snap-fit terminal structure of the mating connectors—presents a reduced differential impedance, close to 70 Ω. The CMF models, designed for broad application, exhibit varying differential impedances: the M/I- CMF models range from 100 to 110 Ω, while the P CMF model ranges from 110 to 120 Ω. Placement of the CMF proximal to the BTB connector results in a stark impedance transition from 70 Ω to upwards of 110 Ω, which, coupled with the intrinsic attenuation of the device and the resultant impedance mismatch, further exacerbates signal integrity as evidenced by the degradation of the

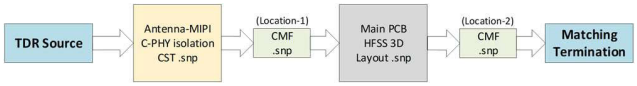

FIGURE 5. MIPI C-PHY TDR simulation with CMF added.

signal's eye height and eye width. Notably, the P-model CMF, with its marginally higher differential impedance relative to the M/I-models, is observed to induce the most pronounced degradation in these parameters when situated adjacent to the BTB connector.

Taking into account the specified target impedance for the complete C-PHY transmission pathway, as well as the impedance discontinuities introduced by BTB connectors, it is advisable to engineer the CMF to exhibit a differential impedance approximately 90 Ω. This design strategy aims to ensure that the CMF exerts minimal influence on the signal integrity of the MIPI C-PHY interface.

C. RADIATED RFI PERFORMANCE WITH CMF ADDED

Utilizing the simulation framework delineated in Figure 3, the analytical model has been streamlined by prescribing the interference source (denoted as RF Tx Aggressor) as a single-carrier RF signal. This signal has an output power of 33 dBm within the 3.5 GHz band, aligning with the 5G New Radio (NR) Band n78. C-PHY data rate setting to 2.9 Gsps/trio. As inferred from the model in Figure 2, the isolation from the antenna to the MIPI C-PHY interface is quantified to be in the vicinity of 31 dB. In pursuit of a rigorous evaluation of RF interference mitigation, this study embarks on a comparative analysis, scrutinizing the efficacy of the CMF in three distinct configurations: the absence of a CMF, the CMF sited at location-1, and the CMF positioned at location-2. The objective is to ascertain the CMF's role in the attenuation of RF interference and to discern the contributory factors that influence the resultant performance enhancements.

In Figure 7, a comparative assessment of eye diagram integrity is presented for three distinct configurations under the influence of RF interference. The configurations evaluated include scenarios absent of a CMF, with a CMF implemented proximal to the BTB, and with a CMF situated at the CPU input juncture. It is observed that the configuration lacking a CMF exhibits a complete breakdown in eye diagram fidelity, signifying a severe degradation in signal quality. In contrast, a marginal enhancement in performance is discernible when the CMF is positioned adjacent to the BTB connector, as opposed to its installation at the CPU input.

This phenomenon can be rationalized by considering the role of the CMF in mitigating common-mode noise from the beginning. The strategic placement of the CMF in close vicinity to the RF noise source enables it to attenuate the common-mode disturbances prior to their propagation through the transmission line, where they might otherwise encounter impedance discontinuities and give rise to signal reflections. Such reflections can compound the interference

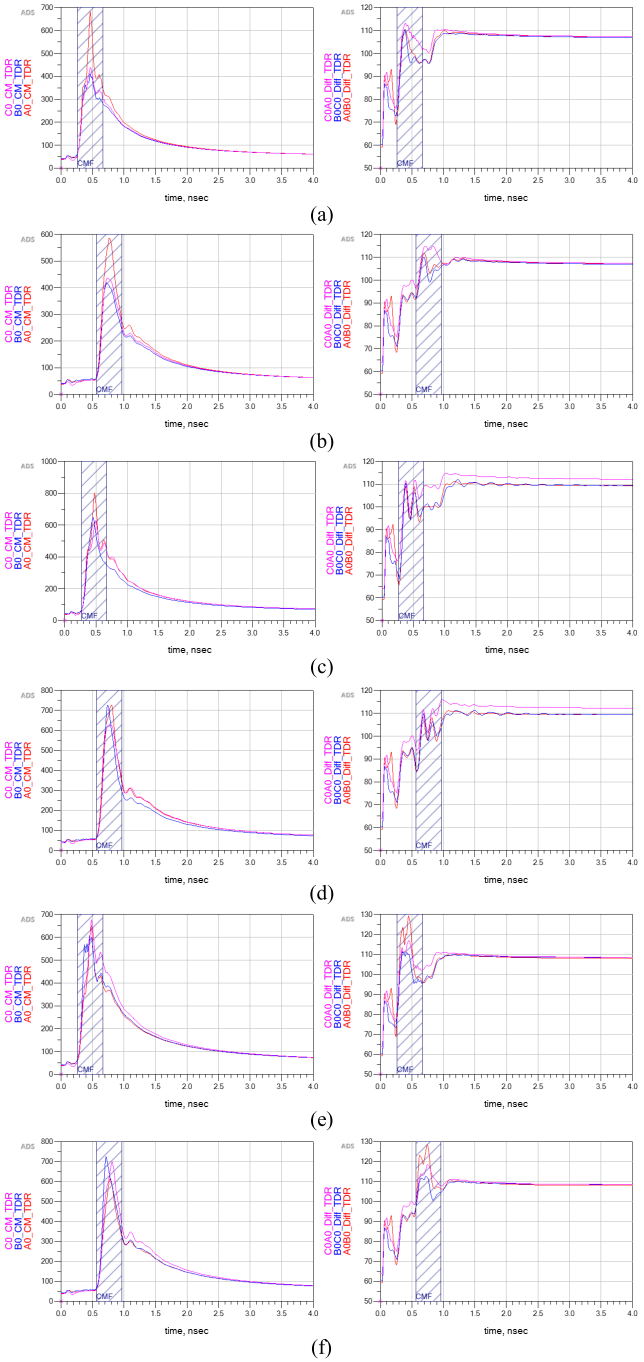

FIGURE 6. Common mode and differential mode TDR results with CMF (a) M-Model at Location-1 (b) M-Model at Location-2 (c) I-Model at Location-1 (d) I-Model at Location-2 (e) P-Model at Location-1 (f) P-Model at Location-2.

effects, further compromising the signal integrity. Hence, the reduced proximity between the CMF and the noise source serves to diminish the potential for noise-induced reflections, thereby preserving the integrity of the desired signal and enhancing the overall signal-to-noise ratio within the system. This insight underscores the significance of CMF placement in the design and optimization of high-speed digital communication interfaces, particularly in environments susceptible to RF interference.

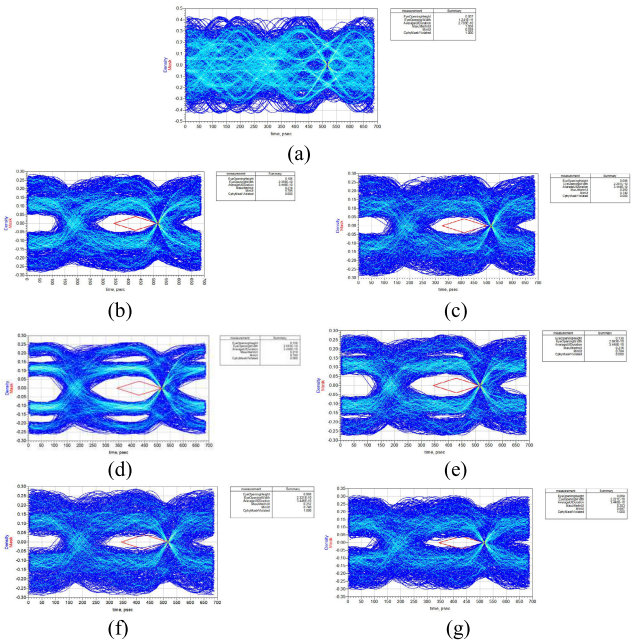

FIGURE 7. Eye Diagram at CPU Die (a) Without CMF (b) M-Model at Location-1 (c) M-Model at Location-2 (d) I-Model at Location-1 (e) I-Model at Location-2 (f) P-Model at Location-1 (g) P-Model at Location-2.

III. RECEIVER COMPENSATION TECHNIQUES

Section II-C examines the degradation of the C-PHY signal eye diagram under RFI conditions, contrasting scenarios without a CMF against those with three distinct CMF models situated in two separate locations, totaling seven conditions. This section delves into the potential for improving the resilience of the C-PHY signal to RFI at the CPU receiver end through algorithmic enhancements.

In principle, differential signals have the characteristic of being immune to RF common-mode noise. If the transmission path including antenna isolation and trace routing are perfectly symmetrical, then the RF common-mode interference signals would be completely canceled out at the CPU's differential interface, leaving no differential interference signal at the receiver end. However, during signal transmission, due to unbalance antenna to C-PHY trace coupling, trace asymmetry, asymmetries in the BTB connectors, and potential asymmetries introduced by additional CMFs, the common-mode RFI signals that reach the differential ports may exhibit different phases and amplitudes. The magnitude and phase differences of these signals vary with the frequency of the RF interference. When the two interference signals are differentially subtracted, they produce a differential-mode interference signal, which can result in decoding failures at the CPU chip end.

A. RFI NOISE PRESENTED AT RECEIVER SIDE

Utilizing the simulation model depicted in Figure 3, we activated the C-PHY driver and receiver models without transmitting the C-PHY signal. This setup facilitated the observation of the inherent characteristics of RFI signals at the CPU receiver end. As illustrated in Figure 8, the RFI observed at the CPU Die end manifests as single-ended noise (left) and differential noise signals (right). Analysis of the output waveforms revealed the following:

1) In the absence of a CMF, the amplitude of the single-ended interference noise signal detected at the receiver end was found to be approximately +/−450 mV.
2) Implementing three distinct CMF models effectively attenuated the interference noise signal amplitude to below +/−50 mV, thereby substantially mitigating RF noise interference. The magnitude of the differential noise signal is contingent upon the amplitude and phase discrepancies between the single-ended noise signals A0, B0, and C0.
3) Specifically, Figure 8 (d) shows that due to minimal amplitude and phase variances in the single-ended noise signals, the resultant differential noise signal is constrained to less than 25 mV.
4) Conversely, Figure 8 (f) reveals that the single-ended noise signal for path C0 exhibits a substantial deviation in both amplitude and phase relative to paths A0 and B0, culminating in a differential noise signal approaching 50 mV post-subtraction.
5) While CMFs are capable of substantially diminishing the amplitude of common-mode signals, their efficacy in resolving RFI challenges is significantly hampered by the intrinsic imbalances present in the tri-path design. These imbalances introduce notable discrepancies in timing and amplitude, thereby constraining the potential benefits in RFI mitigation.

B. PROPOSED RECEIVER COMPENSATION TECHNIQUES WITHOUT CMF

To mitigate RFI without the use of CMFs, we initiate our approach by focusing on the adaptability of the CPU receiver. An examination of the single-ended RF noise waveforms for outputs A0, B0, and C0, as depicted in Figure 8(a), reveals a slight temporal lead in the A0 and B0 signals relative to C0. This observation guides the subsequent fine-tuning process. Adjustments to the A0 and B0 delays are implemented within the simulation environment outlined in Figure 3, with A0 and B0 delays set to 15 ps and 10 ps respectively, while maintaining C0 at its original setting. This calibration is intended to refine the C-PHY eye diagram in the presence of RF noise.

It is important to note that the delay modifications for A0 and B0, amounting to approximately 5% of the C-PHY Unit Interval, are marginal and thus exert minimal perturbation on the integrity of the original C-PHY signal.

The fruits of this optimization are evident in the data presented in Figure 9. It shows a substantial reduction in differential noise levels from approximately 180 mV, as seen in Figure 8(a), to approximately 40 mV. Correspondingly, the eye diagram metrics exhibit marked improvement, with EH reaching 155 mV and EW extending to 272 ps, a significant enhancement over the results displayed in Figure 7(a).

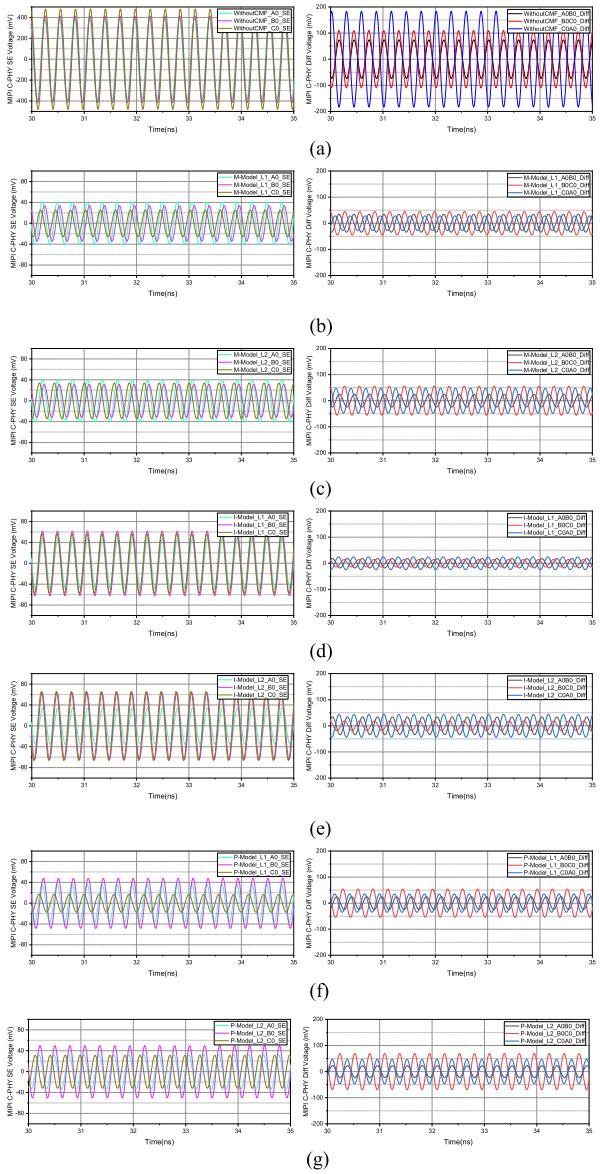

FIGURE 8. RF Noise Only at CPU Die (a) Without CMF (b) M-Model at Location-1 (c) M-Model at Location-2 (d) I-Model at Location-1 (e) I-Model at Location-2 (f) P-Model at Location-1 (g) P-Model at Location-2.

In conclusion, the strategic intra-lane time delay adjustments at the CPU receiver, aimed at achieving phase synchronization across the tri-path configuration, effectively mitigate differential noise. This is accomplished by minimizing the resultant noise signal through the differential combination of the three paths, thereby preserving the fidelity of the C-PHY signal without introducing significant degradation. This methodology underscores the importance of precision in timing calibration to ensure robust signal integrity in high-frequency digital interfaces.

C. PROPOSED RECEIVER COMPENSATION TECHNIQUES WITH CMF

When excessive RF noise is superimposed on MIPI signals, causing the single-ended amplitude of the C-PHY signal to exceed the safe threshold levels of the CPU chip, it becomes necessary to incorporate a CMF to attenuate the RF noise. This reduction ensures that the overall signal amplitude remains within the safe operating range for high-speed interfaces. However, the inclusion of a CMF may inadvertently introduce amplitude and phase imbalances within the MIPI link, as indicated by the experimental outcomes presented in Figure 8. To compensate for these imbalances, it is essential to fine-tune the delay across the three MIPI lanes.

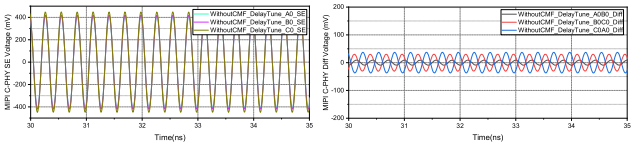

FIGURE 9. RF noise only at CPU Die without CMF (A0 delay15ps, B0 delay10ps).

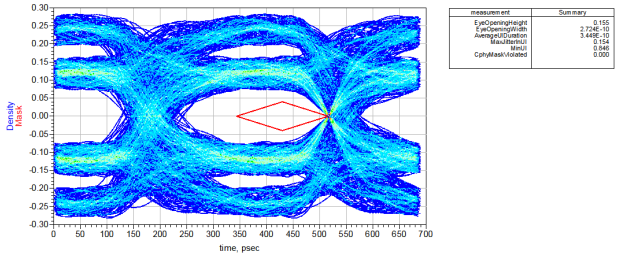

FIGURE 10. Eye diagram (RF Noise overlap C-PHY signal) at CPU Die without CMF (A0 delay15ps, B0 delay10ps).

In the subsequent discussion, we examine a specific scenario wherein three CMF modules are strategically positioned in proximity to the BTB. This case serves to exemplify the practical application of the principle previously outlined. Drawing parallels to the methodology delineated in Section III without CMF part, this approach entails the meticulous adjustment of phase discrepancies among the triad of noise signals (A0, B0, C0) received by the CPU. The objective of this adjustment is to align the RF noise signals towards a coherent phase state. Such alignment is instrumental in enhancing the efficacy of differential noise mitigation strategies. This technique underscores a deliberate manipulation of signal phase relationships, aiming to optimize the MIPI link's robustness against RF interference.

Due to the constraints of symmetry in the CMF structure design, additional discrepancies in time delay were introduced. Observations from Figure 8(b) (d) (f) reveal differential time delays in RF noise across three pathways. Subsequent adjustments in time delay for each of the three CMF types resulted in the improved noise waveforms depicted in Figure 11 (a) (b) (c), with the corresponding eye diagram conditions illustrated in Figure 11 (d) (e) (f). The data in Table 2, titled "Comparison of Differential RF Noise and EH/EW Before and After Delay Tuning," include specific time delay settings, with the 'before delay tuning' data extracted from Figure 7 (b) (d) (f) and Figure 8 (b) (d) (f). The results clearly demonstrate that synchronizing the signal phases across the three pathways, thereby reducing RF noise, significantly enhances the quality of the MIPI C-PHY eye

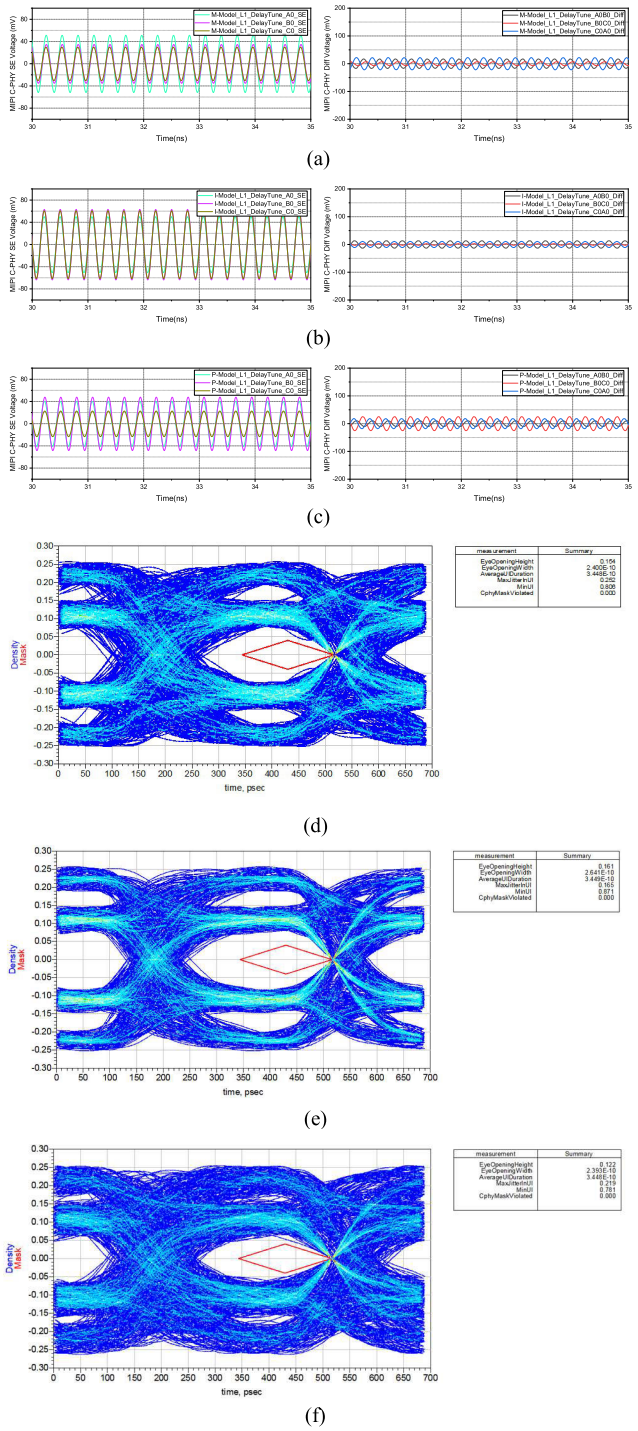

FIGURE 11. RF noise after delay tuning at CPU Die with CMF (a) M-Model (b) I-Model (c) P-Model; Eye diagram (RF Noise overlap C-PHY signal) after delay tuning at CPU Die with CMF (d) M-Model (e) I-Model (f) P-Model.

diagrams in the presence of RF noise (e.g., an increase of 54 mV in EH at P-Model). It is noteworthy that M/P-Model exhibit relatively large inherent time delay discrepancies due to the CMF design (a delay of 65-70 ps on the C0 path, which is close to 20% of the Unit Interval). This excessive time delay discrepancy not only affects the quality of the MIPI C-PHY signal itself but also limits the effectiveness of the optimization.

TABLE 2. Comparison of differential RF noise and EH/EW before and after delay tuning.

CMF Model and Delay Tuning Setting	DM Noise Before Tuning	DM Noise After Tuning	EH/EW Before Tuning	EH/EW After Tuning
M-Model A0 delay 45ps, C0 delay 65ps	~±50mV max	~±25mV max	EH:106mV, EW:239ps	EH:154mV, EW:240ps ↑ 48mV increase in EH
I-Model B0 delay 10ps, C0 delay 20ps	~±25mV max	~±15mV max	EH:150mV, EW:268ps	EH:161mV, EW:264ps ↑ 11mV increase in EH
P-Model A0 delay 20ps, C0 delay 70ps	~±55mV max	~±30mV max	EH:68mV, EW:221ps	EH:122mV, EW:239ps ↑ 54mV increase in EH

In scenarios where further optimization of the C-PHY's resistance to RF interference noise is required, it may be necessary to reduce the MIPI rate to mitigate the adverse effects of excessive time delay adjustments. This approach underscores the delicate balance required between maintaining signal integrity and optimizing for noise reduction in high-speed digital interfaces.

When employing CMFs to suppress CM radiation noise in high-speed signals, it is crucial to focus on mixed-mode S-parameters [14], particularly Scc21 and Scd21. The study presented in [15] discusses design methodologies for enhancing Scc21, while the research in [16] proposes that improving Scd21 is essential for reducing cable radiation emissions and common-mode currents. These parameters are critical as they measure the common-mode to common-mode and common-mode to differential-mode transmission, respectively, providing insights into the effectiveness of CMFs in mitigating unwanted noise [17].

However, when applying CMFs to the MIPI C-PHY interface, the emphasis shifts towards maintaining timing and amplitude balance among the tri-path configuration. To optimize CMF performance in this scenario, minimizing timing and amplitude imbalances among the tri-path signals is essential. This could be achieved through careful design considerations, including ensuring equal path lengths and impedance matching, when utilizing CMFs to address RFI issues in camera interfaces. It is imperative to consider both Scc21, Scd21 and minimize differences in time delay and insertion loss among the three CMF pathways.

IV. CONCLUSION

The advent of high-resolution camera integration in mobile phones has necessitated the adoption of advanced MIPI C-PHY interface technologies for efficient data transmission. However, the compact design of contemporary mobile devices introduces a susceptibility to RFI, potentially degrading the signal quality and resulting in visual anomalies on device displays. This paper presents a comprehensive study on the efficacy of CMFs in mitigating RFI within the MIPI C-PHY interface, with a focus on simulation-based analysis to determine the impact of CMF placement on RF immunity enhancement. Our findings indicate that the proximity of CMF placement to the noise source—specifically, near the BTB connector rather than at the CPU input—significantly influences the effectiveness of common-mode disturbance attenuation, thereby preserving signal integrity and enhancing user experience.

Further, Section III of this study delves into receiver compensation techniques aimed at bolstering the resilience of C-PHY signals against RFI. We underscore the differential signal's inherent immunity to RF common-mode noise under conditions of ideal symmetry and address the challenges posed by imbalances, such as antenna to MIPI trace coupling, trace asymmetry, and discrepancies introduced by CMFs. These imbalances can result in differential-mode interference signals due to phase and amplitude differences in common-mode RFI signals. We propose strategies for mitigating RFI at the CPU receiver end, including the fine-tuning of delays within signal paths to minimize differential noise. Our analysis demonstrates significant improvements in eye diagram metrics, underscoring the critical role of precise time delay adjustments in conjunction with CMF usage to counteract inherent imbalances and optimize signal integrity and noise reduction in high-speed digital interfaces.

This paper contributes to the field of RF/EMC/SIPI by providing insights into the strategic placement of CMFs and the implementation of receiver compensation techniques as effective measures to combat RFI in MIPI C-PHY interfaces, thereby ensuring the reliability and performance of high-resolution camera systems in mobile devices.

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