RESEARCH ARTICLE

A Fast-Transient Output-Capacitor-Less Low-Dropout Regulator With Direct-Coupled Slew Rate Enhancement

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ABSTRACT An output capacitorless low-dropout (OCL-LDO) regulator with a direct-coupled slew rate enhancement (DCSRE) technique. This paper proposes a low-dropout regulator with a simple structure, fast transient response, and the ability to reduce overshoot and undershoot, suitable for system-on-chip (SOC) integration. Instead of a high-pass filter, an error amplifier is used to couple the transient signal to achieve better transient response with higher current efficiency and no significant increase in chip area and power consumption, eliminating the tradeoff with the high-pass filter cutoff frequency and simplifying design considerations. Furthermore, the proposed technique would not affect other characteristics of the LDO regulator such as stability, frequency compensation, line regulation, and load regulation. In addition, the analysis is carried out for the case of many poles and zeros in the unity-gain bandwidth (GBW). From the measurement result, the proposed LDO regulator regulated the output voltage at 1 V from the input range 1.8V up to 3.3V, with $28.8\mu A$ quiescent. The output voltage recovers in $0.23\mu s$ at a voltage spike of less than 43.5mV, where the load current switches from $100\mu A$ to 100mA in 100ns. The LDO regulator is fabricated in a $0.18\mu m$ CMOS process with a core area of $0.0174mm^2$.

I. INTRODUCTION

The OCL-LDO regulator [1], [2], and [3] is a widely used power management IC in practical applications and a promising area of research. It offers advantages over the output capacitor-less low-dropout (OCL-LDO) regulator [4], [5], and [6], such as easy integration with other circuits, fewer

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parasitic effects of wire bonds, and faster transient response. However, designing the stability compensation is relatively more difficult and complex. On the other hand, the excessive overshoot and undershoot caused by the capacitor-less design is also a shortcoming of the OCL-LDO regulator that needs to be improved. Improvements can be made in three ways to ameliorate the problem of excessive voltage variations during transients. Firstly, to improve the f_{-3dB} bandwidth [7], due to the faster response to high frequency with larger

FIGURE 1. Capacitive-coupled slew rate enhancement circuits.

FIGURE 2. Different high-pass filter cutoff frequencies.

FIGURE 3. Coupled signals with different cutoff frequencies.

bandwidth, and the shorter response time of the system in the time domain, the whole system can respond earlier to voltage variations caused by the output, which not only shortens the transient time, but also reduces the transient voltage variations caused by the load transition. Secondly, the LDO regulator is designed as an overdamped system to reduce transient voltage variations. This typically involves stability compensation [8], [9], [10], [11]. Thirdly, to increase the slew rate of the LDO regulator [12], [13], the subsequent problem is that the quiescent current would increase. In the previous literature such as [14], [15], and [16], the transient signal is coupled to the enhancement circuits or transistor by a high-pass filter to increase the transient slew rate, as shown in Fig. 1. In addition, the cutoff frequency fc of the high-pass filter composed of C_X and R_X is particularly critical to the effect of slew-rate enhancement. If the cutoff frequency is lower, this means that the charging time is longer. The ΔV signal can pass for a longer period, as shown in the blue part of Fig. 2, which is positive for slew rate improvement. However, it will cause the accuracy, line regulation, and load regulation of the output voltage of the LDO regulator to decrease. This is because even low-frequency signals can pass through the filter and cause the M_X to generate a ΔI current that changes the bias voltage. The additional slew rate enhancement circuit is not related to V_{ref}, whereas the error amplifier on the main path tracks V_{ref} and the two interfere with each other. On the other hand, a high cutoff frequency has less effect on the accuracy of the output voltage of the LDO regulator, but fewer signals would be coupled to it. As shown in the red part of Fig. 3, most of the time the slew rate enhancement circuit would not operate or would only operate for a short time, so the effect on slew rate enhancement is limited.

In conclusion, the higher the cutoff frequency, the less it affects the output voltage accuracy of the LDO regulator, but also the less the slew rate enhancement effect. The lower the cutoff frequency, the greater the effect of slew rate enhancement, but the worse the interference with the
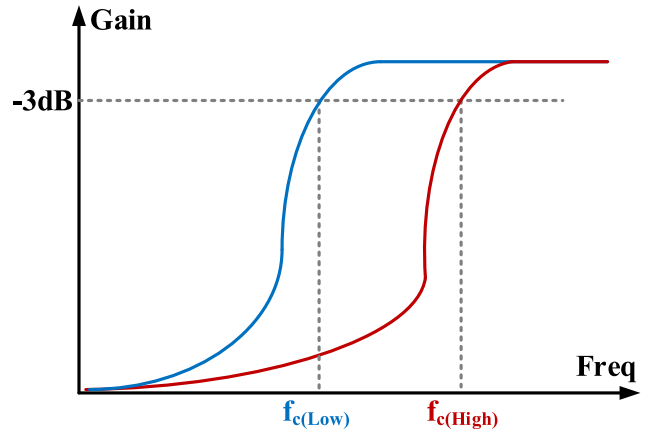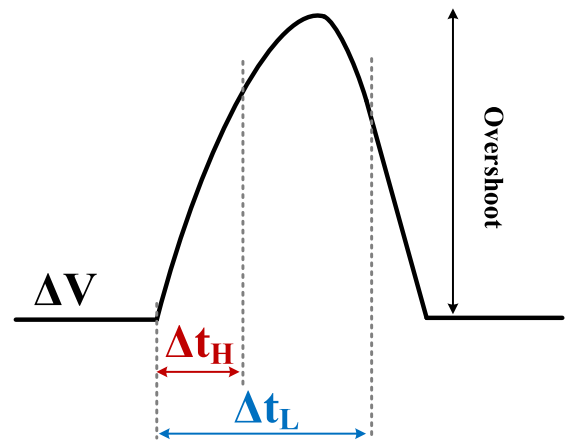
accuracy of the output voltage of the LDO regulator. On the other hand, the voltage variation ΔV during the load transition is coupled to the gate of the M_X transistor through C_X, and the parasitic capacitance C_{gs} connected to C_X in a series structure, ΔV is the analog voltage, which means that the change is small, and because the series structure of the capacitor caused by the voltage drop, it is further shrunk. So ΔV_X is usually only a few tens of mV or less, to increase of ΔI is actually quite limited. Therefore, the width of the M_X transistor must be increased to compensate for this, which also leads to an increase in the quiescent current. In short, this technique is inefficient in current efficiency and weak in slew rate enhancement.

Therefore, if the amplitude of the signal on the transistor gate in the enhancement circuit is increased, the current efficiency is improved. A comparator is inserted between the high-pass filter and the gate to enhance the signal amplitude to turn the analog signal into a digital signal [17]. In this technique, which is achieved by inserting a high-pass filter at one of the inputs of the comparator, the differential pair of the comparator cannot be designed to equalize the two inputs and the high-pass filter must be designed to a weaker at one
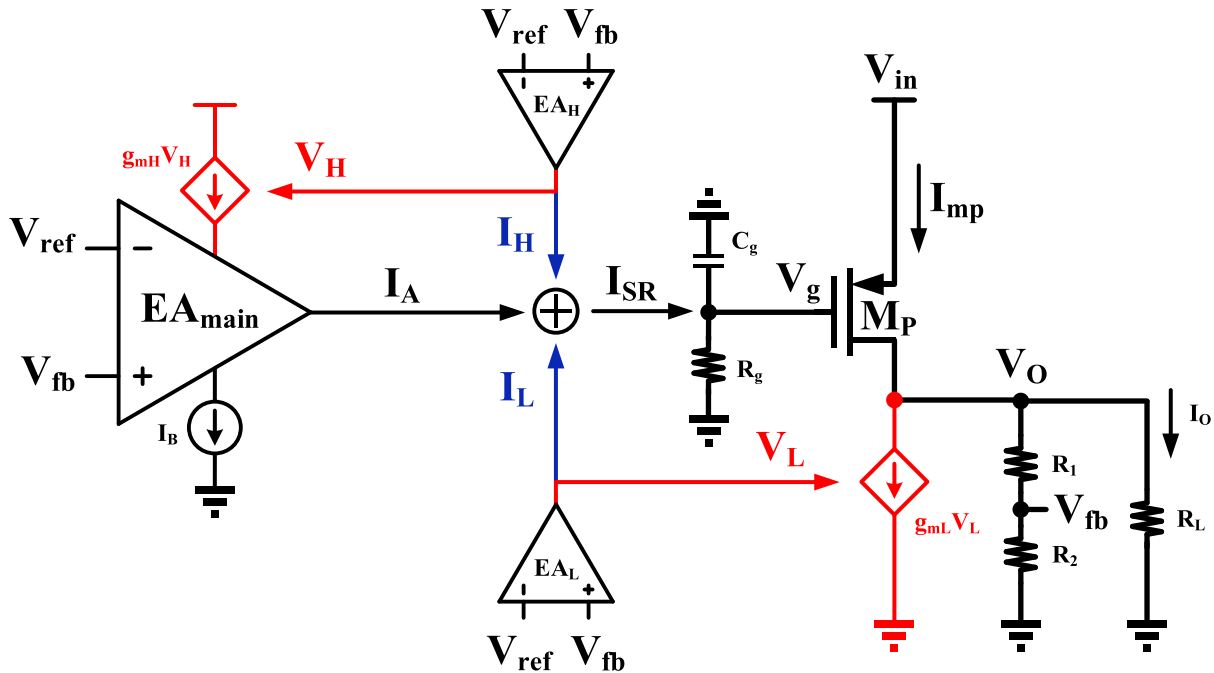
FIGURE 4. Proposed LDO regulator structure.

of the inputs to offset the voltage drop caused by the resistor of the high-pass filter, which results in a circuit that is more sensitive to process, voltage, and temperature variations, and still require a tradeoff in the cutoff frequency of the high-pass filter. Reference [18] detects the gate variations of power transistors, replicates the output current I_{OUT} which is shrunk by a factor of N, and then injects the current $(IOUT/N) \times K$ into the error amplifier as the adaptive bias current I_{AB} by current mirrors, which is able to increase the slew rate and also increase the bandwidth, but the improvement is only achieved when the output current is increased from light to heavy loads. In [19], after detecting the output voltage by another error amplifier, the bulk voltage of the power transistor is controlled by adjusting the g_{mb} to increase the slew rate, which is very effective but causes a serious body effect in the power transistor [20], resulting in a limitation of the maximum output current. Reference [21] added a P-type transistor M_{BOUT} between the output V_{OUT} and G_{ND} to increase the slew rate and reduce the transient variations but at the expensive cost of a large chip area.

Therefore, in this paper, an efficient direct-coupled slew rate enhancement technique is proposed for OCL-LDO regulators, which achieves transient performance enhancement without significant increase in area and power consumption, and the effects of slew rate on overshoot and undershoot of LDO regulators are discussed. Moreover, the proposed technology would not affect the stability, frequency compensation, line regulation, and load regulation of the LDO regulator, and more importantly, other techniques could be combined and achieved on the circuits. The paper is organized as follows. Section II explains the proposed circuits and

analyses the transients; Section III discusses the stability and small signal analysis of the proposed LDO regulator circuit. In Section IV, all the measurements are presented and compared with the recent literature, and finally, in Section V, the conclusion is given.

II. STRUCTURE AND CIRCUITS OF THE PROPOSED LDO
A. STRUCTURE AND CIRCUITS
The structure of the proposed LDO regulator is shown in Fig. 4. It consists of the main error amplifier EA_{main} and the auxiliary amplifiers EA_H and EA_L, which are the main path controlled by EA_{main}, the second path formed by the EA_H, and the third path formed by the EA_L, respectively. The path controlled by EA_H and EA_L will generate $g_{mH}V_H$, $g_{mL}V_L$, I_H, and I_L, where the currents I_H and I_L are combined with the output current I_A of EA_{main} to become the current I_{SR}. The current I_{SR} combined with the output impedance R_g of the error amplifier and the parasitic capacitance C_g of the power transistor gate to ground generates the voltage V_g to control the power transistor M_P to generate Imp current. The $g_{mL}V_L$ current is subtracted from the Imp current (ignoring the very small currents in the feedback resistors R_1 and R_2) to form the output current I_O at the load. On the other hand, the current $g_{mH}V_H$ is combined with the bias current I_B to increase the tail current of the EA_{main} during the transition from light to heavy load, while the current $g_{mL}V_L$ increases the discharge current of the output V_O during the transition from heavy to light load. The proposed LDO transistor level circuit is shown in Fig. 5. The EA_{main} consists of $M_1 \sim M_4$ by I_B current source for bias current, M_1, M_2 with NMOS differential pair M_3, M_4 with current mirror active load. The drain of M_1 and
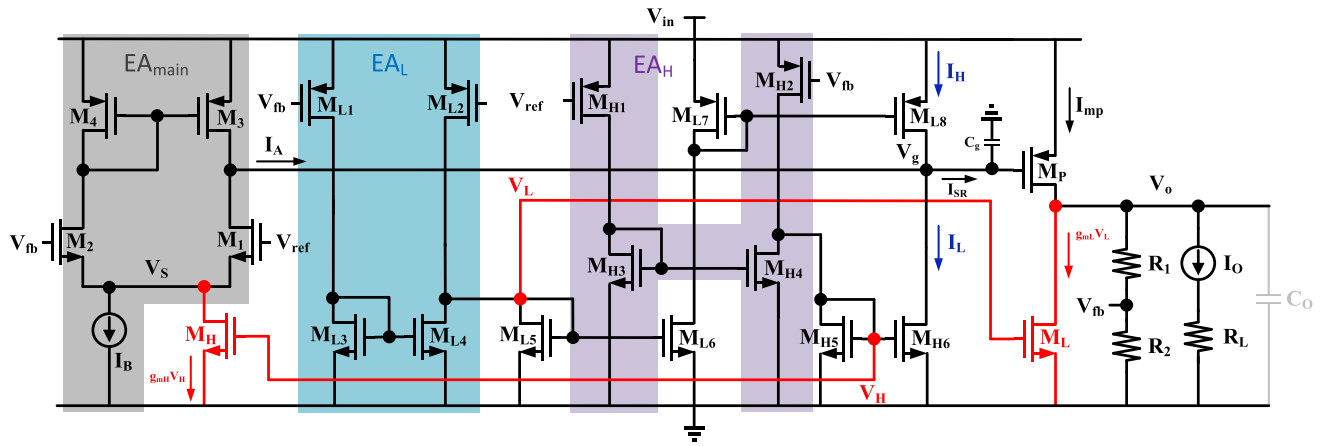
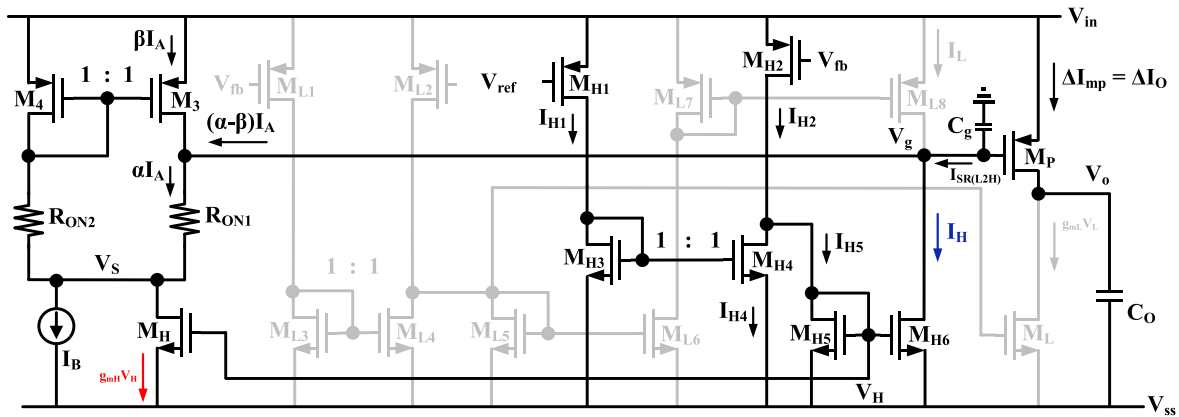**FIGURE 5.** Proposed LDO regulator circuits.

FIGURE 6. Transient operation from light load to heavy load.

M_3 is connected to the gate V_g of M_P. EA_L is composed of $M_{L1} \sim M_{L4}$ and EA_H is composed of $M_{H1} \sim M_{H4}$. The M_{L1}, M_{L2}, and M_{H1}, M_{H2} are PMOS differential pairs and have no bias current source. On the other hand, M_{L3}, M_{L4}, and M_{H3}, M_{H4} are active loads. The $M_{L5} \sim M_{L8}$ and M_{H5}, M_{H6} are current mirrors to amplify the output currents of EA_L and EA_H and connect them to V_g, and eventually, the currents I_H, I_L, and I_A flow together to become the current I_{SR} to charge or discharge C_g. The M_L and M_H transistors are controlled by the output voltages V_L and V_H of EA_L and EA_H, which consume only a tiny quiescent current during steady state, primarily designed to improve the transient response and slew rate of EA_{main} and V_O during the load transient period.

B. TRANSIENT RESPONSE

The direct-coupled slew rate enhancement (DCSRE) technique is proposed in this paper. To eliminate the tradeoff between the cutoff frequency of the high-pass filter as in capacitive-coupled enhancement circuits, and operate in the unity-gain bandwidth of the amplifier. Increasing the static current of the auxiliary amplifier also improves the bandwidth

resulting in a faster response and better slew rate. In addition, the coupling with an auxiliary amplifier offers the advantages of greater amplitude, better slew rate enhancement, and better current efficiency than capacitive-coupled. The transient response of the LDO regulator for light load to heavy load and heavy load to light load, respectively. Thus, the transient response is discussed in two parts.

Case I($I_{O(light)} \rightarrow I_{O(heavy)}$): When the load is transiting from light load to heavy load, the circuit operation is as shown in Fig. 6. The output voltage V_O is not sufficient to respond to the load drop due to the output current I_O. The V_{fb} is connected to the gate of M_2 in the NMOS differential pair of EAmain, and V_{ref} is connected to the gate of M_1. At this time, the V_{fb} voltage is lower than the V_{ref} voltage. Thus, the on-resistance R_{ON1} of M_1 is smaller than the on-resistance R_{ON2} of M_2, and therefore, the αI_A current is larger than the βI_A current. V_{ref} and V_{fb} are connected to the gate of M_{H1} and M_{H2} in the PMOS differential pair of EA_H auxiliary amplifier. I_{H2} is lower than V_{ref} because of V_{fb} voltage, which results in the V_{GS} voltage of M_{H2} being larger than that of M_{H1}, so the I_{H2} current is larger than that of I_{H1}. The M_{H3}
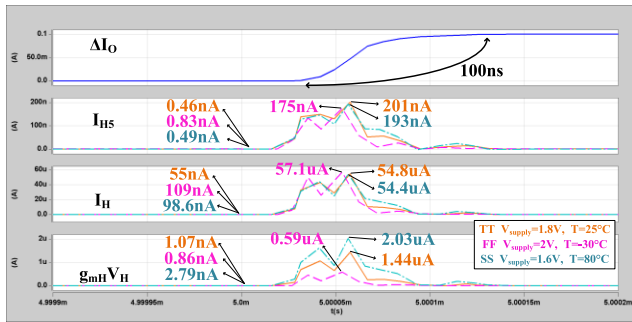
FIGURE 7. Various currents from light load to heavy load.

FIGURE 8. Output variation from light load to heavy load.

and M_{H4} are the same length and width size of the current mirror so the I_{H1} current is equal to the I_{H4} current, while the I_{H5} current is equal to the I_{H2} current subtracted by I_{H4}. The I_{H5} current and the equivalent impedance of M_{H5} form the V_H voltage to control M_{H6} to generate the I_H current and connect to the M_P gate. Hence, the I_H is the M multiple of I_{H5}, and then the charging current $I_{SR(L2H)}$ of C_g is the $(\alpha-\beta)I_A$ current combined with the I_H current.

The current transient of the EA_H amplifier is shown in Fig. 7, which contains three different process corners. In case of TT, when ΔI_O changes from $100\mu A$ to $100mA$ with the edge time of $100ns$, the detected change of ΔI_O. The I_{H5} current increases from $0.5nA$ in a steady state to a maximum peak of $201nA$. The I_H current also increases from $55nA$ to a maximum peak of $54.8\mu A$, and the $g_{mH}V_H$ current increases from $1.07nA$ to a maximum peak of $1.44\mu A$. Regardless of how the current varies during the transient, after the output current I_O is stabilized, I_{H5}, I_H, and $g_{mH}V_H$ will return to the original current state before the transient, which means that the transient current only increases during the transient, and the quiescent current consumption is quite low during steady state. Fig. 8 shows the before and after comparisons with and without the direct-coupled transient enhancement technique. The red dotted line shows the transient response of the LDO regulator without DCSRE, the edge time of the I_O transition from $100\mu A$ to $100mA$ is $1.3\mu s$, and the settling time of the V_O is also $1.3\mu s$, with the undershoot is $849mV$. On the other hand, Fig. 9 shows the transient response of the LDO regulator with DCSRE, the edge time of I_O is $100ns$, in case of TT the settling time of V_O is $180ns$, with the undershoot is $42mV$.

Case II($I_{O(heavy)} \rightarrow I_{O(light)}$): When the load is transiting from heavy load to light load, the circuit operation is shown in Fig. 10. The output voltage V_O is overly high due to the excessive output current I_O, and the V_{fb} voltage is higher than V_{ref} voltage at this time. Therefore, the on-resistance R_{ON2} of M_2 is smaller than the on-resistance R_{ON1} of M_1, and hence the βI_A current is larger than the αI_A current. In addition, V_{ref} and V_{fb} are connected to the gate of M_{L1} and M_{L2} in the PMOS differential pair of the EA_L auxiliary amplifier. Due to the higher V_{fb} voltage than V_{ref}, M_{L2}'s VGS voltage is greater than M_{L1}, so I_{L2} current is greater than I_{L1}. The size
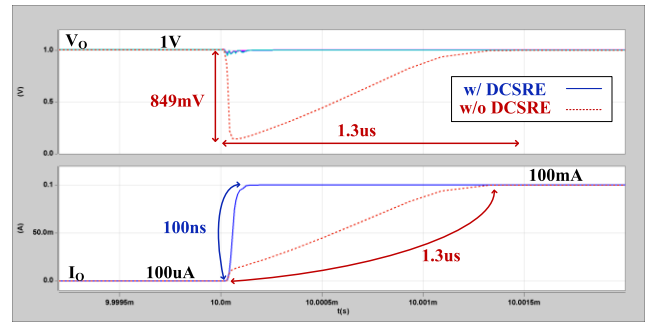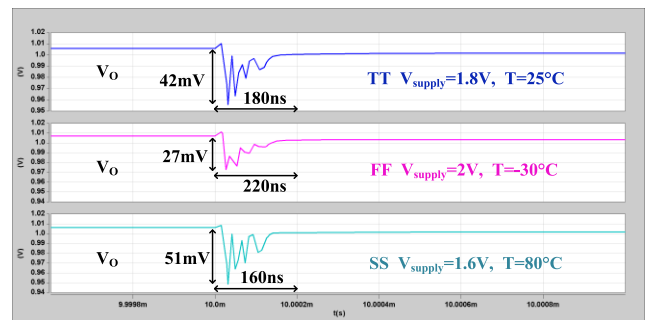

FIGURE 9. Zoom in on output variation from light load to heavy load.

that the current mirrors on M_{L3} and M_{L4} is the same, so I_{L1} current equals I_{L4} current, and I_{L5} current equals I_{L2} current subtracted from I_{L4} current. V_L voltage control M_{L6} is formed by combining M_{L5} current and M_{L5} equivalent impedance and then connecting it to M_P gates.

The current transient of the EA_L amplifier is shown in Fig. 11, which contains three different process corners. In case of TT, when ΔI_O changes from $100mA$ to $100\mu A$ with an edge time of $100ns$, the I_{L5} current detected the change of I_O from $0.2nA$ in steady state to the maximum peak is $76.4nA$. The I_L current also starts to increase from $39.2nA$ to the maximum peak is $48.8\mu A$, and the $g_{mL}V_L$ current starts to increase from $1.04nA$ with a maximum peak of $982nA$. Regardless of how the current varies during the transient, after the output current I_O is stabilized, I_{L5}, I_L, and $g_{mL}V_L$ will return to the original current state before the transient. Fig. 12 shows the before and after comparisons with and without the direct-coupled transient enhancement technique. The red dotted line shows the transient response of the LDO regulator without DCSRE, with an edge time of $130ns$ for the I_O transition from $100mA$ to $100\mu A$, a settling time of $1.3\mu s$ for V_O, and an overshoot of $800mV$. Alternatively, Fig. 13 shows the transient response of the LDO with DCSRE at TT, for an output current edge time of $100ns$, a settling time of $260ns$, and an overshoot of $35mV$. The quiescent current distributions under three different process corners can be observed in Fig. 14, with variations of $V_{supply} \pm 2V$ and Celsius $\pm 55C°$, respectively. The I_Q of FF increases by 77%, while the I_Q of SS decreases by 31%.
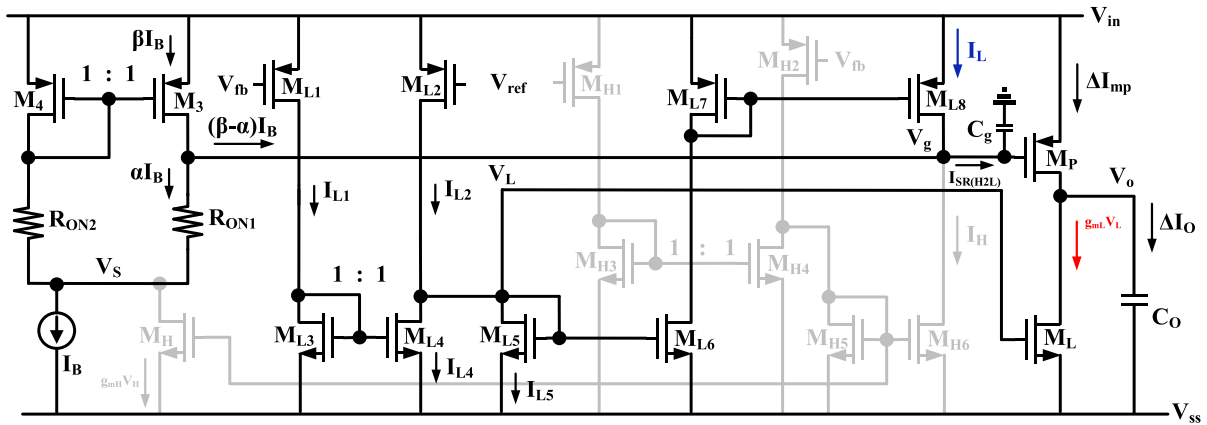
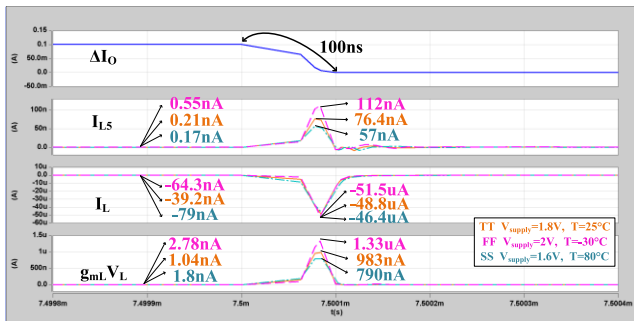**FIGURE 10.** Transient operation from heavy load to light load.

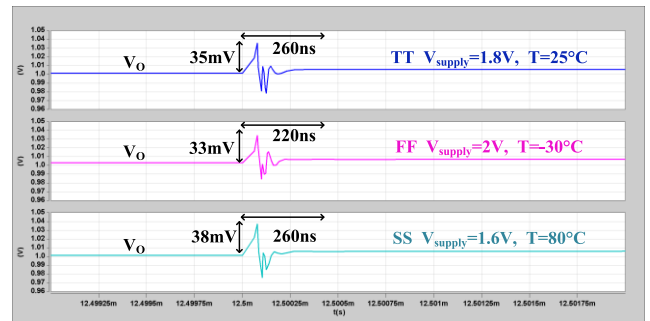**FIGURE 11.** Various currents from heavy load to light load.

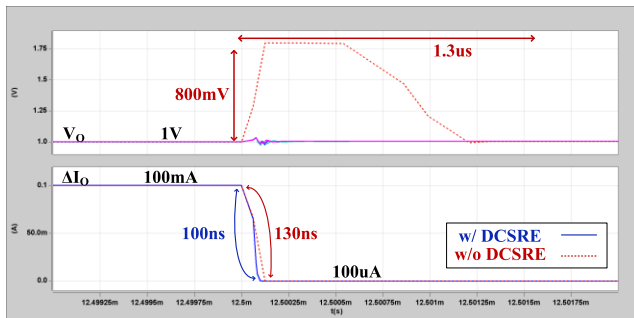**FIGURE 13.** Zoom in on output variation from heavy load to from light.

FIGURE 12. Output variation from heavy load to from light.

C. ANALYSIS OF TRANSIENT CURRENTS

In order to analyze the benefits of the DCSRE technique proposed in this paper, a simplified circuit diagram is drawn as shown in Fig. 15. It contains the node V_{fb} to the node V_g of the power transistor gate and includes four prerequisites. (I)Assume that the transconductance of M_{H1} and M_{H2} are equal, (II)Assume that the transconductance of ML1 and ML2 are equal, (III)Ignore the small parasitic capacitance at each node, and (IV)Ignore the Body effect and Channel length modulation. Considering the transistors of the differential pairs of EA_L and EA_H as equal, that is ignoring the mismatch of the current mirrors. Since the drain voltages

of M_{H1} and M_{H2} are equal, and the drain voltages of M_{L1} and M_{L2} are also equal, and in the case of the same size of the transistors, g_{mH1} equals g_{mH2}, and g_{mL1} equals g_{mL2}, from the simulations in Fig. 7 and Fig. 11. The currents of I_{H5} and I_{L5} in the steady state are both less than 1nA, which shows that the common-mode gains of the EA_L and the EA_H are sufficiently small so that the prerequisites and assumptions for the simplification as reasonable.

Case I($I_{O(light)} \rightarrow I_{O(heavy)}$): When the load is transiting from light load to heavy load, the return voltage is $\Delta V_{fb} = \Delta V_O(R_2/R_1+R_2)$, for a more detailed description of the state at this time, the voltage is expressed as follows.

$$f(\Delta V_{fb}) = V_{under}, \quad \Delta V_{fb} < V_{ref} \quad (1)$$

Equation (1) means that when the ΔV_{fb} voltage is lower than the V_{ref} voltage and V_{under} is defined as the undershoot voltage, the gate-to-source voltage $V_{gsn(M2)}$ of the M_2 transistor with the gate connected to V_{under} is smaller than the gate-to-source voltage $V_{gsn(M1)}$ of the M_1 transistor with the gate connected to V_{ref} for the EA_{main} at that time. When the NMOS gate voltage drops, the on-resistance of the transistor increases, and the on-resistances of M_1 and M_2,
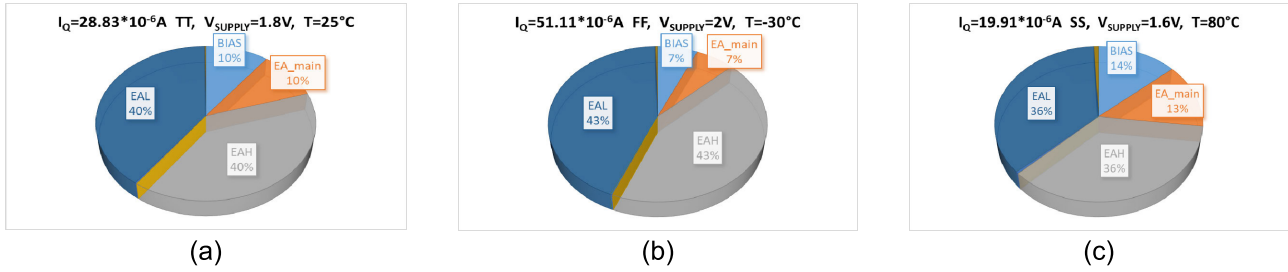
FIGURE 14. Distribution of quiescent current in (a) TT, (b) FF and (c) SS for three different process corners.

R_{ON1} and R_{ON2}, as follows.

$$R_{ON1} \approx \frac{1}{\mu_n c_{ox} \frac{W}{L}(V_{ref} - V_{tn})}$$

$$R_{ON2} \approx \frac{1}{\mu_n c_{ox} \frac{W}{L}(V_{under} - V_{tn})} \quad (2)$$

The gate-to-source voltages V_{gsn} of M_1 and M_2 are approximated as V_{ref} and V_{under}, and when $2(V_{gs}-V_t) \gg V_{ds}$ [22], the on-resistance R_{ON} is as shown above. From the denominator of equation (2) it follows.

$$R_{ON2} > R_{ON1} \quad (3)$$

According to the EA$_{main}$ output current $(\alpha\text{-}\beta)$. I_A in Fig. 6 is as given below.

$$(\alpha - \beta)I_A = \left(\frac{R_{ON2}}{R_{ON1} + R_{ON2}} - \frac{R_{ON1}}{R_{ON1} + R_{ON2}} \right)(g_{mH} + I_B)$$

$$I_A = g_{mH} + I_B, \quad \alpha = \frac{R_{ON2}}{R_{ON1} + R_{ON2}},$$

$$\beta = \frac{R_{ON1}}{R_{ON1} + R_{ON2}} \quad (4)$$

I_A is the tail current of EA$_{main}$, which includes the bias current I_B and $g_{mH}V_H$ current. The α is the ratio of I_A current in M_1 on-resistance R_{ON1}, and β is the ratio of I_A current in M_2 on-resistance R_{ON2}, and α is larger than β because R_{ON1} is smaller than R_{ON2}. V_H in Fig. 15 is given below.

$$V_H = \frac{g_{mH2}(V_{under} - V_{ref})}{g_{mH5}} \quad (5)$$

For EA$_H$, the source-to-gate voltage V_{under} of M_{H2} is larger than the source-to-gate voltage V_{ref} of M_{H1} transistor because the V_{under} voltage is lower than the V_{ref} voltage. According to Fig. 15, the $I_{SR(L2H)}$ current can be derived from the V_g node as follows.

$$I_{SR(L2H)} = g_{mH6}V_H + (\alpha - \beta)I_A - \frac{g_{mL8}g_{mL6}V_L}{g_{mL7}}$$

$$\approx [g_{mH6} + (\alpha - \beta)g_{mH}]\frac{g_{mH2}(V_{under} - V_{ref})}{g_{mH5}}$$

$$+ (\alpha - \beta)I_B \quad (6)$$

In this case, for the EA$_L$, since the source-to-gate voltage V_{under} of M_{L1} is larger than the source-to-gate voltage V_{ref}
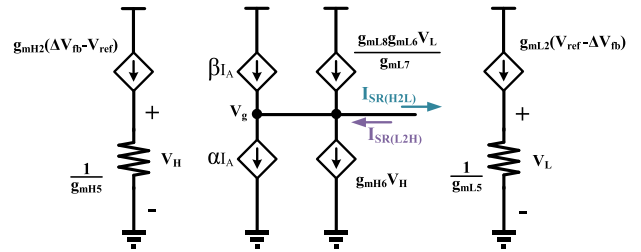

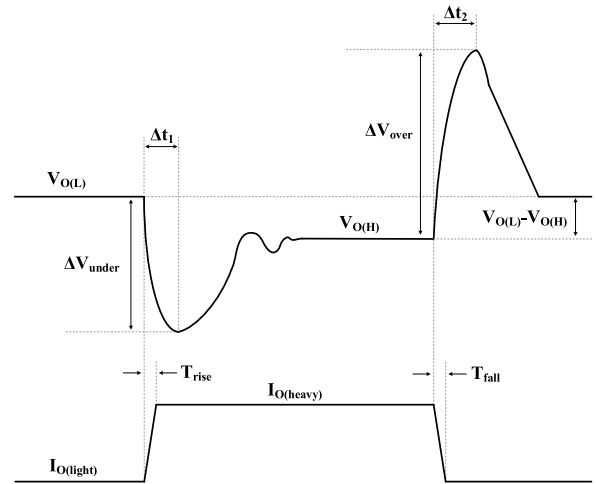**FIGURE 15.** Small signal for transient currents.

FIGURE 16. Output current and output voltage during load transition.

of the M_{L2} transistor, the V_L voltage is approximated to be zero and is ignored.

The output voltage and current during load transition are shown in Fig. 16, where Δt_1 is the response time for the gate capacitance C_g of the power transistor M_P to discharge to the $I_{O(heavy)}$ sufficient for transconductance and the delay time corresponding to the LDO regulator bandwidth $1/2\pi f_{-3dB}$. Therefore, the Δt_1 equation [23], [24], is approximated as.

$$\Delta t_1 \approx \frac{2.3}{2\pi f_{-3dB}} + C_g \left(\frac{|I_{O(light)} - I_{O(heavy)}|}{g_{mp}I_{SR(L2H)}} \right) \quad (7)$$

In the above, $|I_{O(light)} - I_{O(heavy)}|$ is ΔI_O, which is the change of I_O during load transition, g_{mp} is the transconductance of the power transistor, and $I_{SR(L2H)}$ is the discharge current of
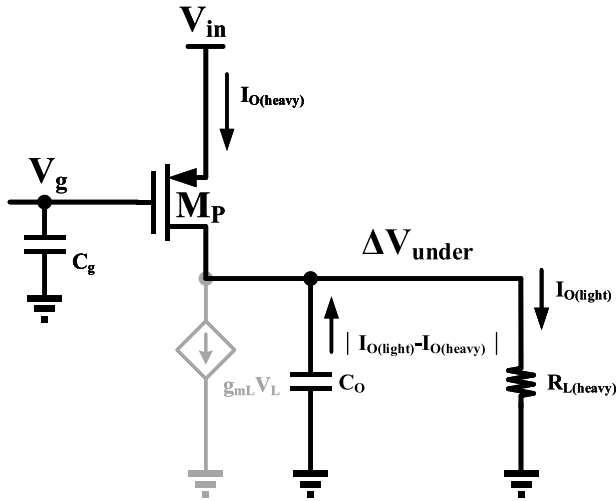
FIGURE 17. Transient from light load to heavy load at output node.

FIGURE 18. Steady state from light load to heavy load.

the C_g capacitor, and the time from 0% charging to 90% is 2.3 times of $1/2\pi f_{-3dB}$, and it can be seen from Eq. (7) that the larger the current of $I_{SR(L2H)}$ is, the shorter the response time of the M_P.

$$
\begin{aligned}
\Delta V_{under} &= V_{O(L)} - \left(\frac{\left| I_{O(light)} - I_{O(heavy)} \right|}{C_O} \right) \Delta t_1 \\
&= I_{O(light)} \times R_{L(light)} - \left(\frac{\left| I_{O(light)} - I_{O(heavy)} \right|}{C_O} \right) \\
&\quad \times \left(\frac{2.3}{2\pi f_{-3dB}} + C_g \left(\frac{\left| I_{O(light)} - I_{O(heavy)} \right|}{g_{mp} I_{SR(L2H)}} \right) \right)
\end{aligned}
\tag{8}
$$

When the load from the light load $R_{L(light)}$ suddenly changed to $R_{L(heavy)}$ as shown in Fig. 17. Then the shortage of output current $I_{O(light)}$ causes the output capacitance (parasitic capacitance) C_O of the stored energy released to attempt to balance the V_O voltage, after Δt_1 time $I_{O(heavy)}$ starts charging C_O again until the heavy load voltage $V_{O(H)}$ to reach balanced as shown in Fig. 18. Thus the magnitude of the undershoot voltage ΔV_{under} depends on the capacitance value of C_O, the time of Δt_1, and the variation of ΔI_O, so that ΔV_{under} equals Eq. (8).

The output voltage $V_{O(L)}$ at light load is equal to $I_{O(light)} \times R_{L(light)}$, and $V_{O(L)}$ added with the inverted voltage generated by C_O at the transient period is ΔV_{under}.

Case II($I_{O(heavy)} \rightarrow I_{O(light)}$): When the load is transiting from light load to heavy load, the output voltage VO overshoots, so the feedback voltage is as follows.

$$
f(\Delta V_{fb}) = V_{over}, \quad \Delta V_{fb} > V_{ref} \tag{9}
$$

Equation (9) shows that when the ΔV_{fb} voltage is higher than the V_{ref} voltage, V_{over} is defined as the overshoot voltage, and at this time, for EA$_{main}$, the gate-to-source voltage of the M_2 transistor with the gate connected to V_{over}, $V_{gsn(M2)}$, is larger
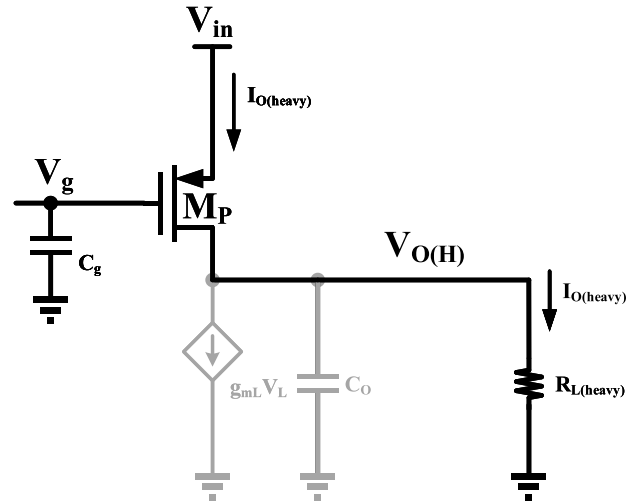
than that of the M_1 transistor with the gate connected to V_{ref}, $V_{gsn(M1)}$, and the conduction resistances R_{ON1} and R_{ON2} of M_1 and M_2 are given as

$$
\begin{aligned}
R_{ON1} &\approx \frac{1}{\mu_n c_{ox} \frac{W}{L} (V_{ref} - V_{tn})} \\
R_{ON2} &\approx \frac{1}{\mu_n c_{ox} \frac{W}{L} (V_{over} - V_{tn})}
\end{aligned}
\tag{10}
$$

Since V_{ref} is larger than V_{over}, based on the denominator of equation (10), gives.

$$
R_{ON1} > R_{ON2} \tag{11}
$$

According to equation (11), β is larger than α. In Fig. 15, V_L is

$$
V_L = \frac{g_{mL2}(V_{over} - V_{ref})}{g_{mL5}} \tag{12}
$$

In this case, for the EA$_L$, the V_{over} voltage is higher than the V_{ref} voltage, and the source-to-gate voltage V_{ref} of M_{L2} is larger than the source-to-gate voltage V_{over} of the M_{L1} transistor. At this time, the tail current I_A of EA$_{main}$ is equal to the bias current I_B, so the $I_{SR(H2L)}$ is as Eq. (13).

$$
\begin{aligned}
&I_{SR(H2L)} \\
&= \frac{g_{mL8} g_{mL6} V_L}{g_{mL7}} + (\beta - \alpha)I_B - g_{mH6} V_H \\
&\approx \frac{g_{mL8} g_{mL6} g_{mL2}(V_{over} - V_{ref})}{g_{mL7} g_{mH5}} + (\beta - \alpha)I_B
\end{aligned}
\tag{13}
$$

For EA$_H$, since the source-to-gate voltage V_{over} of M_{H2} is larger than the source-to-gate voltage V_{ref} of the M_{H1} transistor, the V_H voltage is approximated to be zero and is ignored. The Δt_2 time is the response time for the gate capacitor C_g of the power transistor M_P to charge until the current is sufficiently reduced from $I_{O(heavy)}$ to $I_{O(light)}$
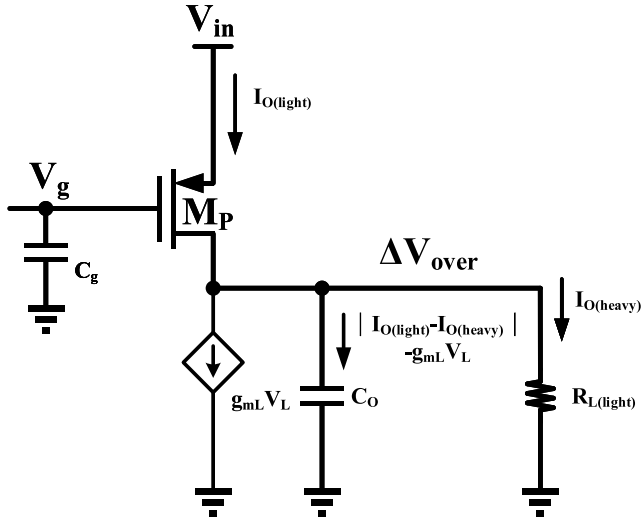
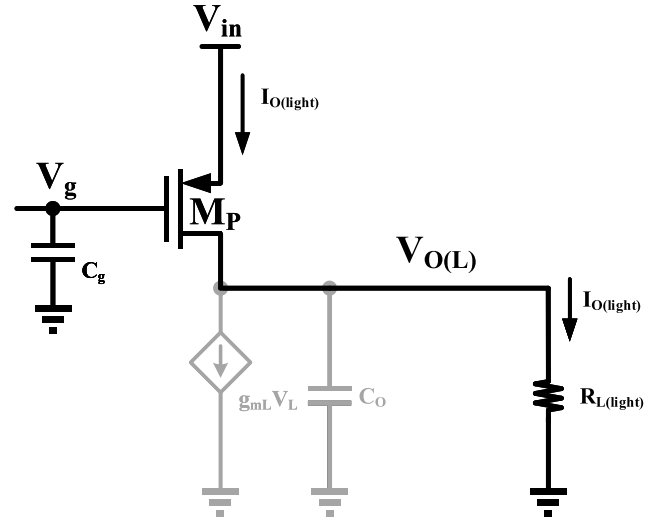**FIGURE 19.** Transient from heavy load to light load at output node.

FIGURE 20. Steady state from heavy load to light load.

and the delay of the LDO regulator. The equation Δt_2 is approximated as

$$\Delta t_2 \approx \frac{2.3}{2\pi f_{-3dB}} + C_g \left(\frac{\left| I_{O(light)} - I_{O(heavy)} \right| - g_{mL}V_L}{g_{mp}I_{SR(H2L)}} \right)$$
(14)

The difference with Eq. (7) is that the change in output current I_O is reduced by the $g_{mL}V_L$ current. ΔI_O is equal to $|I_{O(light)}-I_{O(heavy)}|-g_{mL}V_L$ which shortens Δt_2.

When the load suddenly changed from $R_{L(heavy)}$ to $R_{L(light)}$ during heavy load, as shown in Fig. 19. After Δt_2 time, M_P already transconductance the $I_{O(light)}$ current, and then the excessive output current $I_{O(heavy)}$ by $g_{mL}V_L$ and the parasitic capacitance C_O at the output is coupled to ground to discharging, and when the output voltage $V_{O(L)}$ reaches balanced as shown in Fig. 20. Therefore, the overshoot voltage ΔV_{over} is equal to Eq. (15)

$$\Delta V_{over}$$
$$= \left(\frac{\left| I_{O(light)} - I_{O(heavy)} \right| - g_{mL}V_L}{C_O} \right) \Delta t_2 - V_{O(H)}$$
$$= \left(\frac{\left| I_{O(light)} - I_{O(heavy)} \right| - g_{mL}V_L}{C_O} \right)$$
$$\times \left(\frac{2.3}{2\pi f_{-3dB}} + C_g \left(\frac{\left| I_{O(light)} - I_{O(heavy)} \right| - g_{mL}V_L}{g_{mp}I_{SR(H2L)}} \right) \right)$$
$$- I_{O(heavy)} \times R_{L(heavy)}$$
(15)

Because the size of the M_L transistor is much smaller than that of the M_P. The gate-to-ground parasitic capacitance of the M_L is also much smaller than that of the C_g, and thus the response time of the $g_{mL}V_L$ is also much shorter than that of the Δt_2. Meanwhile, the peak value of V_O subtracted from the $V_{O(H)}$ voltage in the transient period is ΔV_{over}.

III. STABILITY ANALYSIS OF THE PROPOSED LDO
A. SMALL SIGNAL ANALYSIS
The small-signal diagram of the proposed LDO regulator is shown in Fig. 21, where g_{m1}, g_{mH}, g_{mH6}, g_{mL}, g_{mLi}, and g_{mp} represent the transconductance of the main amplifier EA_{main}, the auxiliary amplifier EA_H, the transistor M_{H6}, the auxiliary amplifier EA_L, the transistors $M_{L6} \sim M_{L8}$, and the power transistor M_P, respectively. The parasitic capacitances to the ground of V_H, V_L, $V_{g(Mp)}$, and the output stage V_O are denoted as C_H, C_L, C_g, and C_O, respectively. Moreover, R_g is the output resistance of EA_H, EA_L and EA_{main} in parallel, thus R_g is equal to $R_{O(MH6)}//(R_{O(ML8)}//R_{O(EAmain)}$. Also, R_O is calculated as $R_{ds(Mp)}//R_{LOAD}$, where $R_{ds(MP)}$ represents the output resistance of the M_P, and R_{LOAD} is the load equivalent resistance. The gate-to-drain parasitic capacitance of the power transistor M_P is denoted as C_{gd}. The open-loop input is V_{fb}, and V_O represents the output. The simplified transfer function from the input V_{fb} to the output V_O can be expressed as (16), shown at the bottom of page 11, where A_{dc} is the low-frequency gain of the LDO regulator is mainly composed of EA_{main}, power transistor, and load equivalent resistance, as given below

$$A_{dc} = g_{mp}R_gR_O \left(g_{m1} + \frac{g_{mL}g_{mLi}}{g_{mL5}} + \frac{g_{mH}g_{mH6}}{g_{mH5}} \right)$$
(17)

From equation (17), observe that in addition to the EA_{main}, the EA_H and EA_L paths also contribute to the gain, although the influence is small, and the frequency of the p_{-3dB} pole is not affected at all. According to (15), the transfer function p_{-3dB} pole is expressed as

$$p_{-3dB} = -\frac{1}{C_{gd}g_{mp}R_gR_O}$$
(18)

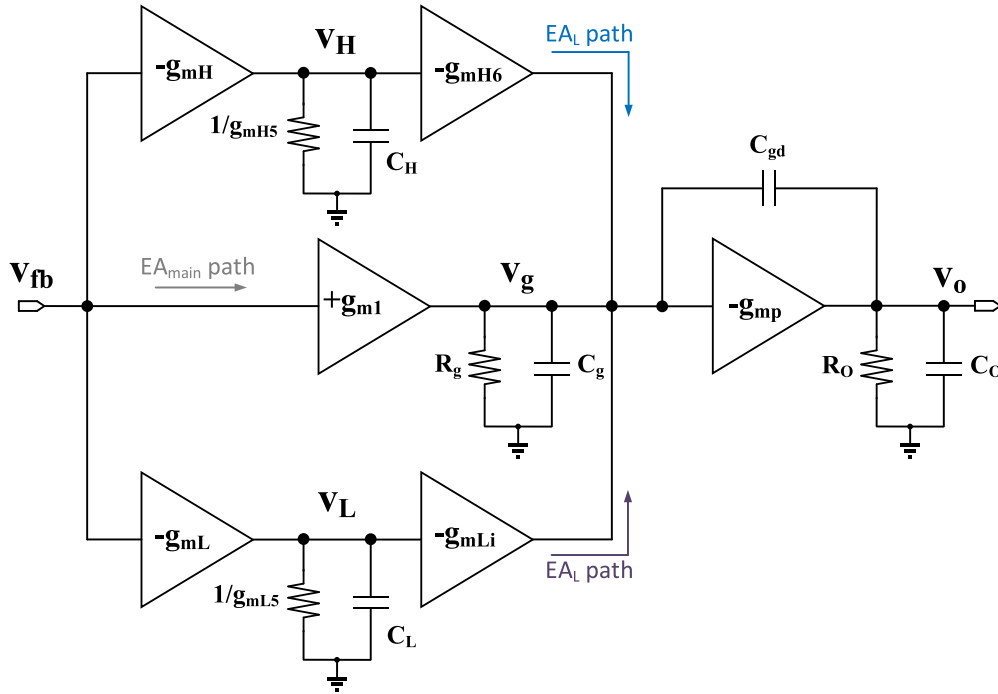The p_{-3dB} pole is the lowest frequency pole, also known as the main pole, and the other two higher frequency
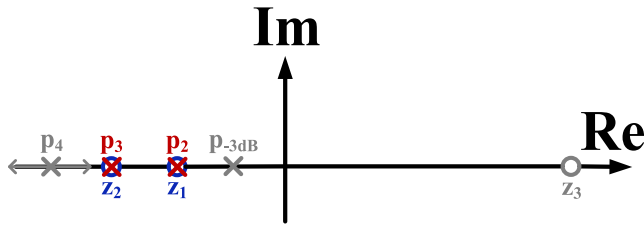
FIGURE 21. Small signal for stability analysis.

FIGURE 22. Poles and zeros in S-plane.

poles p_2 and p_3 are

$$p_2 = -\frac{1}{\frac{C_L}{g_{mL5}} + \frac{C_H}{g_{mH5}}} \tag{19}$$

$$p_3 = -\left(\frac{g_{mL5}}{C_L} + \frac{g_{mH5}}{C_H}\right) \tag{20}$$

Equations (19) and (20), the contribution of the EA_H and EA_L amplifiers can be observed. The p_2 and p_3 poles are formed by the output impedances of the EA_H and EA_L, and in particular, the parameters of both are C_L, C_H, g_{mL5}, and g_{mH5}, which implies that the difference between the frequencies of p_2 and p_3 is fixed and whenever the frequency of p_2 varies, the frequency of p_3 also varies accordingly. and the highest frequency pole p_4 is expressed as

$$p_4 = -\frac{g_{mp}}{C_O} \tag{21}$$

According to equation (21), the frequency of the p_4 pole is dominated by the ground parasitic capacitance C_O at the output of the LDO regulator and the power transistor's transconductance g_{mp}, which is proportional to the output current I_O and inversely proportional to the load equivalent resistance R_{LOAD}, for example, the larger I_O is, the larger g_{mp} is and the smaller R_{LOAD} is. In the case of zeros z_1 and z_2, on the other hand, the zeros are as equations (22) and (23). By observing equations (22) and (23), which are exactly equal to (19) and (20), z_1 is also p_2 and z_2 is also equal to p_3,

$$z_1 = -\frac{1}{\frac{C_L}{g_{mL5}} + \frac{C_H}{g_{mH5}}} \tag{22}$$

$$z_2 = -\left(\frac{g_{mL5}}{C_L} + \frac{g_{mH5}}{C_H}\right) \tag{23}$$

which means that the poles and zeros cancel each other and will not affect the phase and gain of the LDO regulator. Finally, the highest frequency zero point z_4 is denoted as

$$z_3 = \frac{g_{mp}}{C_{gd}} \tag{24}$$

From equation (24), which shows that the frequency of the zero z_3 is higher than that of the pole p_4 because the C_O capacitance is much larger than the gate-to-ground parasitic capacitance C_g of M_P, noteworthy is the difference between z_3 and z_1 and z_2, with z_3 is the right-half-plane zero as shown in Fig. 22. According to the above analysis, the critical for system stability is whether the frequency of pole p_4 and zero z_3 is high enough, and the output current I_O is small at light load, while the gmp transconductance is proportional to I_O. Therefore, the LDO regulator without output capacitance structure would not be suitable for stability in the case of light load and large equivalent capacitance C_O to ground

at the output, According to equation (24), the numerator of the zero z_3 is g_{mp}, which means that not designing the I_O current too small at light load will benefit the stability, The denominator is the capacitance of C_{gd}, which depends on the size and layout of the power transistor, even if the size is large enough to make the C_{gd} capacitance larger, but at the same time the g_{mp} grows, Thus, the z_3 frequency is still quite well designed, so the poles and zeros distribution is shown in Fig. 23. In addition, the phase margin is expressed as

$$PM = 180° - \tan^{-1}\left(\frac{GBW}{p_{-3dB}}\right) - \tan^{-1}\left(\frac{GBW}{p_2}\right)$$
$$+ \tan^{-1}\left(\frac{GBW}{z_1}\right) - \tan^{-1}\left(\frac{GBW}{p_3}\right) + \tan^{-1}\left(\frac{GBW}{z_2}\right)$$
$$- \tan^{-1}\left(\frac{GBW}{p_4}\right) - \tan^{-1}\left(\frac{GBW}{z_3}\right) \tag{25}$$

Equation (25) and Fig. 23 show that only one main pole, p_{-3dB}, is effective in the unity-gain bandwidth, because p_2 and p_3 are canceled by z_1 and z_2, and the frequency of z_3 must be sufficiently high in order not to affect the system, and finally the frequency of p_4 decides the phase margin. To explore the unity-gain bandwidth, all the poles and zeros before the gain is attenuated to 0dB are considered and the following equation is obtained

$$1 = \frac{A_{dc}\left(1 + \frac{s}{z_1}\right)\left(1 + \frac{s}{z_2}\right)}{\left(1 + \frac{s}{p_{-3dB}}\right)\left(1 + \frac{s}{p_2}\right)\left(1 + \frac{s}{p_3}\right)}$$
$$\Rightarrow GBW = \frac{g_{m1} + \frac{g_{mL}g_{mLi}}{g_{mL5}} + \frac{g_{mH}g_{mH6}}{g_{mH5}}}{C_{gd}} \tag{26}$$

According to the definition, gain attenuation to 0dB, so set the equation equal to 1, and already know that p_2, p_3, and z_1, z_2 are equal, after the equation is simplified, only A_{dc} and the main poles are left, and then divide the numerator and denominator together by A_{dc} to calculate the GBW. The common algorithm of analysis of GBW is to multiply the main poles directly by A_{dc}, but that only calculates the situation when only one pole is in the unity-gain-bandwidth, if there are multiple poles and zeros, then it cannot be analyzed. The algorithm used in Eq. (26) can analyze even if there are multiple poles and zeros in the unity-gain bandwidth, and the analysis of the proposed circuit is a special case that is the same as that calculated by the common algorithm.

B. SIMULATION

In the previous sub-section, the circuit was analyzed and some assumptions were made based on the results of the
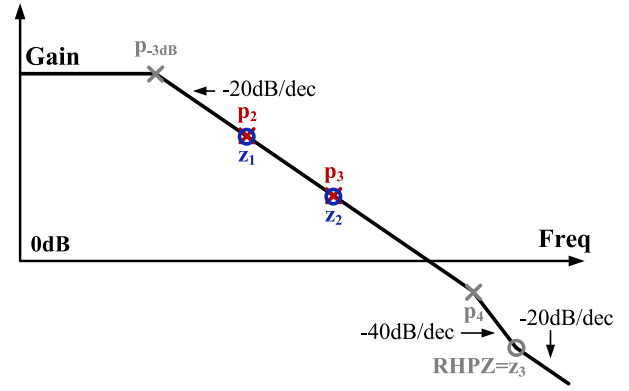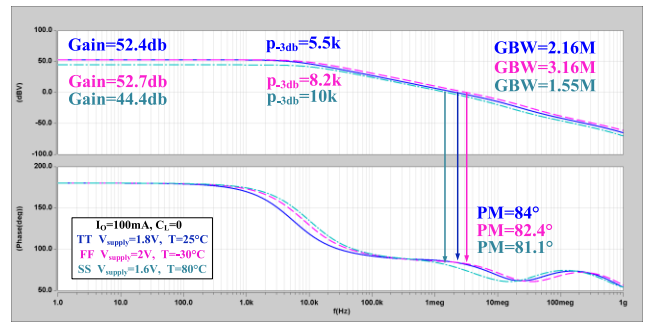

FIGURE 23. Poles and zeros in Bode.

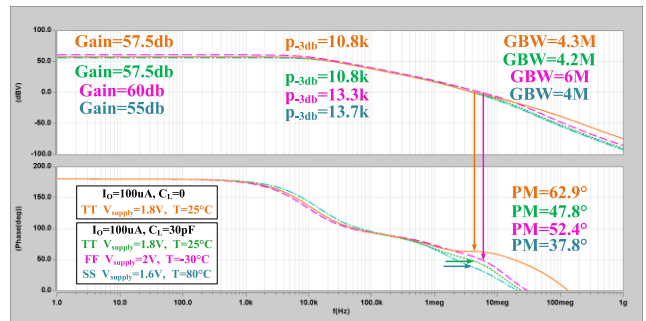**FIGURE 24. Simulation results of Bode plot for heavy load.**

FIGURE 25. Simulation results of Bode plot for light load.

analysis, in this sub-section, the results of the theory and the assumptions are verified to be consistent with the simulation. Fig. 24 shows the simulated Bode plot for three different process corners (Blue, pink and cyan) for heavy load $I_O = 100mA$, pink and cyan indicate FF and SS respectively. In case of TT, the low-frequency gain of 52.4dB, p_{-3dB} pole frequency at 5.5kHz, and GBW frequency at 4.2MHz with 84° phase margin. On the other hand, Fig. 25 shows

$$H_{(s)} = \frac{-A_{dc}\left(1 + s\left(\frac{C_L}{g_{mL5}} + \frac{C_H}{g_{mH5}}\right) + s^2\frac{C_H C_L}{g_{mH5}g_{mL5}} - s^3\frac{C_{gd}C_H C_L}{g_{mp}g_{mH5}g_{mL5}}\right)}{1 + sC_{gd}g_{mp}R_g R_O + s^2C_{gd}g_{mp}R_g R_O\left(\frac{C_L}{g_{mL5}} + \frac{C_H}{g_{mH5}}\right) + s^3\frac{C_{gd}C_H C_L g_{mp}R_g R_O}{g_{mH5}g_{mL5}} + s^4\frac{C_{gd}C_H C_L C_O R_g R_O}{g_{mH5}g_{mL5}}} \tag{16}$$
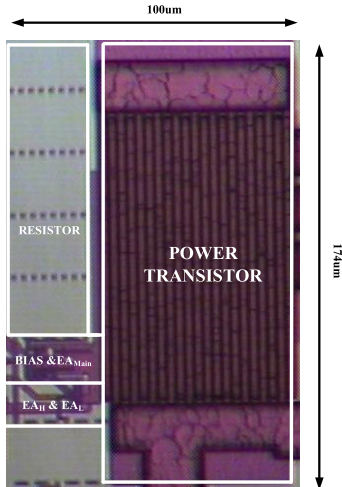
FIGURE 26. Chip microphotograph of the LDO regulator.

FIGURE 27. PSRR measurement setup.

the Bode plot for light load $I_O = 100\mu A$. In case of TT (Indicated by orange), the low-frequency gain is 57.5dB, the p_{-3dB} pole frequency at 10.8kHz, the GBW frequency at 4.38MHz, and the phase margin at 62.9°. With $C_L = 30pF$ (Indicated by green) is almost the same as a light load, except that the bandwidth and phase margins are 4.2MHz and 47.8° respectively. The worst case is the corner SS, phase margin is reduced to 37.8°.

From the phase, it can be seen that the frequencies of the relatively high-frequency pole p_3 and the zero z_2 are not exactly equal. The phase starts to decrease at about 2MHz and increase at about 20MHz at heavy load, that is, the frequency of p_3 and z_2 are between 20MHz and 200MHz. At light load, the phase starts to decrease at about 200kHz and increase at about 2MHz, so the frequencies of p_3 and z_2 are in the range of 2MHz~20MHz, which can be seen that the frequencies are quite close to each other. Even if the load changes from 100mA to 100μA, the distance is about 10 times. The reason for the difference between the simulation and the ideal is that when analyzing the poles or zeros, the numerator, and denominator of the transfer function are polynomials and only one term is taken in each case of s and then factorized. So the result of this calculation is an approximation although it is different from the simulation or the situation, the trend of the change is still the same as the result of the analysis, only the phase margin is a little less than the ideal. It can be observed that as the I_O current becomes smaller and smaller, the R_{LOAD} becomes larger and larger. The unity-gain-bandwidth also shrinks, the situation getting worse if C_O is taken into account, which means that the capacitor-less structure is limited by the load conditions and the impedance of the output node, and causes difficulty in the stabilization.

IV. EXPERIMENTAL RESULTS AND DISCUSSIONS

The proposed LDO regulator is fabricated in 0.18μm CMOS. The chip micrograph is shown in Fig. 26, and the core area is
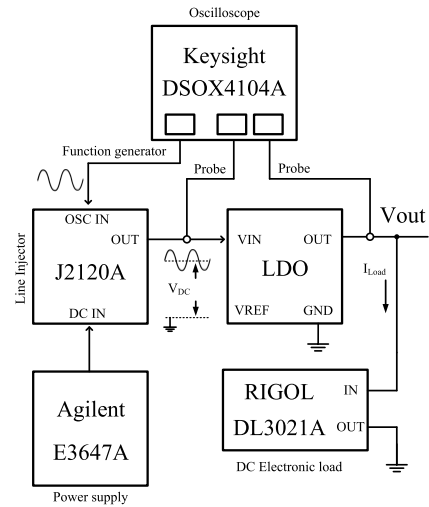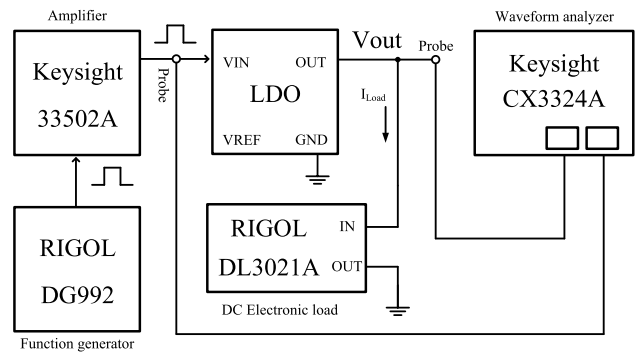

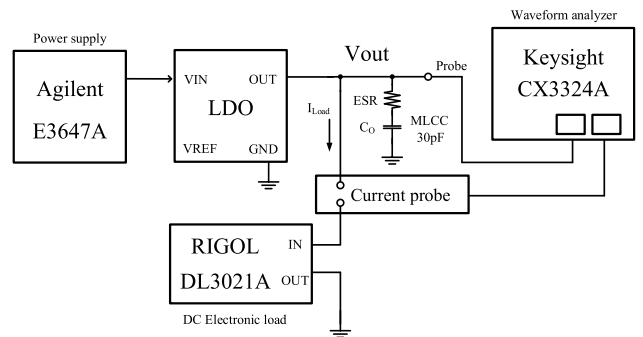**FIGURE 28.** Line transient measurement setup.

FIGURE 29. Load transient measurement setup.

0.0174mm^2. The core area consists of the power transistors, the BIAS circuit, the main error amplifier EA$_{main}$, and the auxiliary amplifiers EA$_H$, EA$_L$, and resistors.

To measure the power supply rejection ratio (PSRR) of the LDO regulator, the DC power supplied by the Agilent E3647A and the test signals are mixed by the Line Injector J2120A and then used as the input source. The RIGOL DL3021A is used as a fixed current source to control the load current, and then the Keysight DSOX4104 measures the input
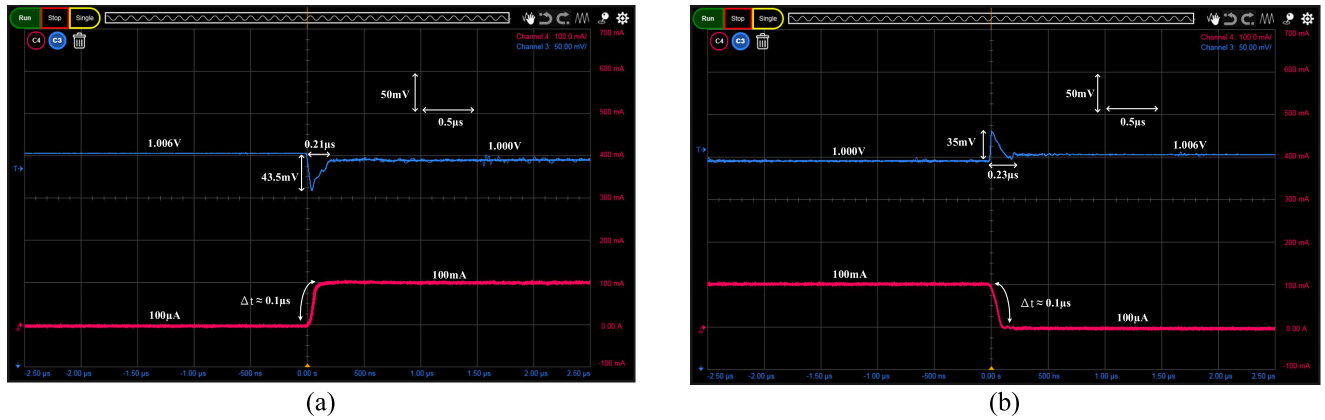
FIGURE 30. Measured load transients of (a) 100μA to 100mA and (b) 100mA to 100μA.
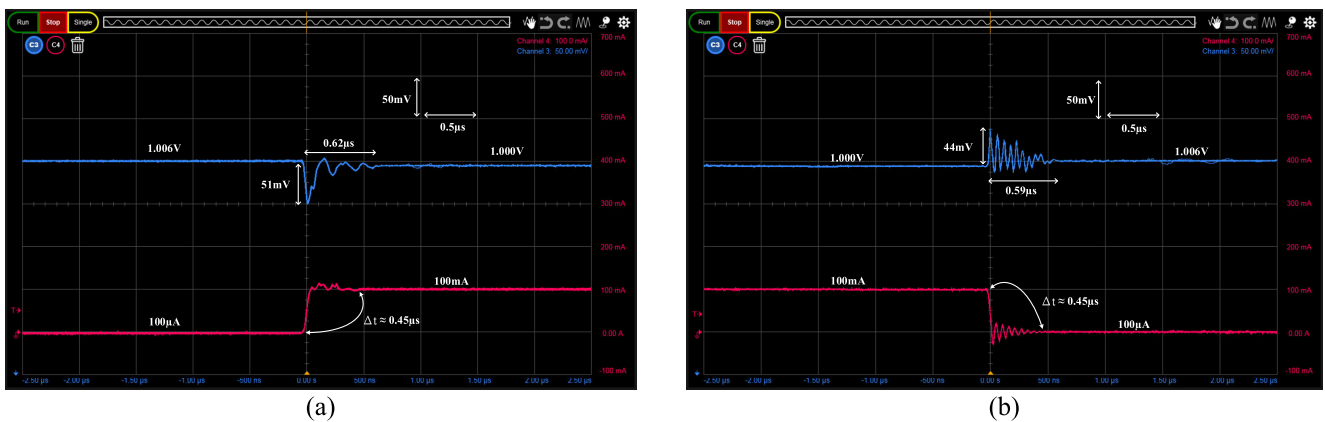
FIGURE 31. Measured load transients at $C_O = 30$pF of (a) 100μA to 100mA and (b) 100mA to 100μA.

and output signals respectively to obtain the measurement results, and the setup is shown in Fig. 27. The transient measurement setup of the line regulation is shown in Fig. 28. To transiently increase the input power from a lower voltage to a higher voltage, to handle the higher load current, the RIGOL DG992 pulse signal must be driven through the Keysight 33502 amplifier. The other settings are the same as those of the PSRR measurement, except for the inputs. The transient measurement setup of the load regulation is shown in Fig. 29, where the DC power supply is supplied by Agilent E3647A, followed by RIGOL DL3021A to control the load current from a small current transiently to a larger current, and then Keysight DSOX4104 to measure the output voltage and the load current respectively to obtain the results.

Fig. 30(a) shows the load transition from light load 100μA to 100mA with no capacitor at the output ($C_O = 0$), the rise time of the load current is about 0.1μs, the input voltage is 1.8V, the output voltage is 1V, the drop voltage is 800mV, the undershoot is 43.5mV, the settling time is 0.21μs, the steady-state output voltage is 1.006V at light load and 1V at heavy load. On the other hand, from a heavy load of 100mA to a light load of 100μA, as shown in Fig. 30(b), the fall time

of the load current is about 0.1μs, the overshoot is 35mV and the settling time is 0.23μs.

The parasitic capacitance at the output node of the OCL-LDO regulator affects stability and transient performance, the larger the capacitance, the more significant the influence, considering the 30pF capacitance at the output node, the phase margin is still 47.8 degrees. However, the PCB wiring and wire bonding will also induce parasitic capacitance and inductance, so 30pF is the maximum allowable for this circuit.

The measured $C_O = 30$pF, input, and output voltages are the same at 1.8V to 1V. In Fig. 31 (a), from 100μA to 100mA, the rise time of the load current is about 0.45μs, and the settling time for the undershoot is 0.21μs at 51mV. On the other hand, in Fig. 31(b), from 100mA to 100μA, the fall time of the load current is about 0.45μs, the overshoot is 44mV and the settling time is 0.59μs. When designing a feedback system, it is important to consider the damping ratio, bandwidth, and slew rate in determining the magnitude of the undershoot and overshoot. If the system is underdamped, the undershoot and overshoot will be greater than in the case of overdamping or critical damping. Furthermore, the
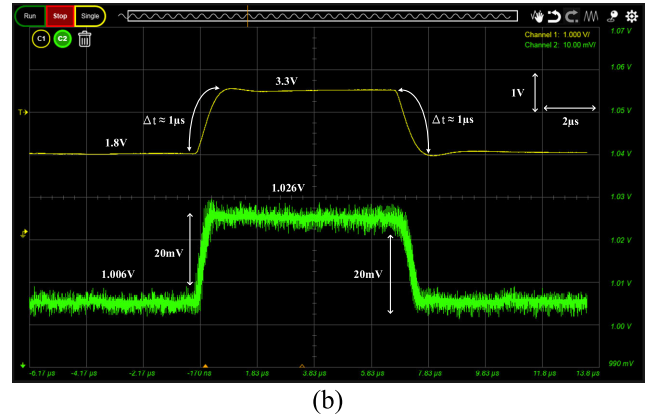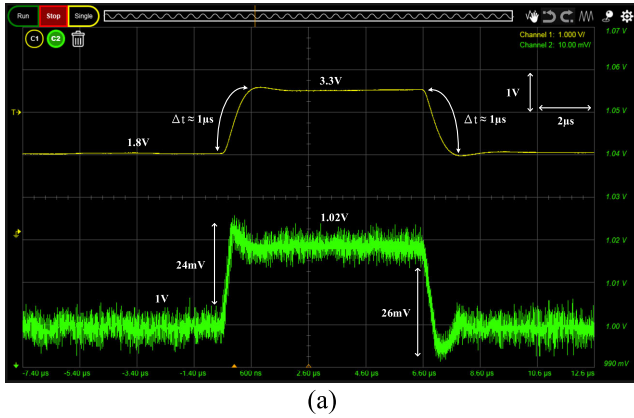
FIGURE 32. Measured line transients from 1.8V to 3.3V with (a) $I_O = 100mA$ and (b) $I_O = 100\mu A$.
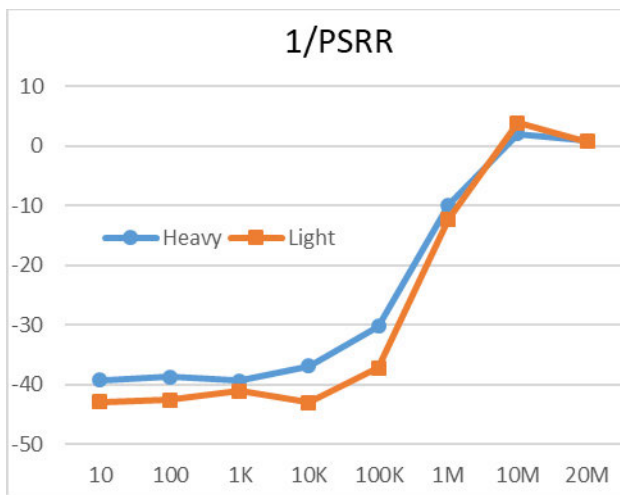

FIGURE 33. PSRR measured results.

output voltage may oscillate as a result of the equivalent series inductance of the bond wire, PCB circuitry, and capacitor. The undershoot and overshoot may also be exacerbated by the equivalent series resistance. OCL-LDOs suffer from parasitic capacitance at the output due to their capacitorless nature. This can cause the output pole to drop to a low frequency, compromising stability and limiting performance, especially if the output current is less or the parasitic capacitance is larger. Thus $C_O = 30pF$ and $I_O = 100\mu A$ are the limit for this LDO regulator.

When the load current is 100mA, V_{IN} rises from 1.8V to 3.3V where the rise time is $1\mu s$ and the overshoot is 24mV. As V_{IN} falls from 3.3V to 1.8V where the fall time is $1\mu s$ and the undershoot is 26mV, as shown in Fig. 32(a). From Fig. 32(a), V_O is 1V when V_{IN} is 1.8V, and V_O is 1.02V when V_{IN} is 3.3V, so the line regulation is 0.013(mV/V). On the other hand, when the load current is $100\mu A$, V_{IN} rises from 1.8V to 3.3V where the rise time is $1\mu s$ and the overshoot is 20mV, and V_{IN} falls from 3.3V to 1.8V where the fall time is $1\mu s$ and the undershoot is 20mV as shown in Fig. 32(b).

Form Fig. 32(b), V_O is 1.006V when V_{IN} is 1.8V and 1.026V when V_{IN} is 3.3V, so the line regulation is 0.2 (mV/mA).

The output voltage offset between heavy and light loads at steady state is too large to observe voltage variation during transients, this is because the output voltage offset of the line regulation is larger than the overshoot and undershoot, and ultimately only the change in the line regulation is visible. As a result, in Fig. 32(b), the overshoot and undershoot variations at light load ($I_O = 100\mu A$) are less than 20mV, but cannot be measured or observed.

Fig. 33 shows the PSRR measured results of the proposed LDO regulator, where the blue line indicates the heavy load ($I_O = 100mA$), which is about -39dB at low frequency before 1kHz, -36.9dB at 10kHz, and then the PSRR decreases significantly with the increase of the frequency, which is 30.2dB at 100kHz, and the remaining -9.9dB at 1MHz. The orange line indicates a light load ($I_O = 100\mu A$) with a low frequency of approximately -42.9dB until 10kHz, -37.2dB at 100kHz, and -12.3 dB at 1MHz, and whether light or heavy loads no longer provide power supply noise rejection after the frequency reaches 10MHz.

TABLE 1, [26] shows the best figure-of-merit (FOM) of 0.0064(ps·V) primarily due to the quiescent current of only 3nA. However, due to the tiny quiescent current, the settling time is slower and the ΔV is significantly larger. However, it is still within the system range and does not reach saturation, such as a dropout voltage of 600 mV and an overshoot voltage of about 520 mV. The ΔV in [30] is particularly small, with the undershoot being only 13mV, although a slightly higher quiescent current of $112\mu A$ is required. Instead of the OCL-LDO regulator, [28] features the output capacitor architecture, which due to the $1\mu F$ output capacitance, the ΔV is very small with 26.25mV and 19.75mV, and the settling time is from $3.75\mu s$ to $6.3\mu s$. This is a very good performance for the output capacitor architecture. The settling time is not inferior to the output capacitor-less architecture, but the quiescent current requires $270\mu A$ as the maximum in the comparison table. Reference [29] shows excellent performance in all

	ACCESS'22 [25]	TCAS-II'22 [26]	TCAS-I'20 [27]	TPE'20 [28]	TCAS-II'19 [29]	TPE'18 [30]	This work
Technology(nm)	130	180	65	180	180	130	180
Area(mm²)	0.018	0.00153	0.01	0.0297	0.031	0.008	0.0174
V_{IN}(V) [Min]-[Max]	1.2-1.5	1.8	1.05-1.2	1.8	1.2-1.8	1-1.4	1.8-3.3
V_O(V) [Min]-[Max]	1	1.2	0.9	1.6	0.8-1.6	0.8	1
Drop(mV) [Min]-[Max]	200-500	600	150-200	200	200-400	200-600	800-2300
I_O(mA) [Min]-[Max]	0.001-100	0.02-11	0.1^η-20	0.01-50	1-100	0.12-25	0.1-100
I_Q(µA) [Min]-[Max]	6.2	0.003	65	1.3-270	10.2	112	28.8
Current eff. [Min]	13.88^Γ(%)	99.98^Γ(%)	60.6^Γ(%)	88.49^Γ(%)	98.99^Γ(%)	51.72^Γ(%)	77.63(%)
Current eff. [Max]	99.99^Γ(%)	99.99^Γ(%)	99.7(%)	99.46(%)	99.98^Γ(%)	99.55(%)	99.97(%)
C_O(pF) [Min]-[Max]	0-1000	10-30	0-100	1000	0-100	0-25	0-30
On-chip cap(pF)	160(80+80)	0.077	1.4	0	0	0.73	0
GBW(MHz) [Min]-[Max]	0.59^ξ-1.54^ξ	N/A	5.9^ξ-53^ξ	0.0045^ξ-1.8^ξ	3.2^ξ-7.5^ξ	100.2^ξ-130.5^ξ	4.2^ξ-4.38^ξ
Δt(ns)	1000	30	5	10	70^η	10	100
Settling time [Min]-[Max]	12^η-24^η(µs)	82-147(µs)	~0.1(µs)	3.75^η-6.3^η(µs)	0.17-0.22(µs)	<0.19(µs)	0.21-0.23(µs)
Overshoot(mV)	$\sim190^\eta$	$\sim520^\eta$	200	19.75	200	22	35
Undershoot(mV)	$\sim220^\eta$	785	200	26.25	190	13	43.5
1/PSRR(dB)	$-70@1KHz^\xi$	-40@10Hz	-52@10KHz	-35.5@1MHz	N/A	-57@1MHz	-43@10KHz
	$-50@10KHz^\xi$	-2.3@10KHz	-23@1MHz	N/A	N/A	-22@10MHz	-12.3@1MHz
Load reg. (mV/mA)	N/A	8.62	N/A	0.32	N/A	0.173	0.2
Line reg. (mV/V)	N/A	0.71	N/A	1.1	N/A	2.25	0.013
FOM[31](ps·V)	13.64	0.0064	3.25	1.42	1.43	0.94	1.25

ξ Simulated results.

η Estimated form reported figures.

Γ Data obtained by calculating the parameters provided in the original paper by the author of this paper.

FOM[31]=($\Delta t \times \Delta V_{O(MAX)} \times I_{Q(MAX)}$ / I_O), $\Delta V_{O(MAX)}$ is the maximum value of the variation of the output voltage during the transient period, which is the larger value of undershoot or overshoot, Δt is the transition time of the output current, $I_{Q(MAX)}$ is the quiescent current, and ΔI_O is the difference between the minimum and maximum output currents of the LDO regulator.

characteristics, with a settling time from $0.17\mu s$ to $0.22\mu s$, except for the overshoot, which is poorer and reaches the maximum voltage of the system (dropout voltage of 200mV). In [27], it is the most advanced 65nm, with a settling time of $0.1\mu s$, which is the fastest in the comparison table, except that the overshoot is worse and also reaches the maximum. In [25], the current transition time Δt is $1\mu s$, which results in an inferior FOM, but only $6.2\mu A$ of quiescent current is required, and the ΔI_O range is extensive from 1nA to 100mA. In particular, the output capacitance range of 0 to $1\mu F$ enables output capacitance and output capacitorless architectures. The proposed LDO regulator ranks in the top three of the comparison table for both settling time and ΔV but presents the largest dropout in the table. The proposed LDO Regulator input and output voltage specifications are suitable for the applications that step down 3.3V, 2.5V and 1.8V to 0.8V~1V, such as lithium batteries and most of the switch mode power supply specifications. Moreover, this paper is mainly to verify the proposed "Direct-Coupled Slew Rate Enhancement" technique, so the larger the voltage range of the step down, the more the improvement of overshoot can be demonstrated.

V. CONCLUSION

In this paper, the direct-coupled slew rate enhancement technique is proposed to be applied to the OCL-LDO regulator. The chip is fabricated in the 0.18um CMOS process. It eliminates the necessity for tradeoffs between high-pass filter cutoff frequencies, as in the case of capacitive-coupled enhancement circuits, and operates within the unity-gain bandwidth of the auxiliary amplifier. Also, increasing the quiescent current of the auxiliary amplifier improves the f_{-3dB} bandwidth, resulting in faster circuit response and better slew rate enhancement. The use of auxiliary amplifiers provides advantages over capacitive-coupled such as greater amplitude, superior enhancement, and better current efficiency. Therefore, significant transient performance improvement can be achieved without an apparent increase in area and power consumption, and the transient slew rate is greatly enhanced. The proposed technique will not affect other characteristics of the LDO regulator such as stability, frequency compensation, line regulation, and load regulation. More importantly, the technique can be implemented on the same circuit as other techniques.

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