IEEE Access
Multidisciplinary ⋮ Rapid Review ⋮ Open Access Journal

Received 18 March 2024, accepted 27 April 2024, date of publication 6 May 2024, date of current version 17 May 2024.

Digital Object Identifier 10.1109/ACCESS.2024.3396923

RESEARCH ARTICLE

Passivity Enhancement and Grid-Current Distortion Mitigation for Inverter-Side Current Controlled *LCL*-Type Grid-Connected Inverters

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This work was supported in part by the National Natural Science Foundation of China under Grant 62173156.

ABSTRACT Inverter-side current (ISC) control has been widely used in *LCL*-type grid-connected inverters due to its cost-effectiveness. However, the ISC-controlled inverters suffer from instability and injected grid current distortion under weak grid conditions, such as grid impedance variations and background harmonics. To solve these problems, this article presents an admittance shaping scheme based on capacitor voltage feedforward (CVF) for ISC-controlled *LCL*-type grid-connected inverters. A delay compensated proportional CVF method is used to shape the inverter output admittance to be passive almost up to the Nyquist frequency. Then, another high-pass filter-based CVF method is employed to shape the grid harmonic admittance to greatly reduce the admittance magnitude at the harmonic frequencies. Thanks to the proposed admittance shaping scheme, the ISC-controlled inverter system can operate stably regardless of the grid impedance and has excellent grid-current harmonic suppression capability. The effectiveness of the proposed admittance shaping scheme is verified by detailed simulation and experimental results.

INDEX TERMS Grid-connected inverter, capacitor voltage feedforward, harmonic suppression, passivity.

I. INTRODUCTION

LCL-type grid-connected inverters, as a key interface unit for connecting renewable energy sources to the power grid, play a critical role in distributed power generation systems [1], which is responsible for injecting high-quality current into the grid. For the *LCL*-type grid-connected inverter, either the inverter-side current (ISC) or the grid-side current (GSC) can be selected for control. The ISC is usually sensed for overcurrent protection, so ISC control is the preferred solution in industrial applications from a cost perspective. In addition, ISC control has the inherent damping characteristics of *LCL* filters [2]. However, the system stability and output power quality are susceptible to the grid impedance variations and background harmonics.

Active damping is preferred for dealing with the *LCL*-filter resonance due to its flexible implementation and high efficiency compared to passive damping. When the digital control delay is ignored, it is found in [3] that among proportional, derivative and integral feedbacks, only the proportional feedback of capacitor current and the derivative feedback of capacitor voltage can yield the resonance damping. Since the capacitor voltage is already measured for grid synchronization, the use of capacitor voltage active damping (CVAD) does not require extra sensors. Consequently, CVAD has been widely used as a cost-effective solution. The direct derivative discretization induces a large phase error and noise amplification at high frequencies, so many efforts have

The associate editor coordinating the review of this manuscript and approving it for publication was Xueguang Zhang.

been focused on using indirect differentiators to emulate the derivative characteristics, such as high-pass filter (HPF) [4], lead-lag element [5], nonideal generalized integrator (GI) [6], and digital differentiators developed directly in the discrete domain [7]. Unfortunately, the derivative CVAD suffers from damping failure in the presence of grid impedance variations, as it is equivalent to proportional capacitor current active damping (CCAD) with a narrow positive damping region up to one-sixth of the sampling frequency ($f_s/6$). It is pointed out in [8] that proportional CVAD can also realize the damping function by utilizing the property of digital control delay, and has a positive damping region up to $f_s/3$. In [9], the proportional and second-derivative feedback are used to extend the positive damping region of CVAD to the Nyquist frequency, but the backward Euler discretization method used cannot achieve accurate derivative characteristic.

For ISC-controlled *LCL*-type grid-connected inverter, an alternative method to enhance the system robustness against the grid impedance variations is to reduce the digital control delay in the capacitor voltage feedforward (CVF) path. It is found in [10] that when the control delay in the feedforward path is ignored, the *LCL*-filter resonance is neutralized and the system is reduced to a first-order system. Subsequently, various delay compensation methods have been proposed for CVF. In order to neutralize the resonance introduced by *LCL* filter, one sampling period delay is compensated in [11] by using the stored capacitor voltage historical data to predict the future value, and one and a half sampling periods delay is compensated in [12] by combining shifting the update instant of reference voltage and digital-filter-based phase lead compensator. It is revealed in [13] that the robustness of system stability can be improved by optimizing the delay in the CVF path, but the delay compensation method based on shifting the sampling instant used will introduce switching noise and aliased harmonics. The above CVAD methods are typically designed based on the stability analysis of the classical closed-loop transfer function under the assumption of inductive grid condition, which cannot guarantee the system stability in the capacitive grid or system comprising multiple inverters [14].

The impedance-based stability criterion is an effective method for system-level stability assessment, which reveals that the interconnected inverter-grid system is stable if the ratio of grid impedance to inverter output impedance satisfies the Nyquist criterion, provided that the inverter itself is stable [15]. Nevertheless, the use of impedance-based stability criterion requires prior knowledge of the specific grid impedance, which limits its application since the grid impedance is complex and variable in practice. The passivity-based stability analysis, as an extension to the impedance-based stability analysis, provides a more promising approach for the interconnection stability assessment [16]. According to frequency-domain passivity theory, as long as the inverter output admittance is passive, the system is always stable regardless of the grid impedance variations [17]. However, it is difficult to obtain a passive admittance up to the Nyquist frequency due to the negative-real-part regions caused by the digital control delay. It is reported in [18] that for ISC control, the negative real part of inverter output admittance appears in the frequency region ($f_s/6$, $f_s/2$). In order to enhance the passivity of the output admittance for ISC control, various admittance shaping methods have been developed, which can be classified into three categories. The first is to insert a phase compensator, such as discrete derivative controller [18] and biquad filter [19], into the current regulator in parallel to extend the passive region, but the nonpassive region still exists at high frequencies. The second is to use the improved pulsewidth modulation (PWM) method, such as multisampled PWM [20] and asymmetric dual edge carrier-based PWM [21], to reduce the control delay, which can eliminate the nonpassive region but increase the implementation cost and complexity. The third is to use active damping to provide an additional positive-real-part admittance, such as CVF or point of common coupling (PCC) voltage feedforward, thus compensating for the negative real part of the output admittance. In [22], the passive region for ISC control is extended to $f_s/3$ with the help of derivative CVF. In [4], the nonpassive region is completely eliminated by modifying the derivative CVF with a phase compensator, but the analog differentiator implemented with a HPF adds additional hardware considerations. For ISC-controlled grid-connected inverters with an *L* filter, an integral PCC voltage feedforward method has been proposed in [23] to shape the output admittance as a passive reactance, and a proportional-derivative PCC voltage feedforward method has been proposed in [24] to expand the passive region up to $0.47f_s$. However, both of the aforementioned methods do not consider the impact of current regulator on passivity, which may jeopardize the passivity [4], [25].

Due to the low inductance of the *LCL* filter, the grid current injected by the *LCL*-type grid-connected inverter can be easily distorted by the background harmonics in the grid voltage. Currently, there are two commonly used schemes to suppress the grid-current distortion for ISC control. One is the voltage feedforward scheme. In [26], the capacitor current feedforward scheme is used to approximate the grid voltage feedforward scheme to suppress the grid-current distortion. However, the effect of digital control delay is not considered and additional cost is required for current sensing. Subsequently, a repetitive predictor is developed in [27] to compensate the delay in the grid voltage feedforward path to improve the performance of feedforward control, but the *LCL* filter is simply treated as an *L* filter. In addition, a weighted proportional-derivative PCC feedforward scheme is proposed in [24] to enhance the passivity and harmonic suppression ability of the inverter with *L* filter. Nevertheless, the effectiveness of the aforementioned two schemes deteriorates when the filter capacitor is considered, since the grid-current harmonics can flow freely into the filter capacitor. The other is to incorporate the resonant harmonic controllers (HCs) into the current regulator to obtain extremely high gain at the target harmonic frequencies.

For *LCL*-type grid-connected inverters with ISC control, the grid-current harmonic suppression capability of HCs is limited and insufficient due to the loss of harmonic information [28]. For this reason, various capacitor current compensation methods without additional sensors have been proposed to provide the required harmonic information for HCs, such as using a differentiator based on nonideal GI [28] or second-order GI [29] to calculate the capacitor current from capacitor voltage, and using state variables of resonant controllers to estimate the capacitor current [30]. However, these control schemes inherit the stability characteristics of the single-loop ISC control system, which has a narrow stable region of $(0, f_s/6)$. Therefore, for ISC-controlled *LCL*-type grid-connected inverters, there is still a lack of a control scheme that can simultaneously ensure high robustness of system stability against grid impedance variations and excellent harmonic attenuation capability under grid voltage distortion.

In this article, a simple and cost-effective admittance shaping scheme based on CVF is proposed for ISC-controlled *LCL*-type grid-connected inverters. A CVF loop with delay compensation is first used to passivate the inverter output admittance almost up to the Nyquist frequency, thus guaranteeing the system stability under any grid impedance. Another CVF loop with second-order HPFs is then introduced to shape the grid harmonic admittance to be extremely small at the working frequencies of HCs, thus enhancing the harmonic attenuation capability. Main contributions are summarized as follows:

1) A delay compensated proportional CVF method is proposed for ISC control to shape the inverter output admittance to be passive. Moreover, a first-order infinite impulse response (IIR) filter is developed to achieve the required delay compensation.
2) A second-order HPF-based CVF method is proposed to greatly reduce the harmonic admittance magnitude at the working frequencies of HCs to achieve sufficient harmonic attenuation, while the passivity of the inverter output admittance is still preserved.
3) Through the equivalent transformation of the control block diagram, the HPF-based CVF is transformed to feed the derivative capacitor voltage into the HCs, thus reducing the implementation complexity and computational cost. In addition, a simple but accurate digital differentiator is proposed.

The rest of this article is organized as follows. In Section II, the admittance model of ISC-controlled *LCL*-type grid-connected inverters is established and the passivity-based stability analysis is introduced. Based on this, an admittance shaping method based on delay compensated CVF is proposed for passivity enhancement in Section III. Then, another admittance shaping method based on second-order high-pass filtered CVF is developed for grid-current harmonic suppression in Section IV. Experimental results are provided in Section V to verify the effectiveness of the proposed method. Finally, Section VI concludes this article.

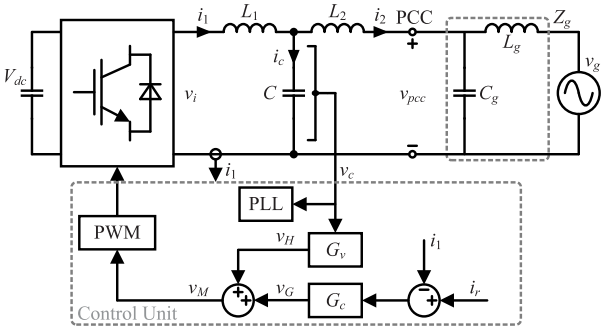

FIGURE 1. System configuration of *LCL*-type grid-connected inverter.

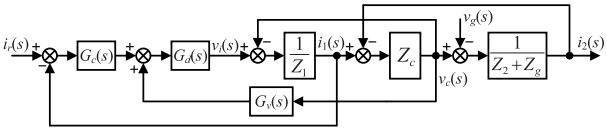

FIGURE 2. Block diagram of *LCL*-type grid-connected inverter with CVF.

II. MODELING AND STABILITY ANALYSIS

A. SYSTEM DESCRIPTION AND ADMITTANCE MODEL

The system configuration of ISC-controlled *LCL*-type grid-connected inverter is illustrated in Fig. 1. The *LCL* filter is comprised of the inverter-side inductor L_1, filter capacitor C, and grid-side inductor L_2. The power grid seen from PCC is modeled as an ideal voltage source v_g in series with a grid impedance Z_g, which is introduced by the inductor L_g of the transmission cable and transformer and the capacitor C_g of the power factor correction circuit. The inverter-side current i_1 is measured for current regulation to track the current reference i_r, and the current regulator G_c is a proportional resonant controller. The capacitor voltage v_c is measured for CVF-based admittance shaping and grid synchronization, and G_v is the CVF controller. The phase-locked loop (PLL) bandwidth is designed to be lower than the grid fundamental frequency to avoid low-frequency oscillations.

The block diagram of ISC-controlled *LCL*-type grid-connected inverter with CVF is depicted in Fig. 2, where Z_1, Z_c, and Z_2 are the impedances of L_1, C, and L_2, respectively. $G_d(s)$ is the digital control delay, which is typically composed of the computation delay of one sampling period and the PWM delay of half a sampling period [12], and is expressed as $G_d(s) = e^{-T_d s}$ where $T_d = 1.5T_s$ and T_s is the sampling period. The ISC-controlled inverter can be modeled as a current source in parallel with an output admittance seen from v_c. Considering v_c as a disturbance, i_1 can be expressed as

$$i_1(s) = T_c(s)i_r(s) - Y_c(s)v_c(s) \tag{1}$$

where the Norton current source transfer function T_c and the inverter output admittance Y_c, respectively, are given by

$$T_c(s) = \left.\frac{i_1(s)}{i_r(s)}\right|_{v_c=0} = \frac{G_c(s)G_d(s)}{Z_1(s) + G_c(s)G_d(s)}, \tag{2}$$

$$Y_c(s) = \left.\frac{i_1(s)}{-v_c(s)}\right|_{i_r=0} = \frac{1 - G_v(s)G_d(s)}{Z_1(s) + G_c(s)G_d(s)}. \tag{3}$$

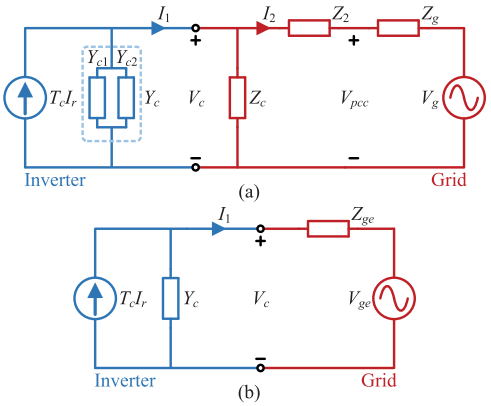

FIGURE 3. Equivalent circuit for the inverter-grid system with ideal voltage source (a) V_g and (b) V_{ge}.

From (3), it can be observed that Y_c can be further decomposed into two parallel subadmittances, and expressed as

$$Y_c(s) = \underbrace{\frac{1}{Z_1(s) + G_c(s)G_d(s)}}_{Y_{c1}} + \underbrace{\frac{-G_v(s)G_d(s)}{Z_1(s) + G_c(s)G_d(s)}}_{Y_{c2}}. \quad (4)$$

where Y_{c1} and Y_{c2} are the subadmittances corresponding to single-loop ISC control and CVF, respectively. Combining the models of the inverter and grid, the inverter-grid system can be represented as an equivalent circuit as shown in Fig. 3(a).

B. PASSIVITY-BASED STABILITY ANALYSIS

To facilitate the stability analysis, Z_c and Z_2 are converted into the grid impedance through the equivalent transformation of the two-terminal network, and the resulting equivalent circuit is shown in Fig. 3(b). The equivalent grid impedance Z_{ge} and voltage source v_{ge} seen from v_c are expressed as

$$Z_{ge} = \frac{Z_c(Z_2 + Z_g)}{Z_c + Z_2 + Z_g}, v_{ge} = \frac{Z_c}{Z_c + Z_2 + Z_g} v_g. \quad (5)$$

According to Fig. 3(b), the capacitor voltage is $v_c = Z_{ge}i_1 + v_{ge}$, and substituting it into (1), the ISC can be derived as

$$i_1(s) = [T_c(s)i_r(s) - Y_c(s)v_{ge}(s)] \cdot \frac{1}{1 + Y_c(s)Z_{ge}(s)}. \quad (6)$$

It is known that v_{ge} is stable and Z_{ge} is passive. According to the impedance-based stability criterion [15], the stability condition for the inverter-grid system is that T_c has no right-half-plane (RHP) poles, which means that Y_c also has no RHP poles, and Y_cZ_{ge} satisfies the Nyquist criterion. If the phase of Y_c is within $[-90°, 90°]$, then the Nyquist curve of Y_cZ_{ge} cannot encircle $(-1, j0)$, which indicates that the Nyquist criterion is satisfied. Therefore, it can be inferred from the above two stability conditions that as long as Y_c is passive, the inverter-grid system remains stable regardless of the grid impedance variations. According to the frequency-domain passivity theory, Y_c is passive if the following two conditions hold [17]:

1) Y_c is stable, which implies that T_c is stable.
2) Y_c has a nonnegative real part, i.e., $\mathrm{Re}\{Y_c(j\omega)\} \geq 0, \forall\omega$.

The stability of T_c can be ensured by designing sufficient phase margin (PM) for the open-loop transfer function of T_c. According to (2), the internal plant of T_c is a simple first-order system with a pure delay element, so T_c can be easily designed to be stable by selecting an appropriate current regulator gain. The following main objective is to shape Y_c to have a nonnegative real part within the Nyquist frequency.

III. ADMITTANCE SHAPING FOR PASSIVITY ENHANCEMENT

A. PASSIVITY ANALYSIS OF SUBADMITTANCE

Since the resonant part of current regulator has a negligible influence outside the resonant frequency, the current regulator is simplified as $G_c = k_p$ to facilitate passivity analysis. In the frequency domain, the real part of Y_{c1} is expressed as

$$\mathrm{Re}\{Y_{c1}(j\omega)\} = \frac{k_p\cos(\omega T_d)}{a^2 + b^2} \quad (7)$$

where $a = k_p\cos(\omega T_d)$ and $b = \omega L_1 - k_p\sin(\omega T_d)$. From (7), it can be seen that the denominator of $\mathrm{Re}\{Y_{c1}(j\omega)\}$ is always positive, so the passivity of Y_{c1} can be investigated according to the numerator of $\mathrm{Re}\{Y_{c1}(j\omega)\}$. According to the properties of the cosine function in the numerator, it is known that $\mathrm{Re}\{Y_{c1}(j\omega)\}$ is positive in the frequency region $(0, 1/4T_d)$ and negative in the frequency region $(1/4T_d, f_s/2)$ when $0.5T_s \leq T_d \leq 1.5T_s$. For the single-loop ISC control with typical digital control delay $T_d = 1.5T_s$, the passive region lies within $(0, f_s/6)$, as shown in Fig. 4. To extend the passive region, the critical frequency $1/4T_d$ can be increased by reducing T_d. When T_d is reduced to $0.5T_s$, a passive Y_{c1} within the Nyquist frequency can be obtained. However, achieving delay reduction for one sampling period is costly and complex [20], [21].

Assuming that the CVF controller G_v is a proportional gain, i.e., $G_v = H_v$, the real part of Y_{c2} can be expressed as

$$\mathrm{Re}\{Y_{c2}(j\omega)\} = \frac{H_v[\omega L_1\sin(\omega T_d) - k_p]}{a^2 + b^2}. \quad (8)$$

It can be observed from (8) that the magnitude of $\mathrm{Re}\{Y_{c2}(j\omega)\}$ is mainly determined by H_v, and the sign change of $\mathrm{Re}\{Y_{c2}(j\omega)\}$ depends on k_p and T_d. According to the properties of the sine function, $\omega L_1\sin(\omega T_d)$ is positive in the frequency region $(0, 1/2T_d)$ and negative in the frequency region $(1/2T_d, f_s/2)$ when $T_s \leq T_d \leq 2T_s$. Ignoring the effect of k_p, for CVF with $T_d = 1.5T_s$, the passive region lies within $(0, f_s/3)$. When T_d is reduced to T_s, the passive region can be extended to the Nyquist frequency. It can be concluded that $\omega L_1\sin(\omega T_d)$ introduces a nonpassive region at high frequencies, which can be eliminated by reducing T_d. When considering k_p, the sign of $\omega L_1\sin(\omega T_d) - k_p$ will change from negative to positive at a certain low frequency and from positive to negative at a certain high frequency due to the non-monotonicity of $\omega L_1\sin(\omega T_d)$, resulting in negative-real-part regions at both low and high

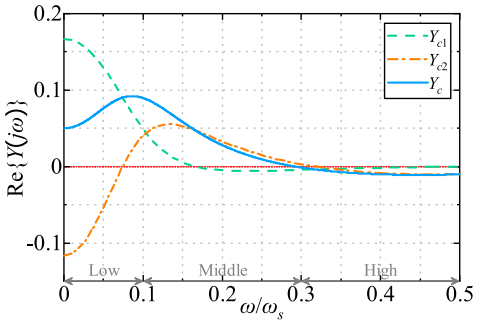

FIGURE 4. The real part of admittances.

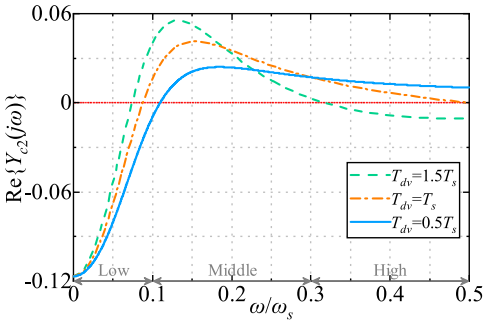

FIGURE 5. $\mathrm{Re}\{Y_{c2}(j\omega)\}$ with different T_{dv}.

frequencies. This means that k_p weakens the passivity of Y_{c2} and introduces additional nonpassive regions at both low and high frequencies. The corresponding $\mathrm{Re}\{Y_{c2}(j\omega)\}$ is shown in Fig. 4. It can be found that although the use of proportional CVF can extend the passive region of the inverter output admittance Y_c for ISC control to a certain extent at the cost of reducing the magnitude of $\mathrm{Re}\{Y_c(j\omega)\}$ at low frequencies, it cannot completely eliminate the nonpassive region at high frequencies. Therefore, in order to completely neutralize the negative real part of Y_{c1}, the positive-real-part region of Y_{c2} at high frequencies needs to be extended to the Nyquist frequency.

B. PROPOSED DELAY COMPENSATED CVF

Based on the above analysis, it can be known that the negative-real-part region of Y_{c2} at high frequencies is caused by T_d and k_p together, and reducing the delay is beneficial to enhance the passivity of Y_{c2}. The influence of the control delay G_{dv} in the CVF path on the passivity of Y_{c2} is investigated in the following. Assuming that $G_{dv}(s) = e^{-T_{dv}s}$, the delay $T_d = 1.5T_s$ in the forward path remains constant, and then the real part of Y_{c2} can be derived as

$$\mathrm{Re}\{Y_{c2}(j\omega)\} = \frac{H_v[\omega L_1 \sin(\omega T_{dv}) - k_p \cos(\omega(T_d - T_{dv}))]}{a^2 + b^2}. \tag{9}$$

It can be seen from (9) that compared with (8), there is an additional cosine term $\cos(\omega(T_d - T_{dv}))$ in the numerator, which can be used to suppress the adverse effects of k_p at high frequencies. The negative-real-part region introduced by $\omega L_1 \sin(\omega T_{dv})$ at high frequencies can be eliminated by reducing T_{dv} to T_s. When $T_{dv} = T_s$, $k_p \cos(\omega(T_d - T_{dv}))$ is zero at the Nyquist frequency, which means that the effect of k_p near the Nyquist frequency is eliminated. At this point, the positive-real-part region of Y_{c2} at high frequencies is extended to the Nyquist frequency, as shown in Fig. 5. It can be seen that reducing the delay in the CVF path to a certain extent can eliminate the negative-real-part region of Y_{c2} at high frequencies, which makes it feasible to achieve a passive inverter output admittance Y_c within the Nyquist frequency.

According to the passivity analysis of the subadmittance, in order to ensure that Y_c has a nonnegative real part within the Nyquist frequency, the following three conditions must hold:

$$\begin{cases} \mathrm{Re}\{Y_{c1}(j0)\} + \mathrm{Re}\{Y_{c2}(j0)\} \geq 0 \\ \mathrm{Re}\{Y_{c1}(j\omega_s/6)\} + \mathrm{Re}\{Y_{c2}(j\omega_s/6)\} \geq 0 \\ \mathrm{Re}\{Y_{c1}(j\omega_s/2)\} + \mathrm{Re}\{Y_{c2}(j\omega_s/2)\} \geq 0 \end{cases} \tag{10}$$

where the first constraint in (10) is the precondition that Y_{c1} is capable of neutralizing the negative real part of Y_{c2} at low frequencies, while the second and third constraints are the preconditions that Y_{c2} is capable of neutralizing the negative real part of Y_{c1} at high frequencies. Assuming that H_v and k_p are positive and $T_d = 1.5T_s$, solving (10) yields the following ranges for H_v, T_{dv}, and k_p:

$$H_v \leq 1,\ 0 \leq T_{dv} \leq T_s,\ k_p \leq \omega_s L_1/6. \tag{11}$$

It can be seen from (11) that in order to achieve a passive Y_c, the delay T_{dv} in the CVF path must be reduced to T_s or below, which means that a delay of at least $0.5T_s$ requires to be compensated. Considering the implementation cost and complexity, this article focuses on the $0.5T_s$ delay compensation, i.e., $T_{dv} = T_s$. k_p can be determined based on the stability analysis of T_c and the required crossover frequency, while satisfying the constraints in (11). The choice of H_v must ensure that Y_{c2} can completely neutralize the negative real part of Y_{c1} in the frequency region $(f_s/6, f_s/2)$, that is, the following condition is satisfied:

$$\mathrm{Re}\{Y_{c1}(j\omega)\} + \mathrm{Re}\{Y_{c2}(j\omega)\} \geq 0, \forall \omega \in (\omega_s/6, \omega_s/2). \tag{12}$$

According to (12), with the chosen k_p and $T_{dv} = T_s$, the lower bound of H_v can be derived as

$$H_v \geq \max_{\omega \in (\omega_s/6, \omega_s/2)} \left\{ \frac{k_p[3 - 4\cos^2(0.5\omega T_s)]}{2\omega L_1 \sin(0.5\omega T_s) - k_p} \right\}. \tag{13}$$

Therefore, after compensating the delay of $0.5T_s$ in the CVF path, a passive Y_c can be obtained within the Nyquist frequency by selecting the appropriate H_v.

Various digital-filter-based delay compensation methods have been developed to compensate the half sampling period delay, such as first-order IIR filter $2/(1 + z^{-1})$ [31], second-order generalized-integrator (SOGI) based digital filter [32], and modified first-order IIR filter [12]. The delay compensator based on the first-order IIR filter proposed in [31] can perfectly compensate the phase lag of the

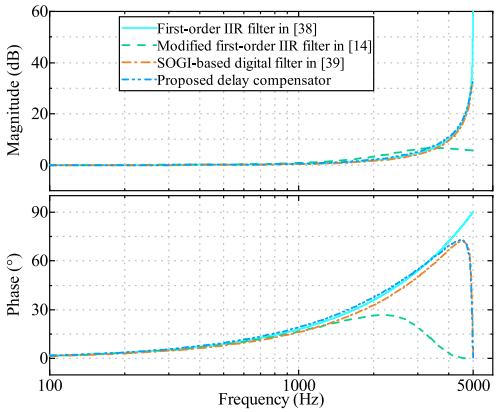

FIGURE 6. Comparison of four half sampling period delay compensators.

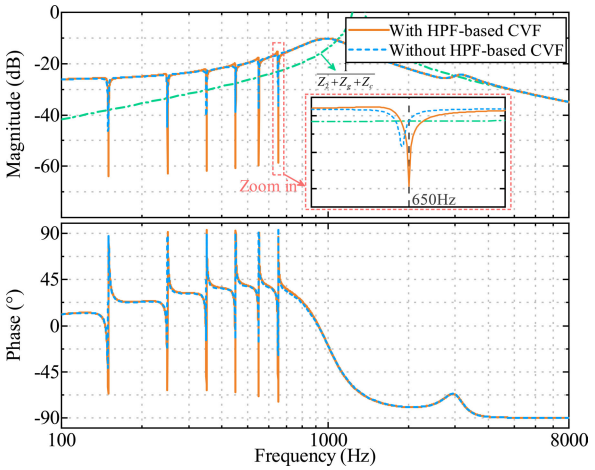

FIGURE 7. Bode diagrams of Y_h with and without HPF-based CVF.

half sampling period delay, but it causes an unacceptable noise amplification problem due to its infinite magnitude at the Nyquist frequency. For this reason, in [12], a first-order zero-phase-shift low-pass filter is employed to modify the first-order IIR filter to attenuate its magnitude peak. In addition, in [32], the SOGI is used to compensate the delay, and a compromise between the noise attenuation and phase lead performance can be achieved by tuning the damping term of SOGI, yet these characteristics are retained in the digital filter only by applying the sophisticated first-order hold discretization method. In this article, a simple but accurate delay compensator is proposed to compensate the half sampling period delay, which is expressed as

$$C(z) = \frac{m+1}{m} \cdot \frac{1+(m-1)z^{-1}}{1+mz^{-1}} \tag{14}$$

where $0 < m < 1$. The closer m is to 1, the more accurate phase compensation effect can be achieved, at the cost of the larger magnitude at high frequencies. Therefore, $m = 0.95$ is chosen to achieve a satisfactory trade-off between phase compensation and gain amplification at high frequencies. Fig. 6 compares the frequency responses of the four delay compensators mentioned above. It can be seen that although the magnitude of the modified first-order IIR filter is attenuated at high frequencies, a large phase compensation error is introduced. For a fair comparison, the parameters of SOGI are chosen such that the SOGI-based delay compensator has the same magnitude of 33dB at the Nyquist frequency as the proposed delay compensator. Then, it can be found from Fig. 6 that the proposed delay compensator can achieve more accurate phase lead compared with the SOGI-based delay compensator. Therefore, the proposed delay compensator provides a better compensation effect of the half sampling period delay.

IV. ADMITTANCE SHAPING FOR GRID-CURRENT HARMONIC SUPPRESSION

A. PROPOSED HIGH-PASS FILTERED CVF

To suppress the grid-current harmonics, the resonant controller is selected as the harmonic controller G_{HC} and added to the current regulator G_c, and then G_c is obtained as follows:

$$G_c(s) = \underbrace{k_p + k_{r1}\frac{s\cos(\phi_1) - \omega_0\sin(\phi_1)}{s^2 + 2\omega_{c1}s + \omega_0^2}}_{G_{PR}(s)} + \underbrace{\sum_{h=3,5,\cdots} k_{rh}\frac{s\cos(\phi_h) - h\omega_0\sin(\phi_h)}{s^2 + 2\omega_{ch}s + (h\omega_0)^2}}_{G_{HC}(s)} \tag{15}$$

where k_p, h, k_{rh}, ϕ_h, ω_0, and ω_{ch} represent the proportional gain, harmonic order, resonant gain, compensation angle, grid fundamental frequency, and resonance cutoff frequency, correspondingly. To investigate the ability of ISC control system to suppress grid-current harmonics caused by grid voltage distortion, according to Fig. 3(a), the grid harmonic admittance is defined and derived as

$$Y_h(s) = \left.\frac{-i_2(s)}{v_g(s)}\right|_{i_r=0} = \frac{1}{Z_2(s) + Z_g(s) + Z_{ic}(s)} \tag{16}$$

where $Z_{ic} = Z_c/(1 + Y_cZ_c)$ is the impedance composed of Z_c and Y_c in parallel. Y_h represents the relationship between the grid-voltage harmonics and the resulting grid-current harmonics. A smaller Y_h indicates more harmonic attenuation, which means that the grid voltage distortion has less effect on the grid current. At the selected harmonic frequencies, G_{HC} has an approximately infinite gain, resulting in an infinitesimal Y_c, i.e., $Z_{ic} \approx Z_c$, and thus Y_h can be approximated as

$$|Y_h(s)|_{s=jh\omega_0} \approx \left|\frac{1}{Z_2(s) + Z_g(s) + Z_c(s)}\right|. \tag{17}$$

From (17), it can be found that at the working frequencies of HCs, Y_h is only determined by the filter impedance and the grid impedance, which means that the harmonic attenuation capability is limited and cannot be improved by designing the controller parameters.

To address this issue, it is necessary to obtain a larger Z_{ic} at the working frequencies of HCs to reduce Y_h. Using (3), Z_{ic}

can be rewritten as

$$Z_{ic}(s) = \frac{Z_c(s)[Z_1(s) + G_c(s)G_d(s)]}{Z_c(s) + Z_1(s) + G_d(s)[G_c(s) - G_v(s)Z_c(s)]}. \quad (18)$$

From (18), it can be observed that the resonant peak of G_c in the numerator can provide an approximately infinite gain for Z_{ic} at the working frequencies of HCs, but the presence of G_c in the denominator causes the infinite gain of Z_{ic} to deviate from the selected harmonic frequencies. Therefore, in order to return the infinite gain of Z_{ic} to the selected harmonic frequencies, an intuitive idea is to introduce an additional CVF function to cancel out the G_{HC} contained in the G_c term of the denominator. The required CVF function is expressed as

$$G_{vf}(s) = \frac{G_{HC}(s)}{Z_c(s)} = \sum_{h=3,5,\cdots} k_{rh}C\frac{\cos(\phi_h)s^2 - h\omega_0\sin(\phi_h)s}{s^2 + 2\omega_{ch}s + (h\omega_0)^2} \quad (19)$$

which consists of multiple second-order HPFs with the filter natural frequencies being the selected harmonic frequencies. Fig. 7 shows the bode diagram of Y_h with and without HPF-based CVF. It can be seen that the characteristics of Y_h near the harmonic frequencies are consistent with the theoretical analysis mentioned above. Without the HPF-based CVF, the resonant notches of Y_h shift away from the selected harmonic frequencies, where the magnitudes of Y_h are determined by Z_2, Z_c, and Z_g. In contrast, with the HPF-based CVF, the resonant notches exactly return to the selected harmonic frequencies and generate smaller magnitudes. Therefore, the proposed admittance shaping method based on high-pass filtered CVF can significantly enhance the grid-current harmonic suppression capability of the ISC-controlled *LCL*-type grid-connected inverter. In addition, since the HPF-based CVF mainly shapes Y_c near the harmonic frequencies, the passivity of Y_c can still be preserved by properly designing the parameters of the resonant parts to eliminate the nonpassive regions introduced by the resonant parts of G_c [25].

B. SIMPLIFIED ADMITTANCE SHAPING SCHEME

In summary, the proposed CVF-based admittance shaping scheme consists of the delay compensated proportional CVF for passivity enhancement and the high-pass filtered CVF for grid-current harmonic suppression, and the corresponding CVF controller is expressed as follows:

$$G_v(s) = H_vC(s) + G_{vf}(s). \quad (20)$$

As can be seen in (19), for each resonant part in G_{HC}, the corresponding second-order HPF is required to be added in G_{vf} and discretized for digital implementation, which leads to the complicated algorithm implementation and heavy computational burden. For this reason, the proposed admittance shaping scheme is simplified in the following by the equivalent transformation of control block diagram.

Fig. 8(a) illustrates the control block diagram of the proposed CVF scheme. Since G_{vf} contains G_{HC}, the feedforward node of v_c passing through G_{vf} can be moved to the input of G_{HC}, resulting in a simple feedforward path transfer function Cs, as shown in Fig. 8 (b). As a result, the high-pass filtered CVF is equivalent to feeding the derivative capacitor voltage into the HCs. At this point, only one digital differentiator needs to be implemented instead of multiple second-order HPFs, which significantly reduces the implementation complexity and computational effort. To this end, a simple but accurate digital differentiator is proposed, which consists of the backward Euler differentiator $D_b(z)$ and the proposed delay compensator $C(z)$ in series, and is expressed as:

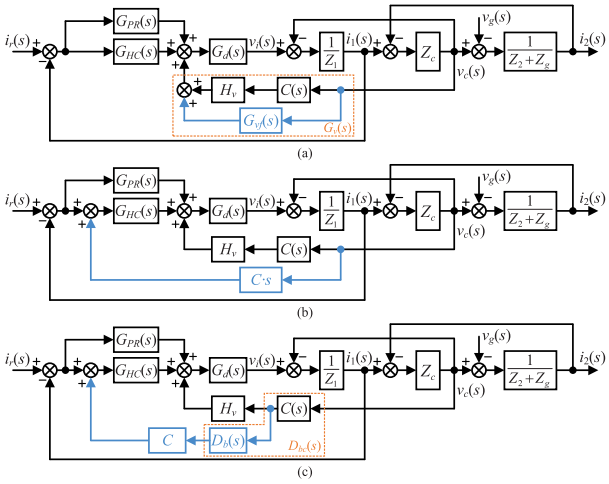

FIGURE 8. Equivalent transformation of block diagram of the ISC control system with the proposed CVF scheme. (a) High-pass filtered CVF. (b) Feeding the derivative capacitor voltage into HCs. (c) Digital differentiator implementation.

$$D_{bc}(z) = \frac{m+1}{mT_s} \cdot \frac{1 + (m-2)z^{-1} - (m-1)z^{-2}}{1 + mz^{-1}}. \quad (21)$$

The basic idea is to use $C(z)$ to compensate the phase lag of the half sampling period delay for $D_b(z)$ to achieve more accurate derivative characteristics. The frequency responses of different digital differentiators are shown in Fig. 9. It can be seen that the proposed differentiator matches the ideal differentiator more closely, achieving a good trade-off between phase lag and noise amplification at high frequencies. Finally, the control block diagram with the simplified admittance shaping scheme can be obtained as shown in Fig. 8(c).

V. EXPERIMENTAL VERIFICATION

In order to verify the correctness of the theoretical analysis and the effectiveness of the proposed scheme, simulations are initially conducted in MATLAB, followed by experiments on a single-phase grid-connected inverter experimental setup. The system parameters corresponding to the simulation model and experimental setup are listed in Table 1.

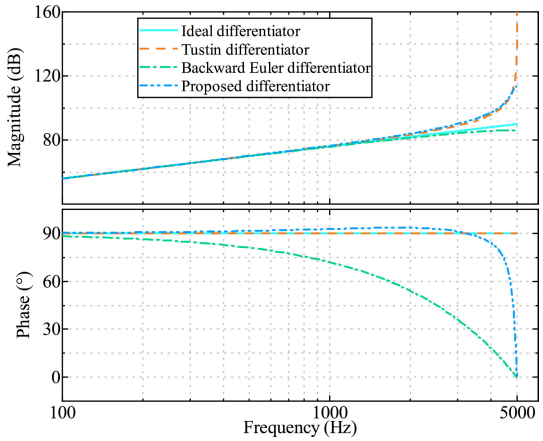

FIGURE 9. Frequency responses of different digital differentiators.

TABLE 1. System parameters.

Parameter	Symbol	Parameter
DC-link voltage	V_{dc}	400 V
Grid voltage	v_g	220 V
Fundamental frequency	f_g	50 Hz
Switching frequency	f_{sw}	16 kHz
Sampling frequency	f_s	16 kHz
Inverter-side inductance	L_1	600 µH
Filter capacitance	C	10 µF
Grid-side inductance	L_2	150 µH
Grid inductance	L_g	100/900 µH
PCC capacitance	C_g	22 µF

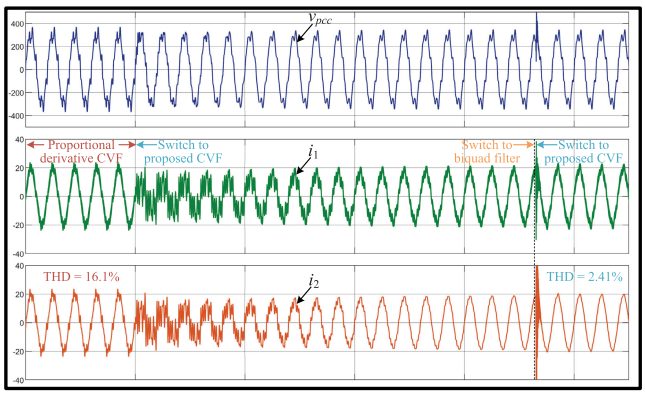

FIGURE 10. Simulation results under $L_g = 900\,\mu\text{H}$ and $C_g = 22\,\mu\text{F}$ when switching between different control schemes.

A. SIMULATION RESULTS

In order to highlight the superior control performance of the proposed CVF-based admittance shaping scheme, the simulation results of the proposed CVF scheme are compared with those of the admittance shaping methods in [19] and [24]. In [19], the biquad filter is used to extend the passive region for ISC control, but there are still nonpassive regions at high frequencies. In [24], the proportional-derivative PCC voltage feedforward is used to extend the passive region for the grid-connected inverter with L filter to $0.47f_s$ and enhance the grid-current harmonic suppression capability.

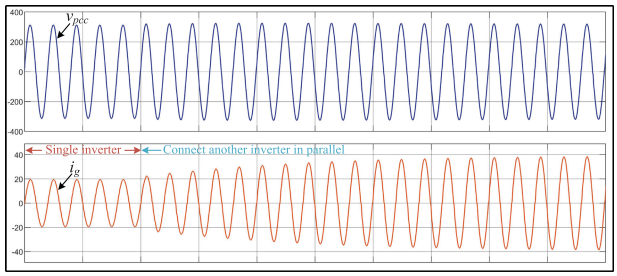

FIGURE 11. Simulation results when the inverter with proposed CVF scheme is connected to bus 2 of the IEEE 14-bus system.

When applied to the ISC-controlled *LCL*-type grid-connected inverter, the PCC voltage feedforward is replaced with CVF. The simulation results of the three control schemes under the capacitive grid condition with a total harmonic distortion (THD) of 14.4% are presented in Fig. 10. It can be seen that when the proportional-derivative CVF is used, the inverter can operate stably, attributed to the passive admittance almost up to the Nyquist frequency. However, the grid-side current i_2 is severely distorted with a THD of 16.1%, which is because the low inductance of the *LCL* filter and the filter capacitor weaken the harmonic suppression capability of the proportional-derivative CVF. When switching to the proposed CVF, the inverter is still able to operate stably, and the distortion in i_2 is significantly mitigated, with a low THD of 2.41%. However, when switching to the biquad filter, the system becomes unstable, and the current exhibits divergent oscillations, which is caused by the intersection of the grid admittance and the inverter output admittance in the nonpassive region at high frequencies. Therefore, the proposed CVF scheme not only achieves high system stability robustness, but also exhibits excellent harmonic suppression capability.

The stability robustness of the inverter system with the proposed CVF scheme is further tested under more complex grid conditions, such as the IEEE 14-bus system. The Simulink model of the IEEE 14-bus system built in [33] is employed, where the base power and base line voltage are set to 20kW and 381V, respectively. The simulation results corresponding to the proposed CVF controlled inverter being connected to bus 2 of the IEEE 14-bus system are depicted in Fig. 11, where the current i_g is the total grid current injected by multiple parallel inverters. It can be observed that when a single inverter is connected to bus 2, the inverter is able to operate stably. After connecting another inverter in parallel, the two inverters can operate stably simultaneously. Therefore, the proposed CVF scheme can ensure the stability of the inverter system under complex grid conditions, and achieve the plug-and-play functionality for the inverters.

B. EXPERIMENTAL RESULTS

Experiments are first conducted under different grid impedance conditions to verify the effectiveness of the proposed delay compensated CVF in enhancing passivity. Before conducting the experiments, theoretical stability

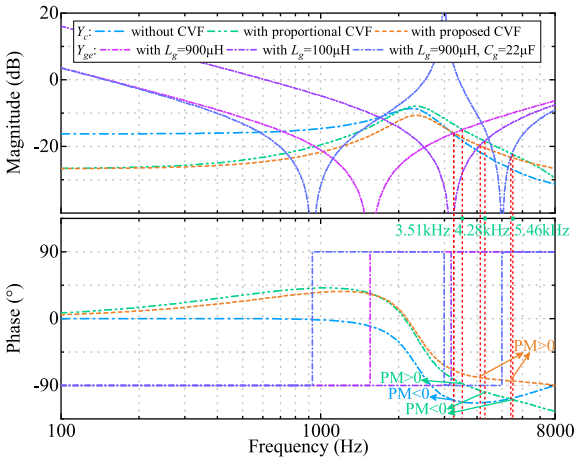

FIGURE 12. Bode diagrams of inverter output admittance Y_c with different CVF and equivalent grid admittance Y_{ge} with different L_g and C_g.

assessments are performed using Bode diagrams of the inverter output admittance Y_c and the equivalent grid admittance Y_{ge}. As shown in Fig. 12, for ISC control without CVF, Y_{ge} intersects Y_c in the nonpassive region under the grid condition with $L_g = 900\,\mu\text{H}$, resulting in a negative PM, which indicates the system instability. Using the proportional CVF can extend the passive region for the ISC control, resulting in a positive PM at the intersection of Y_{ge} and Y_c. The corresponding experimental results are presented in Fig. 13. It can be seen that without CVF, the system becomes unstable and the inverter-side current i_1 exhibit the exponentially amplified oscillation. When the control scheme is switched to with proportional CVF, the oscillation begins to decay and stable operation is eventually restored, where the actual decaying oscillation frequency ($\approx 3.52\,\text{kHz}$) matches very closely with the theoretical one ($\approx 3.51\,\text{kHz}$). However, the proportional CVF cannot completely eliminate the nonpassive region at high frequencies for ISC control. Under the inductive grid condition with $L_g = 100\,\mu\text{H}$ or capacitive grid condition with $L_g = 900\,\mu\text{H}$ and $C_g = 22\,\mu\text{F}$, Y_{ge} and Y_c will intersect in the nonpassive region, as shown in Fig. 12. With the proposed delay compensated proportional CVF, the passive region is extended to the Nyquist frequency, so that the PM at the intersection of Y_{ge} and Y_c is always positive regardless of the grid conditions. The corresponding experimental results are presented in Fig. 14 and 15. It can be seen that when the control scheme is switched to with proportional CVF, the inverter-side current i_1 and the grid-side current i_2 exhibits the exponentially amplified oscillation, where the actual oscillation frequency is very close to the theoretical one. When the control scheme is switched to the delay compensated proportional CVF, the oscillation decays rapidly and stable operation is restored. Therefore, it can be concluded that the proposed delay compensated proportional CVF can passivate the inverter output admittance for ISC control almost up to the Nyquist frequency, which ensures high robustness of system stability against grid impedance variations. Experimental results with

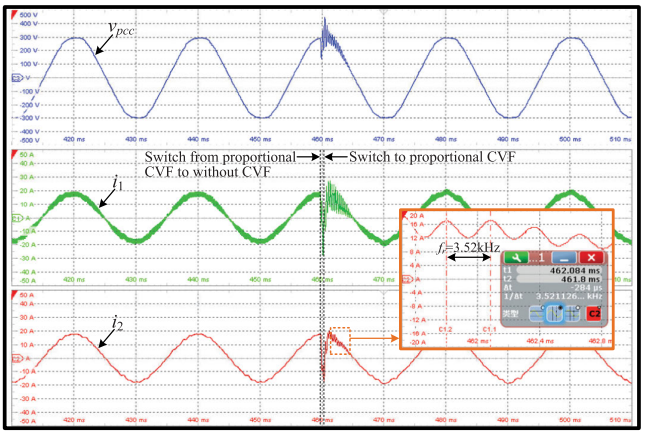

FIGURE 13. Experimental results under $L_g = 900\,\mu\text{H}$ when the ISC control is switched from with proportional CVF to without CVF.

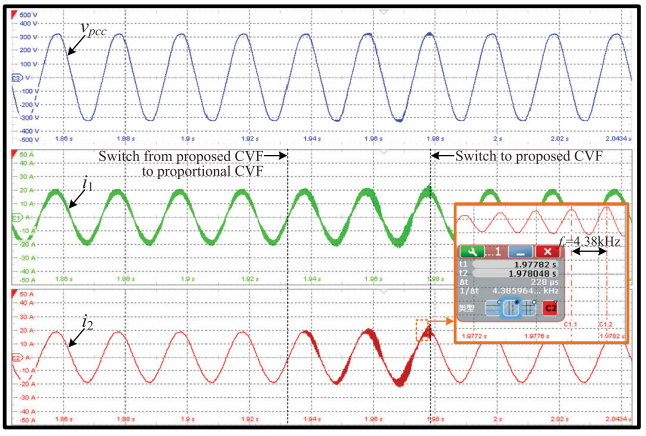

FIGURE 14. Experimental results under $L_g = 100\,\mu\text{H}$ when the ISC control is switched from with delay compensated proportional CVF to proportional CVF.

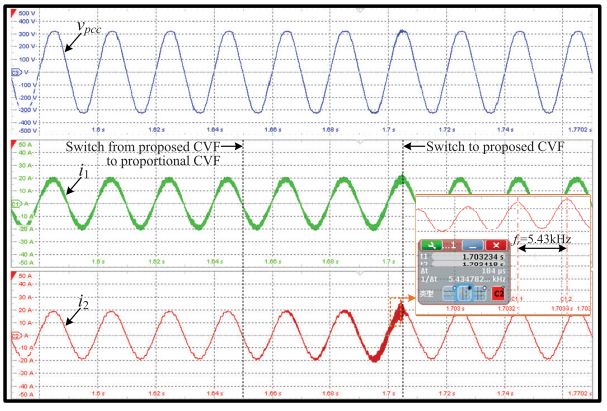

FIGURE 15. Experimental results under $L_g = 900\,\mu\text{H}$ and $C_g = 22\,\mu\text{F}$ when the ISC control is switched from with delay compensated proportional CVF to proportional CVF.

the proposed CVF when the current reference is switched from half load to full load is shown in Fig. 16. It can be seen that the inverter system has good dynamic performance.

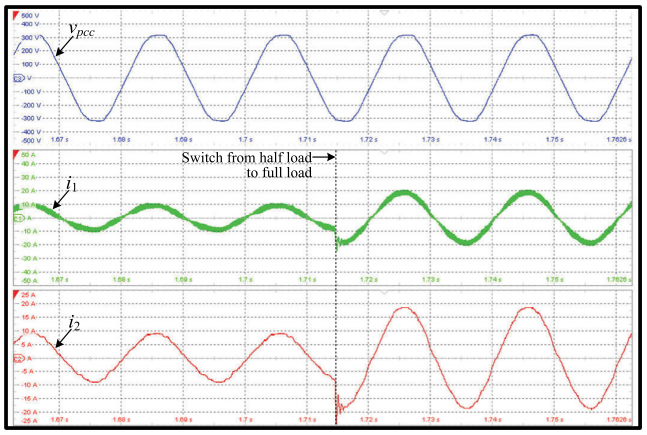

FIGURE 16. Experimental results with the proposed CVF when the current reference is switched from half load to full load.

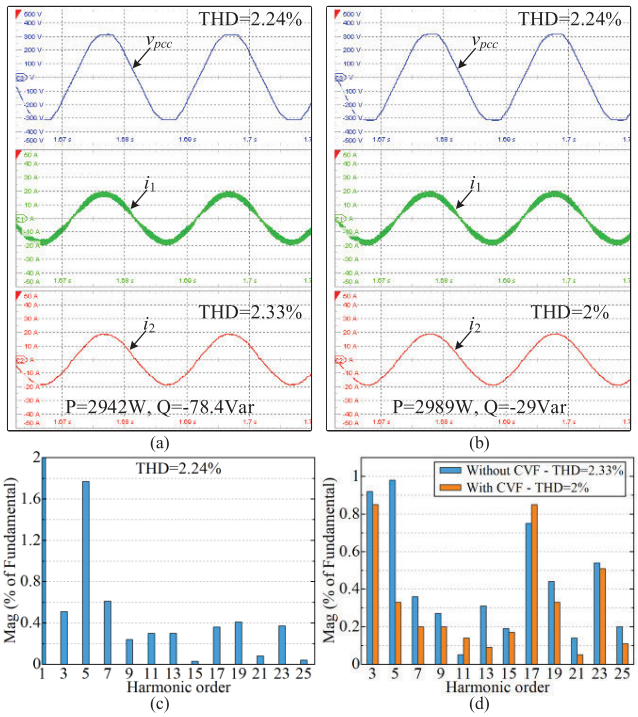

FIGURE 17. Experimental results under $L_g = 100\,\mu$H. (a) Steady-state waveforms without high-pass filtered CVF. (b) Steady-state waveforms with high-pass filtered CVF. (c) FFT result of v_{pcc}. (d) FFT result of i_2.

Then, experiments are carried out under grid voltage distortion to verify the effectiveness of the proposed high-pass filtered CVF in grid-current harmonic suppression. To mitigate the grid-current distortion caused by the dead time effect and grid background harmonics, resonant controllers of the 3rd, 5th, 7th, 9th, 11th, and 13th order harmonics are chosen to form the HCs. Without the high-pass filtered CVF, the resulting steady-state experimental waveforms are presented in Fig. 17(a), and the corresponding fast Fourier transform (FFT) result is given in Fig. 17(d). It can be found that since v_{pcc} has a small total harmonic distortion (THD) of 2.24%, a satisfactory THD of 2.33% can be achieved for i_2 using only HCs. As can be seen from Fig. 17(c), the 5th and 7th harmonics dominate the THD of v_{pcc}. To test the effectiveness of the proposed high-pass filtered CVF, the derivative capacitor voltage is fed into the resonant controllers corresponding to these two harmonics, and the resulting steady-state experimental waveforms are shown in Fig. 17(b). From the corresponding FFT result in Fig. 17(d), it can be found that the 5th and 7th harmonics in i_2 are significantly attenuated, resulting in a smaller THD of 2%. Therefore, it can be concluded that the proposed high-pass filtered CVF can enhance the grid-current harmonic suppression capability of the ISC-controlled *LCL*-type grid-connected inverter.

VI. CONCLUSION

This article proposes a simple and cost-effective admittance shaping scheme based on CVF for the ISC-controlled *LCL*-type grid-connected inverter, which consists of the delay compensated proportional CVF for passivity enhancement and the high-pass filtered CVF for grid-current harmonic suppression. The delay compensated proportional CVF can passivate the inverter output admittance almost up to the Nyquist frequency, and the high-pass filtered CVF can greatly reduce the harmonic admittance magnitude at the harmonic frequencies to achieve sufficient harmonic attenuation. Therefore, the proposed admittance shaping scheme can simultaneously ensure high robustness of system stability against grid impedance variations and excellent harmonic suppression capability under grid voltage distortion. Experimental results have verified the effectiveness of the proposed scheme.

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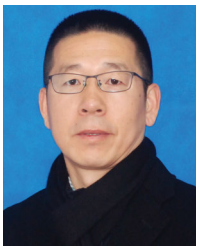

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