RESEARCH ARTICLE

Compact, High-Speed Mach-Zehnder Modulator With On-Chip Linear Drivers in Photonic BiCMOS Technology

CHRISTIAN KRESS[1], **TOBIAS SCHWABE**[1], **HANJO RHEE**[2], **AND J. CHRISTOPH SCHEYTT**[1], (Member, IEEE)

[1]Department of System and Circuit Technology, Heinz Nixdorf Institute, Paderborn University, 33098 Paderborn, Germany
[2]Sicoya GmbH, 12489 Berlin, Germany

Corresponding author: Christian Kress (christian.kress@uni-paderborn.de)

ABSTRACT A monolithically integrated electronic-photonic Mach-Zehnder modulator is presented, incorporating electronic linear drivers along with photonic components. Electro-optical 3 dB & 6 dB bandwidths of 24 GHz and 34 GHz, respectively, were measured. The measurements are in good agreement with electronic-photonic post-layout simulation results and verify the design methodology. A full π phase shift was achieved by applying a differential input voltage of $V_\pi = 420$ mV to the driver input, effectively decreasing the required modulation voltage by a factor of approximately 10.

INDEX TERMS Electronic-photonic-integrated circuit, electro-optical modulators, integrated Mach-Zehnder modulators, photonic BiCMOS technology.

I. INTRODUCTION

Next generation network infrastructure relies on optical broadband systems, delivering high data rates at low power consumption and small form factors [1]. In the competition between different materials and technology approaches, silicon photonics (SiP) is one of the high potential candidates. Decades of fabrication experience, resulting in high material quality, high yield, and easy scalability make SiP an attractive competitor and could be an enabler for new applications on a global scale. In addition, the high refractive index contrast in SiP allows for extremely small waveguides and dense integration of optical components, which makes SiP the only technology platform for highly complex electronic-photonic integrated circuits [2].

The major high-speed modulation mechanism is based on the plasma dispersion effect (PDE). Plasma dispersion phase shifters can be realized as lateral P- and N-doped rib waveguides which form a carrier depletion zone in a PN-junction that can be modulated by an applied reverse

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voltage. Although this mechanism has a slightly non-linear characteristic [3], the main driving scheme is to apply as high voltage as possible to the phase shifters. There are several C- or O-band high-speed SiP modulators in literature, which incorporate silicon Mach-Zehnder modulators (Si-MZM) on a photonic integrated circuit (PIC) [4], [5], [6], [7], [8], [9], [10], where the main focus is on optimizing the bandwidth. But as a PIC modulator, they still need external, robust driving electronics that are capable to deliver high voltage swings to the Si-MZM load for broadband operation. The packaging of an electronic integrated circuit (EIC) which is connected to the Si-MZM PIC is called hybrid chip topology. There are hybrids using bondwire connections of two neighbouring chips or flip-chip, also called 2.5D/3D-integrated solutions [11]. On the electronics side, simple [12] or distributed drivers [13] can be observed. It should be mentioned that hybrids also allow the combination of different material platforms and thereby enable best-in-class photonic and electronic components. However, the scope of this manuscript is fabrication in silicon and CMOS-compatibility. Among the CMOS-compatible photonic platforms there are monolithically integratable photonic circuits, combining

electronic and photonic integration on the same silicon sub-strate [14], [15]. Those electronic-photonic integrated circuits (ePIC) are of particular interest as they allow for shortest interconnects, reduced resistive and capacitive parasitics, and low packaging cost [16]. Our transmitter chip is designed in a photonic BiCMOS technology, featuring silicon-germanium hetero bipolar transistors (HBT), providing improved driving capabilities than their MOS based counterparts [17]. Our ePIC comprises a silicon Mach-Zehnder modulator based on reverse biased PN junction phase shifters and differential, linear segment drivers, reducing the demand for external signal input voltages by a factor of 10. In addition, the linear driving scheme allows for higher modulation formats like PAM4. The measured 3 dB and 6 dB bandwidths of 24 GHz and 34 GHz respectively, are among the highest reported in this technology class while delivering almost twice as much gain [18] (see Tab. 1). Without signal pre-emphasis, we were able to transmit up to 60 Gbit/s in NRZ and 80 GBit/s in PAM4 transmission schemes.

This manuscript is organized in two sections: in section II the design and methodology of the ePIC Si-MZM is being reviewed, followed by section III in which measurement setups and results are being discussed. A state-of-the-art comparison and discussion in section IV concludes this paper.

II. DESIGN CONSIDERATIONS

As already mentioned, high-speed optical modulation in SiP technology is most commonly achieved using the plasma-dispersion effect in reversed biased PN-doped phase shifters (PS). The carrier depletion zone is being modulated by means of an applied voltage. However, the combination of low modulation efficiency and voltage operation range, that are convenient for microelectronic devices, necessitate geometrically long phase shifter structures, which, in turn, require transmission line (TL) theory for proper modeling and simulation. The electro-optic phase shifters (PS) in this photonic BiCMOS technology are lateral, PN-doped photonic waveguides with $V_\pi L = 2.9$ Vcm at -2 V reverse voltage. A modulation voltage of $V_M = 4.6$ V_{pp}, which we have reached with the driving circuitry, would result in a PS length of at least 6.24 mm, when a full π phase shift is targeted. Considering material parameters in this technology and typical microwave velocities, this length equals a wavelength of a 20-30 GHz modulation, which supports the claim that TL theory and phase velocity mismatch compensation has to be considered to achieve high-speed operation.

A feature that monolithically integrated ePICs offer is the possibility to place the driving circuitry along the photonic phase shifters and realize a segmented topology with distributed driving (s. Fig. 1(b) & 3) in contrast to the commonly used traveling-wave electrode (TWE) method (s. Fig. 1(a)). The typical TWE method has several drawbacks favoring the segmented approach: The TLs in a typical TWE MZM are directly loaded with the phase shifters, which influences the characteristic impedance $Z_0 = \sqrt{L_0/(C_0 + C_L)}$ and
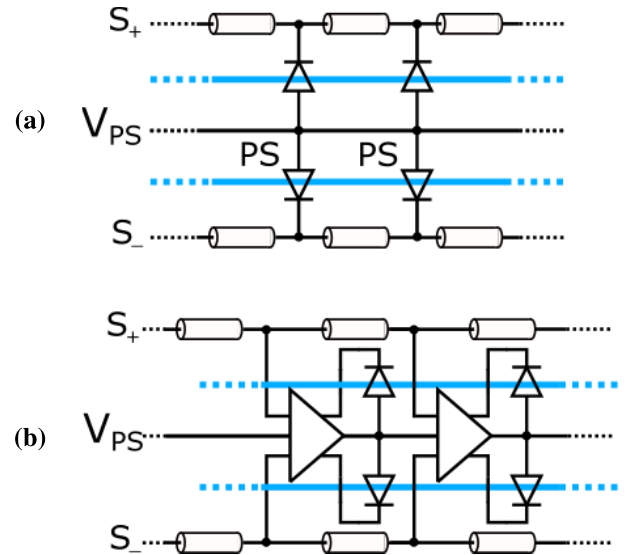
FIGURE 1. (a) Typical topology and setup for co-simulation for TWE MZMs using segmented small phase shifter sections. Phase shifters are directly coupled to the TL. (b) Segmented MZM topology with segment drivers loading the TL. Each segment driver has a pair of phase shifters as differential load.

electrical propagation delay $\tau_e = \sqrt{L_0 \cdot (C_0 + C_L)}$ where L_0 and C_0 are TL length specific inductance and capacitance and C_L the PS's load capacitance [19]. Those two metrics have to be conjugately matched to the load of an electronic driver and optical propagation properties of the MZM (s. sec. II-C). However, as the junction capacitance of the PS is a function of the applied reverse voltage, matching can only be achieved at a certain reverse voltage. This is a drawback as the reverse voltage simultaneously affects the modulation efficiency. In addition, the segmented driving topology has another advantage with regard to the system bandwidth. Loading a TL doesn't only affect it's wave impedance and propagation delay, but also the microwave losses. The output impedance of a minimum sized bipolar transistor in this technology has lower capacity and higher small-signal resistance than a PS segment, which will be further discussed in sec. II-B and sec. II-C. Hence, the loading with small transistors decreases microwave losses and increases bandwidth compared to the case when the TL is directly loaded with PS segments. Obviously, the latter is accompanied by a reduction of the extinction ratio when the modulation frequency is increased [20].

A. MZM ARCHITECTURE & PHOTONIC COMPONENTS

The maximum single-ended voltage swing over a single transistor is limited by collector-base breakdown. Optimal use as a voltage driver can be achieved by choosing a symmetric MZM with phase shifters in each arm, receiving complementary signals, which can be realized using a differential driver in a dual-arm push-pull scheme (s. Fig. 1(b) and 3). By this means, the modulation voltage V_M equals the differential drive voltage V_{diff}, which is twice the

single-ended drive voltage V_{se}, therefore $V_M = V_{diff} = 4.6V_{pp,d} = 2 \cdot V_{se} = 2 \cdot 2.3V_{pp}$. Although a differential driving scheme is chosen, the electrodes for each arms can be treated as single-ended TLs with sufficient distance between the arms. Photonic routing has been implemented using rib waveguides with approximately 0.3 dB/mm intrinsic loss. By suitable doping and metal contacts these rib waveguides can be upgraded to lateral phase shifter segments. Splitting and combining of photonic WGs has been realized by 2 × 2 multi-mode interferometers (MMI). The advantage of using a 2 × 2-MMI is the additional monitoring output at the cost of possible splitting imbalance and, consequentially, reduced extinction ratio. However, the achieved DC extinction ratio of 43 dB (s. Fig. 8) proves that low imbalance can still be achieved, probably due to excellent fabrication tolerance. Optical fiber-to-chip coupling has been achieved by means of tapered grating couplers. As Fig. 3 suggests, the MZM arms consist of 16 PS segments, adding up to an effective PS length of 6.24 mm, matching the driver results for a full π phase shift. The bias point of the Si-MZM is set by using temperature phase shifters, which is further discussed in sec. II-F.
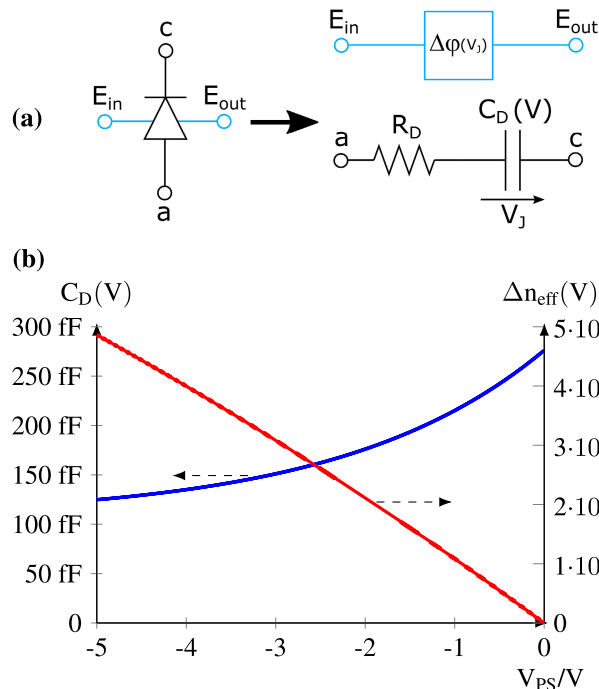
B. PHASE SHIFTER MODELING & ELECTRONIC-PHOTONIC CO-SIMULATION

Precise modeling is key for proper simulation and eventually good measurement results. We have modeled the reverse biased, lateral PN phase-shifter electrically simply by a series resistance R_s, presenting ohmic losses of the doped P and N-regions, and a junction capacitance $C_J(V)$ modelling the PN-junction (s. Fig. 2(a)), which is also voltage dependent [21]. In addition, for the electro-optical interaction a relationship between the applied voltage and acquired phase change is needed when combining electrical and optical simulation. Electro-optical co-simulation is and has been investigated and developed by many groups and software companies [2]. We have implemented a photonic Verilog-A library for all photonics components in that technology according to [22], which is a performant solution for single wavelength transmission (s. Fig. 2(a)). In order to run simulations of the co-designed Si-MZM, all parameters that model electrical, optical and electro-optical behavior had to be determined through measurement or device simulation. With regard to the phase shifters, parameter fitting of R_s, $C_J(V)$ and Δn_{eff} has been performed to approximate measurement S-parameters. Best mathematical approximation has been found using:

$$C_J(V,L) = (169.3e^{0.445V} + 106.6) \text{ fF} \cdot \frac{L}{1 \text{ mm}} \quad (1)$$

$$\Delta n_{eff}(V,L) = 19.4e^{-4}(1 - e^{0.057V}) \cdot \frac{L}{1 \text{ mm}} \quad (2)$$

The series resistance is fitted proportional to the PS length as $R_s = 18.9 \ \Omega \cdot 1 \text{ mm}/L$. The intrinsic cut-off frequency of the phase shifters is independent from the actual length as series resistance and junction capacitance scale inversely
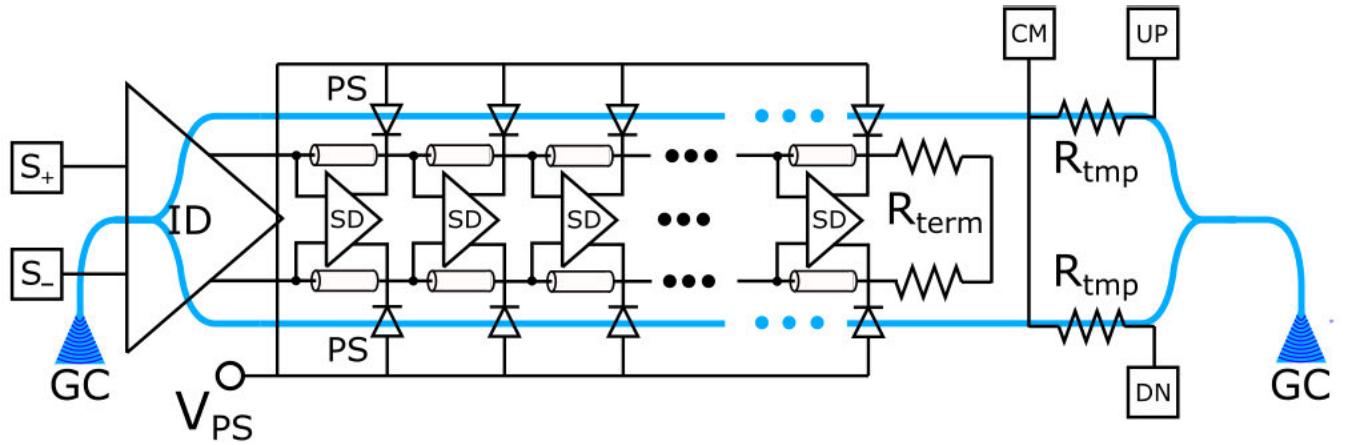

(a)

(b)

FIGURE 2. (a) Photonic Verilog-A model controlling optical and electrical properties. (b) Phase shifter model properties for a 1 mm long phase shifter: Junction capacitance of the lateral phase shifter PN junction. Relative refractive index change according to PN diode voltage in reverse operation.

proportional with the length $f_{3dB}(V) = 1/2\pi R_s C_j(V)$. However, in a lumped element approach the length matters once a voltage source with extrinsic impedance R_{drv} is driving the PS, effectively reducing the maximum bandwidth to $f_{3dB}(V) = 1/2\pi (R_s C_j(V) + LC_j(V)R_{drv})$. Thereby, the intrinsic phase shifter bandwidth scales depending on the actual reverse voltage from approximately 30 GHz at $V_{PS} = 0V$ to 47 GHz at $V_{PS} = -2V$. A length-dependent optical delay of 12.4 ps/mm has been inserted in the model in accordance with an Eigenmode simulation for the utilized rib waveguide geometry. We have chosen a PS length of 390 μ m, well below $1/10^{th}$ of the free-space RF wavelength divided by RF effective index considering bandwidths below 50 GHz [23].

C. TRANSMISSION LINE DESIGN

As well established knowledge, three main design targets have to be met in order to design a high-speed Mach-Zehnder modulator when TL theory has to be considered. First, the velocities of optical and electrical waves have to match, otherwise a reduction of the achievable bandwidth and extinction ratio will occur. The phase transfer function for a traveling wave electrode can be derived as

$$H(f) = e^{\frac{\alpha L}{2}} \sqrt{\frac{\sinh^2\left(\frac{\alpha L}{2}\right) + \sin^2\left(\frac{\psi L}{2}\right)}{\left(\frac{\alpha L}{2}\right)^2 + \left(\frac{\psi L}{2}\right)^2}} \quad (3)$$

FIGURE 3. Block diagram of the chip topology: Optical coupling through grating couplers (GC). An input driver amplifies the input signal to transmission lines, which are loaded with segment drivers (SD). Each SD differentially drives a pair of silicon phase shifters (PS). The transmission lines are terminated with R_{term}. The bias point of the Mach-Zehnder is controlled using heater phase shifters in each arm, which are modelled using R_{tmp}.
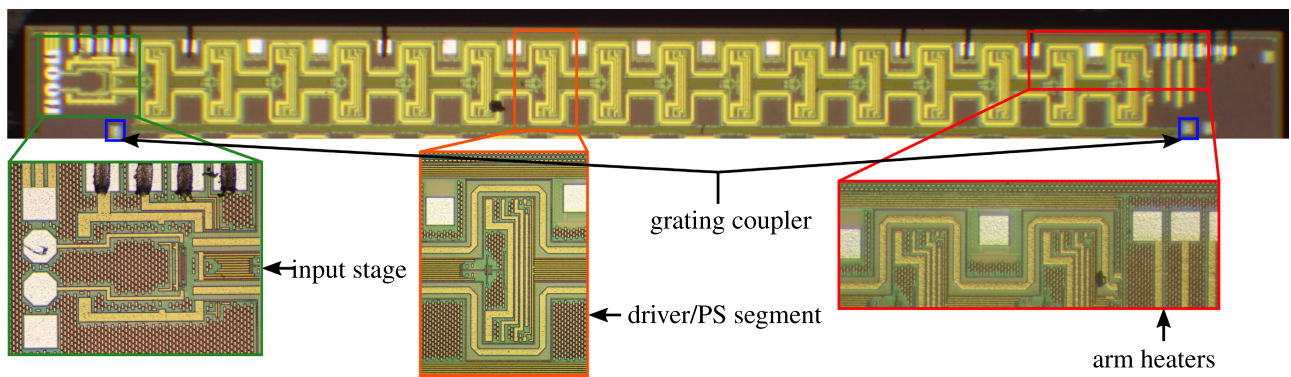
FIGURE 4. Chip picture of the fabricated ePIC transmitter. Supply and bias voltages are applied through bondwire connections and distributed over the whole MZM length. High frequency electrical signals are applied through probing (left). Close-ups of input and segment drivers as well as TL meandering are shown.
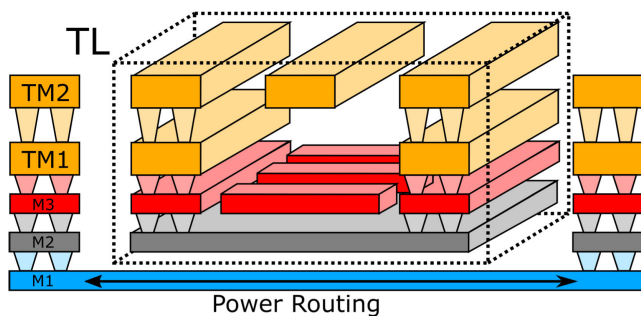
FIGURE 5. Cross section of the slow-wave transmission line. The metal stack allows for 5 routing metals. Utilization of complete metal stack would prevent to route electrical power to segment drivers. The effect of slow-wave structures on M3 level can be engineered by changing the duty cycle.

where $\alpha(f)$ describes the microwave loss, and $\psi(f) = \frac{2\pi f(n_{eff}^e - n_{eff}^o)}{c}$ with n_{eff}^e and n_{eff}^o electrical and optical group refractive indexes [24]. When neglecting microwave losses, the formula simplifies to a sinc-function with the electrode

length L and the group index difference as arguments. It can be derived, that the longer an electrode, the better has to be the velocity matching if bandwidth degradation is to be diminished. Secondly, the wave impedance of the TL must match the source impedance and termination, otherwise reflections will be the major disturbance in the transmitter system. Thirdly, microwave losses have to be kept as small as possible to allow for broadband operation.

In the typical TWE approach, the TL is directly loaded with the phase shifter or phase shifter segments, presenting a large capacitive load to it. As already described, this capacitive load significantly influences the TL's property, namely the wave impedance and electrical wave velocity. In addition, that capacitance is depending on the reverse voltage of the phase shifters and can therefore vary wave impedance and velocity. An easier approach, as mentioned, is to load the TLs with segment drivers, which present significantly lower capacitive and higher resistive loads to the TL as well as add gain in the overall driving scheme (s. sec. II-E). As TLs we have chosen shielded coplanar transmission lines (s. Fig. 5) for several reasons: the shielding

prevents from unwanted signal coupling into the substrate or driver as well as crosstalk between the TLs, which is essential in multi-channel systems. In addition, slow-wave structures on metal 3 layer (red) have been inserted [25]. By controlling the duty cycle of these metals the velocity of the electrical wave can be tuned, which helps with the requirement of velocity matching in the MZM. In the typical TWE approach, the whole metal stack can be utilized to design a TL according to the given requirements. In the segmented approach, electrical power has to be delivered to each of the segment drivers. If those drivers draw a lot of current, supply lines along the TL would experience severe voltage drops and the segment drivers would consequently not operate under optimal conditions. It is better to bridge the TL without interfering it, so we routed the power over wide metal lines of the lowest metal in the stack (s. Fig. 5). Despite using slow-wave TLs, velocity matching is mainly achieved by meandering the TLs, effectively lengthening the TLs by exactly the velocity mismatch proportion (s. Fig. 4). While meandering solves the velocity condition (s. eq. 3), impedance matching and lowering of microwave losses still have to be targeted. Microwave losses consist of conductive, dielectric and radiation losses, where radiation losses are negligible in our TL geometry. Conductive losses have a strong frequency dependency and become the dominant loss factor for broadband operation [26], hence conductive losses should be minimized as much as possible. Hence, the width of the signal line in a coplanar-TL needs to be increased. When trying to keep the wave impedance constant, the gap to ground plane needs to scale with the width of the signal line. When the gap can't be scaled further, the TL becomes more capacitive and the wave impedance reduces. Smaller wave impedance comes with the cost of increased power dissipation of TL driver, however, as the segment drivers provide most of the gain, this is tolerable in our design. Due to geometrical limitations with the meandering approach, a $\sim$40 Ohm TL was found to be a good design trade-off. This has been achieved with a signal line width of 17.8 μ m and a gap of 14.1 μ m. The TL was terminated on-chip with $R_{term} = 40$ Ω (s. Fig. 4(a)).

D. DRIVER INPUT STAGE

The input stage consists of a two-stage amplifier: a first stage with a differential 50 Ω interface and a consecutive stage which drives the loaded transmission line (s. Fig. 6). The first stage comprises a differential common-collector (CC) amplifier presenting high impedance in parallel to the 100 Ω resistor matching to differential 50 Ω lab equipment. In addition, the biasing of the driver can be changed by flexibly adapting the bias voltage. The differential driver with 40 Ω resistors in the collector path is loaded with the TL (s. sec. II-C). Bandwidth extension techniques such as cascode topology to decrease the Miller effect and capacitive peaking were applied to increase bandwidth ($R_E = 18$ Ω, $C_E = 200fF$, $Q_{1,2,casc}$ with 6 emitter fingers). Low-ohmic
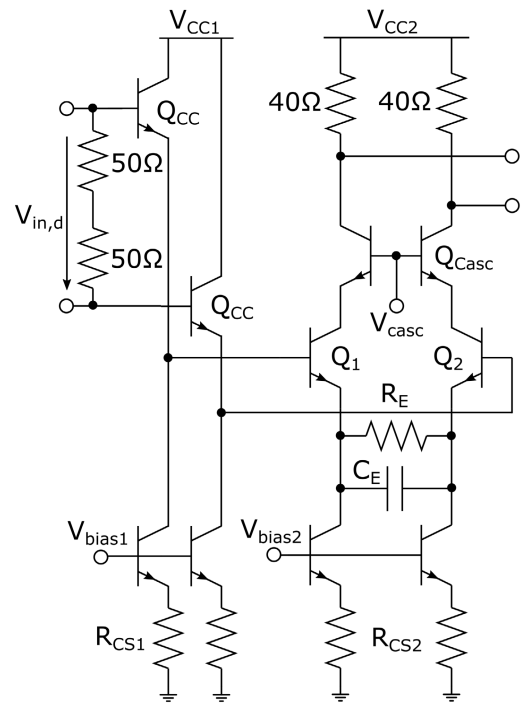

FIGURE 6. Input driver schematic with a 50 Ω input interface. The subsequent driver is a differential 40 Ω TL driver featuring cascode topology and capacitive peaking for bandwidth extension.

termination resistors come at the cost of higher power to achieve a constant voltage swing. The current of the two stages is provided by current mirrors with additional resistors for temperature stability ($R_{CS1} = 430$ Ω, $R_{CS2} = 45$ Ω). Splitting the current sources in the differential amplifier allows for higher current drives. The circuit operates with two supply voltages $V_{CC1} = 3.3V$ and $V_{CC2} = 5V$.

E. SEGMENT DRIVERS

The TLs are loaded with multiple segment drivers differentially driving pairs of phase shifters. The advantage of loading the TL with segment drivers in contrast to directly load it with PN phase shifters is that the segment drivers present a significantly lower capacitive load and thereby have less impact on the TL properties. Methodologically, this allows to separate design and optimization of TL and drivers. The segment driver comprises a differential cascode driver and a two-stage single-ended common-collector driver for each phase shifter pair (s. Fig. 7). The input transistors $Q_{CC,1}$ (1 emitter finger) present ten times less capacitance than the corresponding Si PS for the segment. In addition, negative Miller capacitances C_{Comp} have been inserted, so that the segment drivers effectively do not present capacitive loads to the TL. Voltage gain is provided by the differential driver ($Q_{1,2,casc}$ 2 emitter fingers) with collector resistors $R_C = 735$ Ω. Several methods have been exploited to increase the bandwidth of the segment drivers. A cascode topology has been chosen decreasing the Miller effect. Capacitive peaking has been applied by means of resistive

and capacitive emitter degeneration with C_E = 340 fF and R_E = 120 Ω. Furthermore, the highly capacitive phase shifters are not directly connected to the collector node of Q_{casc}, but buffered using two consecutive common collector amplifiers (Q_{CC1} 1 emitter finger, Q_{CC2} 6 emitter fingers, R_{CC1} = 2 kΩ, R_{CC2} = 400 Ω). As argued in section II-B, a low source impedance of a driver has less degradation affects on the intrinsic PS bandwidth. Hence, the buffering with common-collector amplifiers increases the driving bandwidth as the the effective drive impedance is lowered by means of emitter followers. It is noteworthy, that the reverse voltage of the phase shifters still affects the overall system bandwidth as the reverse voltage affects the capacitance of the segment driver load (s. Fig. 2(b)) and decreases it's electronic bandwidth. The segment drivers provide broadband amplification of 15 dB (post-layout simulation) with a peaking ripple of 17.6 dB. The total voltage gain of the combination of input and individual segment drivers ranges from 20.7 dB, probed at the first segment, to 17.2 dB, probed at the last segment due to transmission lines loss. As the total phase shift is accumulated over each segment, we have measured an effective voltage gain of approximately ten, allowing for a π phase shift with from a differential input voltage of only 420 mV [29].
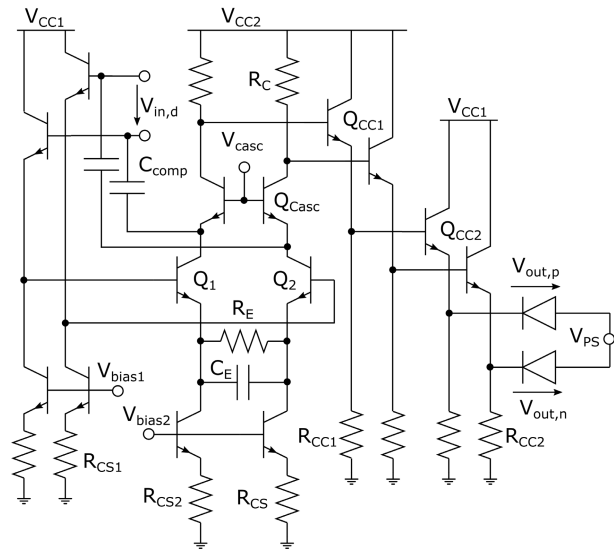

FIGURE 7. Segment driver schematic: Differential amplifier featuring capacitive peaking is utilized for a broadband amplifier. The phase shifters are connected to the differential amplifier via two cascaded emitter followers.

F. MZM BIAS POINT CONTROL

The most suitable method to set the operating point of the Si-MZM is to utilize thermo-optic tuning instead of PDE. First of all, thermo-optic phase shifters do not add optical losses as PN phase shifters do. Secondly, the thermo-optic effect is more efficient than PDE allowing for significantly shorter phase shifter sections [27]. Thirdly, when using the already existent PN phase shifters for setting the bias

point means that a difference in DC voltage has to be applied to the respective arms, which in turn is translated into a asymmetric load to the differential driver (s. eq. 1) which is unwanted. Thermo-optic phase shifters, or simply heaters near waveguides, can be designed in different ways, compliant to Si CMOS processes [28]. Our approach was to use resistive elements in form of highly doped waveguides in close proximity to the actual photonic waveguides. The heaters have been placed after the high-speed PS sections (s. Fig. 3 & 4). Using heaters with less than 300 μ m length, we were able to accumulate a 2π phase shift by applying up to 50 mW in one of both arms (s. Fig. 8). Thereby, any of the typical bias points can be set: maximum, minimum or quadrature point. A DC extinction ratio of 43 dB could be measured, which emphasizes high quality and symmetry of the fabricated waveguides, splitters, combiners, and phase shifters. The long PN phase shifters and heater sections dictate the dimensions and area of the chip of 7.57 mm · 0.66 mm = 5 mm^2.
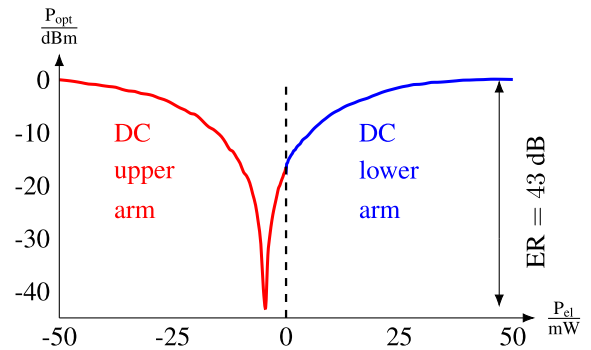
FIGURE 8. Bias control measurement via heater phase shifters. Electrical power is either applied to the heaters in the upper arm or the lower arm. Full 2π phase shift is achieved by applying up to 50 mW in one of the MZM arms.

III. RESULTS & DISCUSSION

Multiple experiments have been carried out to evaluate the performance of the Si-MZM. Optical laser light at 1550 nm wavelength was launched from a CW laser and applied and collected by means of grating couplers (s. Fig. 4). Electrical high-speed signals were applied via a 67 GHz GSSG probe (GGB probe).

An S-parameter measurement at the MZM's quadrature point was conducted using a vector network analyzer (Anritsu MS4746B) and an external 70 GHz photodiode (II/VI XPDV3120R). The influence of the probe and photodiode (PD) were subtracted from S_{21} measurement. A measurement of 3 dB & 6 dB bandwidths lead to 24 GHz and 34 GHz respectively (s. Fig. 9). In addition, graphs of pre- and post-layout simulation results are displayed which validates the approach of optical co-simulation using VerilogA models for the photonic components. Although there are some deviations in the measurement from the post-layout simulation, there is obvious agreement in the identified bandwidths.

TABLE 1. State-of-the-Art Monolithic ePIC Si-MZMs.

	[31]	[18] [34]	[14] [30] [32]	[33]	[35]	[36]	[37]	This work
Technology	0.25 µm Photonic BiCMOS	0.25 µm Photonic BiCMOS	90 nm Photonic CMOS	90 nm Photonic CMOS	0.25 µm Photonic BiCMOS	0.25 µm Photonic BiCMOS	0.25 µm Photonic BiCMOS	0.25 µm Photonic BiCMOS
Modulation type	*PN-PS	*PN-PS	*PN-PS	*PN-PS	*PN-PS	*PN-PS	*PN-PS	*PN-PS
Driver type	Limiting	Linear	Limiting	Limiting (segmented)	Linear	*ns	Linear	Linear
Bandwidth (GHz)	3 dB: *ns 6 dB: *ns	3 dB: 20.8 6 dB: 23.5	3 dB: 12.5 6 dB: 21	3 dB: 21 *ls	3 dB: 18.5 6 dB: 19.5	3 dB: 14.9 6 dB: 25.7 (simulated)	3 dB: 33.4 6 dB: 34.5	3 dB: 24 6 dB: 34
ER (dB)	ns	13.3 (28 Gb/s)	4.7 (28 Gb/s)	6 (50 Gb/s)	13 (28 Gb/s)	7.6 (35 Gb/s)	3 (44 Gb/s)	10 (30 Gb/s)
Max. Data Rate (Gb/s)	74 (PAM4)	32 (NRZ)	32 (NRZ)	56 (PAM4)	50 (PAM4)	37 (NRZ)	44 (NRZ)	80 (PAM4)
Actual V_π (V)	5.03	4.77	5.25	4.9 (MSB+LSB)	4.76	7.5	12	4.7
External V_π (V)	*ns	1.06	*ns	*ns	*ns	*ns	*ns	0.42
Power (W)	1	2	0.135	0.27	1.5	1.44	0.5	1.7
Footprint (mm^2)	14.5	12.7	~ 2.1	*ns	12.7	4.5	5.6	5.06

*ns = not specified
*ls = long segment
*PN-PS = reverse-biased PN-junction phase shifters
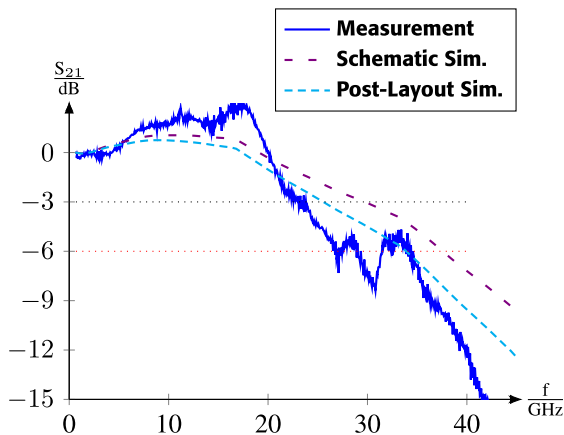*EAM = electro-absorption-modulator (only in L-Band, $\Lambda = 1600 nm$)

FIGURE 9. S21 electro-optical response of ePIC MZM with external 70 GHz photodiode versus pre- and post-layout simulation.

FIGURE 10. Linearity measurement with spurious-free dynamic range (SFDR, green, left), signal-to-distortion (SDR, red, left) and total harmonic distortion (THD, right) of the whole transmission system including ePIC transmitter and external photodiode. Measurements were performed at frequency $f = 1$ GHz. Dotted lines show the MZMs intrinsic non-linearity assuming a V_π of 420 mV.

A linearity measurement was performed setting a signal generator (Anritsu MG3694) to 1 GHz and evaluating the output via a spectrum analyzer (Anritsu MS2760). The quiescent operating point of the modulator was set to the quadrature point via heater elements. In the range of the previously determined V_π of 420 mV [29] the total harmonic distortion is below 2% (s. Fig. 10) which allows for higher order pulse amplitude modulation (PAM) schemes. In addition, the spurious-free dynamic range (SFDR), the measure between the fundamental tone and the strongest harmonic, which was the third harmonic, is depicted in the same graph. As the graph indicates, the SFDR measures 44 dBc at an input voltage of 100 mV, converging to
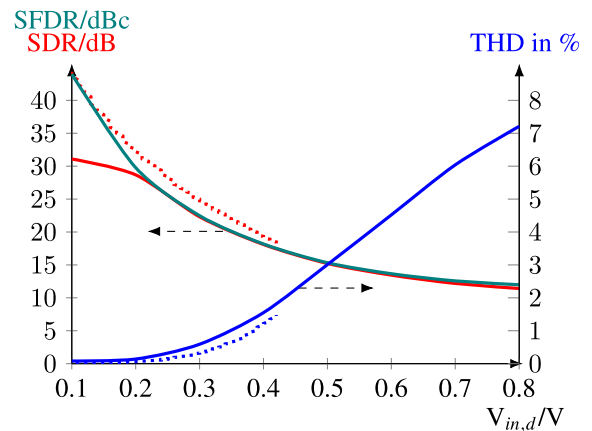
the SDR graph for higher input voltages. The excess non-linearity caused by the drivers can be evaluated comparing the results with the intrinsic non-linearity of the MZM (dotted lines).

Data transmission experiments have been carried out using a real-time scope (Keysight UXR0702A) and arbitrary signal generator (Keysight M8194A). No pre-emphasis or deembedding techniques have been applied, e.g. the degradation coming from the cables, connectors, RF-probe and PD has not been compensated in that measurement.

60Gb/s NRZ
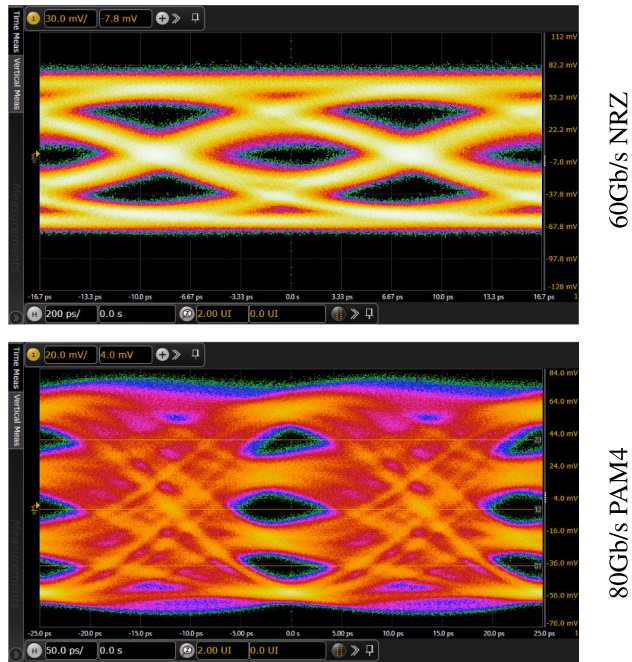
80Gb/s PAM4

FIGURE 11. Eyediagram of data transmission experiment with 60 Gb/s NRZ (up) and 80 Gb/s PAM4 (below).

We have measured bit rates of up to 60 GBit/s in NRZ scheme and 80 GBit/s with PAM4 (s. Fig. 11). Even higher bit rates could be achieved when applying pre-emphasis and post-processing. Technology updates, e.g. increasing the speed of the BJT transistors or introducing a low-loss copper back-end could easily increase the maximum achievable bit rates to more than 100 Gbit/s. This would increase the potential of monolithically integrated Si-transmitters as competitors to hybridly packaged photonic transmitters. Due to high amplification, the voltage to apply a π phase shift, which is needed to switch the MZM completely on and off, V_π is as low as 420 mV, which is a reduction by a factor of approximately 10 compared to a passive silicon MZM of same geometry [29]. The electrical power consumption of 1.77 W is higher compared to best-in-class CMOS counterpart [30]. However, a non-linear CMOS driving schemes can't provide linearity which is crucial for the application of signal pre-emphasis or even higher modulation standards than PAM4.

IV. CONCLUSION

Silicon Mach-Zehnder modulators with monolithically integrated linear drivers based on SiGe HBTs offer high performance and are a suitable candidate for high-speed communication networks. To our knowledge, our ePIC Si-MZM shows best-in-class reported bandwidth and data-rate as well as lowest external V_π due to high gain on-chip drivers (s. table 1). Linear driving scheme is more power-hungry but allows for advanced modulation techniques which is needed

to extend state-of-the-art data throughputs. Our segmented Si-MZM with linear on-chip drivers can be used in a transceiver system without an additional high voltage driver, e.g. it can be directly driven by a low voltage digital-to-analog converter.

DISCLOSURES

The authors declare no conflicts of interest.

DATA AVAILABILITY

Simulation and measurement data underlying the results presented in this paper may be obtained from the authors upon reasonable request.

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CHRISTIAN KRESS received the B.Sc. and M.Sc. degrees in electrical engineering from Paderborn University, Paderborn, Germany, in 2013 and 2017, respectively. He is currently pursuing the Ph.D. degree with the Heinz Nixdorf Institute and the Institute for Photonic Quantum Systems, Paderborn. He is also the Group Leader of the Department System and Circuit Technology, Broadband Electronic-Photonic-Integrated Circuits Subgroup. His research interests include high-frequency analog integrated circuits for broadband transmitters, receivers, and analog-to-digital and digital-to-analog converters in various photonic technologies, such as silicon BiCMOS/CMOS photonics platform or lithium-niobate-on-insulator-PICs.

TOBIAS SCHWABE received the B.S. and M.S. degrees in electrical engineering from Paderborn University, Paderborn, Germany, in 2015 and 2019, respectively. He is currently pursuing the Ph.D. degree with the Heinz Nixdorf Institute, Paderborn. His research interests include novel architectures and circuits for high-frequency broadband transmitters and receivers and sensors in silicon photonics technology.

HANJO RHEE was born in Duisburg, Germany. He received the Ph.D. degree in physics from the Institute for Optics and Atomic Physics, TU Berlin, in 2012. In 2015, he co-founded company Sicoya GmbH, which is developing silicon photonics transceiver solutions for optical communication networks. Starting in the position of the Director Photonics IC Design, he was leading the activities around the chip-level integration of photonic functionalities for applications in data center communication, mobile fronthaul networks, and switch co-packaging, and also supervising several national and EU funded research projects. In his current CTO position with Sicoya GmbH, he is pursuing the goal to establish a global player to bring silicon photonics transceiver solutions into data centers and beyond. His research interests include laser optics and nonlinear spectroscopy, involved on stimulated Raman scattering and Raman lasers in solid-state materials. As part of his research, he investigated Raman lasers in bulk silicon crystals and became deeply involved in the topic of silicon photonics.

J. CHRISTOPH SCHEYTT (Member, IEEE) received the Diploma (M.Sc.) and Ph.D. (Hons.) degrees from Ruhr-University Bochum, Germany, in 1996 and 2000, respectively. In 2000, he co-founded advICo microelectronics GmbH, a German IC design house for RFIC and fiber-optic IC design. For six years he was the CEO of advICo. From 2006 to 2012, he was with the Leibniz Institute for High-Performance Microelectronics (IHP), Frankfurt (Oder), as the Head of the Circuit Design Department. In 2012, he was appointed as a Full Professor of circuit design with the University of Paderborn, Germany, and the Research Group Leader of the Heinz Nixdorf Institute, Paderborn. Since 2016, he has been the Chairperson of the Board of Directors of the Heinz Nixdorf Institute. Since 2018, he has been the Leader of the Priority Program "Ultrafast Electronic Photonic Integrated Systems for Ultrafast Signal Processing" SPP 2111 of Deutsche Forschungsgemeinschaft. He is a co-speaker of the recently established Institute for Photonic Quantum Systems (PhoQS), Paderborn. He has authored and coauthored more than 200 refereed journal articles and conference contributions and holds more than 20 patents. His research interests include high-frequency and broadband IC design for communications and sensing, IC design with SiGe BiCMOS and CMOS technologies, silicon photonics, and photonic quantum signal processing.

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