RESEARCH ARTICLE

Inverse Model Predictive Control for Power Electronic Converters

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ABSTRACT In this paper, a new control technique called inverse model predictive control (IMPC) is proposed for power electronic converters. The proposed IMPC technique is primarily based on the inverse of the conventional finite set model predictive control. The key advantage of this design is that it avoids predicting the controlled states for all possible switching-state vectors, while maintaining the advantage of adhering to multiple constraints and achieving multiple objectives. IMPC predicts the optimal control signal that minimizes the cost function and converts it into a switching vector. Unlike classical MPC, the computational time required for IMPC is significantly reduced which makes it easily applicable to all types and levels of power electronics converters. The proposed method does not depend on the number of possible switching vectors and is compatible with low-cost microcontrollers commonly used for industrial applications. Additionally, the proposed control inherits the benefits of MPC, such as the ability to achieve its objectives while adhering to various constraints, minimal parameters tuning requirements, and reduced computational time. To demonstrate the effectiveness of the proposed technique, experimental results are presented for a five-level active neutral point clamped flying capacitor inverter (ANPC-FC) as a case study.

INDEX TERMS Inverse model predictive control, model predictive control, multi-level converters, power electronics converters control, advanced control.

NOMENCLATURE

Symbol	Description
IMPC	Inverse model predictive control.
$\mathbf{V}_{abc}$	Vector of grid voltages.
$\mathbf{I}_{abc}$	Vector of grid currents.
$\mathbf{u}_{abc}$	Vector of poles' voltages.
L_g	Input filter inductance.
R_g	Filter's internal resistance.
V_{dc}	DC side voltage.
C_l, C_2	DC side capacitors.
S_{ij}	Switching state of the tth switch in the jth leg.
S_{nj}	The normalized pole voltage of the jth leg.
I_{dc}	DC side current.
$\mathbf{I}_{a\beta}$	Vector of grid currents represented in $\alpha\beta$ frame.
$\mathbf{V}_{a\beta}$	Vector of grid voltages represented in $\alpha\beta$ frame.
$\mathbf{S}_{nabc}$	Matrix contains all possible switching states for the tree legs.
$\mathbf{S}_{abc}$	MPC-computed optimal switching vector.
g_o	Optimal cost function.
N	Number of available switching states.
$\mathbf{k}_{a\beta}$	Clarke transformation matrix.
ΔV_c	The difference between DC side capacitors' voltages.
f_s^i	The ith sub-objective function.
W_α, W_β	Weighting factors for α and β states.
$\mathbf{u}_{Oa\beta}$	IMPC optimal poles voltages vector represented in $\alpha\beta$ frame.
$\mathbf{u}_{Oab}$	IMPC optimal poles voltages vector represented in abc frame.

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$\mathbf{S}_{Oabc}$ IMPC-computed optimal switching vector.

$\mathbf{\bar{S}}_{Oabc}$ Digitalized optimal switching vector.

T_s Sampling time.

I. INTRODUCTION

Power electronics converters play a crucial role in various applications, including renewable energy systems, electric drives, electric vehicle battery charging, microgrids, and many smart grid systems [1], [2]. Consequently, the control and management challenges associated with power electronics converters have gained significant attention in both academic and industrial sectors. Power converters can be broadly classified into two main categories: two-level converters and multi-level converters (MLCs). MLCs can provide superior power quality, increased reliability, higher efficiency, and lower voltage stress on the switches [3].

To benefit the advantages offered by MLCs, advanced control algorithms must be adopted to ensure the mentioned expectations. As a result, many advanced and robust control algorithms were proposed in the literature such as disturbance observer based techniques [4], sliding mode control (SMC) [5], MPC [6], direct power control [7], Fuzzy logic control (FLC) [8], Lyapunov based control [9], linear quadratic tracker [10], and deadbeat control [11]. Among the different types of controllers, Model Predictive Control (MPC) has the potential to achieve various objectives while adhering to constraints. MPC offers several advantages, such as requiring fewer tuned parameters, not requiring pulse width modulation (PWM) stage [12]. Unfortunately, MPC tends to have the highest computational load for MLCs compared to other controllers.

The high computational load associated with MPC in the case of MLCs arises from its reliance on predicting the behavior of controlled states across all possible switching state combinations. For instance, in a three-phase N-level converter, there are N^3 potential combinations, resulting in 125 combinations for a five-level converter. Each of these combinations needs to be evaluated individually during every control cycle to determine the optimal combination that minimizes a specific cost function (g). This implies that at each cycle, 125 predictions of currents and corresponding cost function calculations are required.

In practical industrial settings, implementing MPC experimentally for high-level converters using low-cost microcontrollers becomes impossible. To solve this problem, multiple researchers proposed reduced-complexity MPC schemes. In [13], an iterative method is proposed to reduce the computation load, where only three-combinations are examined at each cycle. However, this method does not guarantee that one of the three examined combinations is optimal among all possibilities. Another research proposed a method to reduce the required calculations from N^3 to $3N$ by substituting the switching states directly in the mathematical model [14], [15]. Although this method significantly reduces the computational load, $3N$ predictions and cost function computations

are still required in each cycle. Paper [16] expressed the cost function in terms of the reference poles' and measured poles' voltages instead of the controlled states. This eliminated the need for computing the reference poles' voltages at each cycle. Although computational time can be reduced 50%, N^3 of current predictions are still required at each control cycle. A simplified virtual-vector-based model predictive control technique was proposed in [17]. In this approach, the control-factor technique was used to automatically generate many virtual vectors, then the candidate vectors could be directly identified. Although this method can significantly reduce the computational time, a large size of memory and significant computations are still required to generate these virtual vectors. Similarly, [18] proposed a method to generate 89% additional virtual vectors to eliminate the neutral point voltage balance term from the cost function. Although this method significantly reduces the prediction time, still a huge number of virtual vectors should be generated, and many iterations are required to select the optimal switching vector.

In [19], the computational time of the MPC was reduced using an additional algorithm for selecting and examining different subsets of switching vectors. However, additional algorithm is needed for selection optimization which increases the complexity of the control system. Successive searching algorithms were also employed to reduce the time of selecting the optimal switching vectors [20]. This method depends on eliminating the repeated vectors and then adjusting the direction of searching to determine the optimal switching vector. However, not all repeated vectors can be eliminated as some of the vectors are employed for sub-objectives such as capacitor voltage balancing. Moreover, this technique requires additional algorithms for eliminating the repeated vectors and to control the direction of the search. Another approach to minimize the computational time of the MPC is to avoid using the cost functions [21]. Avoiding the cost functions reduces the time required to examine all available switching vectors. However, this approach limits the flexibility and the ability of the MPC to achieve multiple objectives and adhering to multiple constraints. For example, in [21], additional sorting-based strategy was employed to achieve capacitors voltage balancing, as the proposed method alone is insufficient to achieve all control objectives.

Avoiding the examination of all feasible virtual and redundant vectors (*R:* all switching vectors that generate the redundant pole's voltages) is a common method used for reducing the number of possible combinations from N^3 to N^3-R [22]. However, too many unique possibilities still exist and must be examined continuously. A fast MPC (FMPC) for multi-level T-type converter was proposed in [23] based on the predefined selection of the switching states. This method succeeded to reduce the computation load about 80% without affecting the response of the controlled converter. However, this methodology is not feasible for high-level converters. In the case of seven-level converter, there are 343 possibilities. Even if the number of possibilities is reduced by 80%, 68 possibilities are still required to be examined at

each control cycle which is still very high. The situation gets much worse for multiphase systems (those with more than three phases). Hence, the need for further improvements that respond to the high computational time are required especially for multi-level and multi-phase systems.

In this paper, a new control technique called IMPC which requires low computational power is proposed for power electronics converters. The proposed method requires very low computational load, irrespective of converter type, the number of phases, and the number of levels. Unlike traditional MPC approaches, the IMPC technique does not require the prediction of the controlled states and their impact on the cost function. Instead, the algorithm begins by calculating the optimal value of the cost function and then works backward to compute the required currents that yield this optimal cost function. This is achieved using a discretized mathematical model. Next, the reference poles' voltages are determined based on the required currents, discretized, and then converted into an optimal switching vector. By eliminating the need for state prediction and focusing on computing optimal values, the proposed IMPC technique offers a significant reduction in computational complexity while maintaining effective control over the converter system. To verify the proposed technique on multilevel converter, five-level active neutral point clamped flying capacitor (ANPC) inverter is selected as a case study.

The contributions of this paper can be summarized as follows,

1. A new control technique called inverse model predictive control (IMPC) is proposed for power electronic converters.
2. Proving that the proposed IMPC offers a minimized computational burden regardless the number of converter's levels.
3. Demonstrating that the proposed IMPC is applicable for bidirectional converters and suitable for controlling the direction of power flow.

The rest of the paper is organized as follows; a brief description of the ANPC-FC converter's mathematical model is presented in section II. The design of the proposed IMPC is discussed in section III. Experimental results for five-level three phase ANPC-FC inverter as a case study and comparison studies, are shown in section IV. Then, the paper is concluded in section V.

II. MATHEMATICAL MODEL OF ANPC-FC

For the purpose of this study, the 5-level ANPC-FC inverter is chosen because it exhibits a high number of switching states, making it suitable for evaluating the performance and effectiveness of the proposed control technique. The circuit diagram of this converter is shown in Fig. 1. The converter consists of three legs, each leg is connected to the grid through an L-filter that has an inductance (L_g) and an internal resistance (R_g). For simplicity, it is assumed that inductors and resistors are identical. The legs on the DC side are connected in parallel to the load. The neutral points of these legs are

then connected to the DC link through two capacitors. Each leg comprises eight power switches and a flying capacitor. This configuration allows for efficient power conversion and control in the respective inverter topologies.

In general, all three-phase inverter topologies have the same mathematical model, where the grid and poles' voltages represent the inputs, and the grid currents represent the controlled variables. However, each topology has its own finite set of possible poles' voltages. The possible finite set is resulting from the possible switching states which determine the number of supported levels of each converter. In general, the AC dynamics of the converter can be described as follows [24],

$$\mathbf{u}_{abc} = L_g \frac{d\mathbf{I}_{abc}}{dt} + R_g \mathbf{I}_{abc} + \mathbf{V}_{abc} \qquad (1)$$

where $\mathbf{V}_{abc} = \begin{bmatrix} V_a & V_b & V_c \end{bmatrix}^T$ is the vector of grid voltages, L_g and R_g are the inductance and the internal resistance of the input filter, $\mathbf{I}_{abc} = \begin{bmatrix} I_a & I_b & I_c \end{bmatrix}^T$ is the vector of grid currents, and $\mathbf{u}_{abc} = \begin{bmatrix} u_a & u_b & u_c \end{bmatrix}^T$ is the vector of poles' voltages.

For simplicity, (1) can be transformed into the $\alpha\beta$ frame which reduces the number of controlled states to two as follows,

$$u_\alpha = R_g I_\alpha + L_g \frac{dI_\alpha}{dt} + V_\alpha \qquad (2)$$

$$u_\beta = R_g I_\beta + L_g \frac{dI_\beta}{dt} + V_\beta \qquad (3)$$

This model can then be discretized using Newton-Euler approximation as follows [4],

$$I_\alpha(k+1) = \left(1 - \frac{R_g T_s}{L_g}\right) I_\alpha(k) + \frac{T_s}{L_g}(u_\alpha - V_\alpha) \qquad (4)$$

$$I_\beta(k+1) = \left(1 - \frac{R_g T_s}{L_g}\right) I_\beta(k) + \frac{T_s}{L_g}(u_\beta - V_\beta) \qquad (5)$$

where T_s is the sampling time.

In fact, the poles' voltages have a finite set of values. For the ANPC-FC, there are five-possibilities for each leg, namely positive (P), mid-positive (p), zero (0), mid-negative (n), and negative (N). These possibilities are generated based on the possible switching states shown in Table 1, and the possible combinations are shown in Fig. 2. The symbols S_{1j}, S_{2j}, and S_{3j} represent the switches gates, u_j is the pole's voltage of the jth leg, and S_{nj} is the normalized pole voltage which represents the ratio between the jth leg's pole voltage and the DC link voltage.

The selection of the optimal state is done based on optimizing the primary and secondary objectives including grid current regulation as the primary objective and DC side capacitors voltage balancing as a secondary objective. Moreover, multiple primary and secondary objectives can be included such as input and output constraints

III. THE PROPOSED IMPC

To better understand the proposed IMPC technique, it is helpful to first introduce the conventional MPC algorithm and

Symbol	S_{1j}	S_{3j}	T_{1j}	T_{3j}	u_j	S_{nj}
P	1	1	1	1	V_{dc}	1
p	1	1	1	0	$V_{dc}/2$	0.5
p	1	1	0	1	$V_{dc}/2$	0.5
Z	1	1	0	0	0	0
Z	0	0	1	1	0	0
n	0	0	1	0	$-V_{dc}/2$	-0.5
n	0	0	0	1	$-V_{dc}/2$	-0.5
N	0	0	0	0	$-V_{dc}$	-1
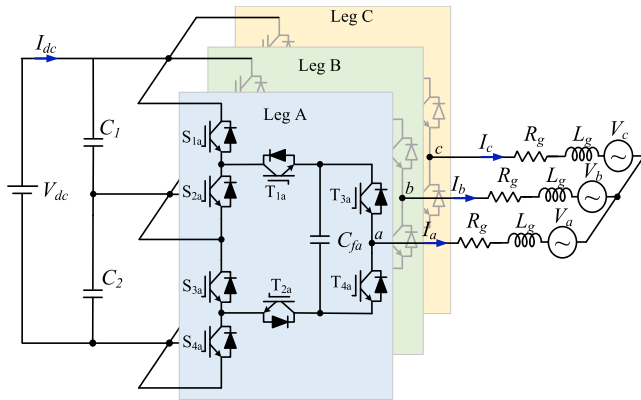
FIGURE 1. Circuit diagrams of the three-phase ANPC-FC converter.

then highlight the approach employed to design IMPC. The conventional MPC algorithm follows a specific sequence of steps to control a system. It begins with predicting the future behavior of the controlled variables using the mathematical model of the system. These predictions are based on a range of possible control inputs, also known as switching-state vectors.

The algorithm then selects the optimal switching state that minimizes a predefined cost function. This process involves solving an optimization problem, often through numerical techniques. In contrast, the IMPC technique takes an inverse approach. Instead of predicting the controlled states and finding the optimal switching state vector, IMPC starts by determining the desired value of the cost function.

It then works backward by calculating the corresponding required currents that would produce this optimal cost function using a discretized mathematical model. The reference poles' voltages are computed based on these required currents, discretized, and converted into an optimal switching vector.

By inverting the MPC algorithm, IMPC avoids the computational burden of predicting the controlled states for all possible switching-state vectors. This makes IMPC computationally efficient, regardless of the converter type, number of phases, and number of levels involved. The understanding of the conventional MPC algorithm sets the foundation for understanding the novel approach presented by IMPC, therefore it is explained next.

A. DESIGN OF THE MPC

For ANPC-FC inverter, there are 125 possible combinations. Assuming that the number of possible combinations is N, then the MPC can be summarized as shown in Algorithm 1. where W_i represents the weighting factors, $\mathbf{S}_{nabc}$ and *states* are the matrices that contain all possible S_{nj} combinations and the corresponding switching states respectively, $\mathbf{S}_{abc}$ is the output vector and containing the optimal states of the power switches, $\mathbf{k}_{\alpha\beta}$ is the Clarke transformation matrix, g_o is the optimal cost function(minimum), i_o is the index of $\mathbf{S}_{abc}$ that produces g_o, $\mathbf{I}^i_{\alpha\beta}(k+1)$ is the predicted currents vector resulting from applying $\mathbf{S}_{nabc}(i)$, **and** Δv_c is the difference between capacitors' voltages.

Algorithm 1 Conventional MPC Algorithm

input : $\mathbf{I}_{\alpha\beta}(k)$, $\mathbf{I}^*_{\alpha\beta}(k+1)$, $\mathbf{V}_{\alpha\beta}(k)$, V_{dc}, $\mathbf{S}_{nabc}$
output: $\mathbf{S}_{abc}$
$g_o = \infty$ % initialize the optimal cost function
$i_o = \infty$ % initialize the index of optimal state
for $i = 1:N^3$
  % Compute the control signal
$$\mathbf{u}_{abc}(i) = V_{dc}\mathbf{S}_{nabc}(i) \quad (6)$$
  % Convert the control signal into $\alpha\beta$
$$\mathbf{u}_{\alpha\beta}(i) = \mathbf{k}_{\alpha\beta}\mathbf{u}_{abc}(i) \quad (7)$$
  % Predict the value of the current at k+1
$$\mathbf{I}^i_{\alpha\beta}(k+1) = \left(1 - \frac{R_g T_s}{L_g}\right)\mathbf{I}_{\alpha\beta}(k) + \frac{T_s}{L_g}\left(\mathbf{u}_{\alpha\beta}(i) - \mathbf{V}_{\alpha\beta}\right) \quad (8)$$
  % Compute the value of cost function
$$g = W_\alpha \left|I^*_\alpha(k+1) - I^i_\alpha(k+1)\right| + \ldots$$
$$W_\beta \left|I^*_\beta(k+1) - I^i_\beta(k+1)\right| + W_c\left|\Delta V\right|_c \quad (9)$$
  % Compare the obtained cost with the optimal one
  if $g < g_o$ **then**
    $g_o = g$
    $i_o = i$
  end
end
$\mathbf{S}_{abc} = states(i_o)$

B. DESIGN OF THE IMPC

To get rid out of the N^3 loop, it is worth starting from (9) with the assumption that the desired optimal value of the cost function approaches zero (i.e. $g \approx 0$). This assumption is considered practical for two reasons, *i*) many studies show that the current tracking error and voltage balancing error are achievable with steady state error approaches zero, (2) to have $g \approx 0$ is the main control objective for any controller. Assuming a general cost function,

$$g = \left|I^*_\alpha(k+1) - I^i_\alpha(k+1)\right| + \beta\left|I^*_\beta(k+1) - I^i_\beta(k+1)\right| \quad (10)$$
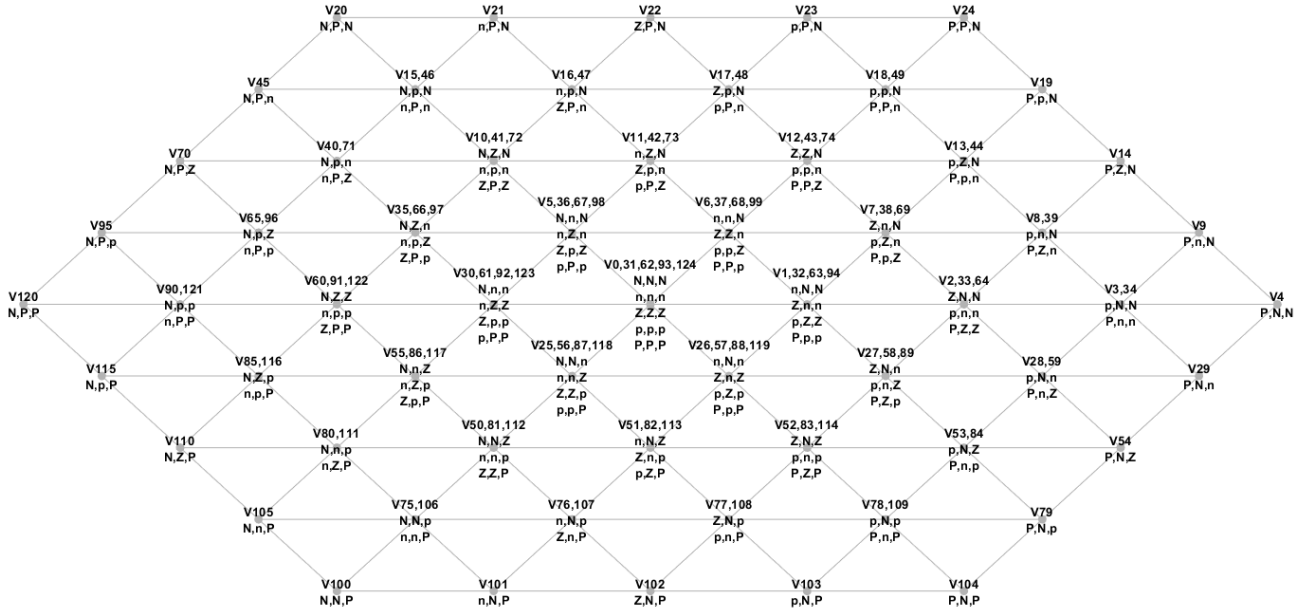
FIGURE 2. Vector diagram for ANPC-FC converter.

The value of the most optimal cost function approaches zero, so,

$$0 \approx \left| I_\alpha^* (k+1) - I_\alpha^i (k+1) \right| + \left| I_\beta^* (k+1) - I_\beta^i (k+1) \right| \tag{11}$$

this case occurs if and only if,

$$I_\alpha^* (k+1) \approx I_\alpha^i (k+1) \tag{12}$$

$$I_\beta^* (k+1) \approx I_\beta^i (k+1) \tag{13}$$

If there are additional objectives or constraints $(f_s^1 \ldots f_s^O)$, they can be distributed on (12) and (13) by the mean of weighting factors $(W_{\alpha 1}, W_{\alpha O}, W_{\beta 1}, W_{\beta O})$ as follows,

$$I_\alpha^* (k+1) \approx I_\alpha^i (k+1) + W_{\alpha 1}f_s^1 + \ldots + W_{\alpha O}f_s^O$$
$$I_\beta^* (k+1) \approx I_\beta^i (k+1) + W_{\beta 1}f_s^1 + \ldots + W_{\beta O}f_s^O \tag{14}$$

where f_s^1 and f_s^O are the first and the Oth sub-objective of the control technique, which may include DC side capacitors' voltage balancing, additional input constraints, and additional output constraints, $W_{\alpha 1}$ and $W_{\alpha O}$ are the first and Oth weighting factors for the α-terms objectives, and $W_{\beta 1}$ and $W_{\beta O}$ are the first and Oth weighting factors for the β-terms objectives. If there are any other sub-objectives, they can be added to the cost function and distributed among α and β axes by the mean of weighting factors. One systematic method to select these factors is the equal-weighted cost function tuning method [25].

Assuming that this controller has two generalized sub-objectives f_s^1 and f_s^2, the equilibrium conditions described in (12) and (13) can now be updated as follows,

$$I_\alpha^* (k+1) \approx I_\alpha^i (k+1) + W_{\alpha 1}f_s^1 + W_{\alpha 2}f_s^2 \tag{15}$$

$$I_\beta^* (k+1) \approx I_\beta^i (k+1) + W_{\beta 1}f_s^1 + W_{\beta 2}f_s^2 \tag{16}$$

Substituting these constraints in (8), leads to compute the required optimal poles' voltages $(\mathbf{u}_{O\alpha\beta})$ required to achieve the desired optimal g,

$$\mathbf{u}_{O\alpha\beta} = \underbrace{\frac{L_g}{T_s}\mathbf{I}_{\alpha\beta}^* (k+1) - \left(\frac{L_g}{T_s} - R_g\right)\mathbf{I}_{\alpha\beta}(k) + \mathbf{V}_{\alpha\beta}}_{\text{primary objective}} \ldots$$
$$+ \underbrace{\frac{L_g}{T_s}\begin{bmatrix} W_{\alpha 1}f_s^1 + W_{\alpha 2}f_s^2 \\ W_{\beta 1}f_s^1 + W_{\beta 2}f_s^2 \end{bmatrix}}_{\text{secondary objectives}} \tag{17}$$

Although the primary objectives side of (17) bears resemblance to conventional deadbeat control as proposed in [26], it's crucial to note the distinctions:

i) Deadbeat control functions by directing the primary objective term straight to a modulation mechanism for PWM generation. Consequently, deadbeat control lacks the capacity to ensure optimality, as seen in conventional Model Predictive Control (MPC) or the proposed Iterative Model Predictive Control (IMPC).

ii) Deadbeat controllers solely focus on primary control objectives, such as current regulation, neglecting secondary objectives. This necessitates the integration of additional controllers, like Proportional-Integral (PI) controllers, in cascade with deadbeat controllers to fulfill secondary objectives.

iii) Unlike IMPC, deadbeat controllers require PWM generation. Moreover, deadbeat controllers presume that the computed pole voltages are always feasible and achievable through PWM.

However, the optimal pole voltages computed may not always be feasible for execution with the selected converter. This issue is addressed in the proposed IMPC by converting the computed reference pole voltages into the nearest feasible switching state. Consequently, substituting equation (17) into equation (7) leads to the computation of optimal pole voltages in the *abc* frame ($\mathbf{u}_{Oabc}$),

$$\mathbf{u}_{Oabc} = \mathbf{k}_{\alpha\beta}^{-1}\mathbf{u}_{O\alpha\beta} \qquad (18)$$

After that, $\mathbf{u}_{Oabc}$ can be converted into the corresponding optimal and normalized poles' state by inserting (18) in (6),

$$\mathbf{S}_{Oabc} = \mathbf{u}_{Oabc}/V_{dc} \qquad (19)$$

However, as $g=0$ is not guaranteed to be possible, $\mathbf{S}_{Oabc}$ may not be available in the possible normalized poles voltages vectors. Therefore, a digitalization process is required to compute $\bar{\mathbf{S}}_{Oabc}$ which is the closest available S_{nj},

$$\bar{\mathbf{S}}_{Oabc} = \min |S_n| \times round\left(\frac{\mathbf{S}_{Oabc}}{\min |S_n|}\right) \qquad (20)$$

In fact, (20) guarantees that $\bar{\mathbf{S}}_{Oabc}$ is always available, belongs to $\mathbf{S}_n$, and represents the closest poles' voltages vector to the $\mathbf{S}_{Oabc}$.

To obtain the digital state of each switch, a simple *if-else* function can be written depending on the topology, for ANPC-FC it can be obtained by Algorithm 2 as follows,

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Algorithm 2 $\bar{S}_{Oj}$ to S_j Conversion for ANPC-FC Converter

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input : $\bar{S}_{Oj}$
output : $\mathbf{S}_j = [S_{1j}, S_{3j}, T_{1j}, T_{2j}], j \in [a\ b\ c]$
if $\bar{S}_{Oj} =1$ **then**
$\quad | \quad S_{1j} = 1, S_{3j} = 1, T_{1j} = 1, T_{3j} = 1$
else if $\bar{S}_{Oj} =0.5$ **then**
$\quad | \quad S_{1j} = 1, S_{3j} = 1, T_{1j} = 1, T_{3j} = 0$
else if $\bar{S}_{Oj} = 0$ **then**
$\quad | \quad S_{1j} = 1, S_{3j} = 1, T_{1j} = 0, T_{3j} = 0$
else if $\bar{S}_{Oj} = -0.5$ **then**
$\quad | \quad S_{1j} = 0, S_{3j} = 0, T_{1j} = 1, T_{3j} = 0$
else
$\quad | \quad S_{1j} = 0, S_{3j} = 0, T_{1j} = 0, T_{3j} = 0$
end

It is worth noting that the ANPC-FC converter has a special case additional objective which is balancing the flying capacitors (C_{fa}, C_{fb}, and C_{fc}) voltages. The balancing process is done using the redundant states [p, p, n, n] shown in Table 1. Therefore, if $\bar{S}_{Oj}$ equals 0.5, one of the positive redundant states can be used to charge or discharge the flying capacitor. If the voltage of C_{fa} is higher than the others, it should be discharged, therefore the state [1 1 0 1] should be selected, while [1 1 1 0] should be selected to charge the flying capacitor

if it is lower than the others. Similar procedures can be followed to select one of the negative redundant switching states (i.e. if $\bar{S}_{Oj} = -0.5$).

The block diagram of the proposed controller is shown in Fig. 3. The PLL function is used to estimate the phase angle which is then used to generate the reference signal based on the reference DC link voltage or the reference power. The generated current reference signal is then applied to the IMPC along with DC link voltage and $\alpha\beta$-represented grid currents and voltages. The IMPC utilizes these measurements and compute the optimal switching signals and applies them to the switches.
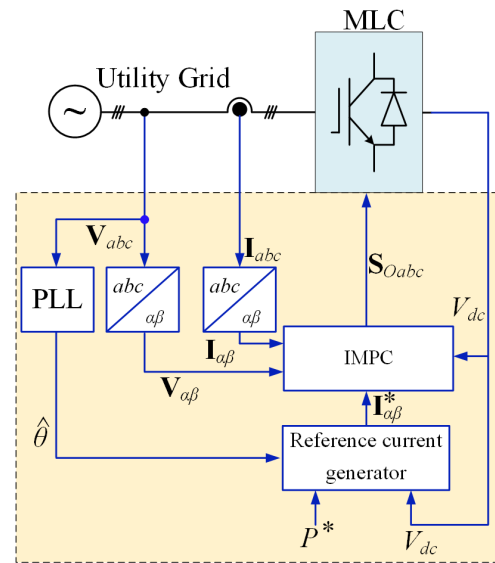

FIGURE 3. (a) Control algorithm flow chart. (b) Block diagram of IMPC.

IV. EXPERIMENTAL RESULTS

Case Study 1: Inverter Operation: To validate the effectiveness of the proposed IMPC technique and demonstrate its feasibility, the approach is implemented experimentally to control a three-phase five-level ANPC-FC inverter. The experimental setup is shown in Fig. 4. The setup consists of grid emulator, L-input filter, ANPC-FC converter, oscilloscope, low voltage DC supply, three-phase protection unit, STM32H745 microcontroller, and battery emulator (Chroma 6200D). The parameters of the system, which are essential for capturing the characteristics of the system, are listed in Table 2.

A. EXPERIMENTAL STEADY STATE AND DYNAMIC RESPONSE ANALYSIS OF IMPC

The IMPC offers an excellent response during both steady state and transient periods as shown in Figs. 5 and 6 respectively. It can be noticed that the grid current is able to track the reference current accurately, rapidly, and smoothly. The grid currents are sinusoidal, with no high frequency

TABLE 2. System's parameters.

Symbol	Value	Unit
$\mathbf{V}_{abc}$	110	V$_{rms}$
R_g	50	mΩ
I^*	5-10	A
L_g	5	mH
$C_{1,2}$	470	μF
V_{dc}	400	V
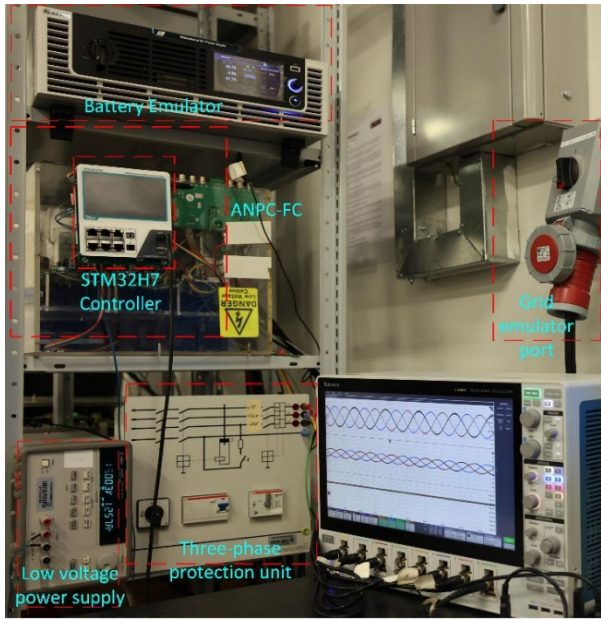
FIGURE 4. Experimental setup.

FIGURE 5. IMPC steady state response analysis (a) Grid voltage, grid current, and V$_{ab}$ pole voltage. (b) Grid currents THD analysis.

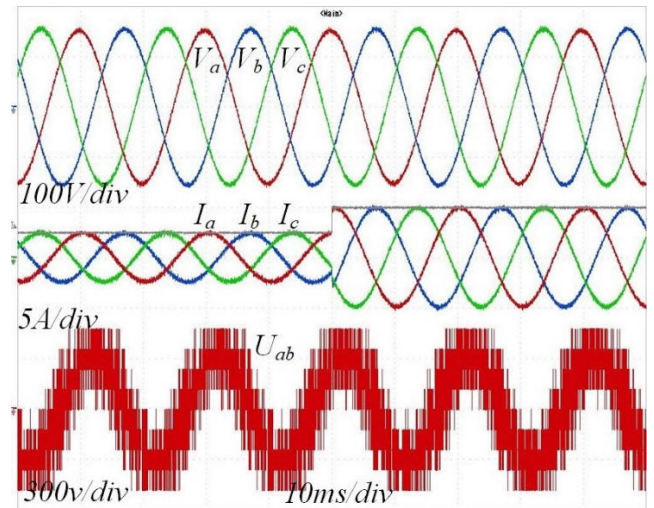**FIGURE 6.** IMPC dynamic response analysis.

noises, and in phase with the grid voltages which insures a unity power factor. Moreover, the overshot in the current at transient is zero. It can be noticed that the current harmonic level is 0.8% which is considerably lower than the standards' limits. These experiments prove that IMPC offers the same response of the conventional MPC, and its ability to provide the optimal switching vector.

B. EXPERIMENTAL RESPONSE ANALYSIS OF IMPC UNDER ABNORMAL GRID CONDITIONS

One of the most challenging problems facing the grid-connected inverters is the unbalanced grid voltages. To show the response of the MPC under such conditions, 10% of unbalanced grid voltages were applied and the response is shown in Fig. 7. It can be noticed that the grid currents are completely balanced, sinusoidal, and almost are not affected by the unbalanced voltages. Grid voltage sag and swell represent another common challenge in practical applications. Grid voltage sag is a short-term decrease in the RMS voltage magnitude that is typically brought on by a power system fault. A rise in the RMS voltage over the nominal voltage or a sliding reference voltage is referred to as a voltage swell. The increment can last anywhere from a cycle to a few seconds.

Voltage increases when heavy loads are turned off, or capacitor banks are powered up. The IMPC shows an impressive response against these cases comparing with the MPC as shown in Figs. 8 and 9 for voltage sag and swell respectively. In both cases, the grid voltage is reduced/ increased from
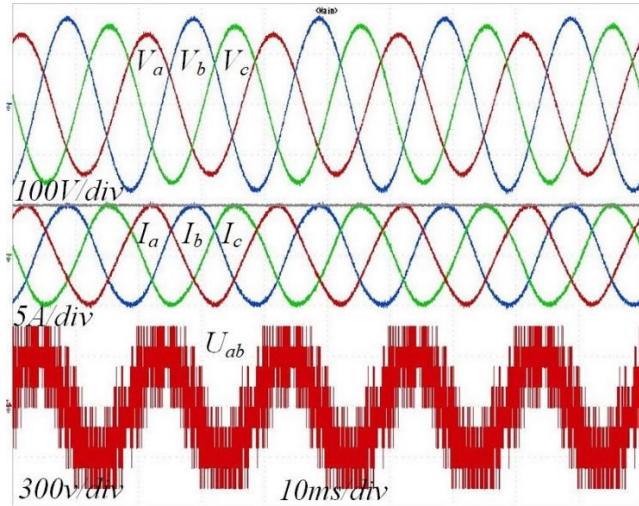
FIGURE 7. IMPC response for unbalanced grid voltages using ANPC-FC inverter.

0.9 p.u. to 1.1 p.u. However, the currents are almost not affected, the tracking error remains zero, no overshoot or transients appear, the power the power factor is kept unity, and the current is still sinusoidal.
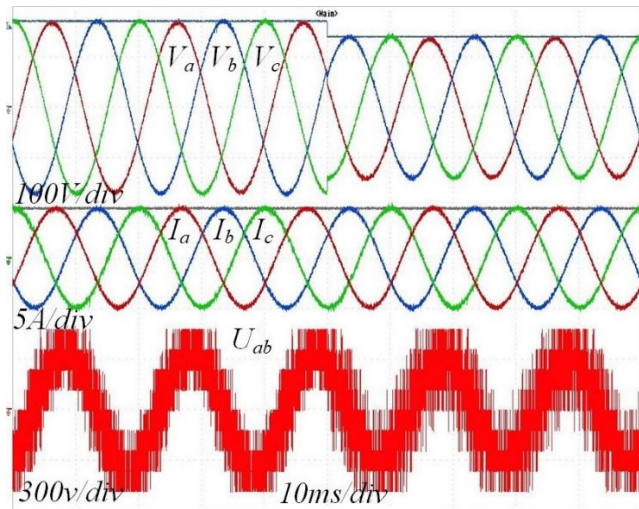

FIGURE 8. IMPC response for grid voltage sag.

Then, a 10% 5th order and 10% 7th order harmonic components are added to the grid voltages. The added harmonic components make the grid voltages highly distorted as shown in Fig. 10. Moreover, the current reference is stepped up from 5A to 10. The IMPC shows a unique ability to handle such conditions, where the grid currents diverge to the reference value accurately, rapidly, with no overshoot, and with no ripples or oscillations. Although the THD of the grid voltages is severe (14.14%), the grid currents are well-regulated, sinusoidal, in phase with the grid voltages, and have a THD less than 1%.
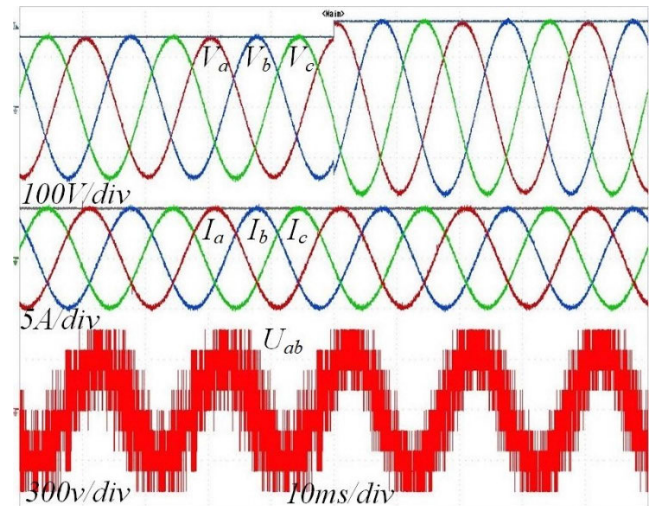

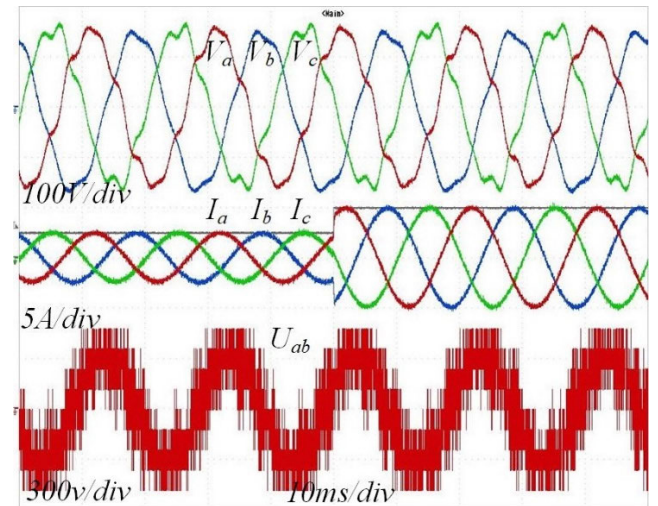**FIGURE 9.** IMPC response for grid voltage swell.

FIGURE 10. IMPC response for distorted grid voltages.

To increase the level of the challenge, all possible abnormal conditions are merged together in one test as shown in Fig. 11 to demonstrate the response of the IMPC in the worst-case scenario. In this experiment, the grid voltages are highly distorted with a 10% 5th order and 10% 7th order harmonic components, 10% unbalance, and 10% voltage swell occurring during the operation. However, the IMPC shows an impressive response and overcome all these challenges. The currents are well-regulated with zero tracking error, unity power factor, sinusoidal, no overshoot or transient due to voltage swell, the THD of the current is less than the international limits (<5% for low voltage applications) [27], and the currents are balanced. Finally, the converter is tested for operation as both inverter and rectifier. Fig. 12 shows the response of the IMPC controlling a hybrid ANPC-FC converter. The ANPC-FC starts working as an inverter, which injects the power from a battery to the grid. Then, the
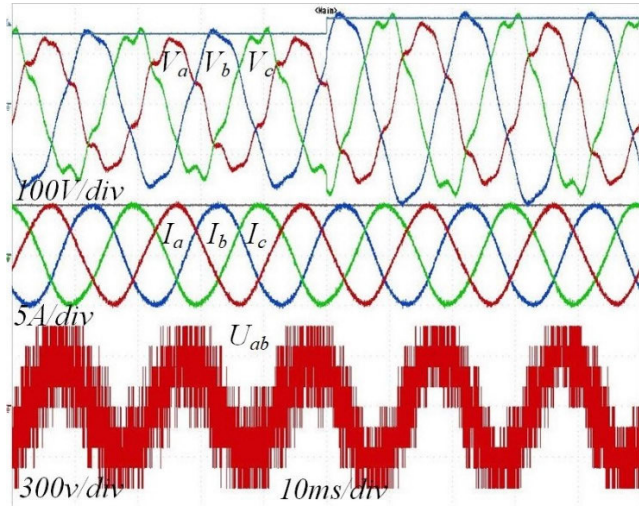
FIGURE 11. IMPC response during the worst-case scenario.

direction of the reference current is changed while maintaining the same amplitude. Therefore, the operation of the ANPC-FC is switched from inverter to active front end rectifier (AFR). The transformation process is done rapidly and accurately with no oscillation or overshot, and the power factor is kept unity for both inverter and AFR operations.
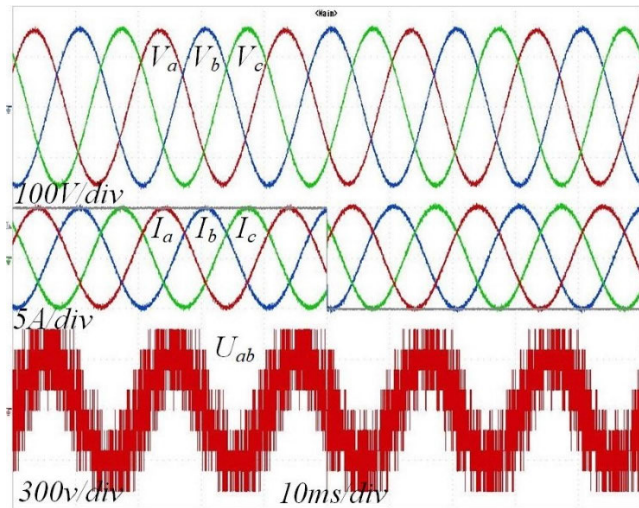

FIGURE 12. IMPC response for bi-directional ANPC-FC converter.

C. EXPERIMENTAL STEADY STATE AND DYNAMIC RESPONSE ANALYSIS OF MPC

Under normal grid conditions, the MPC controller provides excellent steady state and dynamic response as shown in Figs. 13 and 14 respectively. The grid currents are sinusoidal, have no high frequency noise, and in phase with the grid voltages which insures a unity power factor (PF). The THD is 0.7% which less than the limits defined by the standards [28]. The reference current is then stepped-up from 5 to 10A. It can be noticed that the grid currents are tracking the reference

signal rapidly, accurately, and with no overshot or oscillation. It can be noticed from this comparison that IMPC can provide the same optimal response as MPC in both steady state and dynamic response. This confirms the optimality and ability of the proposed controller to achieve the control objectives.
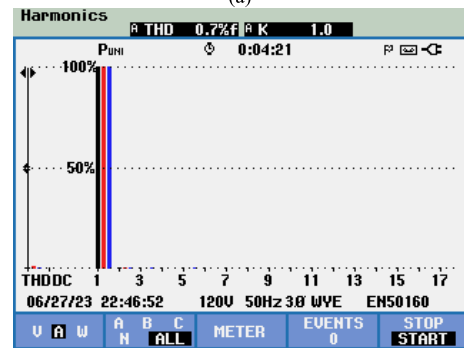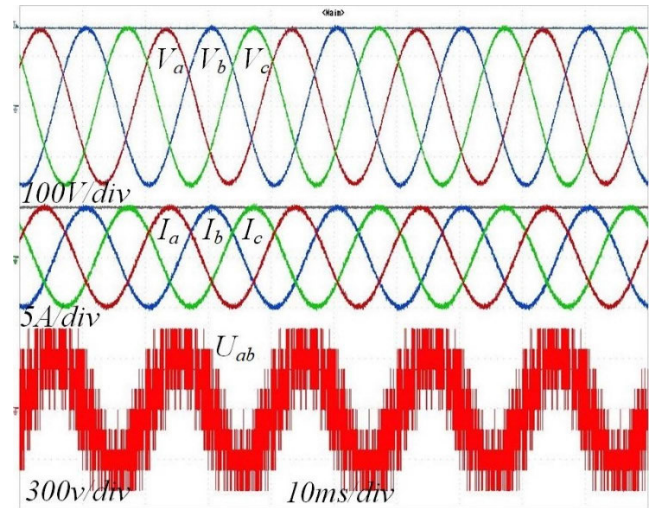

FIGURE 13. MPC steady state response analysis (a) Grid voltage, grid current, and V_{ab} pole voltage. (b) Grid currents THD analysis.

Case Study 2: Rectifier Operation: The control process of multi-level active front-end rectifiers (AFRs) contains three main objectives grid current regulation, DC link voltage regulation, and DC side capacitors balancing, these objectives can be summarized as follows,

$$minimize \left(\Delta \mathbf{I}_{\alpha\beta} = \left|\mathbf{I}_{\alpha\beta}^* - \mathbf{I}_{\alpha\beta}\right|\right) \quad (21)$$

$$minimize \left(\Delta V_{dc} = V_{dc}^* - V_{dc}\right) \quad (22)$$

$$minimize \left(\Delta V_c = V_{c1} - V_{c2}\right) \quad (23)$$

Substituting these objectives into (17), the optimal poles' voltages can be computed as follows,

$$\mathbf{u}_{O\alpha\beta} = \frac{L_g}{T_s} \begin{bmatrix} W_{\alpha 1}\Delta V_{dc} + W_{\alpha 2}\Delta V_c \\ W_{\beta 1}\Delta V_{dc} + W_{\beta 2}\Delta V_c \end{bmatrix} + \cdots \frac{L_g}{T_s}\mathbf{I}_{\alpha\beta}^*(k+1)$$
$$- \left(\frac{L_g}{T_s} - R_g\right)\mathbf{I}_{\alpha\beta}(k) + \mathbf{V}_{\alpha\beta} \quad (24)$$

(24) shows how multiple objectives can be integrated with the optimized poles' voltages computation using one single
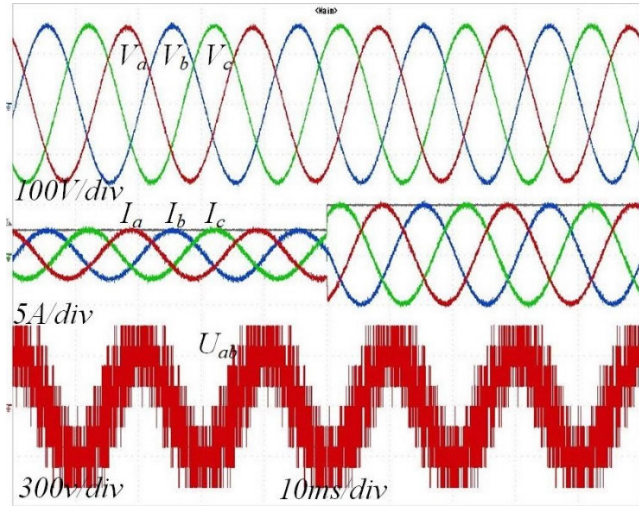
FIGURE 14. MPC dynamic response analysis.

loop controller instead of using multiple cascaded controllers. Similar to the inverter case, the optimal value of the poles' voltages can be then converted to the *abc* frame, normalized, and digitized as shown in (18)-(20).

The response of the controller is demonstrated in Fig. 15 and 16 to show the ability of the IMPC to achieve all objectives accurately. The reference DC link voltage is set to 400V, and its desired to minimize the voltage reference between the DC side capacitors while regulating the AC side currents to be sinusoidal, in phase with grid voltage, and contains minimized THD. It can be seen that the grid currents are sinusoidal, but there is a 180º phase shift between currents and voltages which means that the current flows from the grid to the load. The THD is much lower than the international limits, the DC link voltage is well regulated with no oscillations or ripples, the voltage of the DC side capacitors are balanced, and the transition of the DC link voltage is smooth with almost no overshoot. This experiment proves the ability of the proposed IMPC to efficiently fulfill multiple objectives within a single loop controller.
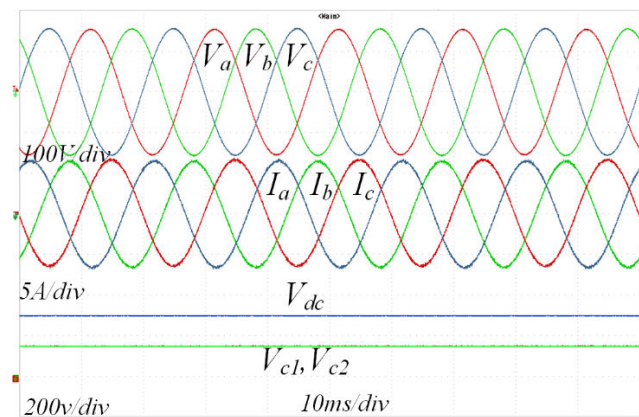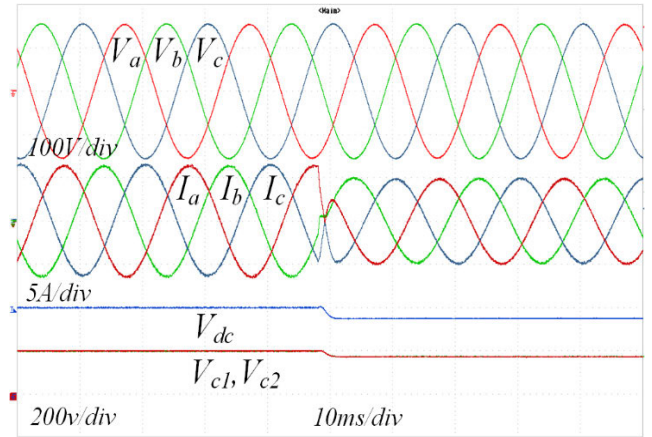

FIGURE 16. IMPC dynamic response for rectifier operation.

Fig. 17 shows the transient tracking response of the current and the voltage balancing of the DC side capacitors. It can be noticed that the IMPC achieved almost the exact response in terms of accuracy, speed, balancing, and stability of the DC link voltage.

Based on the results obtained from the previous case studies, both MPC and IMPC provided excellent response. Both show excellent response during normal steady state and dynamic response, generated balanced grid currents when the grid voltage is 10% unbalanced, offered robust response against 10% voltage and swell, and both showed impressive response against highly distorted grid voltage. Moreover, both are compatible with smooth control of bi-directional power flow. In conclusion, the proposed IMPC can achieve an optimal response like the conventional MPC while significantly minimizing the computational load.

Case Study 3: Experimental-Based Computational Load Comparison: To show the advantages of the proposed IMPC in terms of computational load, the classical MPC, FMPS [23], and IMPC (proposed) are implemented on STM32H745 microcontroller to capture the required com-
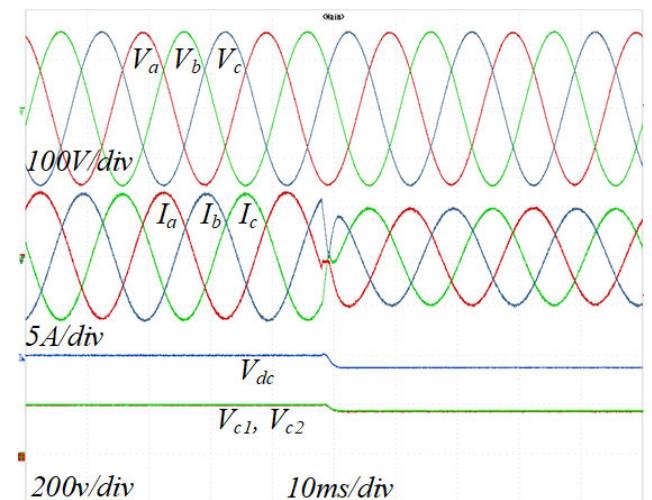

FIGURE 15. IMPC steady state response for rectifier operation.

FIGURE 17. MPC dynamic response for rectifier operation.

putational time for controlling the most common multi-level topologies.

As this experiment aims solely to compute the processing time for classical MPC, FMPS [23], and IMPC, only the control loops were implemented with constant states measurements without using physical multi-level converters.

The results obtained from this comparison are shown in Table 3 for three, five, seven, and nine-level converters.

These results are obtained by taking the average time of 1000 control-cycles for each case without taking into consideration the measurements acquisition time. For three-level converter, all methods can be implemented on a low-cost microcontroller, but the sampling time of the MPC must be set to at least 88 μs, which is considered high for such applications. The FMPC requires 22 μs which is considered suitable and does not affect the stability of the controller. However, the proposed controller requires 5 μs which is considered excellent computational time for industry applications.

For five-level converter, the computational time is severely increased for both MPC and FMPC. In this case, the stability of the MPC becomes arguable as the sampling time must be at least 400 μs. Although the FMPC is much better than the MPC, 100 μs is considered high but still applicable on low-cost controllers. On the other hand, the computational time of the IMPC is not affected when the levels are increased, however, a small variation may be detected.

When a 7-level converter is used, the MPC requires 1060 μss to compute the optimal states, which would deteriorate the response of the control system and would cause instability issues. The FMPC computational load is almost tripled, and the stability of the system becomes arguable. However, the computational time is still almost constant for the IMPC.

TABLE 3. Computational load comparison.

Control method	MPC	FMPC	IMPC
	Time (μs)		
Three-level	87.891	21.973	4.883
Five-level	399.536	99.884	5.981
Seven-level	1059.57	264.893	5.493
Nine-level	2307.665	576.916	5.991

Finally, for a nine-level converter, the MPC is unstable in sampling frequency point of view, because its sampling frequency is almost equals system's frequency (50Hz). The FMPC computational load is increased again, and would lead to instability issues on hardware, while the computational load is still constant for the IMPC. Based on these experiments, it can be concluded that the time complexity for the MPC is O(N), $\approx \mathbf{O}(0.21N)$ for the FMPC, and $\mathbf{O}(1)$ for the IMPC. Where $\mathbf{O}(1)$ represents the worst-case time complexity for a single prediction stage. These results show the superiority of the proposed IMPC among all existing MPCs and FMPCs in terms of computational load.

V. CONCLUSION

This study introduces a new control technique called inverse model predictive control that was experimentally implemented and validated for three-phase 5-level ANPC-FC converter. The results obtained from the implementation of the proposed controller showed excellent performance in challenging scenarios that are typically encountered by power converters. These scenarios include load uncertainty, highly distorted grid voltages, and unbalanced grid voltages. The proposed IMPC controller demonstrated robust response and effectively handled these abnormal conditions. The proposed technique offers the advantages of supporting bi-directional operation of controlled converter. One notable advantage of the IMPC technique is its negligible computational time, making it suitable for industrial applications on low-cost microcontrollers. Additionally, the proposed IMPC technique shares the same advantages as conventional MPC, such as achieving objectives while adhering to constraints, minimal parameter tuning requirements, and a straightforward structure for short horizons.

Overall, the proposed IMPC technique proved to be a promising solution for power electronics converters and electric drives, offering enhanced performance, compatibility with industrial applications, and computational efficiency. The significant reduction in the computational power makes the proposed control an outstanding solution for longer horizons prediction particularly for multilevel and multiphase systems.

REFERENCES

[1] E. M. G. Rodrigues, R. Godina, and E. Pouresmaeil, "Industrial applications of power electronics," *Electronics*, vol. 9, no. 9, p. 1534, Sep. 2020.

[2] J. Fang, F. Blaabjerg, S. Liu, and S. M. Goetz, "A review of multilevel converters with parallel connectivity," *IEEE Trans. Power Electron.*, vol. 36, no. 11, pp. 12468–12489, Nov. 2021.

[3] H. Komurcugil, S. Bayhan, R. Guzman, M. Malinowski, and H. Abu-Rub, *Advanced Control of Power Converters: Techniques and MATLAB Simulink Implementation*. Hoboken, NJ, USA: Wiley, 2023.

[4] A. Sharida, S. Bayhan, and H. Abu-Rub, "Adaptive control strategy for three-phase three-level T-type rectifier based on online disturbance estimation and compensation," *IEEE Access*, vol. 11, pp. 40967–40977, 2023.

[5] O. Gonzales-Zurita, O. L. Andino, J.-M. Clairand, and G. Escrivá-Escrivá, "PSO tuning of a second-order sliding mode controller for adjusting active standard power levels for smart inverter applications," *IEEE Trans. Smart Grid*, vol. 14, no. 6, pp. 4182–4193, Nov. 2023.

[6] E. Zafra, S. Vazquez, T. Geyer, R. P. Aguilera, and L. G. Franquelo, "Long prediction horizon FCS-MPC for power converters and drives," *IEEE Open J. Ind. Electron. Soc.*, vol. 4, pp. 159–175, 2023.

[7] S. Yan, Y. Yang, S. Y. Hui, and F. Blaabjerg, "A review on direct power control of pulsewidth modulation converters," *IEEE Trans. Power Electron.*, vol. 36, no. 10, pp. 11984–12007, Oct. 2021.

[8] B. Chelladurai, C. K. Sundarabalan, S. N. Santhanam, and J. M. Guerrero, "Interval type-2 fuzzy logic controlled shunt converter coupled novel high-quality charging scheme for electric vehicles," *IEEE Trans. Ind. Informat.*, vol. 17, no. 9, pp. 6084–6093, Sep. 2021.

[9] H. Makhamreh, M. Trabelsi, O. Kükrer, and H. Abu-Rub, "A Lyapunov-based model predictive control design with reduced sensors for a PUC7 rectifier," *IEEE Trans. Ind. Electron.*, vol. 68, no. 2, pp. 1139–1147, Feb. 2021.

[10] A. Sharida, S. Bayhan, and H. Abu-Rub, "Fault-tolerant self-tuning control for three-phase three-level T-Type rectifier," *IEEE Trans. Power Electron.*, vol. 38, no. 6, pp. 7049–7058, Jun. 2023.

[11] Y. Bi, C. Wu, T. Zhao, H. Li, J. Xu, G. Shu, and Y. Wang, "Modified deadbeat predictive current control method for single-phase AC–DC PFC converter in EV charging system," *IEEE Trans. Ind. Electron.*, vol. 70, no. 1, pp. 286–297, Jan. 2023.

[12] S. Bayhan and H. Abu-Rub, "Predictive control of power electronic converters," in *Power Electronics Handbook*. Amsterdam, The Netherlands: Elsevier, 2018, pp. 1325–1336.

[13] I. Harbi, M. Abdelrahem, M. Ahmed, and R. Kennel, "Reduced-complexity model predictive control with online parameter assessment for a grid-connected single-phase multilevel inverter," *Sustainability*, vol. 12, no. 19, p. 7997, Sep. 2020.

[14] A. Bahrami, M. Norambuena, M. Narimani, and J. Rodriguez, "Model predictive current control of a seven-level inverter with reduced computational burden," *IEEE Trans. Power Electron.*, vol. 35, no. 6, pp. 5729–5740, Jun. 2020.

[15] I. Kim, R. Chan, and S. Kwak, "Model predictive control method for CHB multi-level inverter with reduced calculation complexity and fast dynamics," *IET Electr. Power Appl.*, vol. 11, no. 5, pp. 784–792, May 2017.

[16] Y. Yang, H. Wen, M. Fan, L. He, M. Xie, R. Chen, M. Norambuena, and J. Rodríguez, "Multiple-voltage-vector model predictive control with reduced complexity for multilevel inverters," *IEEE Trans. Transport. Electrific.*, vol. 6, no. 1, pp. 105–117, Mar. 2020.

[17] H. Lin, S. Niu, Z. Xue, and S. Wang, "A simplified virtual-vector-based model predictive control technique with a control factor for three-phase SPMSM drives," *IEEE Trans. Power Electron.*, vol. 38, no. 6, pp. 7546–7557, Jun. 2023.

[18] R. Mo, Y. Yang, R. Chen, W. Wu, J. Hu, H. Wen, Y. Wang, G. Fang, and J. Rodriguez, "Low-complexity virtual-vector-based FCS-MPC with unaffected neutral-point voltage for three-phase T-type inverters," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 12, no. 2, pp. 1683–1693, Apr. 2024.

[19] I. Gonzalez-Prieto, M. J. Duran, A. Gonzalez-Prieto, and J. J. Aciego, "A simple multi-step solution for model predictive control in multiphase electric drives," *IEEE Trans. Ind. Electron.*, vol. 71, no. 2, pp. 1158–1169, Feb. 2024.

[20] Y. Xie, R. Zhao, L. Shi, J. He, C. Yuan, C. Meng, X. Fan, and J. Gu, "A simplified algorithm of finite set model predictive control for three-phase CHB-based BESSs," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 12, no. 2, pp. 1203–1214, Apr. 2024.

[21] R. Chakraborty, P. M. Gajare, R. Chaki, and A. Dey, "A simplified dual-stage model predictive controller for modular multilevel converters," *Electr. Power Syst. Res.*, vol. 223, Oct. 2023, Art. no. 109525.

[22] B. Liu, G. Li, D. He, and Y. Chen, "DC and AC power quality control for single-phase grid-tied PEMFC systems with low DC-link capacitance by solution-space-reduced MPC," *IEEE Trans. Ind. Electron.*, vol. 69, no. 6, pp. 5625–5636, Jun. 2022.

[23] A. Salem, M. A. Abido, and F. Blaabjerg, "Common-mode voltage mitigation of dual T-type inverter drives using fast MPC approach," *IEEE Trans. Ind. Electron.*, vol. 69, no. 8, pp. 7663–7674, Aug. 2022.

[24] A. Sharida, N. F. Kamal, H. Alnuweiri, S. Bayhan, and H. Abu-Rub, "Digital-twin-based diagnosis and tolerant control of T-type three-level rectifiers," *IEEE Open J. Ind. Electron. Soc.*, vol. 4, pp. 230–241, 2023.

[25] N. Guler, S. Bayhan, and H. Komurcugil, "Equal weighted cost function based weighting factor tuning method for model predictive control in power converters," *IET Power Electron.*, vol. 15, no. 3, pp. 203–215, Feb. 2022.

[26] P. Wang, Y. Bi, F. Gao, T. Song, and Y. Zhang, "An improved deadbeat control method for single-phase PWM rectifiers in charging system for EVs," *IEEE Trans. Veh. Technol.*, vol. 68, no. 10, pp. 9672–9681, Oct. 2019.

[27] *IEEE Recommended Practice for Monitoring Electric Power Quality*, IEEE Standard 1159, 2019.

[28] *IEEE Recommended Practices and Requirements for Harmonic Control in Electrical Power Systems*, Standard IEEE SM 519-199, New York, NY, USA, 1993.

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