IEEE Access
Multidisciplinary | Rapid Review | Open Access Journal

Received 8 April 2024, accepted 28 April 2024, date of publication 1 May 2024, date of current version 14 May 2024.

Digital Object Identifier 10.1109/ACCESS.2024.3396127

RESEARCH ARTICLE

Design of a Solid State Circuit Breaker Using a SiC MOSFET for LVDC Applications

BYONG JO HYON[1,2], POO REUM JANG[1], DONGMYOUNG JOO[1], YONG-SU NOH[1], JUN-HYUK CHOI[1], AND SANG BIN LEE[2], (Fellow, IEEE)

[1]Korea Electronics Technology Institute, Bucheon-si 14502, South Korea
[2]Department of Electrical Engineering, Korea University, Seoul 02841, South Korea

Corresponding author: Sang Bin Lee (sangbinlee@korea.ac.kr)

This work was supported by Korea Institute of Energy Technology Evaluation and Planning (KETEP) through the Ministry of Trade, Industry and Energy of the Republic of Korea under Grant 2019381010001A and Grant 20212020800020.

ABSTRACT In this paper, a solid state circuit breaker(SSCB) for a low voltage direct current (LVDC) system is presented. The LVDC distribution system such as a household distribution, require a DC input source, DC loads, and a DC circuit breaker. The major problems in the DC distribution system are the arc problem of disconnecting power from loads and a fast acting circuit breaker for the existing power converter. Therefore, a fast acting and high-voltage-withstanding circuit breaker such as the SSCB is required. The SSCB is composed of wide-band gap power semiconductor switch, such as a SiC MOSFET. It can operate in a very short time and contain the energy-absorbing or bypass circuit to protect itself and other components in the LVDC distribution system under a short circuit fault. In this paper, an SSCB using a SiC MOSFET for LVDC applications is presented. It contains a parallel bypass circuit to reduce the fault energy. The circuit of the SSCB was simulated using PSIM and validated experimentally using a prototype.

INDEX TERMS LVDC, SSCB, SiC Mosfet, DC grid, protection.

I. INTRODUCTION

Today, the interest in electric energy has increased. In particular, the research on the high-voltage direct current (HVDC) on the transmission side and low voltage direct current (LVDC) on the consumer side is developed widely. In the DC distribution system, several problems are encountered in applying the components of the existing AC system as it is [1], [2]. For a circuit breaker, unlike in the AC system, the problem of arc generation must be considered very seriously. For this problem, several mechanisms exist such as the mechanical arc block method, a hybrid method that mixes mechanical and semiconductor components, and the semiconductor circuit method [3], [4]. Frequently, a power converter with the semiconductor device is used in LVDC applications such as a household distribution. It requires a fast acting circuit breaker to protect the system and other branches under a fault condition. The semiconductor circuit breaker, solid state circuit breaker (SSCB), has the advantage of being able to secure a very short operation time and disadvantage of requiring a high withstand voltage and current specification. The topologies of a typical SSCB are categorized into bypass circuit and energy-absorbing circuit [5], [6], [7]. An energy absorber type SSCB using a snubber circuit can dissipate the stored energy in load inductor and reduce the spike voltage of power device. The bypass circuit type SSCB can seperate the power devices from the fault side. The stored fault energy can be dissipated by freewheeling through bypass path. The topology used in this paper contains parallel bypass circuit. The fault current rapidly rises to threshold level and the bypass path was activated to reduction fault current in main bypass circuit. This could more reduce the peak spike voltage rapidly than other topologies. Also, the power devices of SSCB can be considered. Usually, the insulated gate bipolor transistor(IGBT) or MOSFET were used in SSCB as main power switch. Recently, the SSCB using a SiC MOSFET or a ganlium-nitride(GaN) power device is researched very widely [8], [9]. The design requirement of a SSCB system

The associate editor coordinating the review of this manuscript and approving it for publication was Yuh-Shyan Hwang.

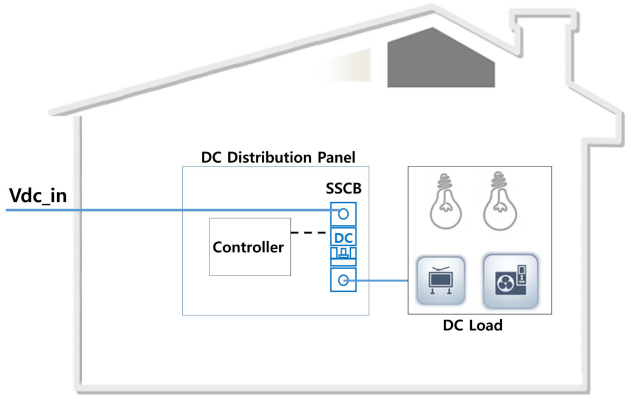

FIGURE 1. Powerline configuration of a DC household.

using wide-band gap(WBG) devices such as a SiC MOSFET or GaN is more complicated. The gate drive circuit and protection circuit is different from conventional IGBT or MOSFET circuit. These are considered to design a topology and protection logic of the SSCB. In the LVDC system, because the voltage rating is approximately 380 V and the current rating is low, it is suitable system for applying the SSCB. In this paper, an SSCB using a SiC MOSFET for LVDC applications is presented. The SiC MOSFET was used in main power switches and the SSCB was designed to protect short circuit accident by desaturation detection circuit. The SSCB contains the parallel bypass circuit to reduce the fault energy. The circuit of the SSCB was simulated using PSIM and validated experimentally using a prototype.

The remainder of this paper is presented as follows. In section II, the SSCB used in LVDC system is presented. In subsections II-A and B, the conventional SSCB and proposed SSCB are described. The operation of the SSCB is presented in subsection II-C. In subsection II-D, the design parameters of the SSCB are presented. The simulation of the SSCB and experimental results are presented in sections III and IV. Finally, section V presents the conclusions of this paper.

II. SOLID STATE CIRCUIT BREAKER OF LVDC SYSTEM

The symbols and acronyms used in this paper as follows:

SSCB	Solid State Circuit Breaker
LVDC	Low Voltage Direct Current
L_{li}	input line inductor
L_{lo}	output line inductor
R_1,R_2,R_3	snubber resistor
C_1,C_2,C_3	snubber resistor
D_1,D_2,D_3	snubber resistor
T_1	thyristor
S_1,S_2	power switch

The power line of system is shown in Fig 1.

1) In LVDC distribution system, the power distribution consists of an input power converter, a distribution panel, a controller, a circuit breaker, and DC loads. The input power of distribution system is connected to a power converter. Therefore, under a fault, the use of a fast acting circuit breaker is required to disconnect only the faulty load branch and to protect the power converter. When a fault occurs, the switch of the SSCB may be destroyed owing to an overvoltage induced by line inductive component. A fault energy reducing method is required to protect the power device of the SSCB. As research on LVDC grid systems has increased, research on the SSCB has also been actively conducted [8], [9], [10], [11], [12].

A. CONVENTIONAL SSCB

The topologies of a typical SSCB are categorized into bypass circuit based type [13], [14] and energy-absorbing circuit based type [15], [16], [17] by reducing fault energy method.

Fig. 2 shows the configuration of a conventional SSCB.

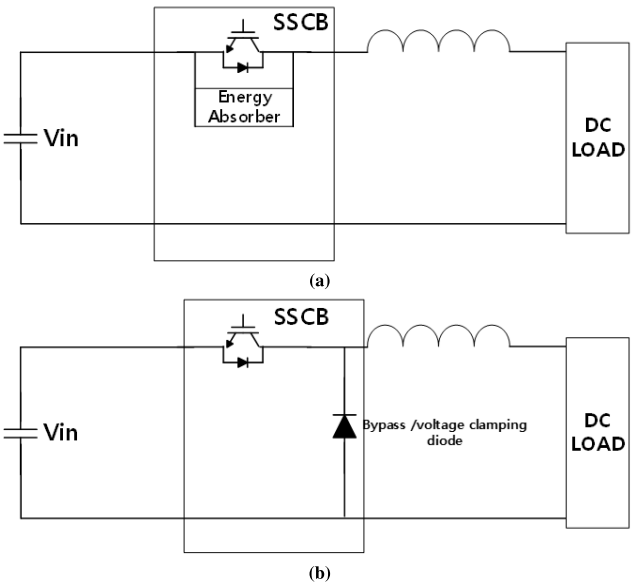

FIGURE 2. Configuration of Conventional SSCB : (a)energy absorber (b)bypass diode.

AS shown in Fig. 2 (a), the SSCB has an energy absorber unit. Under a fault, the stored fault energy in the output line inductor can be dissipated by an energy absorber such as a snubber circuit. The snubber can reduce the spike voltage of the power device. The snubber parameters must designed properly. The stored energy, fault current, and desired spike voltage level are key variables. The parameters of the snubber can be determined through an analysis of an equivalent circuit of the SSCB.

Fig. 2 (b) shows the bypass type SSCB. This topology contains a bypass circuit such as a clamping diode. The bypass circuit separates the power devices from the fault side. The stored energy can be dissipated by freewheeling through the bypass diode. Additionally, it can clamp a spike voltage to prevent exceeding the voltage rating of the power devices. The specifications of the metal oxide varistor should be designed considering the stored energy and desired clamping

voltage with its margin. A series or parallel combination of diode-based circuit design can be developed. In another cases, a combination of two SSCB types is used.

B. PROPOSED SSCB

Fig. 3 shows the configuration of the proposed SSCB.

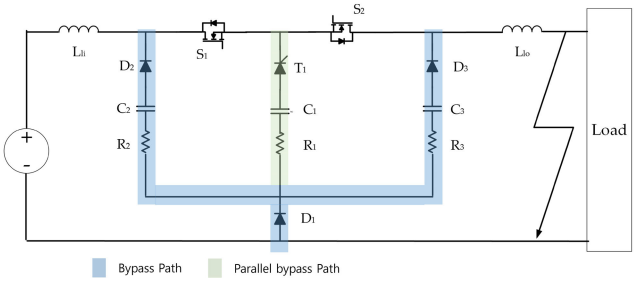

FIGURE 3. Configuration of proposed SSCB.

The proposed SSCB consist of a bypass circuit using R_3, C_3, and D_3 and a second bypass circuit using R_1, C_1, and thyristor T_1. Under a fault, the controller detects a fault current over the threshold level and turns off the power devices S_1 and S_2. The stored energy in L_{lo} flows through the bypass path D_1-R_3-C_3-D_3-L_{lo}. This process reduces overvoltage across the power devices S_1 and S_2. To reduce overvoltage further, the thyristor T_1 turns on at a predetermined fault current level. Subsequently, the fault current flows in the parallel path R_3-C_3-D_3 and R_1-C_1-T_1-freewheeling diode of S2. The current path under a fault is shown in Fig. 5.

C. OPERATION OF SSCB

Figs. 4 and 5 depict the operation waveforms and operation modes of the proposed SSCB.

1) Mode 1 [before t_1]: The SSCB operates in the normal mode. The power devices S_1 and S_2 turn on and transfer power from the source to load. This means $I_{l0} = I_{load}$, $V_{load} = V_{in}$ and D_1, D_2, D_3, and T_1 remain in the off state.
2) Mode 2 [$t_1 \leqslant t < t_2$] : At t_1, a short circuit fault occurs. The load current I_{Lo} increases with a slope depending on output line inductance L_{lo}. At t_2, the load current exceeds the threshold current level I_{th}, and the gate signal of power device V_{gs-s} begins turning off.
3) Mode 3[$t_2 \leqslant t < t_3$] : S_1 and S_2 turn off at t_3. Before t_3, the load current still increases with a same slope as in Mode 2. At t_3, the turning off completes.
4) Mode 4 [$t_3 \leqslant t < t_4$] : After power devices turn off, the fault current freewheels by the bypass path, and the spike voltage across the power devices increases. Moreover, the switch current I_{SW_2} decreases. The stored energy in output line inductance L_{lo} begins flowing through the D_1-R_3-C_3-D_3-L_{lo} path. The bypass current I_{R_3} and the spike voltage across power device S_2 (V_{ds}) is determined by resistor R_3 and capacitor C_3.

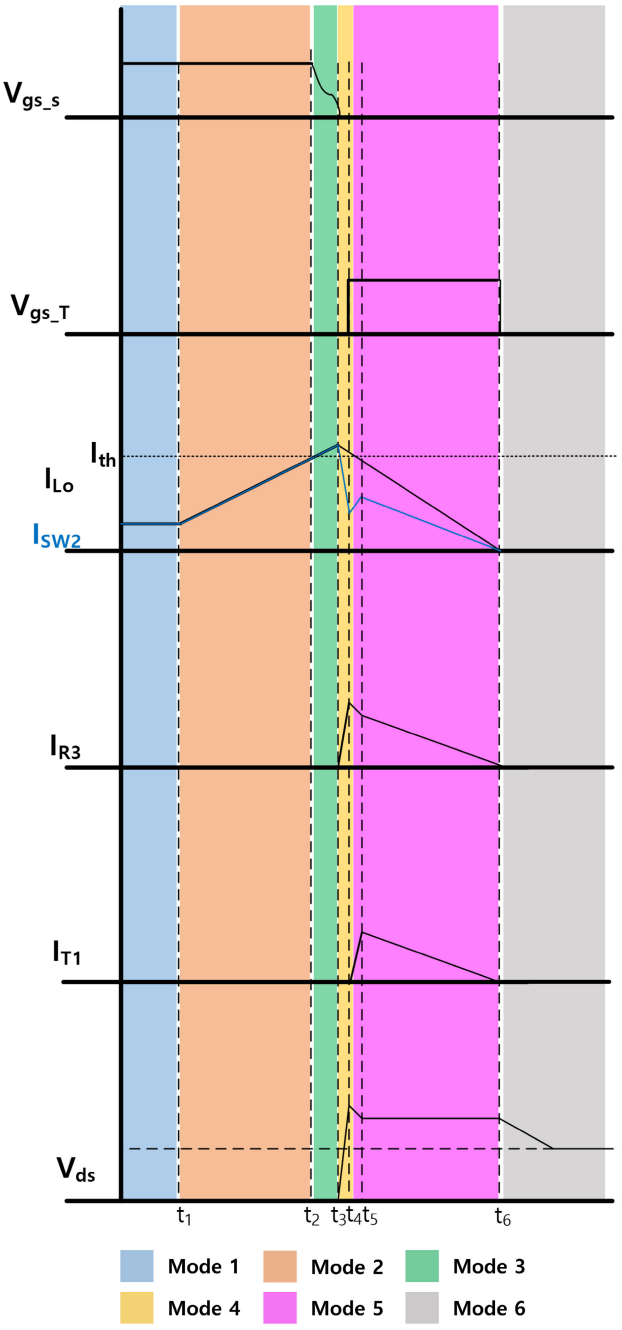

FIGURE 4. The operation waveforms of the proposed SSCB.

5) Mode 5 [$t_4 \leqslant t < t_6$] : At t_4, the thyristor T_1 turns on and the fault current flows through the D_1-R_3-C_3-D_3 path and the D_1-R_1-C_1-T_1-body diode of the S_2 path. The stored energy decreases rapidly at the beginning of the bypass operation. This means that Modes 4 and 5 occur in the very short term. This reduces the spike voltage across the power devices and protects them. The turning on timing of T_1 is determined by the threshold current and the overvoltage margin related on the rating voltage of the power device. As the stored energy

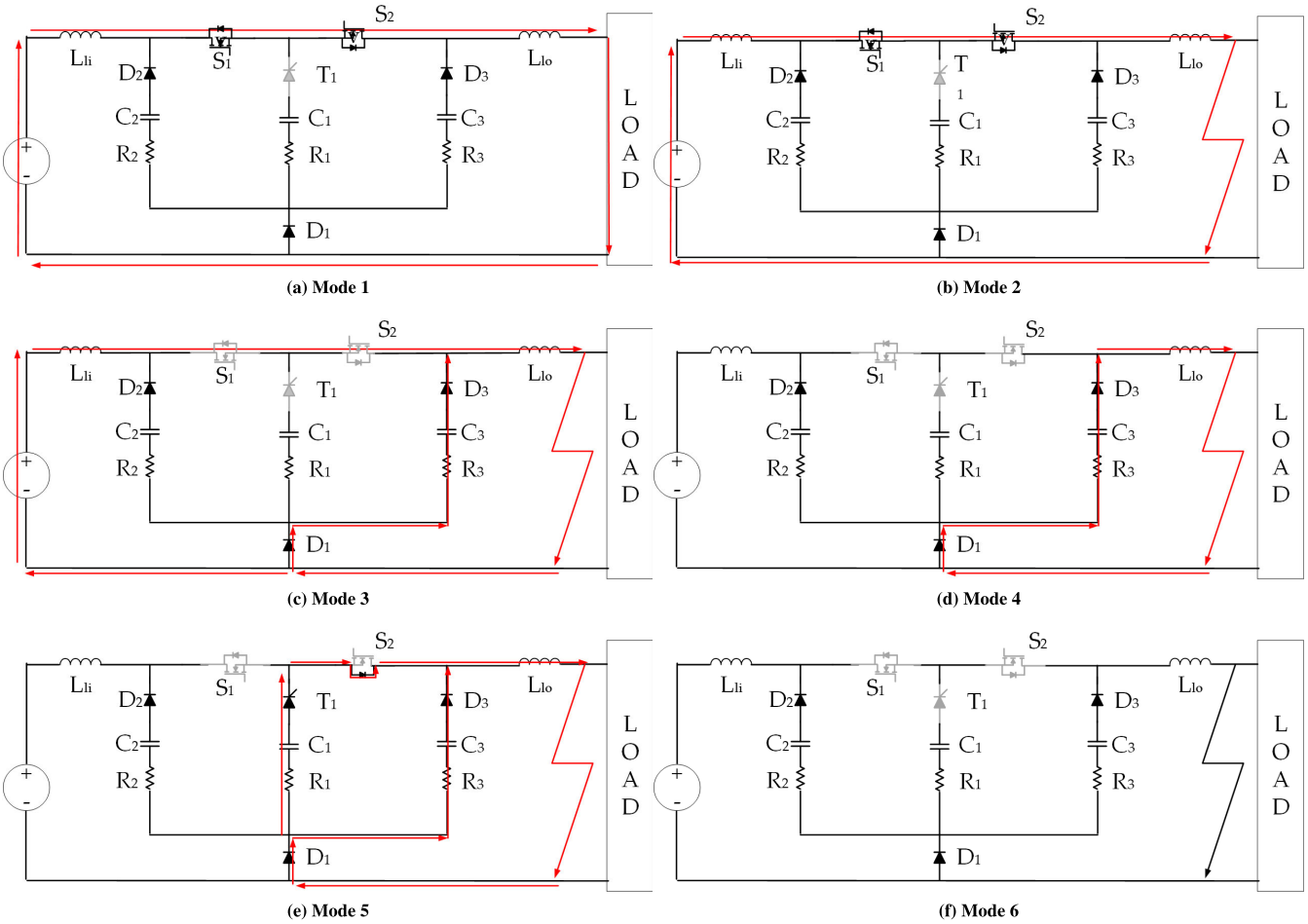

FIGURE 5. Operation modes of the proposed SSCB during a DC current fault condition.

decreases, the bypass currents of parallel path also decrease.

6) Mode 6 [t $\geqslant$ t_6] : At t_6, the fault bypass currents reduce to zero. The sotred fault energy completely is consumed, and the thyristor T_1 turns off.

For a reverse direction, the operation process is same as that above. The difference is the position of fault, a source side fault, and bypass path, R_2-C_2-D_2. In this case, the additional bypass path through T_1 operates through the same mechanism.

D. DESIGN PARAMETERS OF SSCB

The design requirements of the proposed SSCB is shown in Table 1. To design parameter of SSCB, the target spike voltage, fault current and operating temperature were pre-determined. These requirement affected to select power devices of SSCB and could be affected by designed parameters for optimizing procedure. As shown in Fig. 5, the fault current flows through bypass path D_1-R_3-C_3-D_3-L_{lo}. In addition, after T_1 is turned on, the fault current also passes through another path, D_1-R_1-C_1-T_1-body diode of S_2. To design each parameter, we consider the analysis of

TABLE 1. Design requirement of proposed SSCB.

Electrical Requirement	
Input voltage	DC 380 V
Maximum Fault current	$\leqslant 120A$
Normal current rating	10 A
Target spike voltage	$\leqslant 1000V$
Dynamics Requirement	
Breaking time	$\leqslant 20\mu s$
Thermal Requirement	
Cooling method	Air cooling
Operating temperature	$\leqslant 70\,^{\circ}$C
Mechanical mounting Requirement	
Mounting Style	Base plate + power module + PCB + case

equivalent circuit after a fault [18]. In Mode 4, after S_1 and S_2 are turned off, the stored energy in L_{lo} is in capacitor C_3. The spike voltage across the power devices is related to the capacitance of C_3 and the resistance of R_3 [17], [18]. Even in worst case where the thyristor is not operating, the stored energy can be dissipated, and S_1 and S_2 can be protected from the overvoltage stress. Therefore, considering this requirement, the mathematical model of the SSCB circuit

in Mode 4 is represented in (1)-(2). The voltage model is shown in (1) by using KVL analysis. The input voltage is the same as a voltage across an output line inductor, a resistor R_3 and a capacitor C_3.

$$V_{dc} = R_3 i_{R_3}(t) + L_{lo}\frac{di_{lo}(t)}{dt} + V_{C_3}(t)$$
$$i_{lo} = i_{R_3} = C_3\frac{dV_{c_3}(t)}{dt} \quad (1)$$

where V_{C_3} is the charged voltage in C_3, and i_{R_3} is the current passing through R_3, which is the same as the fault current i_{lo}. To achieve a fast reaction of the SSCB, we adopt the underdamped response in this model. The charged capacitor voltage and the bypass current is described in (2).

$$V_{C_3}(t) = V_{dc} + e^{-\alpha t}(D_1\cos\omega_d t + D_2\sin\omega_d t).$$
$$\alpha = \frac{R_3}{2L_{lo}}, \omega_0 = \frac{1}{\sqrt{L_{lo}C_3}}, \omega_d = \sqrt{\omega_0^2 - \alpha^2}.$$
$$D_1 = -V_{dc}, D_2 = \frac{I_{flt}}{C_3} + \alpha V_{dc}. \quad (2)$$

where α is the damping coefficient, ω_0 is the resonant frequency, and ω_d is damped natural frequency. I_{flt} is the fault current, which is the maximum current in the bypass path. At t $= t_4$, the I_{SW_2} reaches its minimum value in the energy dissipation process, and the bypass current reaches the peak value. When operating with T_1, I_{SW_2} does not reach zero. In the other case, I_{SW_2} reaches zero. In both of them, the bypass current I_{R_3} can be the peak current value, and the capacitor voltage V_{C_3} reaches the peak value. To prepare for a scenario where T_1 is not operating, we must consider the parameters of only the single bypass path without the thyristor. The spike voltage across the power devices can be limited in the maximum voltage of the power devices, and the consumption of the bypass path capability should be greater than the fault energy stored in line inductance L_{lo}. The capacitance of C_3 is designed using the criterion described in (3).

$$\frac{1}{2}C_3(V_{spk} - V_{dc})^2 \geqslant \frac{1}{2}L_{lo}I_{flt}^2. \quad (3)$$

where V_{spk} is the maximum target spike voltage.

Therefore, the minimum value of capacitance of C_3 is given by

$$C_3 \geqslant L_{lo}\left(\frac{kI_{flt}}{V_{spk} - V_{dc}}\right)^2, (1 < k \leqslant 1.2). \quad (4)$$

where k is the margin factor.

The resistor R_3 reduces the fault current rapidly. This means that a small resistor value reduces the peak voltage of the power devices. However, in this case, the very large current exceeding the current rating of power devices causes severe damage. Therefore, the resistor value is considered of the initial charging voltage, i.e, V_{dc}. R_3 is expressed in (5). The resistor R_1 in parallel bypass path could be determined by considering fault current level and balancing of current in both path.

$$R_3 \geqslant \frac{V_{C_3}}{kI_{flt}}. \quad (5)$$

The design process of the proposed SSCB is shown in Fig. 6. The parameter C_3 and R_3 are closely related to each other. The change of capacitance C_3 affects the change the peak spike voltage and the energy flowed bypass path. To compensate this, the resistance or R_3 could be changed. Similarly, the change of resistance affects the capacitance of C_3. The target spike voltage and the fault current could be considered again to optimize parameter C_3 and R_3 iterationally.

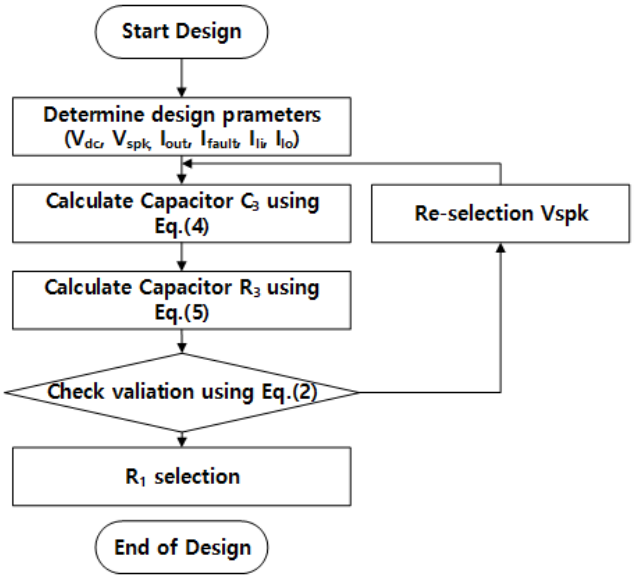

FIGURE 6. The procedure to design parameters of the proposed SSCB.

III. SIMULATIONS

A. SIMULATION SETUP

Fig. 7 shows the simulation setup block using PSIM tools. The simulation parameters are presented in Table 2. The input voltage was 380 Vdc and output rated current was 10 A. The simulation achieved at first normal operating mode and then the short circuit fault occurred at t = 1 ms. The fault current cut off level was set to 120 A, and the load line inductance was 12.5 μH.

B. SIMULATION RESULTS

Fig. 8 shows the simulation results. In Fig.8 (a), the fault current bypass path is only the D_1-R_3-C_3-D_3-L_{lo} path. The simulation the spike voltage across the power device was 923 V. When using T_1, the fault current flowed through the parallel bypass path, D_1-R_3-C_3-D_3 and D_1-R_1-C_1-T_1-body diode of the S_2 path, as shown in Fig. 8 (b). The simulation spike voltage across the power device was 785 V, which was less than the case without thyristor operation. The proposed SSCB reduced the spike voltage peak and mitigated severe damage to the power device.

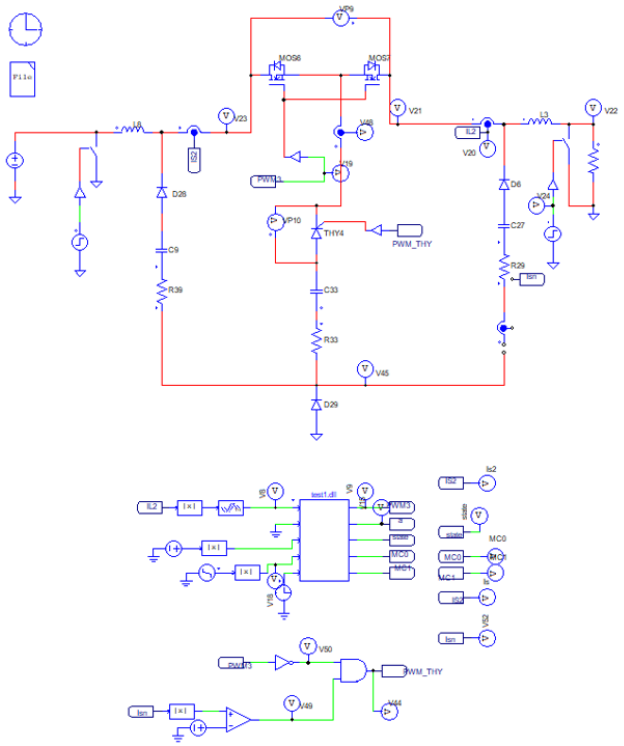

FIGURE 7. Block diagram of the SSCB simulation using PSIM tool.

TABLE 2. Simulation parameters of the proposed SSCB.

Parameter	Specifications	Units
V_{in}	380	V_{dc}
L_{lo}	12.5	μH
R_{load}	40	Ω
R_1, R_3	3.3	Ω
C_1, C_3	1.44	μF
I_{th}	120	A

IV. EXPERIMENTAL RESULTS

A. TEST SYSTEM AND THE SSCB PROTOTYPE HARDWARE

Fig. 9 shows a test system of a prototype of the proposed SSCB. The test system consisted of an input power source, a dc-link capacitor bank, a SSCB prototype, resistor loads, and a fault generator. The circuit breaker separated the dc-link capacitor bank from the input power source to protect the power source. The fault generator was another circuit breaker or fault inductor to produce a short circuit fault. When using the fault inductor, the output total inductance was set to 12.5 μH. The parameters of the SSCB prototype are presented in Table 3. The parameters of the bypass components $R_1 \sim R_3$ and $C_1 \sim C_3$ were selected considering the overvoltage of power device and the fault current level.

The test procedure was conducted as follows. The circuit breaker connected the power source to the capacitor bank, and the capacitor bank charged to 380 V. After the circuit breaker was turned off and a short circuit fault was generated, the SSCB turned on. To test the for reverse direction, we swapped the load and source sides.

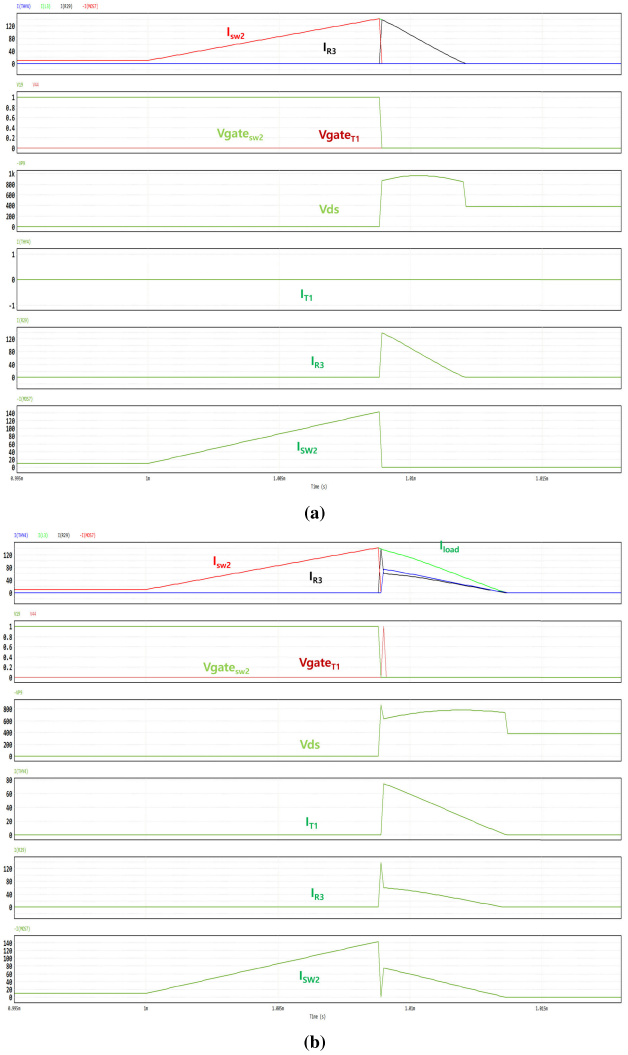

FIGURE 8. Simulation results: (a) without thyristor operation (b) with thyristor operation.

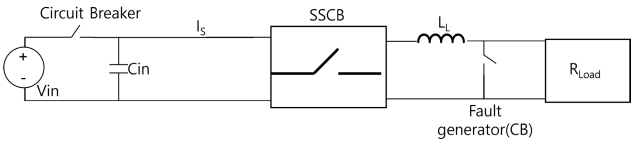

FIGURE 9. Configuration of test system for the proposed SSCB test.

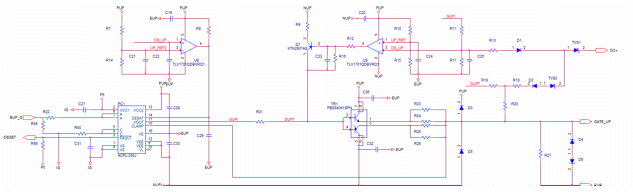

FIGURE 10. Gate drive circuit of the SSCB.

The power device selected for the SSCB was C3M0016120D. This is a discrete SiC MOSFET with a 1.2 kV voltage rating and drain-source on state resistance

TABLE 3. Parameters of proposed SSCB.

Parameter	Specifications	Units
V_{in}	380	V_{dc}
L_{lo}	12.5	μH
R_{load}	40	Ω
R_1, R_2, R_3	3.3	Ω
C_1, C_2, C_3	1.44	μF
I_{th}	120	A
S_1, S_2	C3M0016120D	

of 16 mΩ. S_1 and S_2 were directed to each other for bidirectional operation. The gate signals of S_1 and S_2 were generated using a single gate driver, as shown in Fig. 10. The short circuit current detection and protection were operated using a desaturation detection circuit [19], [20].

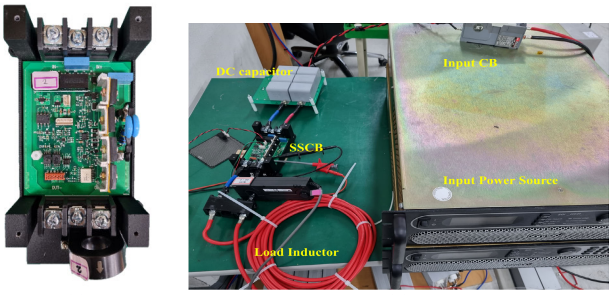

FIGURE 11. Experimental setup : (a) SSCB prototype (b) test setup.

Fig.11 (a) and (b) present the proposed SSCB prototype and test setup.

B. EXPERIMENTAL RESULTS

Fig. 12 presents the experimental results of the proposed SSCB prototype for operation in both directions. As shown in Fig. 12 (a) presents the case when the thyristor was not operating. The gate signal of S_1 and S_2 turned on and the output current increased with slope 32 A/μs. The output current reached the threshold current level 120 A. Subsequently, the gate signal began turning off, and the output current still increased. S_1 and S_2 turned off completely and the voltage across the power devices V_{ds} increased. The output current decreased and the fault current flowed through the bypass path. The bypass current reached the peak value, and V_{ds} reached the peak point. The peak voltage was measured as 917 V. Fig. 12 (b) shows the case for the operating thyristor. Here, when the gate signal completely turned off, the output current decreased but the fault current flowed in the parallel D_1-R_3-C_3-D_3 path and D_1-R_1-C_1-T_1-body diode of S_2 path. The peak voltage of V_{ds} was measured as 775 V. These results were approximate the simulation results 923 and 785 V. Fig. 12 (c) and (d) depict the experimental results of the reverse direction case. The peak output voltages were 919 V(w/o thyristor) and 816V (with thyristor). The

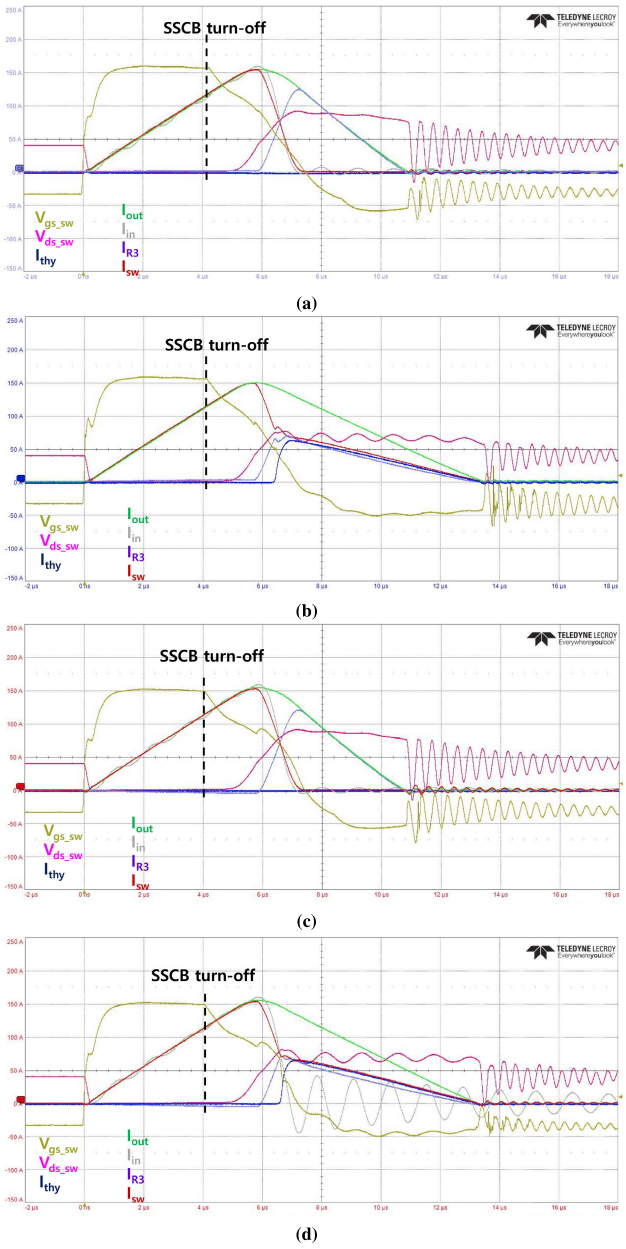

FIGURE 12. Experimental Results : (a) without thyristor operation (b) with thyristor operation (c) without thyristor in reverse direction (d) with thristor in reverse direction.

oscillations of experimental waveforms in Fig. 12 is caused by caused by resonance between output line inductor, capacitor of bypass circuit. The output line inductance is different for each location. After the environment is selected, it can be optimized.

The experimental results validate the proposed SSCB. The peak voltage of V_{ds} with the operating thyristor was lower than without the thyristor. Even when the thyristor was not operating, the peak voltage of V_{ds} was lower than the voltage rating of the power devices. This means that the proposed SSCB can protect the power devices even for changing bypass paths under short circuit faults.

TABLE 4. Comparison table.

SSCBs	Energy absorber topology	Bypass topology	Proposed SSCB
Complexity	○	◎	○
Fault current bypass	X	○	◎
# of component	○	◎	○
Energy absorption	○	X	○
Voltage spike reduction	○	○	◎

○:good, ◎: better, X: no

V. CONCLUSION

In this paper, an SSCB using a SiC MOSFET for LVDC applications is presented. It comprise a parallel bypass circuit to reduce the fault energy. The circuit of the SSCB was simulated using PSIM and validated experimentally using a prototype. The characteristics of other conventional SSCBs and proposed SSCB are compared as shown in Table 4. The proposed SSCB is more than or equal to other SSCBs on the whole. The SSCB operates in a very short time, and the parallel bypass circuit reduces the surge voltage, which is proportional to the fault energy and line inductance. The bypass circuit was designed considering a single bypass operation without thyristor. It protects the power devices under a fault. The parallel bypass operation is useful for reducing the fault energy rapidly at a fault generating moment. The operation in the reverse direction is also studied. The gate drive signals of power devices S_1 and S_2 are generated in a single gate driver. The over current fault is detected and protected by the desaturation circuit of the gate driver.

The circuit of SSCB was simulated using PSIM. The experimental results were obtained using a SSCB prototype. The experiment of operations with and without thyristor T_1 were compared. With the thyristor, the spike voltage of power devices was lower than that without it. Almost similar results with simulation results were obtained, indicating that the proposed SSCB can be useful in the LVDC distribution system.

REFERENCES

[1] C. D. Xu and K. W. E. Cheng, "A survey of distributed power system—AC versus DC distributed power system," in *Proc. 4th Int. Conf. Power Electron. Syst. Appl.*, Jun. 2011, pp. 1–12.

[2] A. T. Elsayed, A. A. Mohamed, and O. A. Mohammed, "DC microgrids and distribution systems: An overview," *Electr. Power Syst. Res.*, vol. 119, pp. 407–417, Feb. 2015.

[3] C. Gu, P. Wheeler, A. Castellazzi, A. J. Watson, and F. Effah, "Semiconductor devices in solid-state/hybrid circuit breakers: Current status and future trends," *Energies*, vol. 10, no. 4, p. 495, Apr. 2017.

[4] Y. He, Q. Yang, Y. Li, S. Kim, F. Z. Peng, M. Bosworth, L. Wang, Z. Jin, Y. Shi, N. Bonaventura, M. Steurer, C. Xu, and L. Graber, "Control development and fault current commutation test for the Edison hybrid circuit breaker," *IEEE Trans. Power Electron.*, vol. 38, no. 7, pp. 8851–8865, Jul. 2023.

[5] Z. J. Shen, Z. Miao, and A. M. Roshandeh, "Solid state circuit breakers for DC micrgrids: Current status and future trends," in *Proc. IEEE 1st Int. Conf. DC Microgrids (ICDCM)*, Jun. 2015, pp. 228–233.

[6] S. Martin. (Jul. 24, 2019). *First Digital Circuit Breaker Certified for Commercial Use*. Engineering 360. [Online]. Available: https://insights.globalspec.com/article/11944/first-digital-circuitbreaker-certified-for-commercial-use

[7] R. Rodrigues, Y. Du, A. Antoniazzi, and P. Cairoli, "A review of solid-state circuit breakers," *IEEE Trans. Power Electron.*, vol. 36, no. 1, pp. 364–377, Jan. 2021, doi: 10.1109/TPEL.2020.3003358.

[8] Y. Zhou, Y. Feng, T. Liu, and Z. J. Shen, "A digital-controlled SiC-based solid state circuit breaker with soft-start function for DC microgrids," in *Proc. 9th IEEE Int. Symp. Power Electron. Distrib. Gener. Syst. (PEDG)*, Jun. 2018, pp. 1–7.

[9] J. Hayes, K. George, P. Killeen, B. McPherson, K. J. Olejniczak, and T. R. McNutt, "Bidirectional, SiC module-based solid-state circuit breakers for 270 V_{dc} MEA/AEA systems," in *Proc. IEEE 4th Workshop Wide Bandgap Power Devices Appl. (WiPDA)*, Nov. 2016, pp. 70–77.

[10] K.-T. Mok, M.-H. Wang, S.-C. Tan, and S. Y. R. Hui, "DC electric springs—A technology for stabilizing DC power distribution systems," *IEEE Trans. Power Electron.*, vol. 32, no. 2, pp. 1088–1105, Feb. 2017.

[11] D. Wang, A. Emhemed, G. Burt, and P. Norman, "Fault analysis of an active LVDC distribution network for utility applications," in *Proc. 51st Int. Universities Power Eng. Conf. (UPEC)*, Coimbra, Portugal, Sep. 2016, pp. 1–6, doi: 10.1109/UPEC.2016.8114002.

[12] D. Marroquí, J. M. Blanes, A. Garrigós, and R. Gutiérrez, "Self-powered 380 V DC SiC solid-state circuit breaker and fault current limiter," *IEEE Trans. Power Electron.*, vol. 34, no. 10, pp. 9600–9608, Oct. 2019.

[13] M. F. Rahman, T. Pang, E. Shoubaki, N. Sakib, and M. Manjrekar, "Active voltage clamping of series connected 1.2 kV SiC MOSFETs for solid state circuit breaker application," in *Proc. IEEE 7th Workshop Wide Bandgap Power Devices Appl. (WiPDA)*, Oct. 2019, pp. 332–336.

[14] T. Pang, M. F. Rahman, E. Shoubaki, and M. Manjrekar, "Diode clamped solid-state circuit breaker: A novel solid-state circuit breaker without dynamic voltage unbalancing issues," in *Proc. IEEE Appl. Power Electron. Conf. Exposit. (APEC)*, Mar. 2020, pp. 2715–2720.

[15] F. Liu, W. Liu, X. Zha, H. Yang, and K. Feng, "Solid-state circuit breaker snubber design for transient overvoltage suppression at bus fault interruption in low-voltage DC microgrid," *IEEE Trans. Power Electron.*, vol. 32, no. 4, pp. 3007–3021, Apr. 2017.

[16] W. Liu, H. Yang, F. Liu, J. Sun, and X. Zha, "An improved RCD snubber for solid-state circuit breaker protection against bus fault in low-voltage DC microgrid," in *Proc. IEEE 2nd Int. Future Energy Electron. Conf. (IFEEC)*, Nov. 2015, pp. 1–5.

[17] A. Mokhberdoran, A. Carvalho, N. Silva, H. Leite, and A. Carrapatoso, "Design and implementation of fast current releasing DC circuit breaker," *Electr. Power Syst. Res.*, vol. 151, pp. 218–232, Oct. 2017.

[18] D. Shin, S.-K. Sul, J. Sim, and Y.-G. Kim, "Snubber circuit of bidirectional solid state DC circuit breaker based on SiC MOSFET," in *Proc. IEEE Energy Convers. Congr. Expo. (ECCE)*, Sep. 2018, pp. 3674–3681.

[19] Y. Zhang and Y. C. Liang, "Over-current protection scheme for SiC power MOSFET DC circuit breaker," in *Proc. IEEE Energy Convers. Congr. Expo. (ECCE)*, Sep. 2014, pp. 1967–1971, doi: 10.1109/ECCE.2014.6953660.

[20] S. Mocevic, J. Wang, R. Burgos, D. Boroyevich, M. Jaksic, C. Stancu, and B. Peaslee, "Comparison and discussion on shortcircuit protections for silicon-carbide MOSFET modules: Desaturation versus Rogowski switch-current sensor," *IEEE Trans. Ind. Appl.*, vol. 56, no. 3, pp. 2880–2893, May 2020, doi: 10.1109/TIA.2020.2972816.

BYONG JO HYON was born in South Korea, in 1984. He received the B.S. and M.S. degrees in electrical engineering from Pohang University of Science and Technology, Pohang, South Korea, in 2010 and 2012, respectively. He is currently pursuing the Ph.D. degree in electrical engineering with Korea University, Seoul, South Korea. Since 2014, he has been a Senior Research Engineer with Korea Electronics Technology Institute (KETI), Bucheon, South Korea. His research interests include ac motor drive and LVDC energy conversion.

POO REUM JANG was born in Yeosoo, South Korea, in 1993. He received the B.S. degree in electrical engineering from Pusan National University, Pusan, South Korea, in 2017, and the M.S. and Ph.D. degrees in electrical engineering from Pohang University of Science and Technology (POSTECH), Pohang, South Korea, in 2019 and 2022, respectively. Since 2023, he has been a Senior Research Engineer with Korea Electronics Technology Institute (KETI), Bucheon, South Korea. His current research interests include ac motor control, electric vehicle, and power converter.

DONGMYOUNG JOO received the B.S., M.S., and Ph.D. degrees in electrical engineering from Sungkyunkwan University, Suwon, South Korea, in 2011, 2013, and 2017, respectively. He is currently with the Intelligent Mechatronics Research Center, Korea Electronics Technology Institute (KETI), Bucheon, South Korea.

YONG-SU NOH received the B.S. degree in electrical and electronic engineering from Ajou University, Suwon, South Korea, and the Ph.D. degree in electrical and computer engineering from Sungkyunkwan University, Suwon. Since 2017, he has been a Senior Research Engineer with Korea Electronics Technology Institute, Bucheon, South Korea. His research interests include dc/dc converters and resonant converters.

JUN-HYUK CHOI was born in Daegu, South Korea, in 1974. He received the M.S. and Ph.D. degrees from the School of Electrical and Electronic Engineering, SungKyunKwan University, Suwon, Korea, in 2003 and 2016, respectively. Since 2003, he has been a Principal Research Engineer with Korea Electronics Technology Institute (KETI), Bucheon, South Korea. His research interests include power electronics and motor control systems.

SANG BIN LEE (Fellow, IEEE) received the B.E. and M.E. degrees in electrical engineering from Korea University, Seoul, South Korea, in 1995 and 1997, respectively, and the Ph.D. degree in electrical engineering from Georgia Institute of Technology, Atlanta, GA, USA, in 2001. From 2001 to 2004, he was a Research Scientist with the General Electric Global Research Center, Schenectady, NY, USA. Since 2004, he has been a Professor of electrical engineering with Korea University. From 2010 to 2011, he was a Visiting Scientist with the Austrian Institute of Technology, Vienna, Austria. From 2017 to 2018, he was a Consultant with Qualitrol Iris Power Engineering, Toronto, ON, Canada, and a Visiting Researcher with the University of Waterloo, Waterloo, ON, Canada. His current research interests include monitoring and diagnostics of electric machines and drives. He was a recipient of the 2017 IEEE SDEMPED Diagnostics Achievement Award and 17 IEEE Society- and Committee-Level Prize Paper Awards. He served as an Associate Editor for IEEE TRANSACTIONS ON INDUSTRY APPLICATIONS for the IEEE IAS Electric Machines Committee. He served as the 2014–2016 Distinguished/Prominent Lecturer for IEEE IAS.