IEEE Access
Multidisciplinary | Rapid Review | Open Access Journal

Received 17 February 2024, accepted 24 April 2024, date of publication 30 April 2024, date of current version 9 May 2024.

*Digital Object Identifier 10.1109/ACCESS.2024.3395539*

RESEARCH ARTICLE

# High-Performance Single Switch High Step-Up Quadratic DC–DC Converter With Switched Capacitor Cell

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This work was supported by Vellore Institute of Technology, Vellore, India, through VIT SEED GRANT (RGEMS) under Grant SG20230050.

**ABSTRACT** This article presents a single-switch high step-up quadratic DC-DC converter for DC microgrid applications. The quadratic boost converter is integrated with switched capacitor cell along with coupled inductor to achieve high gain at reduced duty ratio. The switched-capacitor cell is composed of two diodes and two capacitors. The capacitors charge in parallel and discharge in series to increase the converter's gain. The coupled inductor turn ratio can be increased to elevate the converter's gain further. The inductor at the input minimizes the current ripples and makes the input current to be continuous. Moreover, the proposed converter works as a passive clamp circuit to minimize large voltage spikes across the switch (MOSFET) and it has low $R_{ds}$(on-state) to minimize the conduction losses. As a result, the device's rating improves, losses decrease, and it becomes less expensive to switching devices of the converter. The energy leakage of the coupled inductor is recycled to the output capacitor, it can reduce the reverse recovery issue in diodes and increases efficiency of converter further. The proposed converter working principle and its analysis are explained with different operating modes. The performance of the converter is validated with laboratory hardware setup with rating of 160W. Here, the input and output voltages are considered at 20V and 400V, respectively. Finally, the superiority of the proposed converter is compared with existing literature in terms of gain, stress across various components, switching performance and efficiency.

**INDEX TERMS** Coupled inductor, dc–dc converter, high step-up, passive clamp circuit, quadratic, switched capacitor cell.

## I. INTRODUCTION

As the world's fossil fuel reserves continue to deplete at an alarming rate, it is imperative that countries take effective and persuasive action towards the adoption of green energy resources. Many countries have already recognized the need for this shift and are leading the way towards a sustainable future. In the production of electricity, renewable energy sources (RES) play a crucial role due to their advantages such as pollution-free, abundance, and clean. The schematic diagram of a RES in DC microgrid application is shown in Fig. 1. Among RES, photovoltaic and fuel cells are extensively used due to their compatibility and reliability [1], [2], [3]. Generally, PV cells generate low voltage, and this voltage is not adequate for grid-connected inverters. It is more difficult to manage high voltage when multiple cells are connected in series, and the cost of installation is also significantly higher [4], [5]. For grid-tied as well as standalone systems, an ultra-high step-up boost converter is mandatory to step up available low-voltage to a common DC link voltage. From the literature, the conventional boost converter (CBC) has the following limitations majorly [6], [7].

The associate editor coordinating the review of this manuscript and approving it for publication was Kan Liu.

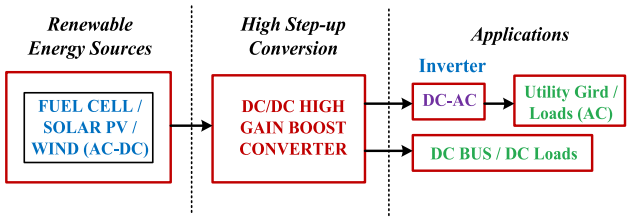


**FIGURE 1.** General schematic of RES.

1) Extreme duty cycle is needed, which leads to conduction losses of the converter.
2) It has no control over input current. At high duty cycle, it draws large current from the source which can damage converter components.
3) Switch and diode voltage stresses are equal to the output voltage. As a result, the rating of the components is high and their cost increases.
4) The components with high on-state resistance create losses in the converter and reduce the efficiency.
5) Reverse recovery issue is experienced by the diodes. It reduces the switching speed and rating of the converter further.
6) The voltage gain is limited due to lack of coupled inductor, voltage multipliers and passive clamp circuit.

Several converters are listed in the literature for the gain improvement of converters. In these converters, the CBC is integrated with various voltage boosting methodologies such as switched capacitor (SC) [8], [9], [10], switched inductor (SI) [11], [12], active network (AN) based SC [13], active network (AN) based SI [14], and AN based SI and SC for the improvement of gain [15]. Later, coupled inductor (CI) based boost converters are developed. This coupled inductor is highly efficient and capable to generate a high gain by the increment of turns ratio [16]. However, the leakage inductance of CI creates high voltage spikes over the semiconductor switches which leads to considerable power losses. This can be avoided by using clamping circuits such as diode clamp [17], passive clamp [18], and active clamp [19], [20] circuits. Clamp circuits can also improve the gain, by recycling the energy leakage of CI. This leakage energy helps to mitigate the reverse recovery issue of diodes.

In [21] and [22], the voltage multiplier is merged with CI-based BC to lift the gain of the converter. In this active clamp is used for recycling energy and alleviating spikes of switching devices. Apart from this, the power switch and auxiliary switch are operated at zero voltage switching. With this, supplementary switch causes extra conduction losses and increase components count. It leads to high costs and complexity of the converter. In [11] and [23] switched capacitor is combined along with coupled inductor-based boost converter towards enhance the gain further. Here, a passive clamp is used to mitigate voltage spikes and recycle leakage energy. These converters have a high ripple of input current. In [24], voltage multiplier and SC boosting methods are implemented in a non-isolated converter. Here, the switch is operating at zero current switching. The major drawback is that the SC cells are increased for gain enhancement. In [25] is also coupled inductor integrated with a voltage multiplier to rise the value of gain. Also, the passive clamp is used to realize soft switching condition which minimizes the cost, improve efficiency and reduce the complexity. The above-mentioned converters can provide higher gain at a lower duty ratio with reduced switch stresses at maximum rating. However, the major drawback is high pulsating input current causes malfunction of protection systems and restricted to limited rating. Thus, the interleaved configuration is implemented to minimize the ripple of input current. In [20], [26], [27], and [28] interleaved converter with coupled inductors is proposed, it has lower input current ripples at high gain. Here, the switches are operated under hard switching. In [29], interleaved converter combined with voltage multiplier and coupled inductors and operate under zero-current switching (ZCS). With this, it provides low input current ripples, lesser switch current and stress. However, lower gain and high components are the major drawbacks. In [30] and [31], zero-voltage switching (ZVS) interleaved converter is proposed, it provides high gain, low switch current, lesser ripple of input, and reduced voltage stress. The major drawback of the aforementioned converter has a greater number of switches which increases complexity of design analysis.

Another solution for providing high gain is a quadratic boost converter. In [32], quadratic boost integrated with coupled inductor and voltage multiplier to lift the voltage gain. Here, the device's stress is equal to the value of the output voltage. In [33], voltage doubler and coupled inductor are combined with a quadratic boost converter to lift the gain. Nevertheless, the stress of devices is remaining unchanged, and the gain increment is also not significant. After considering all the merits and demerits of above-discussed converters, a new converter topology is proposed with the following features.

1) The switched capacitor cell and a coupled inductor incorporated in a quadratic boost converter to get an ultra-high step-up gain converter.
2) The coupled inductor turns ratio further helps to lift the gain of the converter.
3) The inductor at the input side assists in the generation of continuous input current with reduced ripple content hence rating increases.
4) Passive clamp is employed to diminish the switch voltage spikes, which decreases the conduction loss and cost of the switching device.
5) Clamp circuit reclaims the energy leakage of the coupled inductor, which aids in to increment of gain as well as the power density of the converter.
6) Furthermore, the reverse recovery issue of the output diode is successfully resolved by the inclusion of the CI leakage inductance component.

The remaining sections in the article are arranged as follows. Section II provides a description and operating principle

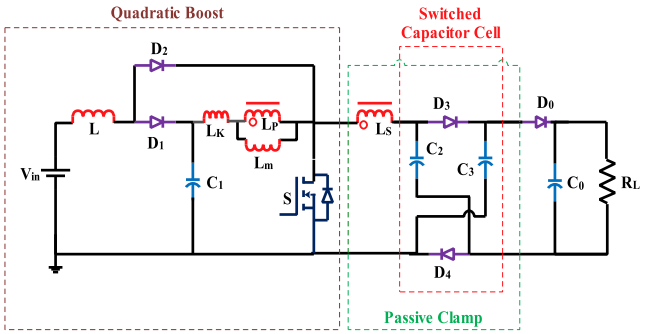


**FIGURE 2.** Proposed single-switch quadratic high step-up converter circuit.

of the proposed converter. Performance analysis is given in Section III. Details regarding design constraints are elaborated in Section IV. Section V represents experimental results and efficiency estimation. Performance comparison among proposed and existing converters is discussed in Section VI. Finally, Section VII gives conclusions.

## II. OPERATING PRINCIPLE AND MODES OF THE PROPOSED CONVERTER

Fig. 2 illustrates the proposed single-switch quadratic high step-up converter circuit. It is mainly composed of a quadratic boost, switched capacitor cell, and a coupled inductor (CI). The magnetizing and leakage inductances ($L_m$, $L_k$) along with turns ratio ($n$) are equivalent to CI. The quadratic boost is formed by MOSFET switch $S$, diodes $D_1$, and $D_2$, input inductor $L$, capacitor $C_1$, and primary of CI. The capacitors $C_2$, $C_3$, and diodes $D_3$, $D_4$ built switched cell. Switched capacitor cell and secondary of CI together form a passive clamp, which provides less voltage spikes of the switch and recycles energy leakage of CI to achieve zero current switching to turn OFF the diodes.

The detailed working of a converter can be explained in two modes, and its corresponding key waveforms are presented in Fig. 3. The relevant equivalent circuit for each mode is presented in Fig. 4.

**Mode 1 [$t_0$-$t_1$]:** At time t = $t_0$, the switch $S$ is turn ON, and the inductor current starts to increase gradually. Also, the CI is starts to energize by the capacitor $C_1$. Whereas, the CI secondary and switched capacitors $C_2$, $C_3$ are discharging energy to load through the diode $D_0$. The diodes $D_1$, $D_3$, and $D_4$ experience reverse voltage and they are in reverse bias.

**Mode 2 [$t_1$-$t_2$]:** At time t = $t_1$, the switch $S$ is turned OFF. The diodes $D_0$, and $D_2$ are in reverse bias due to reverse voltage. Both input and coupled inductors along with supply start to energies the capacitors $C_2$ and $C_3$. In this mode, diodes $D_1$, $D_3$, and $D_4$ are in forward bias. The output capacitor supplies to the load. The same analysis repeats for every cycle.

## III. PERFORMANCE ANALYSIS

The mathematical equations of the proposed converter under steady state conditions are derived by making the following assumptions.

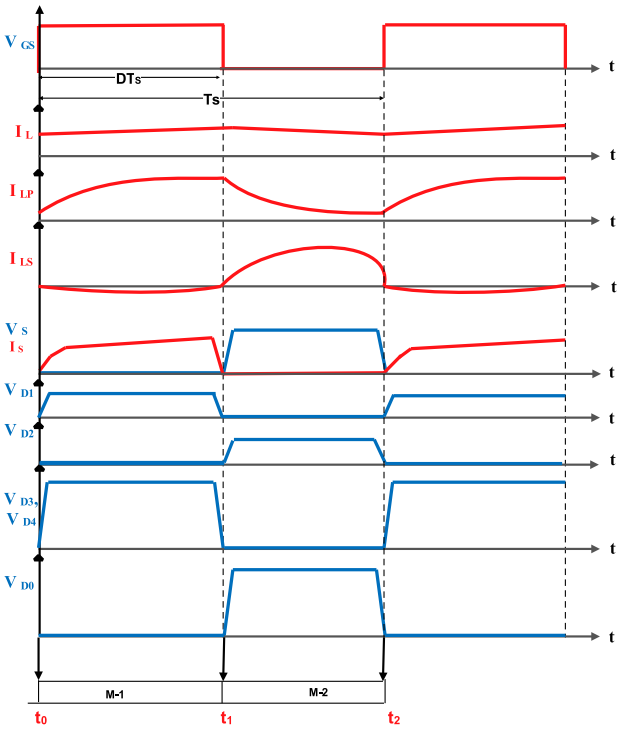


**FIGURE 3.** Key waveforms.

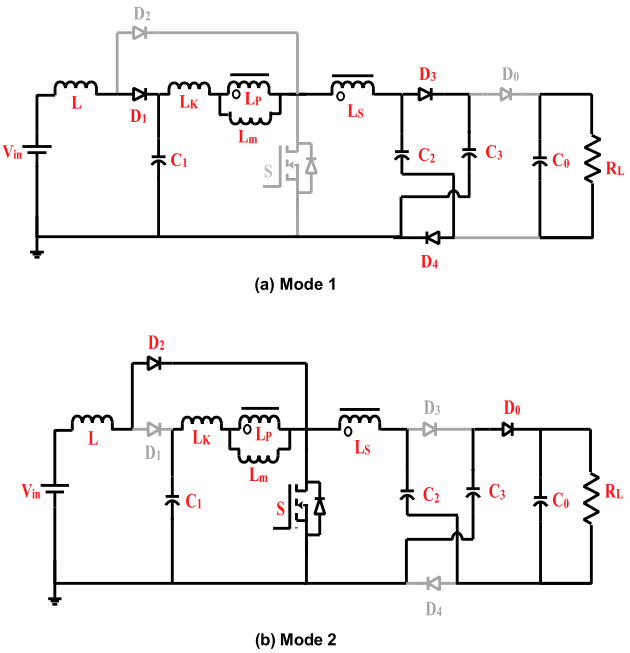


**FIGURE 4.** Equivalent circuit for each mode of operation.

1) All components and semiconductor elements are ideal.
2) Continuous conduction mode (CCM) of operation.
3) The rating of capacitors is adequately large to sustain constant voltage.

### A. STEP-UP GAIN DERIVATION

In mode 1, both the input inductor and primary of CI are energized by the supply and capacitor C1, respectively. The

expressions for input and magnetizing inductor voltages are given below.

$$V_L\,(on) = V_{in} \tag{1}$$
$$V_{Lp}\,(on) = kV_{C1} \tag{2}$$
$$V_0 = V_{C2} + V_{C3} + NV_{C1} \tag{3}$$

Here, $k$ represents the CI coefficient of coupling.

$$k = \frac{L_m}{L_k + L_m} \tag{4}$$

In mode 2, the voltage across the inductors are given below.

$$V_L\,(off) = V_{C1} - V_{in} \tag{5}$$
$$V_{Lp}\,(off) = \frac{k\,(V_2 - V_C)}{(1 + Nk)} \tag{6}$$

After solving, equations (1) and (5), the voltage across capacitor C1 is obtained and is given below.

$$V_{C1} = \frac{V_{in}}{(1\text{-D})} \tag{7}$$

After solving, equations (2), and (6), the voltage across capacitors $C_2$, $C_3$ are obtained, which are same and is given below.

$$V_{C2} = V_{C3} = \frac{(1+NkD)V_{in}}{(1-D)^2} \tag{8}$$

From equation (3), the voltage developed across the capacitor $C_0$ is given below.

$$V_{C0} = \frac{(2+N + 2DNk - ND)V_{in}}{(1-D)^2} \tag{9}$$

Thus, the gain (M) of the converter is obtained and is given below.

$$M = \frac{(2 + N + 2DNk - ND)}{(1 - D)^2} \tag{10}$$

The above equation includes the leakage inductance effect. The gain equation can be simplified with k=1 (neglecting $L_k$ effect).

$$M = \frac{(2 + N + ND)}{(1 - D)^2} \tag{11}$$

The equation (11) affirms that the suggested converter achieves a substantial step-up gain without requiring an excessively high duty ratio. Fig. 5 illustrates the relationship between voltage gain (M), turns ratio (N), and duty ratio (D). From the figure, with a turn's ratio of $N = 2$, the converter achieves a voltage gain of 20 when operating at a duty cycle close to 0.5. It shows the superiority of the proposed converter.

### B. SEMICONDUCTOR STRESSES

The MOSFET voltage stress can be derived from mode 2, the expression for this parameter is given below.

$$V_S = \frac{V_{in}}{(1 - D)^2} = \frac{V_0}{(2 + N + ND)} \tag{12}$$

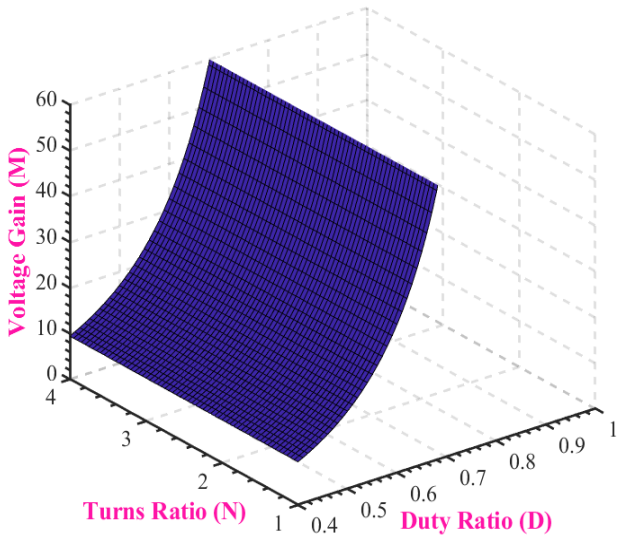


**FIGURE 5.** Proposed converter voltage gain vs. turns ratio vs. duty ratio.

The voltage stress ($V_S$) on the switch is expressed in terms of input voltage ($V_{in}$) and duty ratio ($D$) as well as output voltage ($V_o$), duty ratio ($D$), and turns ratio ($N$). The equation (12) confirms that low voltage rating of MOSFET switches with low $R_{ds}$ (on-state) can be used for the proposed converter to reduce cost and conduction losses of the switches. At $N = 2$ and $D = 0.5$, the voltage stress of the switch is computed 20% of the output voltage.

Similarly, equation (13) gives the voltage stress on diode $D_1$, which is equal to $V_{C1}$. Whereas, the stress on diode $D_2$ is given in equation (14).

$$V_{D1} = V_{C1} = \frac{V_{in}}{(1 - D)} = \frac{V_0(1 - D)}{(2 + N + ND)} \tag{13}$$
$$V_{D2} = \frac{V_{in}D}{(1 - D)^2} = \frac{DV_0}{(2 + N + ND)} \tag{14}$$

The voltage stress on diodes $D_3$, $D_4$ are equal and expressed in equation (15), and stress on diode $D_0$ is expressed in equation (16).

$$V_{D3} = V_{D4} = \frac{(1 + N)V_{in}}{(1 - D)^2} = \frac{(1 + N)V_0}{(2 + N + ND)} \tag{15}$$
$$V_{D0} = \frac{(1 + N)V_{in}}{(1 - D)^2} = \frac{(1 + N)V_0}{(2 + N + ND)} \tag{16}$$

Fig. 6 illustrates the normalized stress on various components of converter versus turns ratio. From the figure, it is realized that normalized voltage stress of switch $V_S$, stress on diodes $V_{D1}$, $V_{D2}$ are decreased with increment in turns ratio at $D = 0.5$. Whereas, stress on diodes $V_{D3}$, $V_{D4}$, $V_{D0}$ are increased with increment in turns ratio at $D = 0.5$.

Assume lossless converter, then the input current ($I_{in}$) can be written as given below.

$$I_{in} = \frac{(2 + N + ND)I_0}{(1 - D)^2} \tag{17}$$

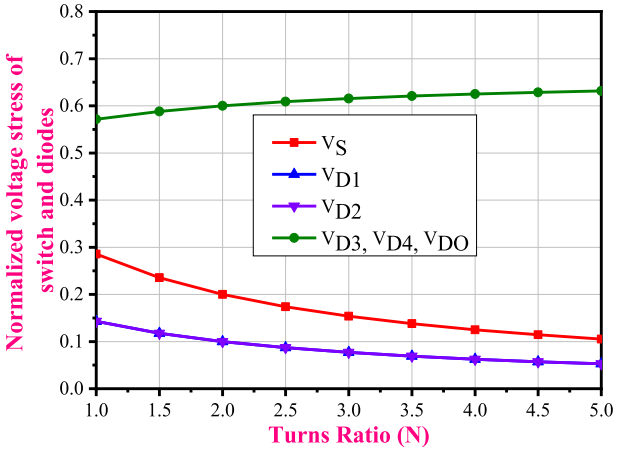


**FIGURE 6.** Normalized voltage stress of switch and diodes vs. turns ratio at $D = 0.5$.

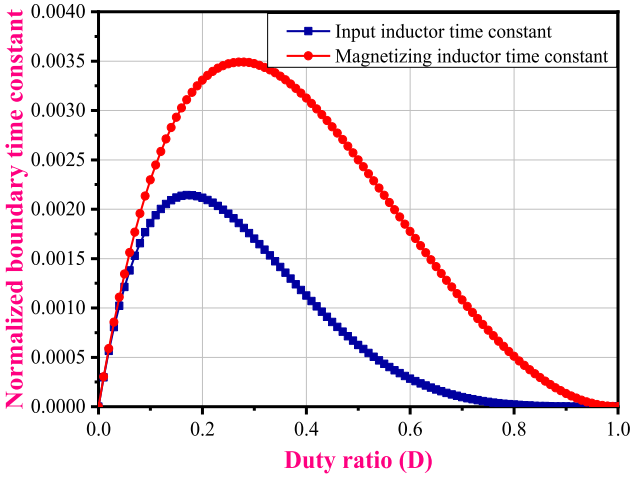


**FIGURE 7.** Normalized boundary time constants of input and coupled inductor vs. duty ratio.

The current stresses on diodes ($I_{D1}$, $I_{D2}$, $I_{D3}$, $I_{D4}$ and $I_{D0}$) are given below.

$$I_{in} = I_{D1} = I_{D2} = \frac{(2+N+ND)I_0}{(1-D)^2} \tag{18}$$

$$I_{D3} = I_{D4} = \frac{I_0}{(1-D)} \tag{19}$$

$$I_{D0}(peak) = \frac{2I_0}{D} \tag{20}$$

### C. BOUNDARY CONDITIONS

The expressions for change in input and magnetizing inductor current ripples are expressed in equation (21) and (22), and relevant maximum conditions are expressed in equation (23) and (24).

$$\Delta I_L = \frac{DV_{in}}{f_s L} \tag{21}$$

$$\Delta I_{Lm} = \frac{DV_{C1}}{f_s L_m} \tag{22}$$

$$I_L(max) = \frac{D(1-D)^2 V_0}{f_s L(2+N+ND)} \tag{23}$$

$$I_{Lm}(max) = \frac{D(1-D)V_0}{f_s L_m(2+N+ND)} \tag{24}$$

Thus, the average value of inductor current is given below.

$$I_L(avg) = \frac{DV_{in}}{2f_s L} \tag{25}$$

After equating equations (23) and (25), the value of output current at the boundary condition is given below.

$$I_{0B} = \frac{D(1-D)^4 V_0}{2f_s L(2+N+ND)^2} \tag{26}$$

The minimum values of input and magnetizing inductances are needed to achieve CCM and is given below.

$$L \geq \frac{(1-D)^4 RD}{2f_s(2+N+ND)^2} \tag{27}$$

$$L_m \geq \frac{D(1-D)^2 R}{2f_s(2+N+ND)^2} \tag{28}$$

The boundary values of inductor time constants ($\tau_{LB}$) are,

$$\tau_{LB} = \frac{L}{RT_s} \tag{29}$$

$$\tau_{LB} = \frac{D(1-D)^4}{2(2+N+ND)^2} \tag{30}$$

$$\tau_{LmB} = \frac{D(1-D)^2}{2(2+N+ND)^2} \tag{31}$$

The normalized boundary time constants of input inductor and coupled inductor versus duty ratio is shown in Fig. 7. At $D = 0.5$, the time constant of input and magnetizing inductors are 0.0006 and 0.0025, respectively.

## IV. DESIGN OF COMPONENTS

### A. SELECTION OF SEMICONDUCTOR COMPONENTS

The rating of semiconductor components such as switch and diodes are selected on the basis of current and voltage stresses experienced across the components. The selected ratings should be more than the calculated values, considering of switching voltage spikes.

### B. SELECTION OF CAPACITORS

The selection of capacitors is predominantly determined by the switching frequency and the magnitude of voltage ripple. The capacitance is expressed in the following equation (33).

$$C = \frac{i_c D}{\%\Delta V_C f_s} \tag{32}$$

The output capacitor with voltage ripple of 0.1% is computed 10.4$\mu$F from equations (33) and (34).

$$C_0 = \frac{I_0 D}{\%\Delta V_0 f_s} \tag{33}$$

**TABLE 1.** Various components and their ratings used in the proposed converter.

| Parameter | Device Type | Rating | Description |
|---|---|---|---|
| Switch S | MOSFET | 200V, 130A, 8.7mΩ | *IRFP4668PbF* |
| Switched capacitors $C_2$, $C_3$ | DC film capacitors | 4.7µF, 450V | *ECWFD2W475J* |
| Input and Coupled inductor cores | EE Cores | 388nH/N$^2$, 90 | *EMS-0552825-090* |
| Diodes $D_0$, $D_1$, $D_2$, $D_3$, $D_4$ | Ultra-fast diodes | 600V, 10A | *BYC 10-600* |
| Switched and output capacitors $C_1$, $C_0$ | Electrolytic capacitors | 47µF, 450V | *EEUEE2W470* |

$$C_0 \geq \frac{0.4 \times 0.52}{0.001 \times 400 \times 50 \times 10^3} = 10.4\mu F \tag{34}$$

The effect of series equivalent resistance is reduced by using two 47 $\mu$F capacitors connected in parallel, and net capacitance is 94 $\mu$F. The circuit capacitors $C_1$, $C_{M1}$, $C_{M2}$ are calculated by considering 5% to 10% of ripple content in the voltage.

$$C_i = \frac{DI_0}{\%\Delta V_{Ci} f_s} \quad where,\ i = 1, M1, M2 \tag{35}$$

The rating of capacitors is higher than the calculated value to account of loss due to equivalent series resistance.

### C. DESIGN OF COUPLED-INDUCTOR (CI)

In proposed converter, the CI is placed at the middle and after the input inductor. Thus, it is not necessary to design with low current ripple. The following is an expression for the magnetizing inductance.

$$L_m = \frac{DV_{C1}}{\delta I_{Lm} f_s} \tag{36}$$

$$L_m = \frac{0.52 \times 41.66}{0.7 \times 6.5 \times 50 \times 10^3} = 95.20\mu H \tag{37}$$

where, $\delta$ is peak to peak ripple content and considered as 70%. The value of computed $L_m$ is 95.20 $\mu$H. Hence, the magnetizing inductance of 100 $\mu$H is chosen by considering the leakage inductance of 2 $\mu$H. To obtain this value in hardware development a sendust core (micrometals) is used to made CI with turns ratio $N = 2$.

### D. INDUCTOR DESIGN

An inductor is placed after the input to minimize input current ripples. The expression for input inductance is given in equation (38).

$$L = \frac{DV_{in}}{\delta I_{in} f_s} \tag{38}$$

$$L = \frac{0.52 \times 20}{0.05 \times 9 \times 50 \times 10^3} = 462.22\mu H \tag{39}$$

where, $\delta$ is peak to peak input current ripples. By considering 5% current ripples and 0.52 duty cycle at 50 kHz switching frequency. The calculated value of inductance is 462.22 $\mu$H. Hence, it is selected as 500 $\mu$H for better performance in hardware development.

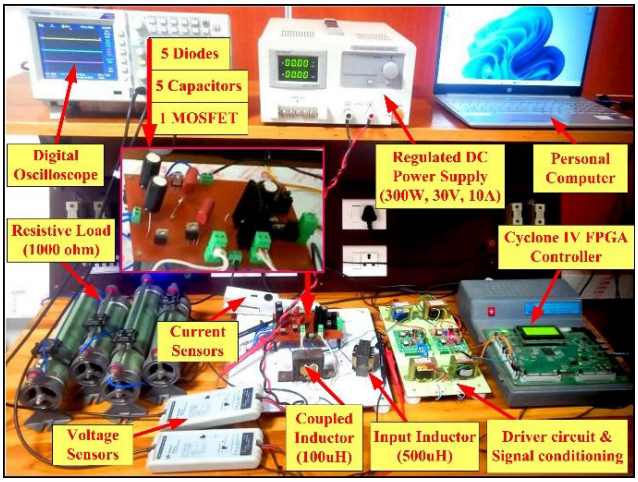


**FIGURE 8.** Prototype experimental setup of proposed converter.

## V. RESULTS AND EFFICIENCY ESTIMATION

Theoretical analysis was used to design a 160 W rating at 50 kHz switching frequency. This was validated through prototype hardware development in a laboratory, with input and output voltages of 20 V and 400 V, respectively. The prototype experimental setup of proposed converter is shown in Fig. 8. The gate signal for the switch is generated using FPGA controller (Intel Cyclone IV evaluation board) and TLP-350 is used for gate driving of power MOSFET to amplify the signal. The 4-channel DSO (Tektronix) is used to record and store the waveforms with the help of differentially voltage and current probes. Other than these, the various components and their ratings used in the proposed converter are presented in Table 1.

Fig. 9 illustrates the DSO captured experimental waveforms of proposed converter. Fig. 9 (a) represents the gate pulse of MOSFET device, input voltage waveform of 20V and the output voltage waveform of 400 V at duty ratio of 0.52. The MOSFET gate pulse along with input inductor and coupled-inductor (primary and secondary) current waveforms are shown in Fig. 9 (b). Fig. 9 (c) shows gate pulse, voltage and current of the switch. The waveforms of voltage across the clamp ($C_C$) and voltage multiplier capacitors ($C_2$, $C_3$) with gate pulse is presented in Fig. 9 (d). Fig. 9(e) represents the waveforms of voltage stress experienced by the diodes ($D_1$, $D_2$) with respect to the pulse of gate. The

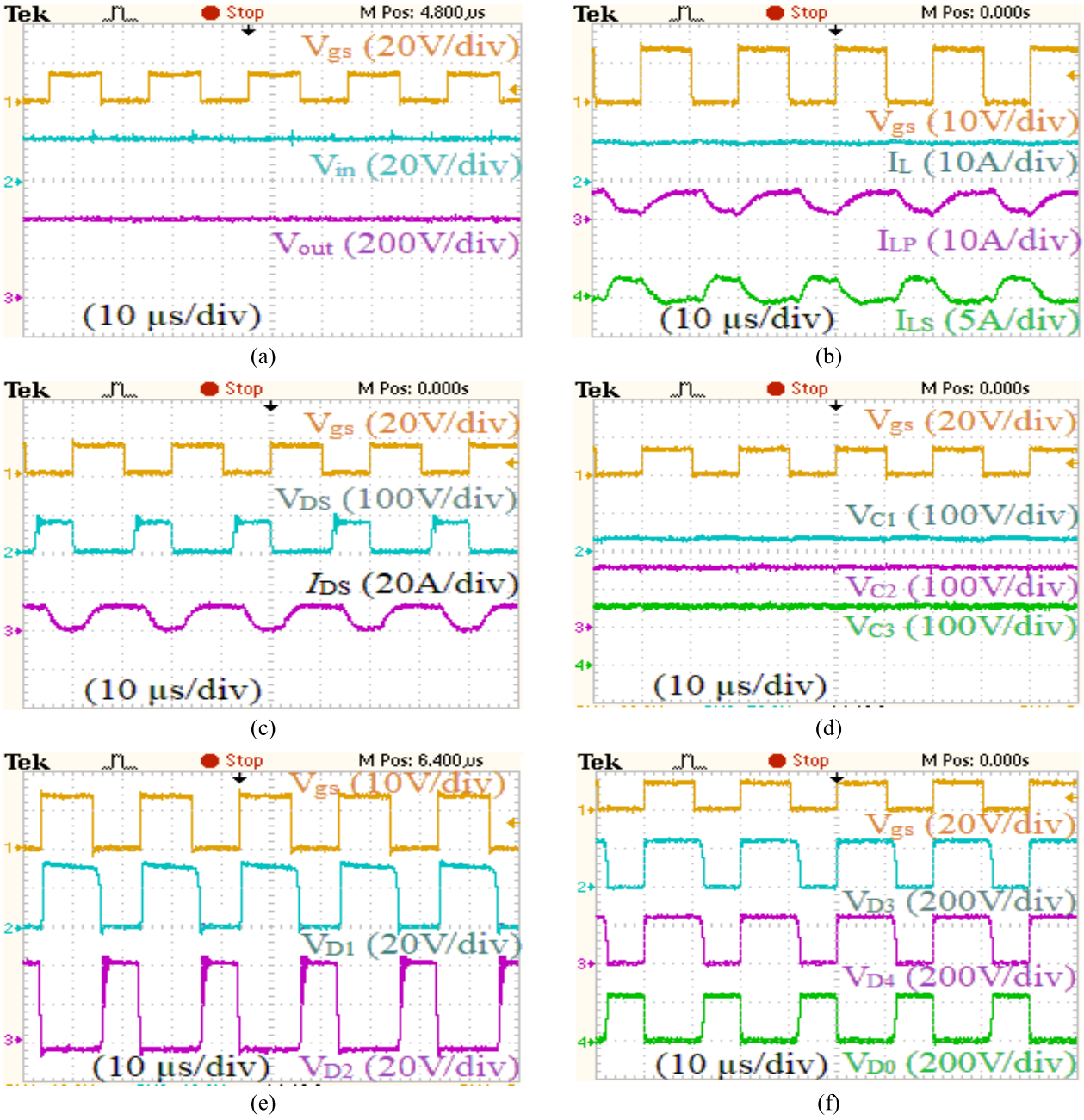


**FIGURE 9.** Experimental results (a) Gate pulse, input and output voltage waveforms, (b) Gate pulse, input inductor, coupled inductor primary and secondary currents waveforms, (c) Gate pulse, voltage and current waveforms of the switch, (d) Gate pulse, voltage across the switched capacitors (*C1, C2, C3*) waveforms, (e) Gate pulse and voltage across the diodes (*D1, D2*) waveforms, (f) Gate pulse and voltage across the diodes (*D3, D4, D0*) waveforms.

waveforms for the voltage stress of the diodes ($D_3$, $D_4$, and $D_0$) with respect to the gate pulse is presented in Fig. 9 (f).

### A. EFFICIENCY ESTIMATION

The proposed converter efficiency is estimated by computing the losses occurred in the various components such switch, diodes, capacitors, and coupled-inductor.

The power loss of switch is computed using equation (40). Equation (41) represents the expression for the power losses occurred in the diodes. The coupled-inductor power and core losses are calculated using equation (42) and (43), respectively. The power losses of capacitors are computed using equation (44).

$$P_{S-loss} = (I_S^2(rms) \times R_{ds}(on)) + P_S(on) + P_S(off) \quad (40)$$

where, $R_{ds}$(on-state) is MOSFET on-state resistance.

$$P_{D-loss} = \sum (I_d^2(rms) \times R_d(on)) + \sum (I_d(avg) \times V_f) \quad (41)$$

**TABLE 2.** Performance comparison of converters.

| Topologies | Quantity of various components | | | | | Expression for voltage gain | Expression for switch stress | Expression for diode stress | Nature of Switching |
|---|---|---|---|---|---|---|---|---|---|
| | *S* | *Di* | *C* | *CI+I* | *TC* | | | | |
| **Ref. [28]** | 2 | 4 | 3 | 2+0 | 12 | $\frac{(1+2N)}{(1-D)}$ | $\frac{V_0}{1+2N}$ | $\frac{2NV_0}{(1+2N)}$ | ZCS |
| **Ref. [29]** | 4 | 2 | 4 | 2+0 | 12 | $\frac{(2+2N)}{(1-D)}$ | $\frac{V_0}{(2+2N)}$ | $V_0$ | ZVS |
| **Ref. [30]** | 4 | 2 | 3 | 2+0 | 11 | $\frac{(2+2N)}{(1-D)}$ | $\frac{V_0}{(2+2N)}$ | $\frac{(2N+1)V_0}{(2N+2)}$ | ZVS |
| **Ref. [31]** | 1 | 5 | 5 | 0+3 | 14 | $\frac{2}{(1-D)^2}$ | $V_0$ | $V_0$ | Hard |
| **Ref. [32]** | 1 | 5 | 4 | 1+1 | 12 | $\frac{(1+N)}{(1-D)^2}$ | $\frac{V_0}{(1+N)}$ | $\frac{NV_0}{(1+N)}$ | Hard |
| **Ref. [33]** | 1 | 4 | 3 | 1+1 | 10 | $\frac{(1+ND)}{(1-D)^2}$ | $\frac{V_0}{(1+ND)}$ | $\frac{NDV_0}{(1+ND)}$ | Hard |
| **Ref. [34]** | 1 | 6 | 5 | 1+1 | 14 | $\frac{N(3D+2)+(2-D)}{2(1-D)^2}$ | $\frac{(2+D(N-1))V_0}{N(2+3D)+(2-D)}$ | $\frac{2NV_0}{N(2+3D)+(2-D)}$ | Hard |
| **Ref. [35]** | 1 | 6 | 5 | 1+1 | 14 | $\frac{(1+N+ND)}{(1-D)^2}$ | $\frac{V_0}{(1+N+ND)}$ | $\frac{NV_0}{(1+N+ND)}$ | Hard |
| **Ref. [36]** | 3 | 3 | 4 | 2+0 | 12 | $\frac{2(2D_1+D_2)}{(1-D_1-D_2)}$ | $\frac{(1+D_1)V_0}{4(2D_1+D_2)}$ | $\frac{(2-D_2)V_0}{4(2D_1+D_2)}$ | Hard |
| **Ref. [37]** | 2 | 5 | 5 | 0+2 | 14 | $\frac{(4)}{(1-D)}$ | $\frac{V_0}{4}$ | $\frac{V_0}{2}$ | Hard |
| **Ref. [38]** | 3 | 4 | 3 | 1+0 | 11 | $\frac{(3+D_1-D_2)}{(1-D_1-D_2)}$ | $\frac{(1-D_1-D_2)V_0}{(3+D_1-D_2)}$ | $\frac{(-2+D_2)V_0}{(3+D_1-D_2)}$ | Hard |
| **Proposed topology** | 1 | 5 | 4 | 1+1 | 12 | $\frac{(2+N+ND)}{(1-D)^2}$ | $\frac{V_0}{(2+N+ND)}$ | $\frac{(1+N)V_0}{(2+N+ND)}$ | Hard |

Note:- $N$ = Turns ratio, $D$ = Duty ratio, $S$ = Switches, $D_i$ = Diodes, $C$ = Capacitors, $I$ = Inductors, $CI$ = Coupled inductors, $TC$ = Total count.

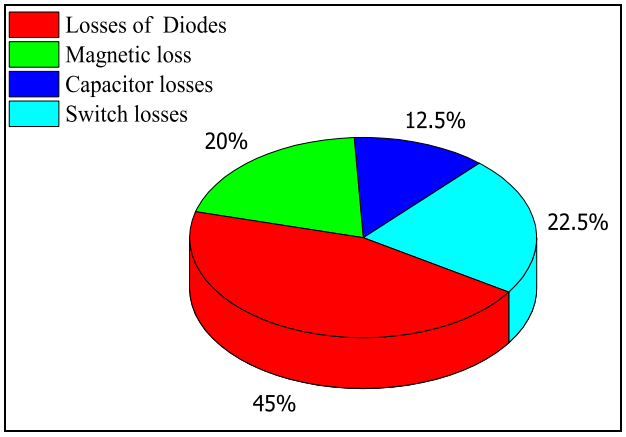


**FIGURE 10.** Power loss distribution of converter.

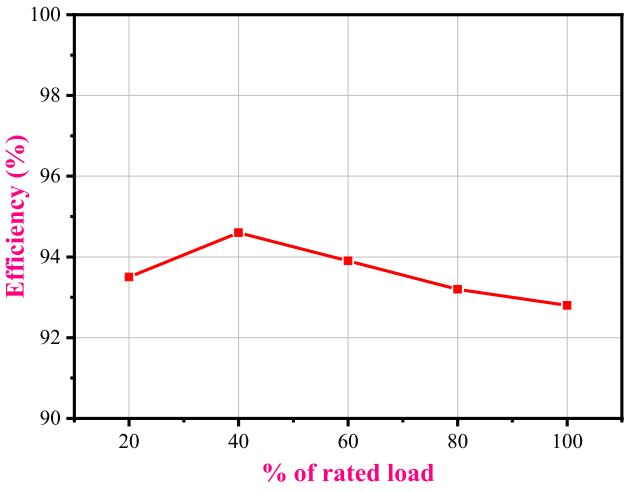


**FIGURE 11.** Efficiency vs. % of rated load.

where, $V_f$ is forward voltage across diode.

$$P_{CI-power} = \left(I_{LP}^2\,(rms) \times r_p\right) + \left(I_{LS}^2\,(rms) \times r_s\right) \quad (42)$$

where, $r_p$, $r_s$ are primary and secondary resistances of coupled-inductor.

$$P_{CI-core} = k \times A_c \times l_c \times B_{max}^{\beta} \times f^{\alpha} \quad (43)$$

where, $l_c$, $B_{max}$, $A_c$ are mean length, maximum flux density, and cross-sectional area of core, respectively. $\alpha$, $\beta$ and $k$ are constants.

$$P_{C-loss} = (I_C^2(rms) * r_c) \quad (44)$$

where, $r_c$ is capacitor's series equivalent resistance.

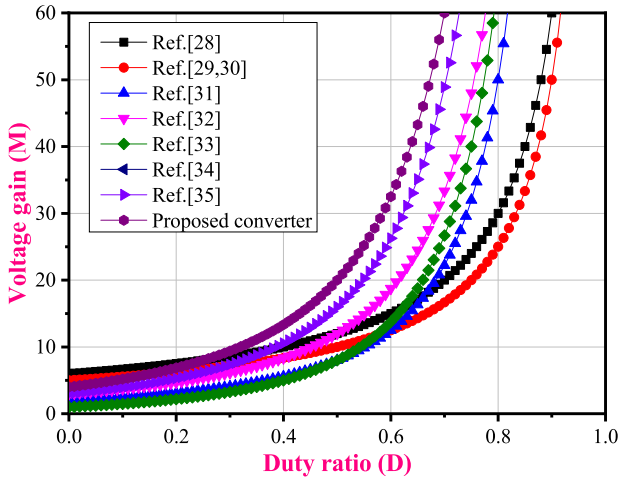


**FIGURE 12.** Voltage gain comparison.

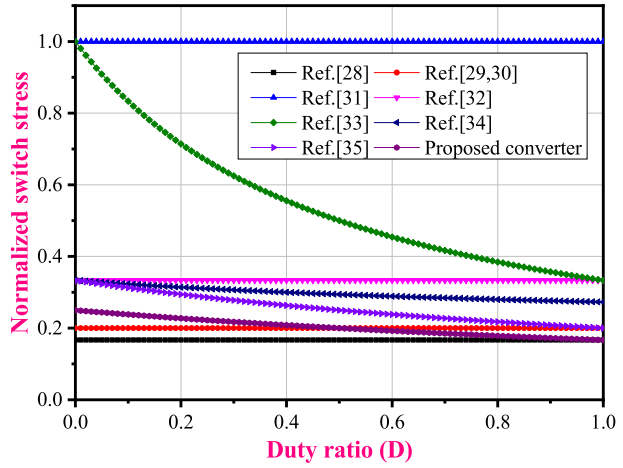


**FIGURE 13.** Normalized switch stress comparison.

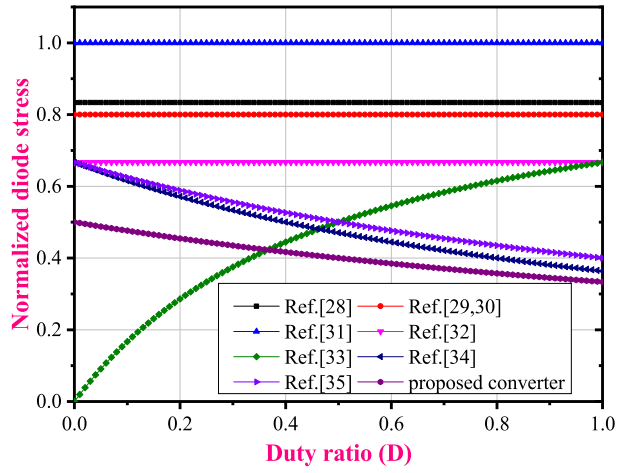


**FIGURE 14.** Normalized diode stress comparison.

Thus, the efficiency of proposed converter is estimated using equation (45).

$$Efficiency = \frac{P_0}{P_0+P_S+P_D+P_{CI}+P_C} \tag{45}$$

The distribution of power loss among the various components of proposed converter is presented in Fig. 10. The major portion of losses is constituted by diodes, while the least portion is constituted by capacitors.

Therefore, the full load efficiency of converter at 160 W is 92.48%. The efficiency curve for different percentages of rated loads is shown in Fig. 11. The converter achieves its highest efficiency when operating at nearly 40% of its rated load.

## VI. PERFORMANCE COMPARISON

Table 2 shows the comparison of proposed converter with existing converters in literature in terms of quantity of various components, voltage gain, stress of switch and diodes. Fig. 12 represents the voltage gain comparison of proposed converter with others mentioned in literature. Finally, the proposed converter provides high gain in the wide range of operating duty cycle.

Normalized switch stress comparison of converters is shown in the Fig. 13. Except [28] remaining converters are more switch stress compared to proposed converter. Fig. 14 represents normalized diode stress comparison of converters. Proposed converter provides lower diode stress for wide range of operating duty cycle compared to other converters. However, the proposed converter provides high gain with least switch and diodes stress. It shows superiority of proposed converter in various aspects for real-time implementation.

## VII. CONCLUSION

This paper has been presented a quadratic boost converter with switched capacitor cell and coupled-inductor. An ultra-high step-up gain is achieved with help of switched capacitor cell and turns ratio of coupled inductor. Continuous input current and minimization of input current ripples are achieved through an input inductor. Most importantly, the proposed converter is used single switch to reduce the complexity of the control circuit. Passive clamp circuit mitigate the voltage spikes across the switching device. As a result, the switch stress is significantly reduced to 20% of the output voltage at $N = 2$, and $D = 0.5$. Thus, it reduces the rating, cost, conduction losses of switch and increases the efficiency of the converter effectively. The maximum voltage stress of diode is also reduced to 60% of the output voltage. Further, efficiency enhancement and reduction of reverse recovery problem in diodes are achieved by recycling the energy leakage of coupled inductor to the output capacitor. The proposed converter description, steady-state analysis, and merits in comparison to other related converters have been extensively discussed. Further, a prototype of 160 W proposed converter with input voltage 20 V and output voltage 400 V is developed, and peak efficiency of 94.8% is achieved. This feature makes the proposed converter is more suitable for high step-up converter for DC microgrid applications.

## ACKNOWLEDGMENT

S. Thangavel and D. V. Sudarsan Reddy, a modified high-gain quadratic dc–dc converter with switched capacitor cell and coupled-inductor for photovoltaic applications. Patent

number (IN, Patent application number: 202341015468), date of filing (08/03/2023), and issued date of publication (26/05/2023).

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