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RESEARCH ARTICLE

Blocker-Tolerant Broadband CMOS Low-Noise Amplifier Employing N-Path Filter-Based Load

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ABSTRACT This study proposes a broadband complementary metal-oxide semiconductor (CMOS) low-noise amplifier (LNA) with intrinsic band-selective out-of-band (OB) blocker rejection capabilities. The proposed LNA design utilizes a differential four-phase N-path filter as the amplifier load to offer a substantial total load impedance difference between the in-band (IB) and OB frequency bands. This ensures that the LNA design securely accomplishes a high-quality-factor frequency selectivity response with lower radio frequency signal losses and its OB rejection performance is maintained against process, voltage, and temperature variations, compared with the case of using the N-path filter as a signal path. To validate its blocker-tolerable performance, the designed LNA was fabricated using a 65-nm CMOS technology and was primarily characterized in the frequency division duplexing bands of the long-term evolution and fifth-generation new radio standards, spanning from 1.7 to 2.7 GHz. The implemented design consistently achieved a transmitter leakage rejection greater than 17 dB across all target frequency bands from several samples. Furthermore, the design attained IB voltage gains greater than 36.4 dB and 40.4 dB, noise figures (NFs) of 1.78 dB and 1.5 dB, OB input 1-dB compression point greater than –27.0 dBm and –26.7 dBm, and full-/half-duplexing OB input-referred third-order intercept points greater than 4.1/3.8 dBm and 4.8/5.0 dBm at the mid- and high-bands, respectively. The OB-induced NF degradation was maintained at less than 0.7 dB. A total bias current of 37.7 mA was required with a nominal supply voltage of 1.2 V. The occupied active area of the implemented design was approximately 0.77 mm^2, excluding the bonding pads and input/output cells.

INDEX TERMS Broadband, cellular, CMOS, fifth-generation (5G) new radio (NR), long-term evolution (LTE), low-noise amplifier (LNA), N-path filter, out-of-band (OB) blocker, wideband.

I. INTRODUCTION

Recently, in the rapidly evolving landscape of wireless communication networks, the demand for high-speed broadband connectivity has surged to realize low-cost high-performance solutions. Therefore, related technological advances have led to the convergence of wireless communication systems, enabling the support of multiple standards on a single platform. This is particularly evident in cellular applications, where front-end modules (FEMs) and transceiver blocks have been co-designed to support a wide frequency range (specifically, sub-6 GHz bands) for long-term evolution (LTE) and fifth-generation (5G) new radio (NR) standards. The emergence of LTE and 5G NR networks fostered an era of unparalleled connectivity, enabling a diverse array of applications ranging from augmented reality to the Internet of Things (IoT) [1], [2]. However, this evolution has brought forth new challenges with respect to signal interference, particularly in

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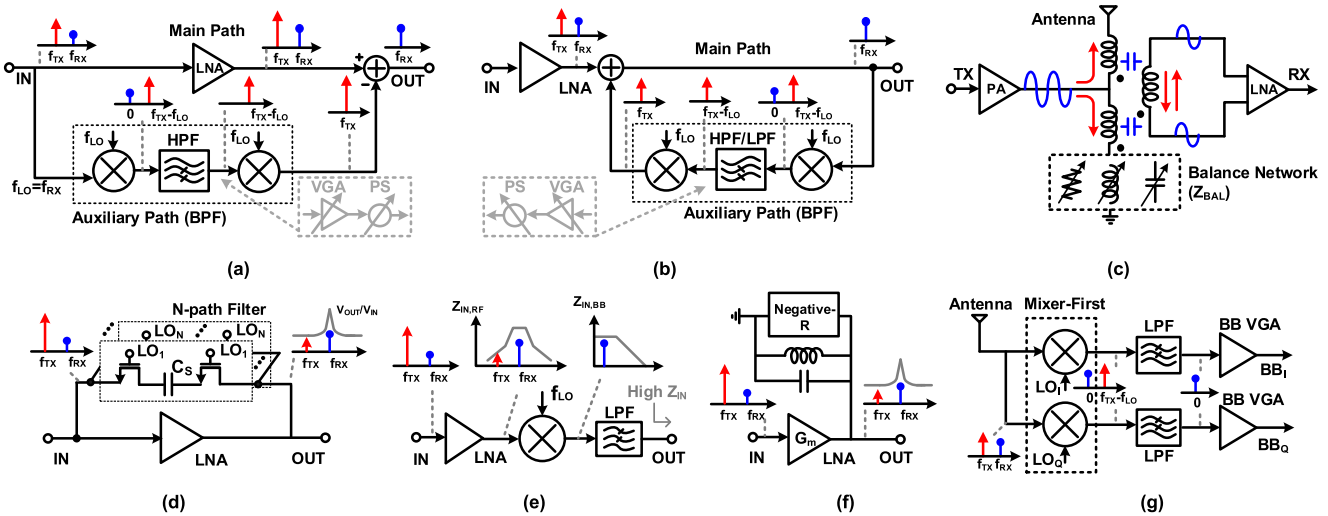

FIGURE 1. OB blocker rejection approaches with respect to TX leakage with; (a) FF-based active blocker cancellation [4], [5], [6], [7], [8], [9], (b) FB-based active blocker cancellation [9], [10], (c) an EBD integrating with a hybrid transformer [11], [12], [13], [14], [15], [16], [17], (d) a N-path filter-based FB loop [18], [19], [20], [21], [22], [23], [24], [25], [26], [27], [28], (e) a frequency-translated impedance property [29], [30], [31], [32], (f) a negative-R load [17], [33], [34], and (g) a mixer-first architecture [35], [36], [37].

the presence of out-of-band (OB) blockers. To ensure reliable multistandard and multiband operations, broadband receiver (RX) front-end (FE) designs should effectively manage complex OB blocker scenarios while minimally compromising gain, noise, and power consumption performance. Applying preceding radio frequency (RF) filtering to the RX FE side indeed improves the overall linearity performance and lowers the design requirements of the subsequent stages. Specifically, in high-end platforms, the utilization of a broadband or band-switchable FEMs combined with low-noise amplifiers (LNAs), power amplifiers, and duplexer filters has gained popularity in reducing the RF FE complexity [3]. However, the sizes of these types of FEMs have become comparable to or larger than those of the main transceiver at a higher cost. Thus, to alleviate this dependency on bulky and expensive FEMs, all or part of RF filtering must be executed within the RF RX path of the transceiver design.

Previous studies have explored various architectures and related circuit techniques for configuring a blocker-tolerant RX FE capable of handling strong OB blockers, such as a transmitter (TX) leakage, across a wide frequency range [4], [5], [6], [7], [8], [9], [10], [11], [12], [13], [14], [15], [16], [17], [18], [19], [20], [21], [22], [23], [24], [25], [26], [27], [28], [29], [30], [31], [32], [33], [34], [35], [36], [37]. These approaches generally aim to suppress undesirable OB blockers at the input of the RX path by combining out-of-phase blockers each other to cancel [4], [5], [6], [7], [8], [9], [10], [11], [12], [13], [14], [15], [16], [17] or facilitate high-quality-factor (high-Q) band-pass filter (BPF)/band-stop filter (BSF) properties within the design [18], [19], [20], [21], [22], [23], [24], [25], [26], [27], [28], [29], [30], [31], [32], [33], [34], [35], [36], [37]. Fig. 1 illustrates conceptual views of the aforementioned OB blocker-tolerant RX designs for TX leakage, which is considered the most challenging blocker condition in frequency division duplexing (FDD) operation modes. Figs. 1(a) and 1(b) representatively illustrate feedforward (FF)- and feedback (FB)-based active blocker cancellation methods, respectively [4], [5], [6], [7], [8], [9], [10]. In these approaches, the main path of the RX passes both an in-band (IB) RF signal and a TX blocker to the output. In contrast, a parallelly utilized FF/FB auxiliary path, typically consisting of a high-pass filter (HPF), variable-gain amplifier (VGA), a phase shifter (PS), and mixers, solely delivers the replicated TX blocker. Once the amplitudes and phases of the blockers from both paths match well, the output subtraction effectively achieves significant blocker cancellation. However, owing to the explicit vulnerability of path gain and phase mismatches by process, voltage, and temperature (PVT) variations can limit the amount of cancellation. An electrical-balanced duplexer (EBD), along with a hybrid transformer, is a feasible alternative for canceling the TX leakage at the RX input. The basic operation of the EBD is illustrated in Fig. 1(c) [11], [12], [13], [14], [15], [16], [17]. This EBD structure concurrently induces an identical but opposite-phase TX leakage into the differential RX input port by precisely tracking the antenna impedance variation using a balance network (Z_{BAL}). Thus, when the antenna impedance perfectly corresponds with Z_{BAL}, effective blocker cancellation can be achieved. Although a relatively high degree of TX-to-RX isolation ($>$ 60 dB) is ensured, this EBD-based blocker rejection method relies on a complex and bulky balance network design to accommodate a wide range of antenna impedance variations. In addition, owing to the gain and phase dependency on the frequency, blocker cancellation is eventually feasible only for a specific frequency, indicating that an extra calibration process is required to maintain the blocker rejection capability. Unlike the cancellation approaches shown in Figs. 1(a)–(c), a high-Q RF

BPF/BSF can also be realized within the design to suppress OB blockers. A representative N-phase N-path filter, as shown in Fig. 1(d), provides a high-Q BPF/BSF property by precisely manipulating a nonoverlapped N-phase switched scheme [18], [19], [20], [21], [22], [23], [24], [25], [26], [27], [28]. This N-path filter can be applied as either a standalone BPF/BSF in the signal path or as an FB loop in parallel with the LNA to obtain OB blocker rejection with frequency tunability. Nevertheless, the parasitic capacitance and on-resistance of the utilized switches critically cause an RF signal insertion loss through the RF N-path filtering. Figs. 1(e) and 1(f) depict alternate ways to implement a built-in high-Q RF BPF/BSF using the frequency-translated impedance property [29], [30], [31], [32] and negative-resistance (negative-R) load [17], [33], [34], respectively. The mixer in Fig. 1(e) concurrently performes RF signal down-conversion to the baseband (BB) frequency and reverse frequency-translation of the BB impedance ($Z_{IN,BB}$) to the RF so that a low-pass response in the BB freuqency appears at the mixer input as the RF high-Q BPF. The negative-R load in Fig. 1(f) also enhances Q of a combined LC network. However, both approaches require a trade-off between the OB blocker rejection for linearity and the stability in the design. Alternatively, as shown in Fig. 1(g), a passive-type mixer-first architecture provides excellent resilient toward a strong OB blocker with enhanced linearity at the FE side and readily executes its rejection at the BB side [35], [36], [37]. However, noise performance degradation is critical owing to the absense of an LNA; therefore, additional RF amplification is essential from the FEM, albeit an extra cost.

This paper introduces a broadband complementary metal-oxide semiconductor (CMOS) LNA, intrinsically equipped with a band-selective OB blocker rejection capability. In the proposed LNA design, a differential four-phase N-path filter serves as the amplifier load instead of an RF signal path. This N-path filter-based load offers the substantial load impedance and gain difference between IB and OB frequencies by leveraging its switches' on/off states and low-pass filtering response. Consequently, a high-Q frequency selectivity response is securely accomplished with lower RF signal losses and higher robustness of OB rejection performance over PVT variations, compared with the case where the N-path filter is used as a signal path. This blocker-tolerant characteristic of the proposed LNA design was implemented and demonstrated using a 65-nm RF CMOS technology.

The remainder of this paper is organized as follows. Section II briefly outlines the proposed LNA design based on a block diagram and describes its frequency selectivity principle using an N-path filter load. In Section III, specific circuit schematics of the designed LNA blocks are presented, along with performance analyses. Additionally, the robust capability of the OB blocker rejection across PVT variations is emphasized through corner simulations. The experimental results of the implemented LNA are presented in Section IV. Finally, Section V provides the concluding remarks.

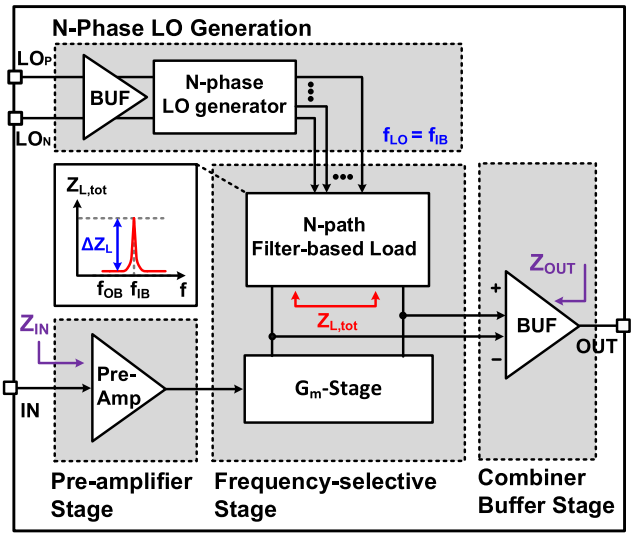

FIGURE 2. Block diagram of the proposed blocker-tolerant broadband LNA, including a low-noise pre-amplifier stage, a N-path filter loaded frequency-selective stage, a combiner buffer stage, and a N-phase LO generation circuitry.

II. PROPOSED BLOCKER-TOLERANT LOW-NOISE AMPLIFIER EMPLOYING N-PATH FILTER LOAD

The block diagram of the proposed blocker-tolerant broadband low-noise LNA design is shown in Fig. 2; it comprises a broadband pre-amplifier stage, an N-path filter-loaded frequency-selective stage, a combiner buffer stage, and an N-phase local oscillator (LO) generation circuitry. First, the primary purpose of the pre-amplifier is to secure broadband solid input matching (Z_{IN}) for multiple operating frequency bands and low-noise characteristics through the preceding RF signal amplification. To minimally impact on the linearity degradation against the strong OB blocker, the blocker resilience of the pre-amplifier is critical in this design. In particular, the removal of this pre-amplifier stage further lowers the linearity requirements of the subsequent stages. However, the achievable gain and noise figure (NF) performance of the design can be limited. The second frequency-selective stage, featuring the N-path filter-based load, is practically responsible for providing a high-Q BPF response according to the load impedance difference (ΔZ_L) between IB and OB frequencies. The differential outputs from the frequency-selective stage can eventually be combined to the single-ended output at the combiner buffer stage under broadband output impedance (Z_{OUT}) matching conditions. To operate the N-path filter appropriately, an N-phase LO generator is used, where its frequency (f_{LO}) is set to the IB frequency (f_{IB}) ($f_{LO} = f_{IB}$).

The primary characteristic of the N-phase N-path filter in the frequency-selective stage as the load is its inherent ability to provide high-Q frequency filtering or impedance translation properties through N-phase switched capacitor operation. Fig. 3(a) shows a simplified schematic of a conventional single-ended N-phase N-path filter, typically configured with series capacitors ($C_{S,1}$–$C_{S,N}$) and N-phase LO-driven switches ($M_{SW,1}$–$M_{SW,N}$). From the above

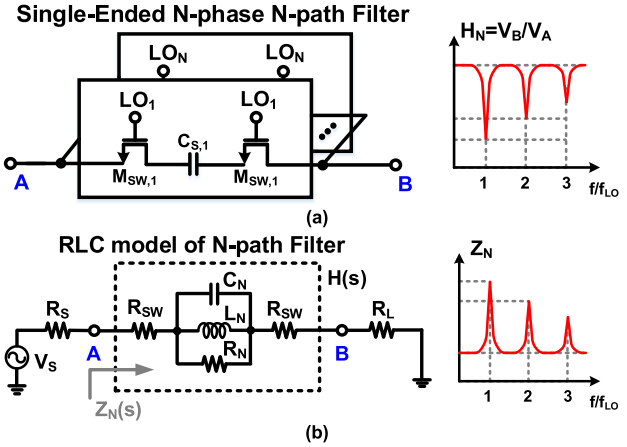

FIGURE 3. A single-ended N-phase N-path filter; (a) simplified schematic and (b) equivalent circuit model including R_S and R_L.

structure, a comb-type notch filtering characteristic is explicitly observed at the harmonics of f_{LO} in the transfer function ($H_N = V_B/V_A$) (Fig. 3(a)). According to [20], [22], and [24], this N-phase N-path filter can be approximated as a simple parallel RLC equivalent model at f_{LO}, as shown in Fig. 3(b). Its equivalent values of the RLC components (R_N, C_N, and L_N) are expressed as follows:

$$R_N = \frac{N^2 \sin^2(\pi/N)}{\pi^2 - N^2 \sin^2(\pi/N)} \cdot (R_{SW} + R_S + R_L) \quad (1)$$

$$C_N = \frac{\pi^2}{2N \sin^2(\pi/N)} \cdot C_{S,X} \quad (2)$$

$$L_N = \frac{1}{(2\pi f_{LO})^2 C_N} \quad (3)$$

where N is the number of non-overlapping LO phases and R_{SW} is the on-resistance of the switch ($M_{SW,X}$). R_S and R_L denote the source and load resistances, applied at the input and output of the equivalent N-path filter model, respectively. Interestingly, as noticed from the Fig. 3(b) and (1)–(3), the input impedance looking into the N-path filter at node A also represents the peak values at the harmonics of f_{LO}, which are mainly given by the impedance translation property of the filter. Therefore, the corresponding transfer function ($H_N(s)$) and input impedance ($Z_N(s)$) of the N-phase N-path filter over the frequency can be calculated as follows:

$$H_N(s) = \frac{V_B(s)}{V_A(s)} = \frac{R_L}{2R_{SW} + R_L + R_N || sL_N || 1/sC_N} \quad (4)$$

$$Z_N(s) = 2R_{SW} + R_L + R_N || sL_N || 1/sC_N \quad (5)$$

When $f_{LO} = f_{IB} = 1/(2\pi\sqrt{L_N C_N})$ and $|f_{IB} - f_{OB}| \gg 0$ are set, the relative transfer function ($H_N(j\omega_{IB})$ / $H_N(j\omega_{OB})$) of the N-path filter between IB and OB frequencies can be derived as follows:

$$\frac{H_N(j\omega_{IB})}{H_N(j\omega_{OB})} = \frac{V_B/V_A|_{OB}}{V_B/V_A|_{IB}} \cong \frac{R_L/(2R_{SW} + R_L + R_N)}{R_L/(2R_{SW} + R_L)} \quad (6)$$

$$= \frac{2R_{SW} + R_L}{2R_{SW} + R_L + R_N} \quad (7)$$

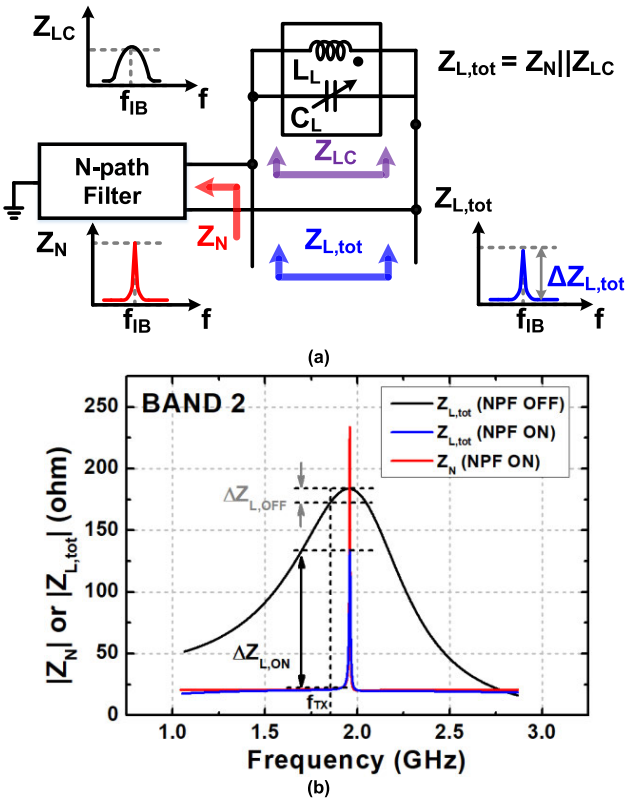

FIGURE 4. (a) Block diagram of the proposed N-phase N-path filter load, along with LC tank and (b) simulated $Z_{L,tot}$ and Z_N with the enabled/disabled N-path filter (NPF).

As readily seen from (6) and (7), when $R_N \gg R_L$ and R_{SW}, the notch depth of its BSF response can be maximized through the largest relative transfer gain. Similarly, the N-path filter translates the frequency-dependent load impedance to the node A with respect to f_{LO}. From the equivalent RLC model shown in Fig. 3(b), the relative input impedance ($Z_N(j\omega_{IB})$ / $Z_N(j\omega_{OB})$) between the IB and OB frequencies can also be obtained by

$$\frac{Z_N(j\omega_{IB})}{Z_N(j\omega_{OB})} \cong \frac{2R_{SW} + R_L + R_N}{2R_{SW} + R_L} = 1 + \frac{R_N}{2R_{SW} + R_L} \quad (8)$$

According to (8), a larger R_N and smaller R_{SW} or R_L surely entail higher Z_N distinction between the IB and OB frequencies. For example, with R_N ($N = 4$), R_{SW}, and R_L of 256.7 Ω, 10 Ω, and 0 Ω, the evaluated relative input impedance is approximately 13.8 (22.8 dB).

The N-path filter can be effectively utilized as part of the load at the frequency-selective stage by employing the aforementioned IB and OB impedance transition properties. This implies that an IB RF signal current from a transconductance (G_m)-stage can be selectively converted to a voltage with a higher gain at the load than OB blockers; hence, IB signal frequency selectivity is ultimately accomplished. Fig. 4(a) shows the parallel configuration of the N-path filter and LC loads (L_L and C_L). The utilized LC load provides a parallel load (Z_{LC}) under resonant conditions with reserving voltage

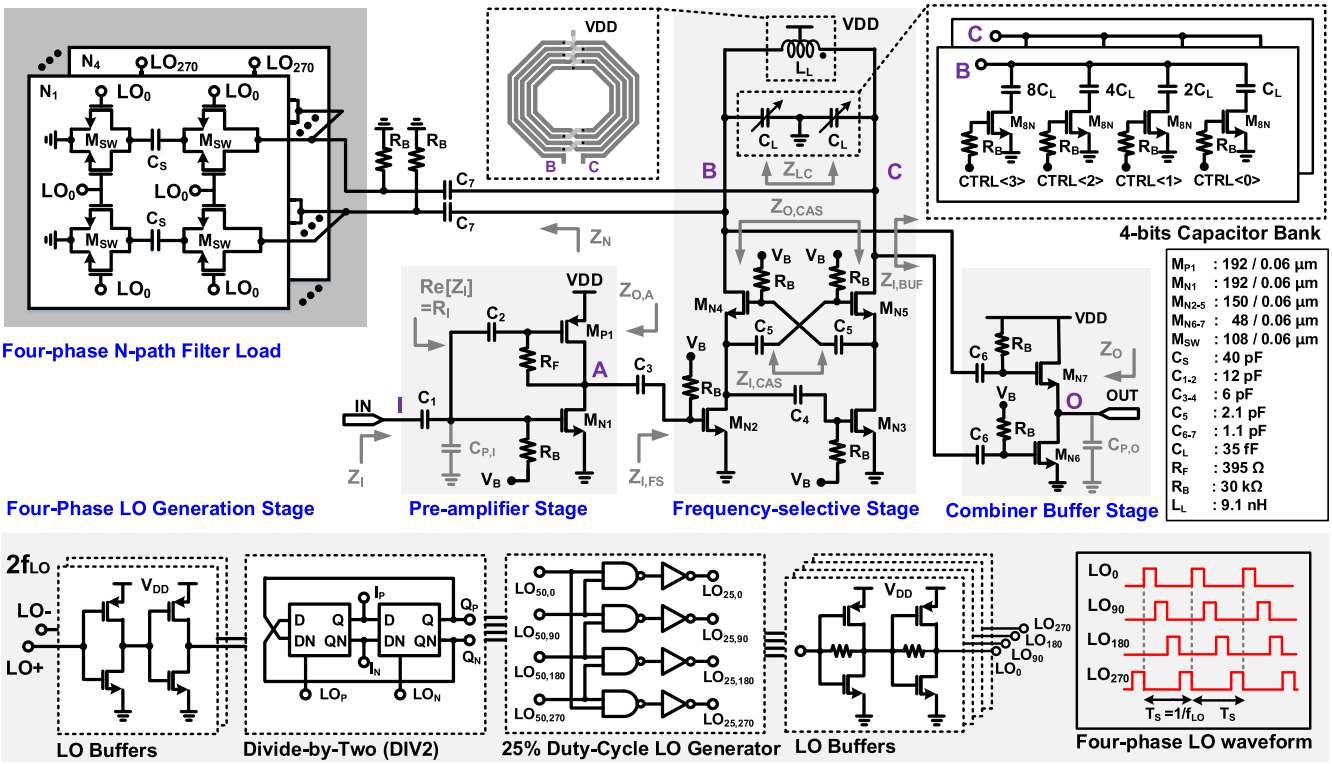

FIGURE 5. Schematic of the proposed blocker-tolerant LNA employing N-path filter.

headroom. In this configuration, the total load impedance ($Z_{L,tot}$) of the frequency-selective stages is given by

$$Z_{L,tot}\,(s) = Z_N\,(s)\,||Z_{LC}\,(s) \tag{9}$$

To optimize its blocker rejection capability, the $Z_{L,tot}$ difference ($\Delta Z_{L,tot}$) between IB and OB frequencies should be maximized. For analogous conditions of $f_{IB} = 1/(2\pi\sqrt{L_N C_N}) = 1/(2\pi\sqrt{L_L C_L})$, the $Z_{L,tot}$ at f_{IB} and f_{OB} can also be determined by

$$Z_{L,tot}\,(j\omega_{IB}) \cong (2R_{SW} + R_L + R_N)\,||Q_L^2 R_{LS} \tag{10}$$

$$Z_{L,tot}\,(j\omega_{OB}) \cong 2R_{SW}||\left[j\omega_{OB}L_L \Big/ \left(1 - \omega_{OB}^2 L_L C_L\right)\right] \cong 0 \;\text{ for } |f_{IB} - f_{OB}| \gg 0 \tag{11}$$

where R_{LS} and Q_L denote the parasitic series resistance and the Q value of the load inductor (L_L). Similarly, assuming $R_N \gg R_L$ and R_{SW}, the $Z_{L,tot}$ at f_{IB} and f_{OB} can be simplified to $R_N \;||\; Q_L^2 R_{LS}$ and approach to zero, respectively. As the Q_L becomes higher, the relative $Z_{L,tot}$ between IB and OB increases. Fig. 4(b) shows the simulated $|Z_{L,tot}|$ and $|Z_N|$ of the parallel N-path filter and LC loads for LTE/5G NR Band 2, offering the most rigorous TX leakage condition with the duplexer spacing of only 80 MHz for mid-band (MB) and high-band (HB) frequency range (1.7–2.7 GHz). In particular, R_N, R_{SW}, R_L, and Q_L were set to 256.7 Ω, 10 Ω, 0 Ω, and 10 in the simulation, respectively. When the N-path filter is disabled, $Z_{L,tot}$ exhibits a normal resonant LC response ($Z_{L,tot} \approx Z_{LC}$) with poor frequency selectivity ($\Delta Z_{L,OFF}$). By contrast, the enabled N-path filter in parallel with the LC load entails large relative impedance values of Z_N and $Z_{L,tot}$ between the IB and OB frequencies, which represents $\Delta Z_{L,ON}$. Consequently, considerably enhanced frequency selectivity against OB blockers can be attained with a wide range of frequency tunability owing to $\Delta Z_{L,ON} \gg \Delta Z_{L,OFF}$.

III. CIRCUIT IMPLEMENTATION

By primarily using the N-path filter-based load impedance transition property over the frequency range as discussed in Section II, a tunable and broadband OB blocker rejection LNA is realized through practical circuit implementation. The implemented design is targeted to support the frequency range of 1.7–2.7 GHz, specifically focusing on the LTE/5G NR FDD MB and HB frequency bands. Depending on the operating IB RF frequencies (f_{IB}), the center frequency of the high-Q BPF response is readily tuned by setting $f_{LO} = f_{IB}$ while maintaining the blocker tolerance over a wide frequency range. In accordance with the block diagram in Fig. 2, detailed circuit schematics of the proposed LNA were built, as depicted in Fig. 5. The circuit includes the broadband current-reuse low-noise pre-amplifier, the differential N-path filter-loaded frequency-selective stage, and the combiner buffer stages along with the quadrature-phase LO generation circuitry. The utilized passive devices and their parasitic components were accurately modeled and optimized by tools in the circuit simulation phase using Cadence EMX.

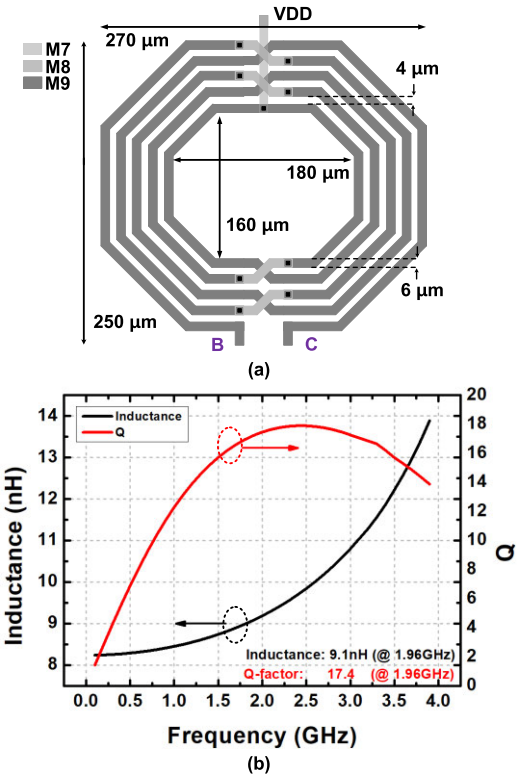

FIGURE 6. Load inductor of the frequency-selective stage; (a) inductor layout and (b) simulated inductance and quality-factor (Q).

A. BROADBAND LOW-NOISE PRE-AMPLIFIER

The low-noise pre-amplifier, preferentially placed in the first stage of the LNA, mainly provides broadband input matching and low-noise characteristics through the preceding signal amplification. The single-ended pre-amplifier design forms a complementary common-source (CS) configuration that utilizes input devices (M_{1N} and M_{1P}) with a feedback resistor (R_F) [8], [38], [39]. This current-reuse topology indeed facilitates the gain boosting and NF reduction in an amplifier for a particular current consumption. R_F is responsible for biasing M_{1P} and maintaining a nearly constant real part of the input impedance (R_I) over a wide frequency range. The input impedance (Z_I) of the low-noise pre-amplifier stage shown in Fig. 5 can be expressed as follows:

$$Z_I(s) = \frac{1 + R_F/Z_{L,A}(s)}{(g_{m,N1} + g_{m,P1}) + 1/Z_{L,A}(s)} \| \frac{1}{sC_{P,I}} \quad (12)$$

$$\cong \frac{1}{(g_{m,N1} + g_{m,P1})} \| \frac{1}{sC_{P,I}} \text{ for } Z_{L,A}(s) \gg R_F \quad (13)$$

where $g_{m,X}$ and $C_{P,X}$ denote the transconductance of M_X and total parasitic capacitance at node X, respectively. The total load impedance at node A, $Z_{L,A}$, is defined as $r_{o,N1} \| r_{o,P1} \| Z_{I,FS}$ where $r_{o,X}$ is the output impedance of M_X, and $Z_{I,FS}$ is the input impedance of the subsequent frequency-selective stage. As noticed from (13), for $Z_{L,A}(s) \gg R_F$ at the operating IB frequency (f_{IB}), Z_I becomes less sensitive to R_F; however, its dependency on parasitic input capacitance ($C_{P,I}$) still remains. Moreover, when $Z_{L,A}$ is sufficiently large, the output impedance ($Z_{O,A}$), looking into the output of the first stage, becomes $(R_F + R_S)/2$: This implies that the voltage swing at node A can be managed minimal with a small value of R_F, which directly mitigates linearity degradation due to the pre-amplifier stage. With the similar approximation of $Z_{L,A} \gg R_F$, the voltage gain ($A_{V,A}$) of the low-noise pre-amplifier can be derived as

$$A_{V,A}(s) = \frac{V_A(s)}{V_I(s)} = \frac{1 - R_F \cdot (g_{m,N1} + g_{m,P1})}{1 + R_F/Z_{L,A}(s)} \quad (14)$$

$$\cong 1 - R_F(g_{m,N1} + g_{m,P1}) = \left(1 - \frac{R_F}{R_S}\right) \quad (15)$$

Under the condition of $(g_{m,N1} + g_{m,P1}) = 1/R_S$, the voltage gain can be further simplified as (15). According to (12)–(15), the noise factor (F) of the low-noise pre-amplifier stage can also be calculated as follows:

$$F = 1 + EF|_{g_{m,N1}+g_{m,P1}} + EF|_{R_F} \quad (16)$$

$$= 1 + \frac{\gamma R_S (g_{m,N1} + g_{m,P1})(1 + R_F/R_S)^2}{(1 - R_F/R_S)^2} + \frac{4(R_F/R_S)}{(1 - R_F/R_S)^2} \cong 1 + \frac{4R_S}{R_F} + \gamma \text{ for } R_F \gg R_S \quad (17)$$

The excess noise factor (EF) signifies the noise contribution of each component. γ denotes the excess noise coefficient of the devices, which is typically greater than two. Eqs. (12)–(17) obviously indicate that a large R_F value enhances the gain and NF performance. However, as the R_F approaches the load impedance $Z_{L,A}$, Z_I can deviate from the solid matching condition.

B. FREQUENCY-SELECTIVE STAGE WITH N-PATH FILTER LOAD

The single-ended low-noise pre-amplifier is followed by a frequency-selective stage, mainly featuring a high-Q BPF response using N-path filter loads in the differential manner. This stage priorly performs a single-ended-to-differential conversion through a pseudo-differential architecture. As depicted in Fig. 5, the drain of the input CS device (M_{N2}) is ac-coupled to the gain of the secondary CS device (M_{N3}) to create an out-of-phase signal; therefore, differential RF signal currents flow into the cascode devices (M_{N4} and M_{N5}). Moreover, the cross-coupled connections between the gate and source terminals of the cascode devices further lower their differential input impedance ($Z_{I,CAS}$) seen from input devices (M_{N2} and M_{N3}) and increases the differential output impedance ($Z_{O,CAS}$) seen from the load, approximately twice times, compared to those of the conventional cascode devices, which are $Z_{I,CAS} \approx 1/g_{m,N4/5}$ and $Z_{O,CAS} \approx 4g_{m,N4/5} \cdot (r_{o,N2/3}) \cdot (r_{o,N4/5})$, respectively. This truly improves the transconductance/voltage gain and noise performance of the amplifier with an enhanced matched amplitude/phase of the RF signal currents, common-mode rejection, and reverse isolation properties [40]. To achieve the

OB blocker rejection capability, as described in Section II, the load of the frequency-selective stage was formed by parallelly combining an LC tank (L_L and C_L) with differential four-phase N-path filters. To support the sufficiently wide LC resonance conditions for a 1.7–2.7 GHz frequency range, a binary-weighted controlled capacitor bank with four bits was utilized along with a center-tapped differential inductor (Figs. 5 and 6(a)). Fig. 6(b) shows the simulated inductance and Q values of the designed differential inductor at 1.96 GHz, with approximately 9.1 nH and 17.4, respectively. In particular, in this implementation, separate N-path filters are differentially utilized at each output node instead of a single N-path filter between two differential output nodes, which leads to double the Z_N at f_{IB} in the differential manner. This also ensures that the implemented design provides rejection capability even to common-mode OB blockers at the expense of area. For the optimum operation of the N-path filters, their switches must be entirely driven by non-overlapping four-phase LO signals generated by the cascaded circuitry of a current-mode-logic (CML)-based divide-by-two (DIV2), a NAND-based 25% duty-cycle generator, and LO buffers with/without resistor feedback. A differential LO signal of $2f_{LO}$ is externally applied in the implemented design after undergoing single-ended-to-differential conversion. By considering the load impedance at nodes B/C, the voltage gain ($A_{V,FS}$(s)) of the frequency-selective stage can be expressed as follows:

$$A_{V,FS}(s) = -g_{m,N2/3} \cdot Z_{L,tot}(s) \tag{18}$$

$$\cong -g_{m,N2/3} \cdot [2Z_N(s) \,||\, Z_{LC}(s)] \tag{19}$$

where $Z_{L,tot}(s) = 2Z_N(s) \,||\, Z_{LC}(s) \,||\, Z_{O,CAS}(s) \,||\, Z_{I,BUF}(s)$

$Z_{I,BUF}$ is the input impedance of the combiner buffer stage. Therefore, assuming $Z_{O,CAS}$ and $Z_{I,BUF} \gg 2Z_N \,||\, Z_{LC}$ at both IB and OB frequencies, the total load impedance ($Z_{L,tot}$) and voltage gain of the frequency-selective stage can be chiefly determined by the parallel configuration of the Z_{LC} from the resonant LC load and Z_N from the N-path filter setting to $f_{LO} = f_{IB}$.

C. COMBINER BUFFER STAGE

Finally, the combiner buffer stage is included for testing purposes, which configures basic CS and source-follower stages. This stage particularly aims to conduct differential-to-single-ended conversion and provide solid output matching condition (Z_O) to drive a 50 Ω load impedance. Assuming $g_{m,N6} = g_{m,N7}$, the voltage gain ($A_{V,BUF}$) of the combiner buffer stage can be obtained as

$$A_{V,BUF}(s) = \frac{V_O(s)}{V_B(s) - V_C(s)} = \frac{g_{m,N6/7}}{2\left[g_{m,N6/7} + 1/Z_L(s)\right]} \tag{20}$$

where Z_L(s) represents the total impedance at node O, defined as $r_{o,N6} \,||\, r_{o,N7} \,||\, R_L \,||\, (1/sC_{P,O})$. For $g_{m,N6/7} = 1/R_L$ and $r_{o,N6/7} \gg R_L$, the voltage gain and output impedance (Z_O) of the combiner buffer stage approach to almost unity and $R_L \,||\, (1/sC_{P,O})$, respectively.

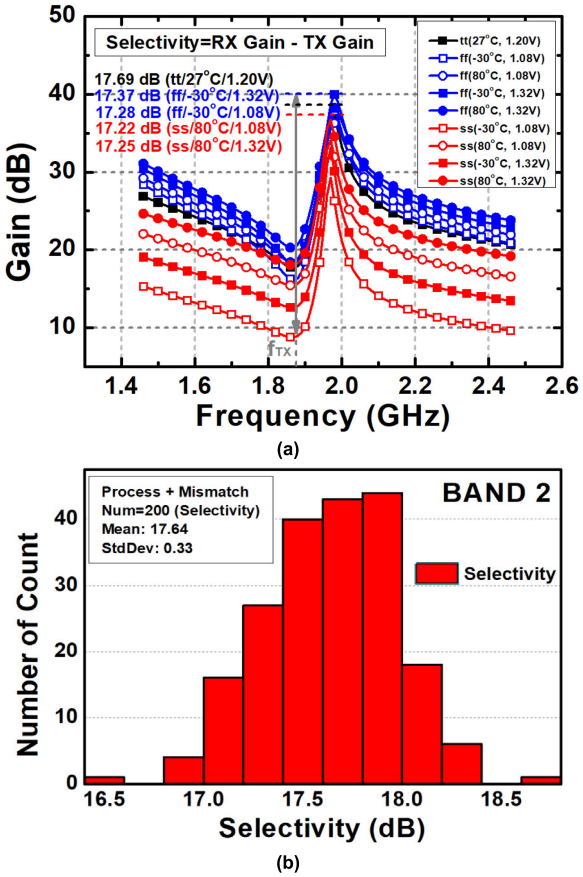

FIGURE 7. Simulated selectivity performance of the proposed blocker-tolerant LNA; (a) overall gain response for corner conditions and (b) Monte Carlo simulation with options of both device mismatch and process variations (NUM=200).

D. SELECTIVITY SIMULATION ANALYSIS

Considering all designed stages, the overall OB blocker rejection capability was analyzed with emphasis on selectivity performance. Fig. 7(a) presents the corner simulation results for the overall gain (A_V) response at the buffer output, specifically for LTE Band 2. The simulated corners were defined as the process conditions of typical-typical (TT)/slow-slow (SS)/fast-fast (FF), the temperature of –30°C/27°C/80°C, and the supply voltages of 1.08 V/1.2 V/1.32 V. Selectivity performance was evaluated by subtracting the gains at the IB RX and OB TX frequency bands ($A_V|_{@IB} - A_V|_{@TX}$). As can be observed in Fig. 7(a), the simulated frequency selectivity greater than 17.2 dB is consistently achieved for all extreme corner conditions. To further assess the design regarding the robustness of OB blocker rejection, Monte Carlo (MC) simulations, as illustrated in Fig. 7(b), were additionally conducted, considering three sigma (σ) variations in both process and device mismatches with 200 runs (NUM = 200). The obtained mean value of the simulated frequency selectivity for Band 2 is approximately 17.6 dB with a standard deviation

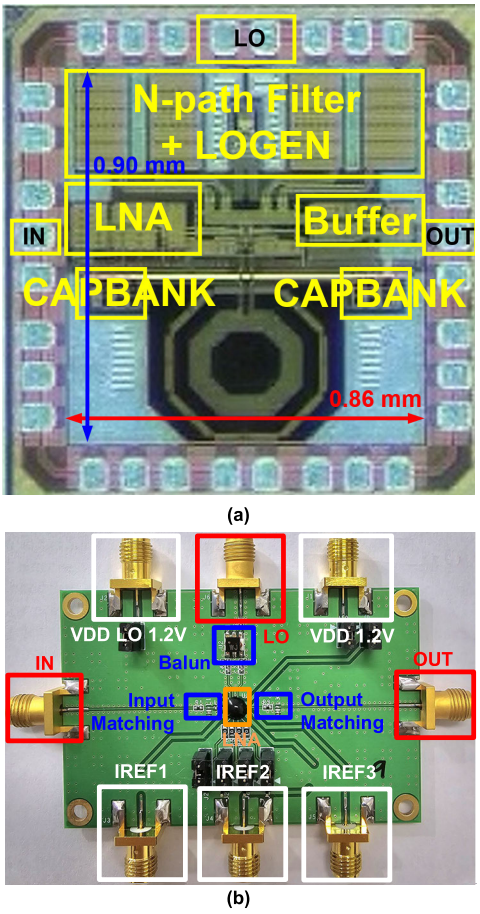

FIGURE 8. (a) Chip microphotograph and (b) DUT board setup.

(StdDev) of 0.33 dB. Similarly, robust frequency selectivity and OB blocker rejection performance can also be observed in other frequency bands through identical corners and MC simulations. It should be noted that the IB and OB gain variations are maintained almost identically over the corners in the proposed design. Consequently, the proposed N-path filter-loaded LNA design achieves reliable and consistent blocker tolerance based on the built-in high-Q BPF response regardless of several corner conditions. This result surely contrasts with those previously reported using N-path filter-based FF/FB OB blocker cancellation approaches, which are typically sensitive to PVT variations.

IV. EXPERIMENTAL RESULTS

For the validation of the OB blocker rejection capability, the proposed broadband LNA employing an N-path filter load was implemented in a 65-nm CMOS technology. Fig. 8(a) shows the chip microphotograph of the implemented design, whose active area occupies approximately 0.77 mm^2 (0.86 mm x 0.9 mm), excluding the bonding pad and input/output cells. For the performance characterization, the chip die was assembled through a chip-on-board package on a printed circuit board (PCB) as shown in Fig. 8(b). 50 Ω coplanar waveguides with a ground (CPWG) structure

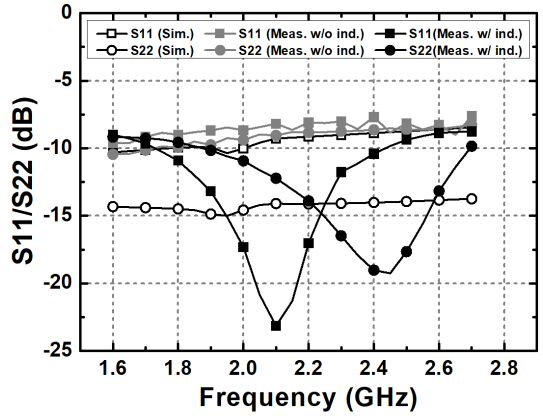

FIGURE 9. Measured and simulated S11s and S22s versus RF frequency.

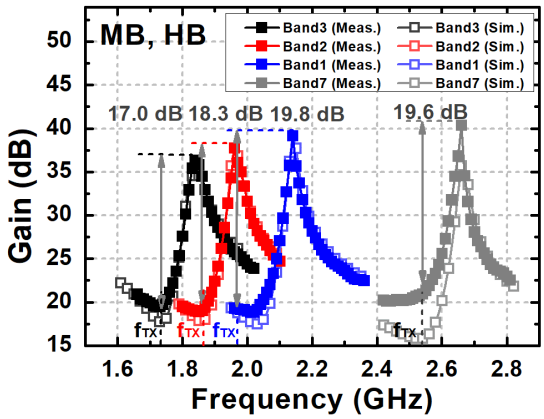

FIGURE 10. Measured and simulated gain responses and selectivity versus RF MB and HB frequencies.

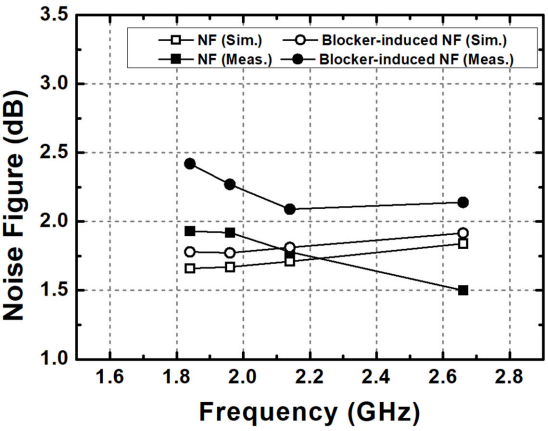

FIGURE 11. Measured and simulated noise figures versus RF MB and HB frequencies.

were applied to form all the RF signal traces. To supply a differential LO signal ($2f_{LO}$) of up to 6 GHz, a commercial off-chip balun (Mini-circuit TCM2-63WX+) was utilized with an external matching network. Prior to measurements, the insertion losses due to the PCB traces and cables were also estimated to reflect them in the results at all the characterized frequencies. All measurements were conducted at

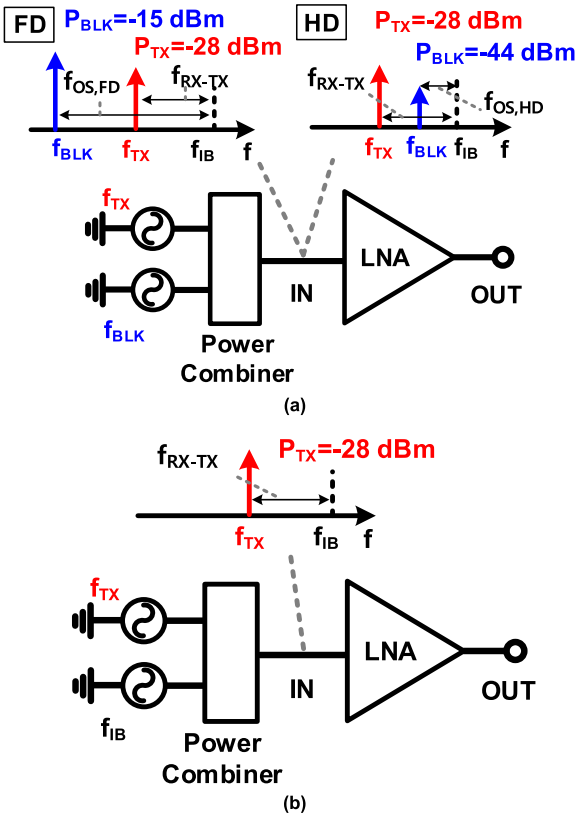

FIGURE 12. Measurement setups; (a) OB-IIP3 for FD and HD blocker distance scenarios and IB-IIP3 and (b) OB-P1dB for TX leakage blocker.

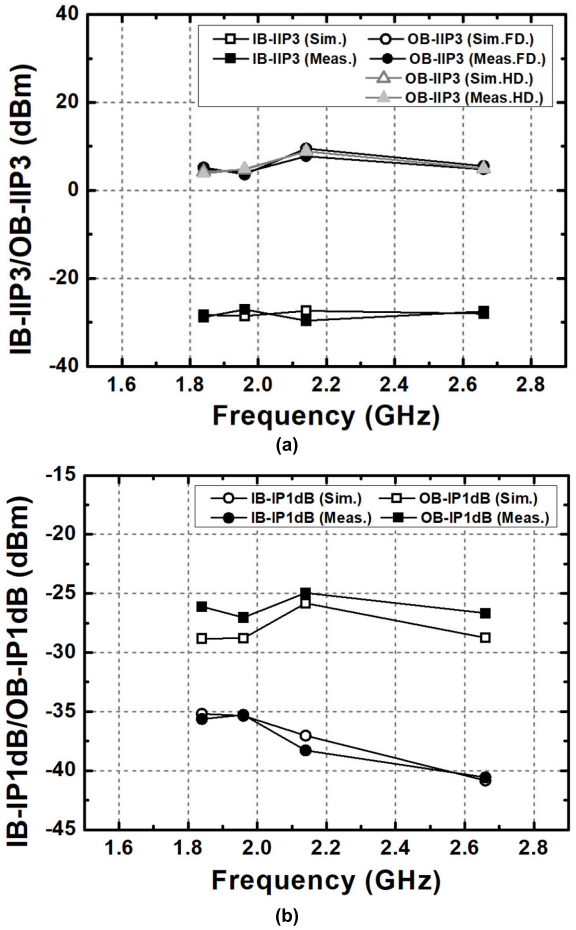

FIGURE 13. Measured and simulated; (a) OB-IIP3s for FD and HD distance scenarios and IB-IIP3s and (b) OB and IB-IP1dB.

representative LTE/5G NR FDD bands, ranging from 1.7 to 2.2 GHz in the MB (Band 1/n1, 2/n2, and 3/n3) and from 2.6 to 2.7 GHz in the HB (Band 7/n7). The minimum duplexer spacings (f_{RX-TX}) for MB and HB are 80 and 120 MHz for Band 2/n2 and Band 7/n7, respectively. The implemented LNA consumed 37.7 mA, excluding the LO circuitry, with a nominal supply voltage of 1.2 V, which was identical for all operating bands (pre-amplifier stage: 13.3 mA, frequency-selective stage: 21.5 mA, and combiner buffer stage: 2.9 mA).

First, the input and output matching conditions of the design were evaluated to verify its broadband characteristics. Fig. 9 shows the measured and simulated S11 and S22 results for the entire MB and HB frequency ranges without and with series inductors. Owing to the effect of parasitic capacitance, the measured S11 and S22 results were slightly inferior to simulated results, which range from –10.5 to –7.5 dB. Series inductors of 3.3 nH and 3.9 nH were used at the input and output for the improved matching by compensating for the parasitic capacitance, respectively. Almost identical matching conditions were obtained regardless of the applied f_{LO}. Although the frequency responses of S11 and S22 rely on parasitic components from PCB traces and pads, both obtained S11 and S22 values are well below –10 dB for nearly target frequency bands. Under satisfactory broadband matching conditions, the gain responses and frequency selectivity were identified to validate the OB blocker rejection capability of the proposed LNA design. The measured and simulated voltage gains with respect to the RF input frequency for each band are presented in Fig. 10. As seen from Fig. 10, the overall IB voltage gains for the MB and HB reach 36.4–39.2 dB and 40.4 dB with a 3-dB channel bandwidth greater than 30 MHz and 20 MHz, respectively. The attained IB-TX frequency selectivity performance exceeds 17 dB and reaches 19.6 dB for MB and HB, respectively. However, it can be observed that the achieved OB blocker rejection/selectivity is degraded in the lower-frequency band. This was primarily attributed to the presence of additional parasitic components from the four-bits control capacitor bank. Note that a larger capacitance is necessary to resonate at a lower f_{IB}. Thus, the most significant bit-controlled switches and their capacitor arrays should be activated. Therefore, the effect of their extra capacitance and on-resistance eventually lowers the Q of the LC load, resulting in the degradation of IB gains and selectivity. Despite of relatively high IB gains of the implemented LNA, its stability condition is verified through both measurements and simulations (K > 1 over the entire frequency). Fig. 11 shows the measured and simulated NFs of the implemented design with respect to the RF input frequency. The attained measured NFs ranged from 1.78 dB to 1.93 dB and were 1.5 dB for MB and HB, respectively.

TABLE 1. Summary of performance.

Frequency (GHz) (LTE/5G NR Bands)	1.84 (Band 3/n3)	1.96 (Band 2/n2)	2.14 (Band 1/n1)	2.66 (Band 7/n7)
IB Gain (dB)	36.4	37.8	39.2	40.4
Selectivity (dB)	17.0	18.3	19.8	19.6
NF / Blocker-induced NF (dB)	1.93 / 2.42	1.92 / 2.27	1.78 / 2.09	1.50 / 2.14
S11 / S22 (dB)	< –10 / < –10	< –10 / < –10	< –10 / < –10	< –10 / < –10
IB-IIP3 (dBm)	–28.8	–27.1	–29.6	–27.5
OB-IIP3 (FD/HD) (dBm)	4.8 / 3.8	4.1 / 4.9	7.7 / 8.9	4.8 / 5.0
IB- / OB-P1dB (dBm)	–35.6 / –26.1	–35.3 / –27.0	-38.3 / -24.9	–40.6 / –26.7

TABLE 2. Comparions and summary of performance.

References	This Work		Access2023 [8]		JSSC2007 [5]	TMTT2022 [7]	TMTT2021 [16]	MWCL2018 [17]	MWCL2020 [25]	TCAS2022 [26]
Architecture	OB-blocker cancellation with N-path filter load		FF-based N-path filter OB-blocker cancellation		FF-based blocker cancellation	FF-based blocker cancellation	EBD-based N-path Filter blocker cancellation	EBD-based Notch filter blocker cancellation	N-path filter-based FB loop blocker cancellation	N-path filter-based FB loop blocker cancellation
Process (CMOS)	65 nm		65 nm		65 nm	65 nm	65 nm	65 nm	65 nm	28 nm
Power Supply (V)	1.2		1.2		1.2, 2.5	1.0	1.2, 2.5	1.2	1.2	1.0
Area (mm^2)	0.77		1.0		0.28	1.16	2.0	1.19	0.62	0.24
Power (mW)[(1)]	37.7		28.7		29	20	28.6	9.6 (LNA)	15.6	22
Frequency (GHz)	1.7–2.2	2.6–2.7	1.7–2.2	2.7	1.96	1.35–2.7	1.8–2.2	1.6–2.2	0.7–2.2	0.1–2.0
Gain (dB)	36.4–39.2	40.4	9.3–10	8	20.9	16.8–19.3	3.7–5.9	21.1–24.8	11.2–20.4	22–24
Selectivity[(2)] (dB)	> 17.0	19.6	> 18.1	16	> 21	> 27.8	58.9	> 50	> 56.4	20–50
3-dB BW (MHz)	> 30	20	7	7	4.5	5–20	7	N/A	5–20	2.5–20
NF (dB)	1.78–1.93	1.50	3.8–4.0	4.9	6.8	5.1–5.5	12.1	6.4–6.8	3.24–5.4	3.1
Blocker NF (dB)	2.09–2.42	2.14	4.4–4.6	5.4	N/A	N/A	13.5	N/A	3.75–5.4	13.7
S11 (dB)	< –10	< –10	< –10	< –10	< –10	< –10	< –10	< –9.5	N/A	< –17
S22 (dB)	< –10	< –10	< –10	< –10	N/A	N/A	N/A	N/A	N/A	N/A
IB-IIP3[(3)] (dBm)	> –29.6	-27.5	> –3	1.3	2.6	7.2	12.5	–12.5	–8	N/A
OB-IIP3$_{FD}$[(4)] (dBm)	> 4.1	4.8	> 9.8	10.5	N/A	18.8	43.1	52.4	17	5.4
OB-IIP3$_{HD}$[(5)](dBm)	> 3.8	5.0	N/A†	N/A	N/A	24.9	29.6	19	N/A	N/A
IB-P1dB (dBm)	> –38.3	–40.6	> –13.4	–10.4	N/A	N/A	–4	N/A	N/A	N/A
OB-P1dB (dBm)	> –27.0	–26.7	> –5.5	–3.2	0	10.8	24.9	N/A	N/A	–12.5

[(1)] Excluding LO circuitry [(2)] Selectivity = RX IB Gain – TX Gain
[(3)] $f_{1,IB} = f_{IB}$ + BW/2 + 7.5 MHz, $f_{2,IB} = f_{IB}$ + BW/2 +14 MHz ($P_{1/2,IB}$ = –46 dBm)
[(4)] f_{TX} and $f_{FD} = f_{IB} - f_{OS,FD}$ + 1 MHz (P_{TX} = –28 dBm, P_{FD} = –60 dBm),
[(5)] f_{TX} and $f_{HD} = f_{IB} - f_{OS,HD}$ + 1 MHz (P_{TX} = –28 dBm, P_{HD} = –48.5 dBm)
† N/A: Not Available

Note that the first stage primarily determines the overall noise NF performance, and the subsequent frequency selective and buffer stages contribute less noise owing to the preceding amplification. Furthermore, the measured blocker-induced NFs under a –28 dBm TX leakage blocker exhibited less than 0.7 dB degradation compared to the NFs without the blocker for all operating frequency bands.

The linearity performance of the proposed LNA design is also crucial for evaluating blocker-tolerance capability. The third-order intercept points (IP3s) and 1-dB compression points (P1dBs) of the implemented design were identified in the presence of various OB blocker conditions, as illustrated in Fig. 12. In particular, for OB IP3 characterization, the full-duplexing (FD) and half-duplexing (HD) distance intermodulation scenarios were separately speculated in the design. These FD and HD scenarios specified their power level of –15 and –44 dBm at the offset frequency of $f_{OS,FD}$ ($f_{OS,FD} = 2 \cdot f_{RX-TX}$) and $f_{OS,HD}$ ($f_{OS,HD} = f_{RX-TX} / 2$), respectively [1], [7], and [17]. Assuming the TX-to-RX and antenna-to-RX duplexer attenuation of approximately 52 dB at f_{TX} and 45 / 4.5 dB at the offset frequency of $f_{OS,FD}/f_{OS,HD}$, the applied power level of two tones (f_{TX} and $f_{FD/HD}$) for the FD/HD OB input-referred IP3s (IIP3s) were adjusted, which were P_{TX} = –28 dBm and $P_{FD/HD}$ = –60 / –48.5 dBm, respectively ($f_{FD} = f_{IB} - f_{OS,FD} + 1$ MHz and $f_{HD} = f_{IB} - f_{OS,HD} + 1$ MHz). As shown in Fig. 13(a), the obtained FD and HD OB-IIP3s are 4.1–7.7 and 3.8–8.9 dBm for MB and 4.8 and 5.0 dBm for HB, respectively. Moreover, two tones, f_1 and f_2, were also applied to evaluate the IB-IIP3 performance of the design, defined as $f_{1,IB} = f_{IB}$ + BW/2 + 7.5 MHz and $f_{2,IB} = f_{IB}$ + BW + 14 MHz where BW represents the channel bandwidth [1], [2]. With $P_{1/2,IB}$ = –46 dBm for the BW = 10 MHz, the measured IB-IIP3s are greater than –29.6 dBm for MB and –27.5 dBm for HB.

IB blockers are relatively close to the passband, f_{IB}; therefore, the blocker rejection of the design is less effective. Fig. 13(b) also shows the measured OB-input-referred P1dBs (IP1dBs) and IB-IP1dBs with the OB and IB blocker at f_{TX} and f_{IB}, which are greater than –27.0 dBm and –40.6 dBm from whole measured frequency bands, respectively. The corresponding output-referred P1dBs for the IB tone were almost identical, that is, approximately 1 dBm.

The measured performance of the implemented blocker-tolerant LNA for all measured LTE/5G NR frequency bands is summarized in Table 1. Furthermore, Table 2 presents a comprehensive performance comparison of the implemented design with previously reported state-of-the-art OB blocker-tolerant designs. Although previous designs based on the blocker cancellation approach achieve a high level of OB blocker rejection specifically against the TX leakage blocker of up to approximately 60 dB, the amount of cancellation is relatively vulnerable to frequency-dependent PVT variations. Therefore, additional calibration steps are essential for each operating frequency band with an extra cost. On the contrary, the proposed LNA effectively sustains a robust OB blocker rejection ratio greater than 17 dB because the utilized N-path filter-based load provides almost identical gain variations at both the IB and OB frequencies even if PVT variations exist. Consequently, the proposed LNA design can accomplish robust and reliable BPF response over a broad range of OB blockers without extra calibration.

V. CONCLUSION

This study demonstrated a broadband CMOS LNA design that reliably mitigated the effects of OB blockers across a wide frequency range. The utilized N-path filters as the load provide load impedance transition properties according to the switching LO frequency so that the total relative load impedance of the amplifier determining the overall gains between the IB and OB frequencies can be effectively controlled. The proposed design is distinct from the previously reported N-path filter-based blocker cancellation approaches where the filters are used in the signal path. Furthermore, the demonstrated blocker rejection techniques are highly immune to PVT variations. Thus, this proposed calibration-free blocker rejection scheme can be well-applicable to the receiver design, supporting multiple frequency bands at a lower cost.

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