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RESEARCH ARTICLE

Harmonics Minimization of Symmetric Five-Level Inverter Using Improved LSF Modulation Scheme

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ABSTRACT The use of multilevel inverters has gained popularity due to their ability to generate high-quality output voltage with reduced harmonic distortion. The performance of these multilevel inverters can be improved by using a low switching frequency modulation scheme as it enables precise amplitude and harmonic control in the output voltage. Determination of optimum switching angles for minimum total harmonic distortion generally requires complex algorithms with large number of iterations. This work presents a novel approach for calculating optimum switching angles at low frequencies that produces low total harmonic distortion in the output voltage. The calculation process uses only one controlling parameter that allows easy computation of optimum switching angles with a lesser number of iterations. The effectiveness of the calculated switching angles in producing lower total harmonic distortion is verified through simulation in MATLAB/Simulink platform as well as experimentally by developing a small-scale lab prototype of symmetric five-level inverter systems. For generalization, the proposed switching angle calculation technique is examined through different levels of inverter for minimum total harmonic distortions. The superiority of the proposed switching technique is verified through an extensive comparison with other popular low-frequency strategies which revealed that the proposed technique produces lower total harmonic distortions and higher fundamental voltage than those of the Equal Phase, Feed Forward, and Half Height methods. This feature of producing higher-quality fundamental voltage would make it a preferred choice for high power multi-level inverters.

INDEX TERMS Multilevel inverter, optimum switching angle calculation, total harmonic distortion, fundamental voltage, low frequency switching.

I. INTRODUCTION

With the proliferation of high-power semiconductor devices and innovative modulation techniques, multilevel inverters (MLIs) have appeared as a preferred choice for medium- and high-voltage applications, including renewable energy (RE) applications, because of their ability to convert dc sources into staircase voltage near a sinusoidal waveform. Among the attractive benefits of MLIs are: better quality of output voltage, i.e., lower total harmonic distortion (THD), higher operating voltage with lower-rated semiconductor devices, lower dv/dt stress, lower electromagnetic interference (EMI), reduced requirement of passive filters, and fault-tolerant operation [1]. These features allow transformer-less PV

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TABLE 1. Research gaps among different switching angle calculation methods.

Switching angle calculation Methods	Limitations/Research gaps	Reference
Newton-Raphson algorithm (NRA)	• Difficulties in determining the appropriate initial values. This exacerbates as the number of switching angle becomes higher. • Needs large number of iterations.	[18]
Equal phase (EP) method	• Produces higher total harmonics distortion. • The dominate THD is observed at lower frequency that requires high filter size.	[18], [19]
Half height (HH) method	• Produces relatively higher total harmonics distortion. • The dominate THD is observed at low frequency. Poor output voltage and current quality. • Large voltage ripple. • Needs higher size filter.	[20], [21]
Feed forward (FF) method	• Poor output voltage and current quality. • Large voltage ripple. • Needs higher size filter. • High amount of total harmonic distortion.	[8]
Nearest-level control (NLC)	• Poor output voltage and current quality. • Large voltage ripple. • Higher total harmonics distortion. • Needs high size filter.	[22]
Selective harmonic elimination (SHE)	• Requires the solution of complex transcendental equations. • Commonly adopted Newton-Raphson based method requires initial values that can be difficult to determine.	[23]
Space vector modulation (SVM)	• Requires a lookup table and sector identification to implement. • SVM can be difficult to execute as the number of levels in the inverter increases.	[24]

integration with the grid [2], [3]. A variety of MLI topologies have been developed in the past to increase power quality while using a lower number of dc sources and switches at reduced ratings [4], [5], [6], [7].

When using a specific architecture, the output voltage quality and inverter efficiency both are affected by the modulation technique used. On the basis of the fundamental switching frequency or low frequency as well as the high switching frequency, numerous modulation schemes have been developed to improve harmonic performance while minimizing losses [8]. In high switching frequencies, there are multiple switching pulses per cycle, whereas in fundamental switching frequencies, there are one or two switching pulses per cycle [1]. Traditional pulse width modulation (PWM), sinusoidal PWM (SPWM), and space vector modulation (SVM) are in the category of high-frequency switching techniques. Whereas selective harmonic elimination (SHE), space vector control (SVC), and nearest level control (NLC) are in the low frequency switching group [4]. Besides, various carrier-based as well as carrier-less pulse width modulation (CLPWM) strategies are proposed. While a high switching frequency scheme provides a faster transient response, it produces higher switching loss, and is less efficient. It is favorable for low-power applications where power quality is more important than converter efficiency. For medium-voltage and high-power applications, low switching frequency techniques are preferred to minimize thermal stress on switches due to large switching losses [9], [10]. But low switching frequency produces output voltage or current of higher distortion [11]. Although low-pass filters can be used to dampen higher-order harmonics, PWM approaches are limited in their ability to get rid of the more pervasive lower-order harmonics. For this purpose, SHE is the best option due to the fact that appropriate switching angles can be calculated to get rid of certain low-order harmonics [12].

The primary difficulty with the SHE method is finding a workable solution to a system of highly nonlinear transcendental equations. These are primarily multi-angle trigonometric equations obtained from the study of Fourier series. These equations may have several solutions, a single solution, or no solution within a specific range of modulation index [13]. Various metaheuristic optimization techniques have also been widely used for harmonic minimization in multilevel inverters. A species-based Particle Swarm Optimization (PSO) was introduced [14]. The PSO approach was originally developed for a framework with unequal DC sources [15], [16], but this resulted in an increase in the total number of switching angles. The computing load associated with a small number of switching angles is alleviated by the PSO approach, which takes into account the asymmetry of the supernatural comparisons. The proposed methodology entails the application of a Self-learning Particle Swarm Optimizer (SLPSO) to tackle global optimization problems. This is in contrast to conventional PSO techniques, which typically employ a uniform learning model for all particles [17], where each particle has four methods at its disposal to adjust to different conditions in the search space. This adaptable selection tool is utilized to enable particles to select the appropriate learning aiming at the appropriate moment during the inquiry process. Nevertheless, the aforementioned optimization approach requires the first guess, which is an extremely important step.

In order to reduce THD, a number of switching techniques (NRA, EP, HH, FF, NLC, SHE and SVM) have been presented in various literatures [25]. The EP and HEP methods carry equal duty cycle that may apparently produce large staircase output voltage and current, but it contains large THDs. For this, the RMS values of voltage and current will be reduced. They are not a recommended PWM scheme due to their low power conversion efficiency. HH approach has been widely used to generate firing pulses of modular multilevel inverters. Compared to EP and HEP, this technique produces the lowest value of THD with reduced power losses. An improved modular multilevel inverter harmonics mitigation method was presented in [26]. Although its modulation strategy yields the best total harmonic distortion, it requires more iterations and a complex programing algorithm. To reduce THD in five-level inverter output voltage, a neural network based selective harmonic elimination method have been attempted [27]. While the artificial neural network (ANN) model performs well in estimating switching angles quickly and accurately, the generated output contains higher THD. Table 1 presents a comprehensive overview of the limitations associated with various widely used techniques for calculating switching angles.

From this table, it can be seen that existing switching angle calculation methods produce higher THD, low fundamental voltage and current gain. Besides that, most of them have inherent computational complexity and require a higher number of iterations. To achieve a nearly sinusoidal output voltage of minimum THD, there is always a need for simple and fast calculation method that will produce required switching angles precisely. To address this demand, this paper proposes a new switching angle calculation method for generating the firing pulses of modular multilevel inverter. The key objectives of the paper are listed below:

1. To propose an initial guess free optimum switching angle calculation approach. Ensuring proper initial value is the single biggest problem with the existing popular iterative based methods like - Newton Raphson, PSO, GA, SLPSO based SHE method. Failure to provide proper initial values the solution will not converge.
2. To reduce the complexity in determining the switching angles of any number.
3. To guarantee optimum switching angles for minimum THD with a smaller number of iterations.
4. To enhance the magnitude of inverter output voltage.

The rest of the paper is organized as follows: the operating principle of the symmetric five-level inverter is discussed in Section II. Effect of Fundamental Switching Angles on THDs is presented in Section III. A brief description of existing different switching angle calculation methods and proposed method are presented in Section IV. Simulation results are demonstrated in section V. Performance validation, experimental results, and discussion are presented in Section VI. Comparative analysis is presented in Section VII, Finally, Section VIII summarizes the conclusion drawn from the proposed study.

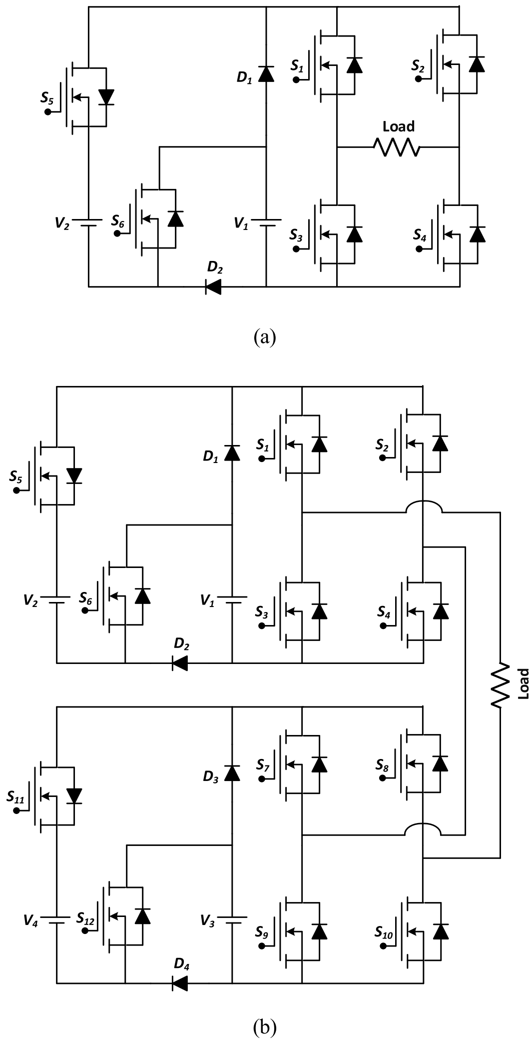

FIGURE 1. Circuit diagram of multilevel inverter – (a) 5-level inverter, and (b) cascaded connection.

II. PROPOSED MULTILEVEL INVERTER

Fig. 1(a) illustrates the proposed symmetrical five-level inverter [28]. It employs a total of six switching devices, two diodes, and two voltage sources of identical values to provide five separate levels of output voltage. It consists of two main units, namely the level generation unit and the polarity generation unit. The level generation unit utilizes two switching devices S_5 and S_6, to produce output voltages of V and 2V. On the other hand, the H-bridge unit functions as a circuit for generating polarity including the zero level of

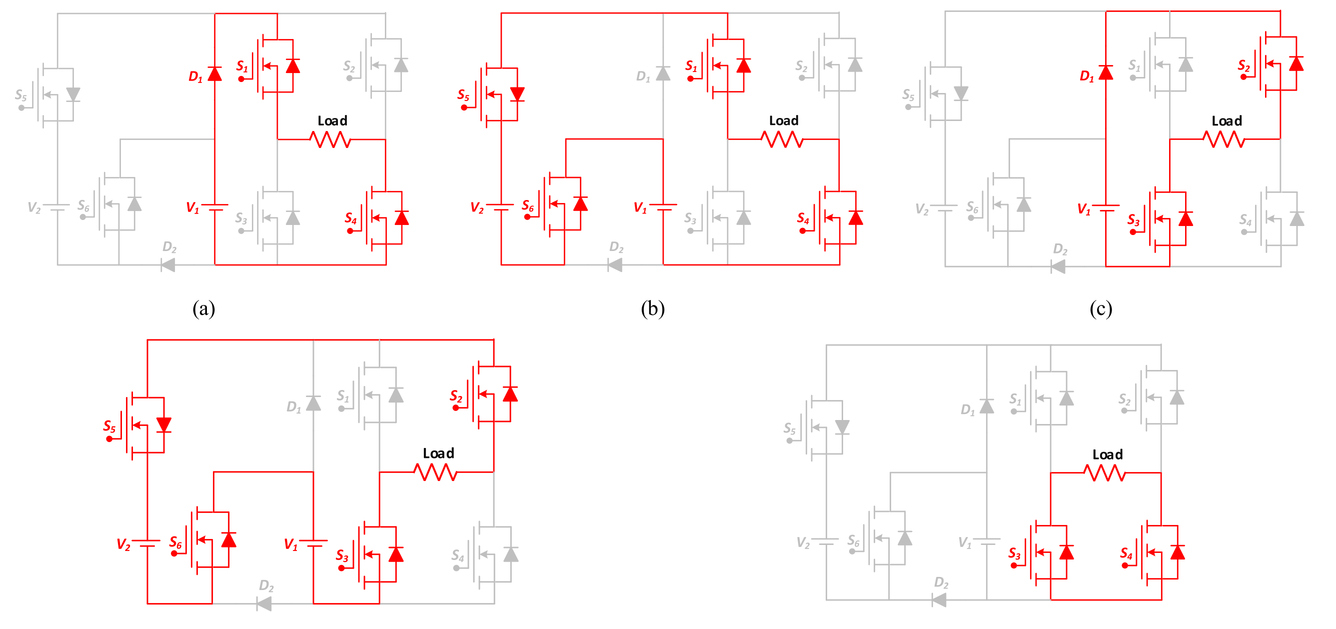

FIGURE 2. Generation of different modes of symmetric 5-level inverter: (a) mode 1, (b) mode 2, (c) mode 3, (d) mode 4, and (e) mode 5.

TABLE 2. Functional modes of symmetric five-level inverter.

Modes	Different switching states						Output voltage
	S_1	S_2	S_3	S_4	S_5	S_6	
Mode 1	1	0	0	1	0	0	V
Mode 2	1	0	0	1	1	1	2V
Mode 3	0	1	1	0	0	0	-V
Mode 4	0	1	1	0	1	1	-2V
Mode 5	0	0	1	1	0	0	0

the output voltage. This five-level inverter can be connected in cascade to create 9-level to 31-level inverter based on different values of four voltage sources. The cascaded circuit diagram has been presented in Fig. 1(b).

A. FIVE-LEVEL INVERTER

In this section, the operating principle of 5-level inverter is presented. For symmetrical operation, two voltage sources are equal i.e., $V_1 = V_2 = V$. Table 2 shows different switching modes for generating the various voltage levels. Operation of each mode is given below:

Mode 1: This mode generates voltage across the load terminal by turning on S_1 and S_4 switching devices. In this mode diode D_1 has also participated in conduction. Fig. 2(a) presents this mode's voltage generation procedure.

Mode 2: By activating switches S_1, S_4, S_5, and S_6, this mode can produce a voltage of 2V across the load terminal. Fig. 2(b) depicts the steps involved in creating voltage in this mode.

Mode 3: This mode generates -V volt across the load terminal by turning on S_2 and S_3 switching devices. In this mode diode D_1 has also participated in conduction. The voltage generation procedure of this mode is presented in Fig. 2(c).

Mode 4: By activating switches S_2, S_3, S_5, and S_6, this mode can produce a voltage of -2V across the load terminal. Fig. 2(d) depicts the steps involved in creating voltage in this mode.

Mode 5: This mode is very important for the inductive load. The generated voltage across the load is 0 volts. The voltage generation procedure is presented in Fig. 2(e). Only S_3 and S_4 switches are turned on during this mode.

B. NINE-LEVEL INVERTER

A cascaded reduced switch inverter shown in Fig. 1(b) can achieve nine levels in its output by carefully controlling the states of the switches in each stage. In this case, the value of voltage sources is selected as V. Therefore, by activating appropriate switching devices, V, 2V, 3V, 4V, -V, -2V, -3V, -4V and zero levels can be generated. The functional modes of nine-level inverter have been presented in Table 3.

C. FIFTEEN-LEVEL INVERTER

In this case, the value of voltage sources V_1, V_2, V_3 and V_4 are selected as V, 2V, 2V and 2V respectively. The cascaded inverter shown in Fig. 1(b), now can generate fifteen levels in its output voltage waveform by carefully controlling the states of the switches in each stage as shown in Table 4. Therefore, by activating appropriate switching devices, fifteen levels of output voltage can be generated.

III. EFFECT OF FUNDAMENTAL SWITCHING ANGLES ON THD

The switching angles have a crucial effect on THD of the output voltage of a symmetric multilevel inverter. To illustrate this, a voltage waveform of the symmetric multi-level inverter is considered, as shown in Fig. 3. Such a signal can be

TABLE 3. Functional modes of nine-level inverter.

V_{out}	S_1	S_2	S_3	S_4	S_5	S_6	S_7	S_8	S_9	S_{10}	S_{11}	S_{12}
V_1	1	0	0	1	0	0	0	0	1	1	0	0
$V_1 + V_2$	1	0	0	1	1	1	0	0	1	1	0	0
$V_1 + V_2 + V_3$	1	0	0	1	1	1	1	0	0	1	0	0
$V_1 + V_2 + V_3 + V_4$	1	0	0	1	1	1	1	0	0	1	1	1
0	0	0	1	1	0	0	0	0	1	1	0	0
$-V_1$	0	1	1	0	0	0	0	0	1	1	0	0
$-(V_1 + V_2)$	0	1	1	0	1	1	0	0	1	1	0	0
$-(V_1 + V_2 + V_3)$	0	1	1	0	1	1	0	1	1	0	0	0
$-(V_1 + V_2 + V_3 + V_4)$	0	1	1	0	1	1	0	1	1	0	1	1

TABLE 4. Functional modes of fifteen-level inverter.

V_{out}	S_1	S_2	S_3	S_4	S_5	S_6	S_7	S_8	S_9	S_{10}	S_{11}	S_{12}
V_1	1	0	0	1	0	0	0	0	1	1	0	0
V_2	1	0	0	1	1	0	0	0	1	1	0	0
$V_1 + V_2$	1	0	0	1	1	1	0	0	1	1	0	0
$V_3 + V_4$	0	0	1	1	0	0	1	0	0	1	1	1
$V_1 + V_2 + V_3$	1	0	0	1	0	0	1	0	0	1	1	1
$V_2 + V_3 + V_4$	1	0	0	1	1	0	1	0	0	1	1	1
$V_1 + V_2 + V_3 + V_4$	1	0	0	1	1	1	1	0	0	1	1	1
0	0	0	1	1	0	0	0	0	1	1	0	0
$-V_1$	0	1	1	0	0	0	0	0	1	1	0	0
$-V_2$	0	1	1	0	1	0	0	0	1	1	0	0
$-(V_1 + V_2)$	0	1	1	0	1	1	0	0	1	1	0	0
$-(V_3 + V_4)$	0	0	1	1	0	0	0	1	1	0	1	1
$-(V_1 + V_2 + V_3)$	0	1	1	0	0	0	0	1	1	0	1	1
$-(V_2 + V_3 + V_4)$	0	1	1	0	1	0	0	1	1	0	1	1
$-(V_1 + V_2 + V_3 + V_4)$	0	1	1	0	1	1	0	1	1	0	1	1

represented by the Fourier series as:

$$V(\omega t) = a_0 + \sum_{n=1}^{\infty} (a_n cos n\omega t + b_n sin n\omega t) \tag{1}$$

Due to quarter wave symmetry, $a_0 = 0$, $a_n = 0$, and

$$b_n = \frac{2}{T} \int_0^T \cos(n\omega t) \tag{2}$$

$$b_n = \frac{4V_{dc}}{n\pi} \sum_{k=1}^{m} \cos(n\alpha_k) \tag{3}$$

where, $n = 1,3,5,\ldots\ldots\ldots$ an odd number and m is the number of switching angles in the first quadrant i.e., in the first quarter cycle. The voltage THD of the unfiltered inverter output is given by:

$$THD = \frac{\sqrt{V_{rms}^2 - V_1^2}}{V_1} \tag{4}$$

which is equivalent to:

$$THD = \frac{\sqrt{\sum_{n=2}^{\infty} b_n^2}}{b_1} \tag{5}$$

Using (3) it can be written as: [17], [34], [35]

$$THD = \frac{\sqrt{\frac{\pi^2 m^2}{8} - \frac{\pi}{4}\sum_{i=0}^{m-1}(2i+1)\alpha_{i+1} - \left(\sum_{i=1}^{m}\cos(\alpha_i)\right)^2}}{\sum_{i=1}^{m}\cos(\alpha_i)} \tag{6}$$

For five-level inverter, the equation (5) can be written as:

$$THD = \frac{\sqrt{\frac{\pi^2}{2} - \frac{\pi}{4}(\alpha_1 + 3\alpha_2) - (cos\alpha_1 + cos\alpha_2)^2}}{cos\alpha_1 + cos\alpha_2} \tag{7}$$

It is seen from (7) that THD mainly depends on the switching angles (α_1, α_2) in the first quarter of a cycle. Therefore, precise calculation of these angles has the potential to reduce the THD. Several methodologies have been suggested in the past for the computation of these angles. The next section provides a concise overview of some notable methods.

IV. SWITCHING ANGLE CALCULATION METHODS

Switching angle calculation method is also considered as low switching frequency modulation technique. There are several switching angle calculation methods for getting optimum firing angle of multilevel inverter. Among these EP, HEP and FF methods have been analysed.

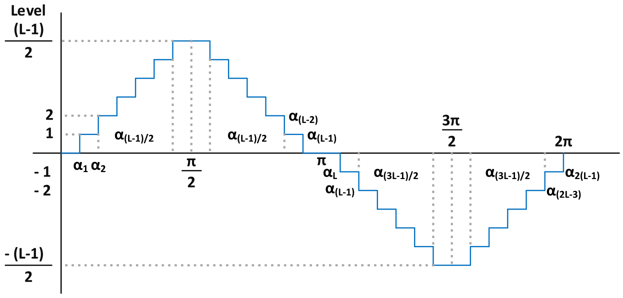

FIGURE 3. Output voltage waveform of a symmetric multilevel inverter.

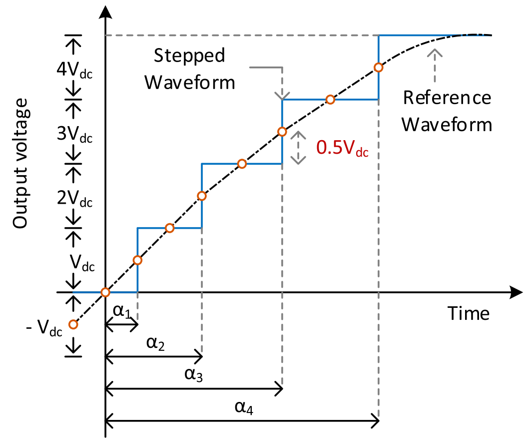

FIGURE 4. Waveform synthesis of nine level inverter.

A. EQUAL-PHASE (EP) METHOD

The equal phase approach typically uses a uniform distribution of switching angles between 0º – 180º. The main switching angles are calculated by,

$$\alpha_i = \left(\frac{180^\circ}{L}\right) i,\ where\ i = 1, 2, 3, \ldots.. \frac{L-1}{2} \tag{8}$$

The EP technique produces an output voltage just like a triangle waveform with increased total harmonic distortion.

B. HALF-EQUAL-PHASE (HEP) METHOD

Since the triangle waveform is generated by the EP method, the HEP is utilized to generate a better quality output with low harmonic content. The following formula is used to determine the primary switching angles of the HEP technique.

$$\alpha_i = \frac{90^\circ}{\left(\frac{L+1}{2}\right)} i,\ where\ i = 1, 2, 3, \ldots.. \frac{L-1}{2} \tag{9}$$

C. HALF-HEIGHT (HH) METHOD

Compared to the EP and HEP methods, the half-height approach reduces the total harmonic distortion more effectively. This approach establishes a switching angle at the point where the value of the sine function reaches half of the amplitude of each level. HH is known to have lowest THD [29]. The primary switching angles within the range of 0 to 90 degrees are derived by the following formula:

$$\alpha_i = \sin^{-1}\left[\left(i - \frac{1}{2}\right)\left(\frac{2}{L-1}\right)\right] = \sin^{-1}\left(\frac{2i-1}{L-1}\right)$$
$$where\ i = 1, 2, 3, \ldots.. \left(\frac{L-1}{2}\right) \tag{10}$$

D. FEED-FORWARD (FF) METHOD

FF method is a modified version of HH where the switching angles are reduced to half of HH value. FF results in wider switching pulse and higher THD compared to HH method. The primary switching angles within the range of 0 to 90 degrees are derived by the following formula.

$$\alpha_i = \frac{1}{2}\sin^{-1}\left(\frac{2i-1}{L-1}\right),$$
$$where\ i = 1, 2, 3, \ldots.. \left(\frac{L-1}{2}\right) \tag{11}$$

V. PROPOSED SWITCHING ANGLE CALCULATION METHOD

To minimize THD, a new switching angle calculation method has been introduced. Fig. 4 illustrates the waveform synthesis of a conventional 9-level inverter. It is apparent from this Fig. 4 that the reference waveform falls within the range of $0.55V_{dc}$ to $0.6V_{dc}$, and the THD is contingent upon the precise positioning of the reference voltage waveform. To ascertain the exact placement of the reference waveform, a controlled parameter denoted as "r" is utilized. This parameter is incrementally added to 0.55V until the minimum THD is achieved. The main switching angles are determined using equation (12), where the controlling parameter (r) is updated during the iterative process.

$$\alpha_i = \sin^{-1}\left(\frac{2\,(i - rj - 0.55)}{L-1}\right),$$
$$where\ i = 1, 2, 3, \ldots.. \left(\frac{L-1}{2}\right);$$
$$and\ j = 0, 1, 2, \ldots (i-1) \tag{12}$$

A. DESCRIPTION OF THE ALGORITHM

The angle calculation begins with setting desired number of output voltage levels (L), initial value of r (≈ 0) and initial THD_m (≈ 100) as shown in Fig. 5. By using equation (12), α_i is calculated. Using these values of α_i in equation (7), estimated value of THD_f is determined and compared with THD_m. If the value of THD_f is less than THD_m, then the value of r is increased to $r + 0.001$ and the initial THD_m is set to THD_f.

Then the value of α_i is recalculated and the THD_f is estimated using the updated value of α_i. This process is repeated until the final THD_f is greater than THD_m. If the value of THD_f is greater than THD_m, the iterative process is stopped and optimum switching angles are displayed. The pseudocode of the proposed method is given in Pseudocode 1.

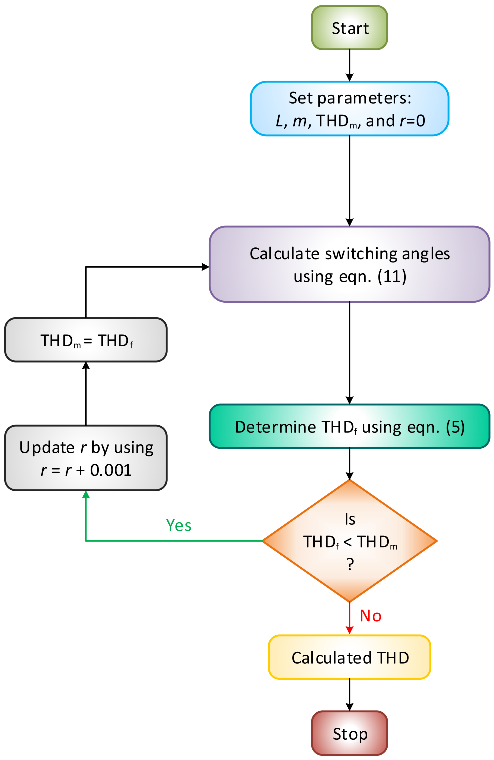

FIGURE 5. Algorithm of the proposed LSF modulation technique.

Pseudo Code 1: Proposed Switching Angle Calculation Method

Step 1: Initialize number of level (L), control parameter (r), total harmonic distortion (THD_m)
Step 2: Calculate the value of m by using $m = (L\text{-}1)/2$
Step 3: Calculate the switching angles (α_i) as follows
for $i = 1{:}\ m$ **do**
  for $j = 0{:}(i\text{-}1)$ **do**
  $\alpha_i = \sin^{-1}\left(\frac{2\times(i-r\times j-0.55)}{L-1}\right)$
end
$j = j+1$
end
Step 4: Calculate the total harmonic distortion (THD_f) by using eq. (5)
Step 5: If $THD_f < THD_m$ **then**
  Update the value of THD_m and r using
  $THD_m = THD_f$
  $r = r + 0.001$
  Continue from step 3 to step 5 until $THD_f > THD_m$
  end if
Step 6: If $THD_f > THD_m$ **then**
  Calculate the optimized switching angles and THD_f
  end if
stop

B. SUPERIORITY OF THE PROPOSED METHOD

The calculated switching angles and obtained THD for 5 to 11 level inverters are tabulated in Table 5. It shows that the proposed topology reduces THDs significantly for all level of multilevel inverter. A comparative analysis has been conducted between existing topologies and a proposed topology based on the number of iteration levels, as presented in Table 6. From this table, it is evident that for calculating the switching angles of an eleven-level inverter, references [25] utilize a maximum of 500 iteration levels, whereas the proposed switching angle calculation method requires only 36 iteration levels to achieve the desired output. Furthermore, the proposed topology also reduces the complexity of the modified NLC method outlined in reference [26]. For higher-level multilevel inverters, many more optimized switching angles must be calculated using iterative methods. This process is time-consuming and demands a large number of iterations. For example, the modified NLC approach detailed in reference [26] needs 168 iterations to generate optimal switching angles for a nine-level inverter. However, the proposed topology can be optimized using a single iterative approach and a lone regulating parameter. Specifically, the proposed approach requires only 47 iterations to generate switching pulses for a nine-level inverter. Consequently, the proposed topology simplifies the methodology outlined in reference [26]. Besides, a comparison is made between proposed and HH method for different levels of inverter topologies as shown in Fig. 6. The general trend is that as the voltage levels increase, the THD decreases for both methods.

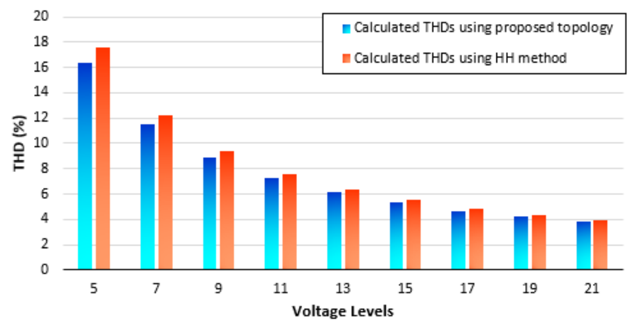

FIGURE 6. A comparison between proposed switching technique and half height method.

However, the proposed method demonstrates superiority at all the voltage levels.

VI. SIMULATION RESULTS AND DISCUSSION

In this section, the simulation results of the 5-level, 9-level and 15-level inverters using proposed switching angle calculation method and HH method have been demonstrated. The simulations are carried out in Matlab/Simulink platform with the simulation parameters shown in Table 7. Voltage and current wave forms and their harmonic spectrums are observed to demonstrate the superiority of the proposed switching angle calculation method.

A. CASE STUDY 1: 5-LEVEL INVERTER

In this case, the calculated switching angles using the proposed method are shown in Table 8. A close observation on

TABLE 5. Performance comparison between proposed switching method and half height method.

Proposed switched method				HF method		% of Improvement of THD using proposed method
No. of levels	No. of iterations	Calculated switching angles (deg)	Calculated THD (%)	Calculated switching angles (deg)	Calculated THD (%)	
5	16	$\alpha_1 = 13.0029$, $\alpha_2 = 41.8359$	16.4226	$\alpha_1 = 14.477$, $\alpha_2 = 48.590$	17.6	6.69
7	67	$\alpha_1 = 8.6269$, $\alpha_2 = 27.4301$, $\alpha_3 = 50.4738$	11.5344	$\alpha_1 = 9.59$, $\alpha_2 = 30$, $\alpha_3 = 56.442$	12.23	5.68
9	47	$\alpha_1 = 6.4594$, $\alpha_2 = 20.5485$, $\alpha_3 = 36.1215$, $\alpha_4 = 55.8938$	8.9106	$\alpha_1 = 7.18$, $\alpha_2 = 22.024$, $\alpha_3 = 38.682$, $\alpha_4 = 61.044$	9.37	4.91
11	36	$\alpha_1 = 5.1636$, $\alpha_2 = 16.4274$, $\alpha_3 = 28.3984$, $\alpha_4 = 41.9437$, $\alpha_5 = 59.4516$	7.2669	$\alpha_1 = 5.739$, $\alpha_2 = 17.457$, $\alpha_3 = 30$, $\alpha_4 = 44.427$, $\alpha_5 = 64.158$	7.59	4.25

TABLE 6. Comparison based on number of iteration level.

Reference	No. of level	Maximum iteration level	Proposed
[25]	11	500	36
[26]	9	168	47
[30]	11	500	36
[31]	-	1000	Less than 100

TABLE 7. Simulation parameters.

Parameters	Values
Supply DC voltage	5-level: 150 V, 150 V 9-level: 75 V, 75 V, 75 V, 75 V 15-level: 43 V, 86 V, 86 V, 86 V
Fundamental frequency (f)	50 Hz
Resistive load	200 Ω
Switching angle calculation method	Proposed, half height method

TABLE 8. Calculated THD and switching angles of 5-level inverter using proposed switching angle calculation method.

No. of iterations	α_1 (degree)	α_2 (degree)	Calculated THD (%)
5	13.0029	42.2990	16.4278
10	13.0029	42.1057	16.4242
15	13.0029	41.9129	16.4227
17	13.0029	41.8359	16.4226

the calculated switching angles reveals that the value of α_2 and THD decrease for increasing the number of iterations.

TABLE 9. Calculated THD and switching angles of 9-level inverter using proposed switching angle calculation method.

No. of iterations	α_1 (degree)	α_2 (degree)	α_3 (degree)	α_4 (degree)	Calculated THD (%)
5	6.4594	21.1923	37.6257	59.2605	9.1055
10	6.4594	21.1156	37.4450	58.8427	9.0620
20	6.4594	20.9621	37.0851	58.0218	8.9913
25	6.4594	20.8854	36.9057	57.6184	8.9642
40	6.4594	20.6556	36.1702	56.4341	8.9161
48	6.4594	20.5332	36.0861	55.8173	8.9107

After 17 iterations, the optimized switching angles and THD are achieved. The output voltage and harmonic spectrum using proposed method and HH method are presented in Fig. 7. Fig. 7(a) reveals that the proposed method generates 16.39% THDs while the HH method produces 17.48% as depicted in Fig. 7(b). The reduction in THD using the proposed method is approximately 6.23%. Besides, compared to the existing HH method, the proposed method increases the fundamental voltage by about 5.5%. From Fig. 7(c) and Fig. 7(d), it is also seen that the harmonic spectrum of output voltage of five level inverter using HH method contains odd harmonics at a significant level which may lead to increased motor heating, reduced efficiency, and even motor failure over time. On the other hand, the harmonic spectrum using the proposed method doesn't contain any even harmonics and it reduces significant harmonic contents above 15th order harmonics.

B. CASE STUDY 2: 9-LEVEL INVERTER

For 9-level inverter four optimized switching angles are calculated using proposed method are tabulated in Table 9.

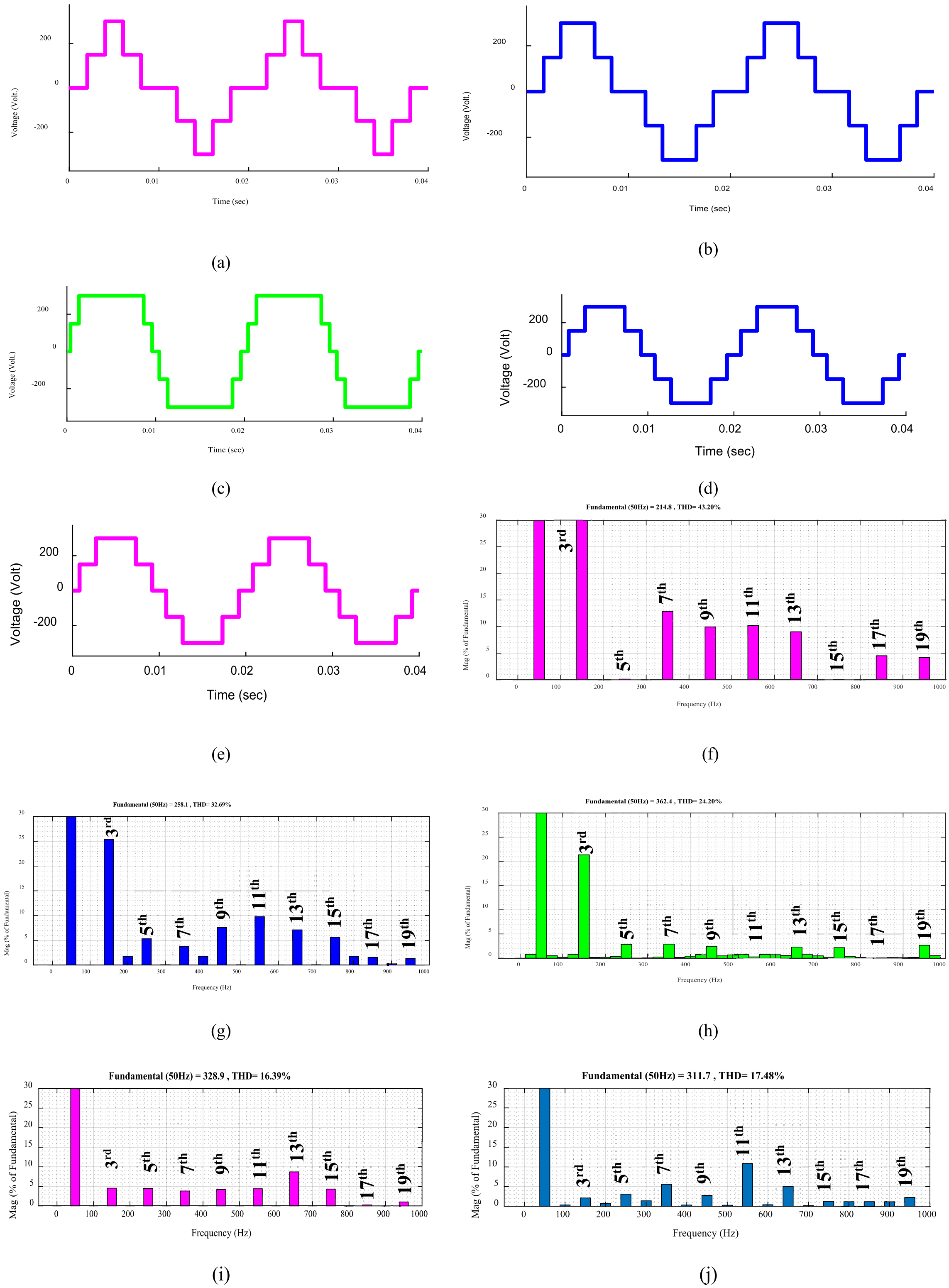

FIGURE 7. Simulation result of 5-level inverter for constant R load. Voltage waveform using (a) equal phase method, (b) half equal phase method, (c) feed forward method (d) using half height method (e) using proposed method, and harmonic spectrum (f) using equal phase method (g) using half equal phase method (h) using feed forward method (i) using proposed method (j) using half height method.

Fig. 8 shows simulation outcomes for the nine-level inverter utilizing both the new method and conventional techniques.

Fig. 8(a) and Fig. 8(b) depict the output voltage waveforms of the nine-level inverter using the equal phase and half-equal

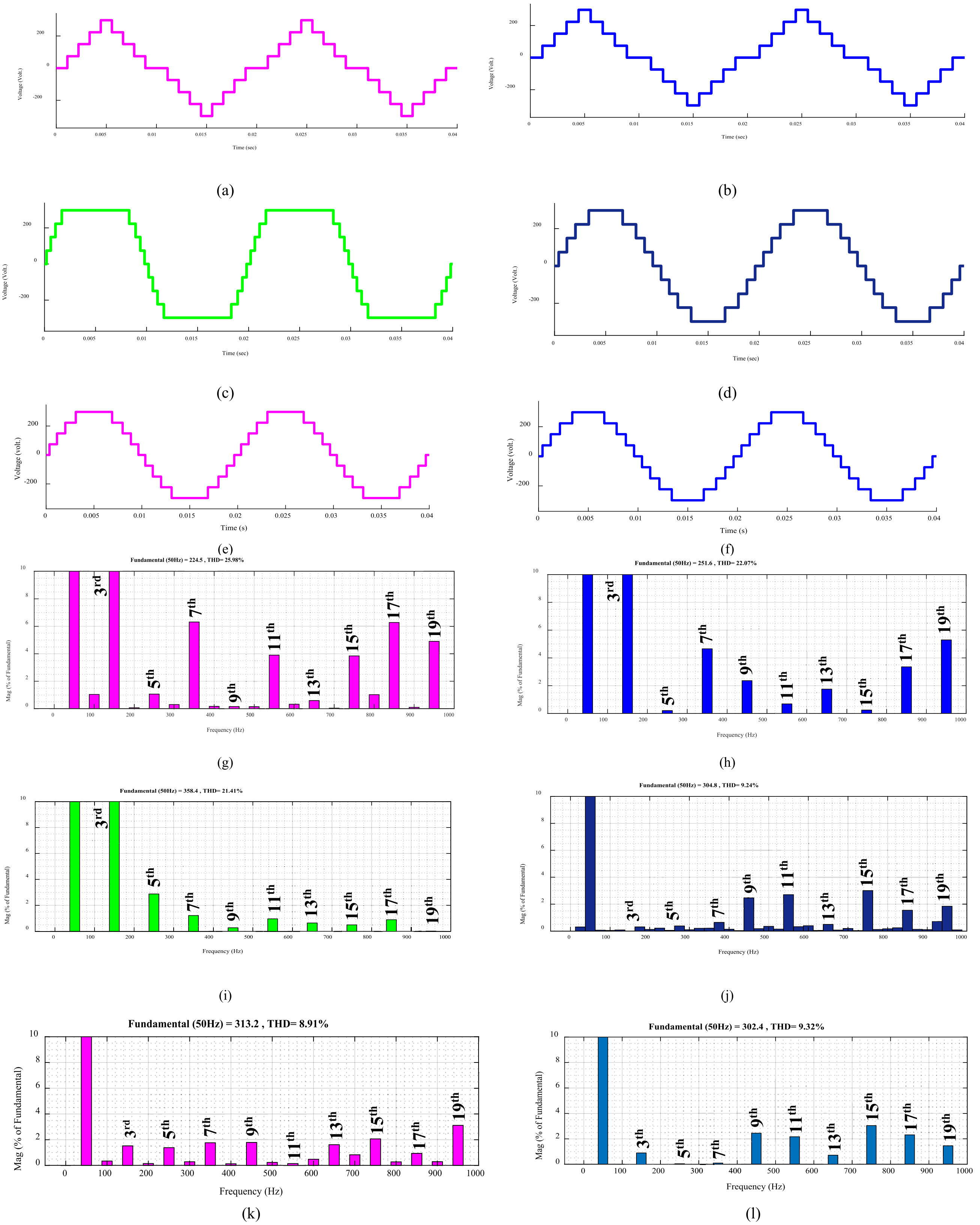

FIGURE 8. Simulation result of 9-level inverter for constant R load. Voltage waveform using (a) equal phase method, (b) half equal phase method, (c) feed forward method (d) selective harmonic elimination method (e) proposed method (f) half height method. Harmonic spectrum using (g) equal phase method (h) half equal phase method (i) feed forward method (j) selective harmonic elimination method (k) proposed method (l) half height method.

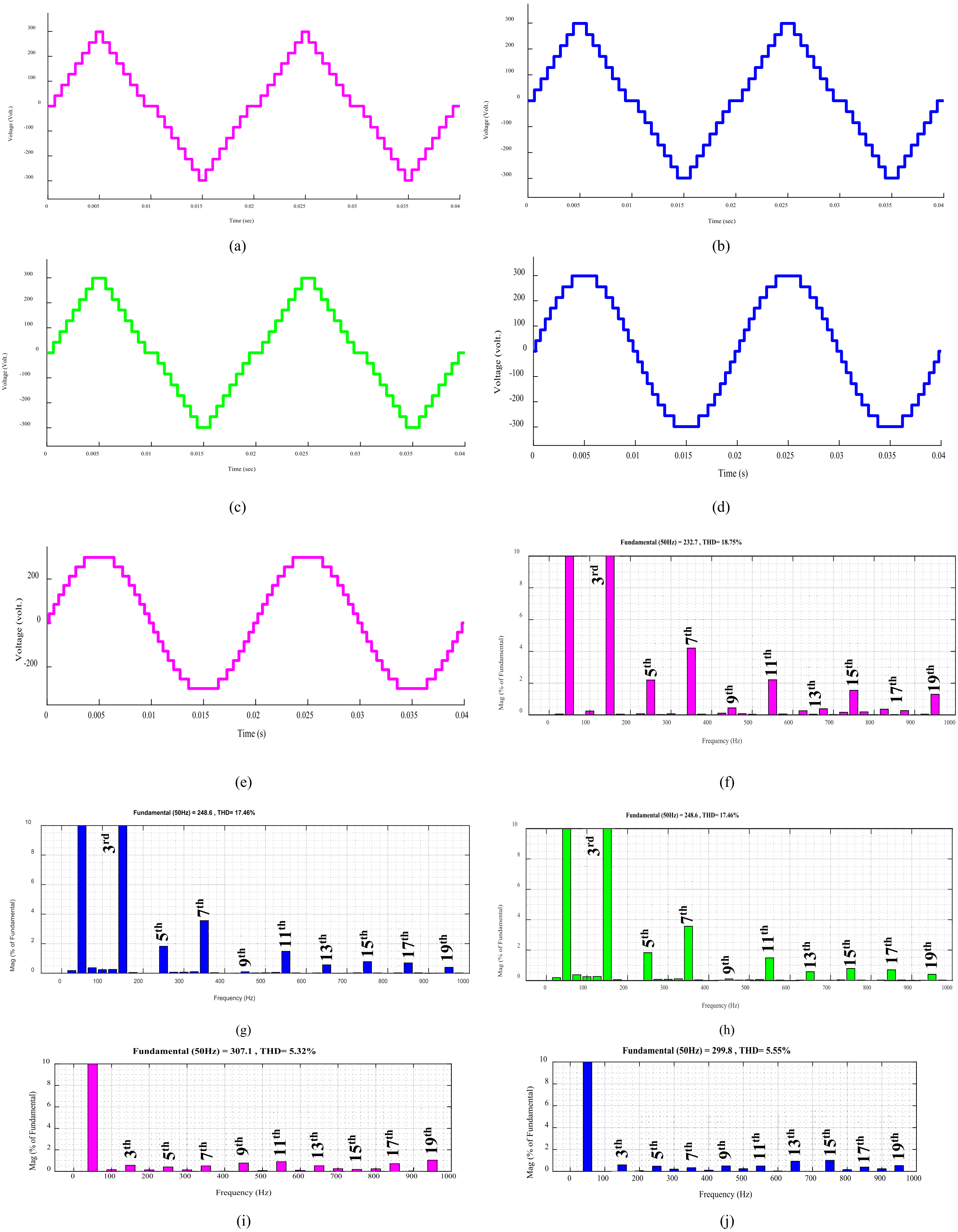

FIGURE 9. Simulation result of 15-level inverter for constant R load. Voltage waveform using (a) equal phase method, (b) half equal phase method, (c) feed forward method (d) half height method (e) proposed method. Harmonic spectrum using (f) equal phase method (g) half equal phase method (h) feed forward method (i) proposed method (j) half height method.

TABLE 10. Calculated THD and switching angles of 15-level inverter using proposed switching angle calculation method.

No. of iterations	α_1 (degree)	α_2 (degree)	α_3 (degree)	α_4 (degree)	α_5 (degree)	α_6 (degree)	α_7 (degree)	Calculated THD (%)
5	3.6858	11.9215	20.4174	29.4157	39.3035	50.8698	66.6354	5.3832
10	3.6858	11.8797	20.3301	29.2749	39.0923	50.5467	66.0238	5.3527
15	3.6858	11.8379	20.2429	29.1342	38.8817	50.2258	65.4265	5.3312
25	3.6858	11.7542	20.0685	28.8535	38.4623	49.5903	64.2710	5.3159

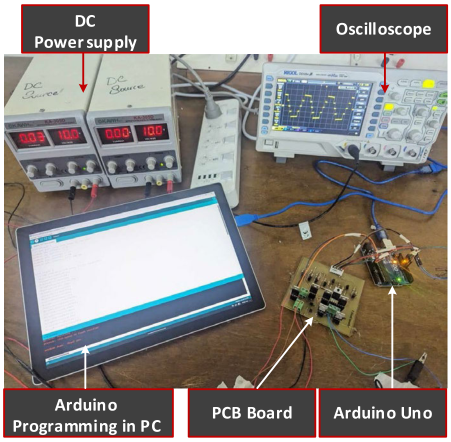

FIGURE 10. Experimental setup of the proposed approach.

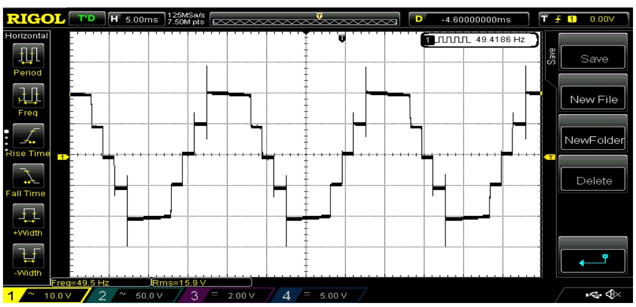

FIGURE 11. Output voltage of symmetric five-level inverter using proposed switching angle calculation method.

TABLE 11. Experimental parameters.

S. No.	Parameters	Model no.	Ratings
1	DC source	PL-3003T	30 V, 3A
2	MOSFET	IRF540N, IRF9530	33 A, 100 V
3	Diodes	1N4007	1000 V, 1 A
4	Controller	Arduino UNO	-
5	Load	Resistive	220 Ω
6	Modulation technique		NR, ANN based SHE, EP, HEP, HH, FF and proposed method

phase methods, respectively. While the half-equal phase method marginally enhances voltage quality, it falls short of delivering substantial improvements. The harmonic spectra of both topologies are shown in Fig. 8(g) and Fig. 8(h), respectively. Output voltage quality and THD performance exhibit slight enhancements in the feed-forward and selective harmonic elimination methods, as evident in Fig. 8(c), Fig. 8 (d), Fig. 8(i), and Fig. 8(j). The selective harmonic elimination method yields a THD value of approximately 9.24% and the widely adopted half-height method yields a THD of 9.32% shown in Fig. 8(f) and Fig. 8(l), respectively. The proposed topology demonstrates significant improvements in output voltage and harmonic spectrum for the 9-level inverter, as depicted in Fig. 8(e) and Fig. 8(k). This proves the superiority of the new method in reducing overall THD by up to 4.4% and enhancing fundamental voltage compared to the half-height method.

C. CASE STUDY 3: 15-LEVEL INVERTER

Table 10 shows the switching angles of 15-level inverter for different iterations. It depicts the pattern of the switching changes by increasing the number of iterations. Here, total seven switching angles are optimized by using proposed algorithm. After 25 iteration, the optimized switching angles and THD are obtained. The outcomes of the optimized switching angles are (i) reduced overall total harmonic distortion (ii) increased fundamental voltage, and (iii) reduced harmonic components above 9^{th} harmonic. The simulation results of 15-level inverter using proposed switching angle calculation method and HH method are shown in Fig. 9(a) and Fig. 9(b), respectively. From these Fig. 9(a) and Fig. 9(b), it is seen that the proposed switching angle calculation method reduces the overall total harmonic distortion to a significant amount and also increases the fundamental voltage. Almost 4.3% THD is reduced by using the proposed method as depicted in Fig. 9(c). It is also seen that the proposed switching angle calculation method reduces a significant amount of total harmonic distortion from 9^{th} harmonic to 15^{th} harmonic as shown in Fig. 9(d). For this reason, the overall THDs is reduced in the proposed method.

VII. EXPERIMENTAL RESULTS AND DISCUSSION

A scaled-down prototype is developed to demonstrate the efficacy of the optimal switching angles. Experimental parameters and technical details of components are shown in Table 11. In this experiment, pMOS transistors are employed for switches S_1, S_2, S_5, and S_6, while nMOS transistors are utilized for switches S_3 and S_4.

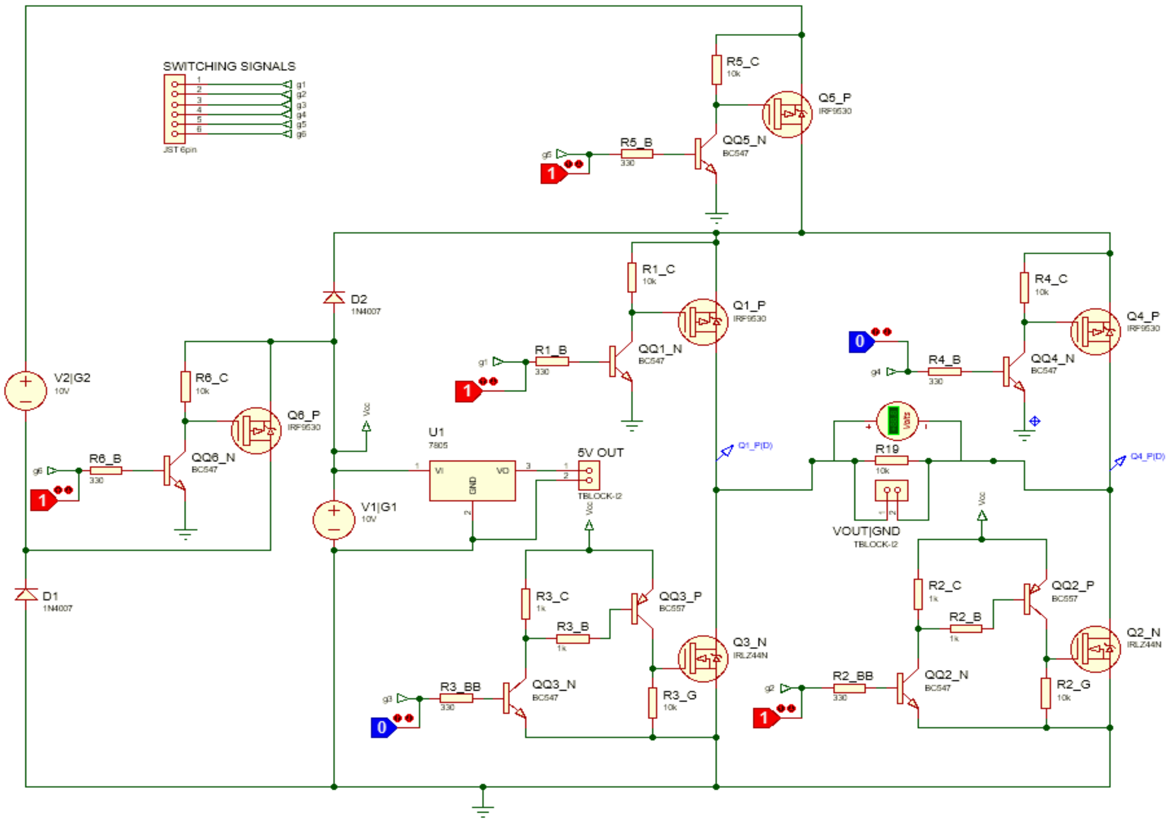

FIGURE 12. Hardware circuit diagram of symmetric 5-level inverter using proteus.

TABLE 12. Comparative analysis among different switching angle calculation methods.

Switching angle Calculation method	Case Study 1 (5-level inverter) Fundamental voltage gain	Case Study 1 (5-level inverter) THD (%)	Case Study 2 (9-level inverter) Fundamental voltage gain	Case Study 2 (9-level inverter) THD (%)	Case Study 3 (15-level inverter) Fundamental voltage gain	Case Study 3 (15-level inverter) THD (%)
Equal phase (EP) [32], [19]	0.71	42.89	0.82	22.05	0.78	18.62
Half equal phase (HEP) [19]	0.87	31.92	0.8	16.54	0.83	17.48
Half height (HH) [19]	1.03	17.60	1.008	9.36	0.998	5.56
Feed forward (FF) [19]	1.207	23.80		21.46	1.2	20.61
Newton Raphson based SHE [33]	1.206	26.76	1	10.20	-	-
ANN based SHE [34], [27]	1.087	19.50	-	-	-	-
Nearest level control (NLC) [35]	1.03	17.60	0.98	9.75	0.998	5.56
Triangular number series method (TNSM) [36]	1.12	17.69	-	-	-	-
Proposed	1.093	16.39	1.044	8.91	1.023	5.32

Fig. 10 shows the experimental configuration of the suggested topology. The Arduino Uno microcontroller device is employed for the generation of firing pulses. The resulting output responses are presented Fig. 11 which is quite similar to simulation result as shown in Fig. 6(e). Slight discrepancies between hardware and simulation results arises due to several reasons like component variability, parasitic elements, model accuracy, gate driver limitations, temperature effects, and external factors during both simulation and hardware testing phases.

Fig. 12 presents the comprehensive hardware diagram. In the case of the pMOS, the Arduino pulses are delivered via a BC 547 transistor, whereas the Arduino pulses are directed to the nMOS using a 330Ω resistor, as depicted in Fig. 10. It is to be mentioned here that pMOS transistors serve as pull-up devices because they conduct when the input signal is low, making them ideal for connecting to the power supply (V_{DD}). Conversely, nMOS transistors function as pull-down devices because they conduct when the input signal is high, suitable for connecting to ground (GND). This setup enables the creation of paths to either V_{DD} or GND based on the input signal. Considering this, pMOS and nMOS devices are utilized.

VIII. COMPARATIVE ANALYSIS

In this section, a comparative analysis among different switching angle calculation methods has been presented. The

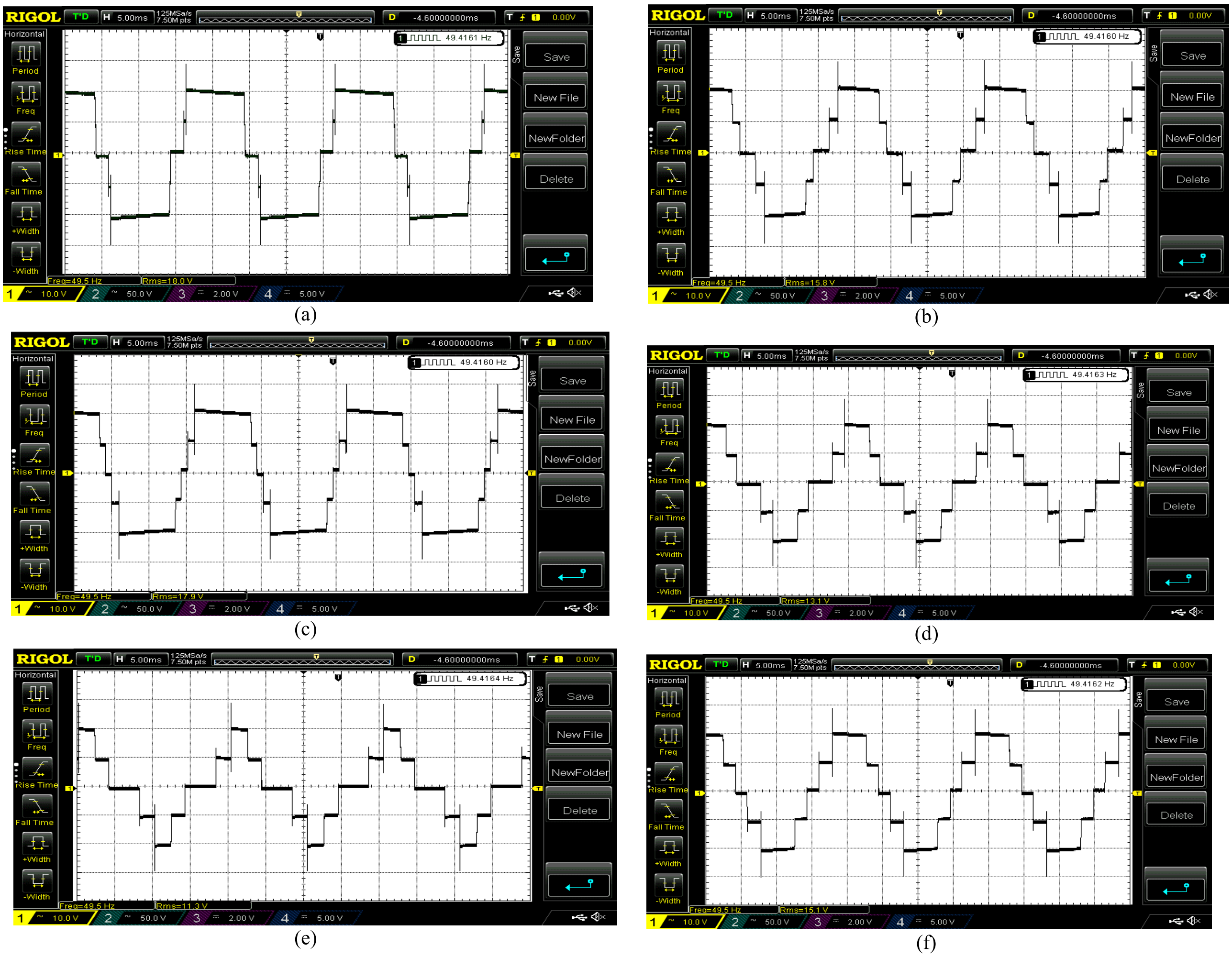

FIGURE 13. Experimental output of symmetric 5-level inverter using (a) newton Raphson based SHE (b) ANN based SHE (c) equal phase (d) half equal phase (e) feed forward (f) half height method.

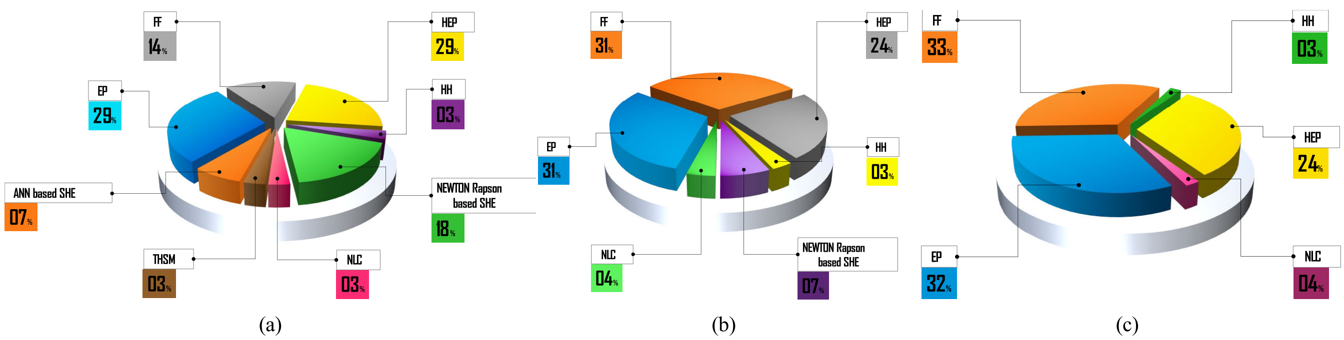

FIGURE 14. THD reduction of proposed topology with respect to other topologies based on: (a) case study 1, (b) case study 2, (c) case study 3.

comparison parameters are: fundamental voltage gain and total harmonic distortion as shown in Table 11.

Fig. 13 demonstrates the experimental result of symmetric five-level inverter using (a) NRA, (b) ANN based SHE, (c) EP method, (d) HEP method, (e) FF method, and (f) HH method. Their fundamental voltage gain and THD values obtained from recent publications are tabulated. For comparative purposes, output voltage quality of other two higher levels inverters i.e., (i) 9-level and (ii) 15-level inverter outputs are also analyzed. From the past records it is observed that incase of 5-level inverter, feed forward (FF) and Newton-Raphson based SHE method produce appreciably higher value of fundamental voltage (voltage gain ≈ 1.2). However, their voltage quality is worse with higher value of THD (≈ 25%).

Half-height, ANN based SHE, Triangular number series method (TNSM), and NLC method produce moderate fundamental output voltage (voltage gain ≈ 1.03) with better quality THD (≈ 17.6%). The proposed technique outperforms with combination of fundamental output voltage (voltage gain ≈ 1.093) and with a better quality THD (≈ 16.39%). In case of higher number of voltage levels inverters, the proposed method maintains the best performance with regard to fundamental voltage gain and total harmonic distortion. Compared to other switching techniques, the percentage reduction of THD by using proposed switching technique is shown in Fig. 14.

IX. CONCLUSION

This research presents a novel approach for calculating the switching angle in order to enhance the performance of a five-level inverter. The proposed approach demonstrates a reduction in total harmonic distortion when compared to the half-height method. Additionally, it decreases the complexity level and iteration number of the improved nearest level-controlled technique. The complete simulation is conducted using MATLAB/Simulink platform. To assess the accuracy of the suggested approach for calculating switching angles, two factors are considered: total harmonic distortions, and fundamental voltage. Based on the analysis of simulation and experimental outcomes, it is evident that the proposed switching scheme improves the output voltage quality by reducing total harmonic distortions while concurrently enhances the fundamental voltage in comparison to existing topologies. Because of its outstanding attributes viz simplicity in calculation, initial value free and faster calculation process, while producing high quality output voltage, this switching method can be adopted for high power multi-level inverters. Determination of switching losses and comparative analysis with other low frequency switching techniques, to be included in the future studies.

REFERENCES

[1] N. Prabaharan and K. Palanisamy, ''A comprehensive review on reduced switch multilevel inverter topologies, modulation techniques and applications,'' *Renew. Sustain. Energy Rev.*, vol. 76, pp. 1248–1282, Sep. 2017.

[2] R. Barzegarkhoo, M. Farhangi, R. P. Aguilera, S. S. Lee, F. Blaabjerg, and Y. P. Siwakoti, ''Common-ground grid-connected five-level transformerless inverter with integrated dynamic voltage boosting feature,'' *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 10, no. 6, pp. 6661–6672, Dec. 2022.

[3] B. Guo, X. Zhang, M. Su, H. Ma, Y. Yang, and Y. P. Siwakoti, ''A single-phase common-ground five-level transformerless inverter with low component count for PV applications,'' *IEEE Trans. Ind. Electron.*, vol. 70, no. 3, pp. 2662–2674, Mar. 2023.

[4] S. T. Meraj, S. S. Yu, M. S. Rahman, K. Hasan, M. S. H. Lipu, and H. Trinh, ''Energy management schemes, challenges and impacts of emerging inverter technology for renewable energy integration towards grid decarbonization,'' *J. Cleaner Prod.*, vol. 405, Jun. 2023, Art. no. 137002.

[5] M. Sarebanzadeh, M. A. Hosseinzadeh, C. Garcia, E. Babaei, S. Islam, and J. Rodriguez, ''Reduced switch multilevel inverter topologies for renewable energy sources,'' *IEEE Access*, vol. 9, pp. 120580–120595, 2021.

[6] S. T. Meraj, S. S. Yu, M. S. Rahman, A. A. Arefin, M. S. H. Lipu, and H. Trinh, ''A novel extendable multilevel inverter for efficient energy conversion with fewer power components: Configuration and experimental validation,'' *Int. J. Circuit Theory Appl.*, Dec. 2023.

[7] M. S. B. Arif, Z. Sarwer, M. D. Siddique, S. Md. Ayob, A. Iqbal, and S. Mekhilef, ''Asymmetrical multilevel inverter topology with low total standing voltage and reduced switches count,'' *Int. J. Circuit Theory Appl.*, vol. 49, no. 6, pp. 1757–1775, Jun. 2021.

[8] A. Poorfakhraei, M. Narimani, and A. Emadi, ''A review of modulation and control techniques for multilevel inverters in traction applications,'' *IEEE Access*, vol. 9, pp. 24187–24204, 2021.

[9] S. T. Meraj, M. S. A. Rahman, N. Z. Yahaya, P. J. Ker, T. M. Hossain, M. S. H. Lipu, K. M. Muttaqi, and M. A. Hannan, ''A pencil shaped 9-Level multilevel inverter with voltage boosting ability: Configuration and experimental investigation,'' *IEEE Access*, vol. 10, pp. 111310–111321, 2022.

[10] U. R. Muthyala and A. Dhabale, ''Comparative analysis of switching angle calculation methods for multilevel inverters,'' *Int. Trans. Electr. Energy Syst.*, vol. 31, no. 8, Aug. 2021, Art. no. e12978.

[11] T. Jing, A. Maklakov, A. Radionov, V. Gasiyarov, and Y. Liang, ''Formulations, solving algorithms, existing problems and future challenges of pre-programmed PWM techniques for high-power AFE converters: A comprehensive review,'' *Energies*, vol. 15, no. 5, p. 1696, Feb. 2022.

[12] K. Chenchireddy and V. Jegathesan, ''A review paper on the elimination of low-order harmonics in multilevel inverters using different modulation techniques,'' *Inven. Commun. Comput. Technol.*, vol. 2020, pp. 961–971, 2021.

[13] M. Al-Hitmi, S. Ahmad, A. Iqbal, S. Padmanaban, and I. Ashraf, ''Selective harmonic elimination in a wide modulation range using modified Newton-raphson and pattern generation methods for a multilevel inverter,'' *Energies*, vol. 11, no. 2, p. 458, Feb. 2018.

[14] M. Tarafdar Hagh, H. Taghizadeh, and K. Razi, ''Harmonic minimization in multilevel inverters using modified species-based particle swarm optimization,'' *IEEE Trans. Power Electron.*, vol. 24, no. 10, pp. 2259–2267, Oct. 2009.

[15] A. Kavousi, B. Vahidi, R. Salehi, M. K. Bakhshizadeh, N. Farokhnia, and S. H. Fathi, ''Application of the bee algorithm for selective harmonic elimination strategy in multilevel inverters,'' *IEEE Trans. Power Electron.*, vol. 27, no. 4, pp. 1689–1696, Apr. 2012.

[16] H. Taghizadeh and M. Tarafdar Hagh, ''Harmonic elimination of cascade multilevel inverters with nonequal DC sources using particle swarm optimization,'' *IEEE Trans. Ind. Electron.*, vol. 57, no. 11, pp. 3678–3684, Nov. 2010.

[17] C. Li, S. Yang, and T. T. Nguyen, ''A self-learning particle swarm optimizer for global optimization problems,'' *IEEE Trans. Syst. Man, Cybern., Part B*, vol. 42, no. 3, pp. 627–646, Jun. 2012.

[18] M. Marín-Reyes, J. Aguayo-Alquicira, and S. E. De León-Aldaco, ''Calculation of optimal switching angles for a multilevel inverter using NR, PSO, and GA—A comparison,'' *Eur. J. Electr. Eng.*, vol. 22, nos. 4–5, pp. 349–355, Oct. 2020.

[19] U. R. Muthyala and A. Dhabale, ''A new switching angle calculation method for a symmetrical multilevel inverter,'' in *Proc. IEEE Int. Conf. Power Electron., Smart Grid Renew. Energy (PESGRE)*, Jan. 2020, pp. 1–6.

[20] M. T. Islam, H. H. Fayek, E. Rusu, and M. F. Rahman, ''A novel hexagonal-shaped multilevel inverter with reduced switches for grid-integrated photovoltaic system,'' *Sustainability*, vol. 13, no. 21, p. 12018, Oct. 2021.

[21] M. T. Islam, M. A. Alam, M. S. H. Lipu, K. Hasan, S. T. Meraj, H. Masrur, and M. F. Rahman, ''A single DC source five-level switched capacitor inverter for grid-integrated solar photovoltaic system: Modeling and performance investigation,'' *Sustainability*, vol. 15, no. 10, p. 8405, May 2023.

[22] M. H. Nguyen and S. Kwak, ''Nearest-level control method with improved output quality for modular multilevel converters,'' *IEEE Access*, vol. 8, pp. 110237–110250, 2020.

[23] P. L. Kamani and M. A. Mulla, ''Simplified SHE pulse-amplitude modulation for multilevel inverters,'' *IET Power Electron.*, vol. 11, no. 14, pp. 2191–2197, Nov. 2018.

[24] V. Jayakumar, B. Chokkalingam, and J. L. Munda, ''A comprehensive review on space vector modulation techniques for neutral point clamped multi-level inverters,'' *IEEE Access*, vol. 9, pp. 112104–112144, 2021.

[25] J. Islam, S. T. Meraj, A. Masaoud, M. A. Mahmud, A. Nazir, M. A. Kabir, M. M. Hossain, and F. Mumtaz, "Opposition-based quantum bat algorithm to eliminate lower-order harmonics of multilevel inverters," *IEEE Access*, vol. 9, pp. 103610–103626, 2021.

[26] A. R. Kumar, M. S. Bhaskar, U. Subramaniam, D. Almakhles, S. Padmanaban, and J. Bo-Holm Nielsen, "An improved harmonics mitigation scheme for a modular multilevel converter," *IEEE Access*, vol. 7, pp. 147244–147255, 2019.

[27] A. E. Toubal Maamar, M. Helaimi, R. Taleb, M. Kermadi, and S. Mekhilef, "A neural network-based selective harmonic elimination scheme for five-level inverter," *Int. J. Circuit Theory Appl.*, vol. 50, no. 1, pp. 298–316, Jan. 2022.

[28] M. T. Islam, M. R. Islam, M. F. Rahman, M. R. Kiran, and A. S. M. R. Hasan, "A novel asymmetric multilevel inverter with phase disposed switching technique for grid integration of solar photovoltaic systems," in *Proc. IEEE Region 10 Symp. (TENSYMP)*, Jun. 2020, pp. 726–729.

[29] F. L. Luo and H. Ye, *Advanced DC/AC Inverters: Applications in Renewable Energy*. Boca Raton, FL, USA: CRC Press, 2017.

[30] S. Kumar Dash, B. Nayak, and J. Ballav Sahu, "Selective harmonic elimination of an eleven level inverter using whale optimization technique," *Int. J. Power Electron. Drive Syst. (IJPEDS)*, vol. 9, no. 4, p. 1944, Dec. 2018.

[31] L. Sheng, S. Q. Qian, Y. Q. Ye, and Y. H. Wu, "An improved immune algorithm for optimizing the pulse width modulation control sequence of inverters," *Eng. Optim.*, vol. 49, no. 9, pp. 1463–1482, Sep. 2017.

[32] F. Armi, L. Manai, and M. Besbes, "FPGA implementation of selective harmonic elimination controlled asymmetrical cascaded nine levels inverter using newton raphson algorithm," in *Proc. Eng. Technol. (PET)*, Liège, Belgium, 2016, pp. 377–382.

[33] S. T. Meraj, A. Ahmed, L. K. Haw, A. Arif, and A. Masaoud, "DSP based implementation of SHE-PWM for cross-switched multilevel inverter," in *Proc. IEEE 15th Int. Colloq. Signal Process. Appl. (CSPA)*, Mar. 2019, pp. 54–59.

[34] M. Rasheed, R. Omar, M. Sulaiman, W. Abd Halim, and M. M. A. Alakkad, "Analysis of a switching angle calculation by ANN for nine level inverter apply into experimental case study with elimination of lower and higher order harmonics," *Indonesian J. Electr. Eng. Comput. Sci.*, vol. 20, no. 2, p. 948, Nov. 2020.

[35] S. K. Yadav, N. Mishra, and B. Singh, "Multilevel converter with nearest level control for integrating solar photovoltaic system," *IEEE Trans. Ind. Appl.*, vol. 58, no. 4, pp. 5117–5126, Jul. 2022.

[36] U. R. Muthyala and A. Dhabale, "Numerical series based switching angle calculation for multilevel inverters," in *Proc. IEEE 1st Int. Conf. Smart Technol. Power, Energy Control (STPEC)*, Sep. 2020, pp. 1–6.

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