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RESEARCH ARTICLE

Simplified High-Efficiency Soldering Method for the Fabrication of Devices on Empty Substrate Integrated Waveguides

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ABSTRACT It is well-known that Empty Substrate Integrated Waveguides allow not only the integration of classic waveguides, such as rectangular waveguides, into a printed circuit board maintaining the quality of traditional waveguide devices, but also keeping in these circuits the advantages of planar devices: low cost, high integration and mass production capabilities. Nevertheless, a critical point to consider in the success of manufacturing these devices is the soldering of metal covers that close the structure and create the waveguide. This paper presents a new soldering process that simplifies the former procedures, making it easier and reducing economic and time costs. To validate this new assembling procedure, two prototypes have been manufactured and measured: a back-to-back from microstrip to ESIW, and a Ku-band filter; repeteability of the fabrication process has been proved and high performance results have been obtained.

INDEX TERMS Covers, soldering, ESIW, low cost, low loss, efficiency, fabrication.

I. INTRODUCTION

Empty substrate integrated waveguides (ESIW) [1], [2] are created by integrating a rectangular waveguide on a printed circuit board (PCB). This allows for more compact and integrated designs, with better performance than classical planar solutions and a substantial improvement in terms of cost compared to traditional waveguides.

To build an ESIW, a rectangular hole (in the shape of the H-plane of the entire guided structure to be manufactured) is drilled in a PCB or central layer of the waveguide. This hole is metallised to form the sidewalls of the waveguide on the inner edges of the hole made in the substrate. Finally, to finish forming the waveguide structure, metal covers are placed to close the hole. The placement of these covers is critical, because in order to sustain the propagation of the fundamental mode of the guide without significant losses and other pernicious effects (unwanted resonances), it is necessary to ensure that the conductivity is excellent and uniformly maintained among the covers and the central layer along the whole waveguide. A complete description of manufacturing processes can be found in the initial ESIW paper [1], whereas specific details and the equipment involved in the fabrication of ESIW is given in [3].

To ensure the electrical continuity, the covers are soldered to the central layer with tin. In the first devices made in this technology, to carry out this soldering, tin paste was simply deposited around the central layer orifice on both sides (top and bottom), the covers were placed on the paste, the structure was pressed and aligned with a set of screws and, finally, the tin paste was melted using a reflow oven (see Fig. 1).

This strategy works well, in fact we can find several perfectly functional devices made in this way [1], [4], [5], [6], [7], [8], but it has occasional failures that it would be very interesting to minimise. The main problems of this strategy are the difficulty of the uniform distribution of the

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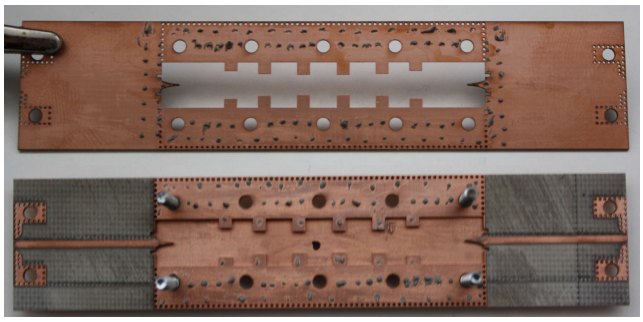


FIGURE 1. Solder paste deposition on the central layer and screw alignment on a Ka-band filter made with ESIW technology.

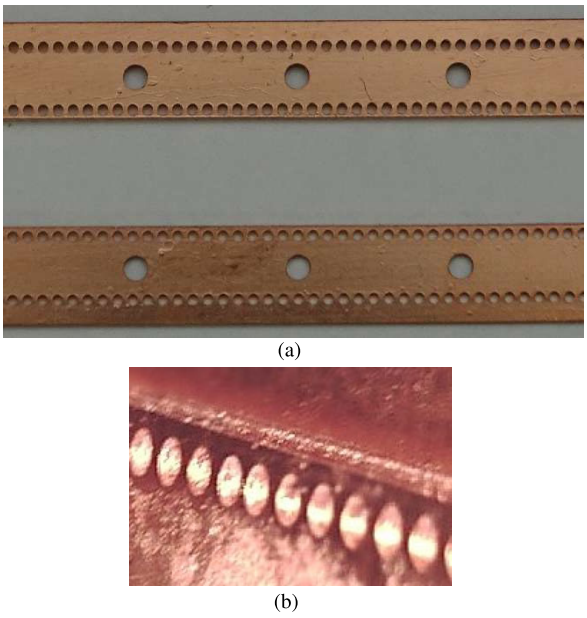


FIGURE 2. Soldering vias to maximise the number of successful prototypes in the soldering phase. (a) Surrounding the guide in the central layer. (b) Detail of the soldering vias.

solder paste and the non-uniform pressure of the screws in the soldering phase. These two factors mean that the molten solder may not be evenly distributed, leaving gaps between the covers and the central layer. If these gaps are completely closed between the layers, there are no consequences, but if they open up to the guide, they spoil its continuity, form unwanted couplings with the guide and the resulting device does not work properly. Furthermore, there is a notable escalation in surface roughness, concomitant with the emergence of unintended adverse effects [9], [10], [11]. It can also happen that the tin paste overflows into the guide, which also impairs its function. This solution has also been used with the term bumping to force small cavities between plates that are joined by solder bumps and can be useful for radiant devices, but with the disadvantage that the thickness of the cavity is difficult to control and not very homogeneous, as it varies depending on the temperature and the time the device is in the reflow oven [12].

A possible alternative way to avoid the use of tin paste would be the use of intermediate sheets of no-flow prepeg, which, if suitably mechanised, would be used to bond the covers to the central layer at high temperature by means of a press. The problem now is that the prepeg material is non-conductive, so to force electrical continuity between layers it is necessary to add a perimeter of metallised vias to all layers [13]. Thus, although soldering is avoided and the separation between layers is now homogeneous, non-conductive materials are added which can increase losses, complicate the manufacturing process and make the devices more expensive.

A possible solution to these problems is proposed in [9] using an efficient soldering technique. To ensure that the tin gets as close as possible to the vertical walls of the central layer without overflowing inside it, vias are added around the waveguide to guide the tin to the area to be soldered (see Fig. 2), given that the solder paste is introduced through these vias (which are designed according to the principles stated in [14]). This means that even if there are bubbles between the layers, they do not connect to the waveguide and do not affect its operation, and also prevents the tin from overflowing. Although the strategy works well and generates high success rates, it complicates fabrication, as it provides the best results when combined with a press to ensure proximity between the solder vias of the different layers (covers and central layer) and adds a large number of metallised vias to the design; this makes prototypes more expensive and increases manufacturing times.

It is widely demonstrated in the literature, for example in [15] and [16], that in all types of empty planar waveguides one of the main critical points that increase the losses and impair the performance of the devices is the attainment of electrical continuity, whether through conductive holes or by a proper soldering technique to close the cavity with its covers. In fact, despite the importance of the former, it is very rare to find in the papers available in the literature the way the planar devices are built in detail; after an exhaustive search just a few include information about how the cavity is closed: the majority uses several screws and nuts without mentioning if soldering is required or not [17], [18], some make use of soldering vias and screws [19], others just soldering vias and a reflow oven or a press [9], or only soldering in a reflow oven [1], or even prepreg layers with metallised vias [13], [20].

Usually, circuit design is the main aspect considered to achieve a good performance, but the fabrication process is of paramount importance to make an optimum device that fulfills the desired performance. Hence, this work brings the focus to the fabrication process by presenting a new simple and efficient way of soldering the covers to the ESIW central layer. In this proposal, there is no need for guiding vias and no press or reflow oven, which makes the fabrication of these prototypes more affordable for laboratories with scarce financial resources. In fact, with this approach, the covers can be soldered simply with a tin soldering iron available

in any electronics lab. In addition, the resulting covers are smaller than in previous designs and therefore reduce the weight of the devices. Also, because they are smaller, their manufacturing cost is lower.

II. NEW SOLDERING PROCESS FOR COVERS ON ESIW DEVICES

As mentioned in the introduction, the main challenge in sealing the ESIW structure with its covers is to ensure a good and uniform conductivity between the covers and the ESIW central layer. In [9], this continuity is ensured by distributing a series of metallised vias along the contour of the guide, through which the tin paste is then injected. For this strategy to work well, a press is needed to compact the structure well while heating it to allow the tin paste to melt and diffuse through the holes near the ESIW. It is also possible to press with screws and melt the tin paste using a reflow oven, although with a lower success rate. In any case, the equipment required is expensive and makes it difficult to access device fabrication in this technology in low-budget laboratories.

The ideal situation would be that the cover could be attached to the central layer with the means available in any electronics laboratory, such as a simple tin soldering iron. For this, another way has to be found to solve the problem avoided by the soldering vias of [9], i.e. to bring the tin as close as possible to the guide structure without it overflowing into the waveguide structure.

The problem of tin distribution occurs because it is not possible to access the solder area, as the cover itself prevents this. This is because the cover completely overlaps the central layer. This has been done in the devices presented so far, both in ESIW technology (some examples can be found in [1], [4], [5], [6], [7], [8]), and in other similar technologies such as AFSIW (some examples in [21], [22], [23], [24]).

Since the problem is that it is not possible to access the area of interest for soldering, the simplest solution is to vary the geometry of the cover in such a way that access is possible. The modification of the cover geometry must not affect the boundary conditions in the waveguide. Both conditions can be achieved with a cover whose contour matches as closely as possible the outer contour of the ESIW guides, i.e. the outer contour of the hole in the central layer of the structure (see Fig. 3). The ideal situation would be achieved with a cover that exactly fills the hole that allows the ESIW to be created in the central layer. Although this is the ideal situation, in practice it is not advisable. If the cover is tightened all the way, it may be possible that the cover is pushed slightly into the hole, modifying the ESIW. It is more advisable to allow a slight overlap, as shown in Fig. 3, as small as the manufacturing resolution permits (the resolution of the cutting system that allows the cover and the hole in the central layer of the ESIW to be manufactured).

With this proposal of covers, the soldering process is simplified to the maximum, as it is possible to fix the cover with a tin paste line along the contour of the cover by simply using a soldering iron. The results obtained with this modified

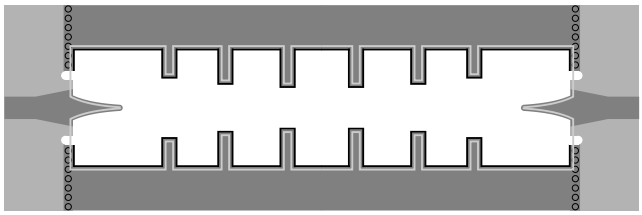


FIGURE 3. Example of a cover (light grey outline) fitted to the geometry of a coupled cavity ESIW filter of 5th order as in the results section.

cover are excellent, as shown in the results section. These are results of comparable quality to press and soldering vias assemblies, but achieved with a manufacturing and assembly process that is much simpler and cheaper to carry out.

III. RESULTS AND DISCUSSION

In order to verify that the proposed soldering strategy provides the expected results, two different ESIW devices have been fabricated. These devices have been aligned with the transition of [25], although slightly modified. The distribution of the vias isolating the sides of the substrate and the overlap distribution has been slightly changed, as shown in figures 4(a) and 4(b). These changes facilitate the soldering procedure and have virtually no effect on the transition performance, so that the design procedure of [25] can be applied directly without changes.

The prototypes have been manufactured using a Rogers 4003C substrate of 0.813 mm thickness and 18 microns of copper metallisation for the central layer; the overlap between the covers and the central layer has been only 0.3 mm. For the covers, two different manufacturing series were carried out: in one of the series, the covers were fully metallised (as well as the central layer, by means of a galvanic electroplating process and using the same Rogers 4003C substrate), while in the other one, the covers were not metallised again after being mechanised (so they kept non-conductive parts and a FR4 type substrate with a single metallised side facing the inside of the ESIW was used for this purpose). The transition in Fig. 4(b) has been specifically designed for both cases of metallised and non-metallised covers, applying the procedure of [25], to feed from a 50 Ω microstrip ESIW devices (a = 15.7988 mm) at Ku-band. The transition dimensions for both cases can be found in Table 1.

TABLE 1. Dimensions (in mm) of the microstrip to ESIW transition used in the prototypes, both for metallised (met) and non-metallised (non) covers.

Dim.	Value-met	Value-non	Dim.	Value-met	Value-non
d_f	1	1	w_{tms}	2.6603	2.5750
d_v	1	1	l_{tms}	2.1194	2.2409
s_v	1.5	1.5	w_{ti}	2.5650	2.5788
w_{ms}	1.85195	1.85195	l_t	6.3341	6.3918
a	15.7988	15.7988	w_{ir}	8.4619	8.5899
w_{tm}	0.5	0.5	c^*	0.2626	0.2591
s_l	1.5	1.5	–	–	–

The first device that was fabricated to test the soldering of the covers was a simple back-to-back of the transition.

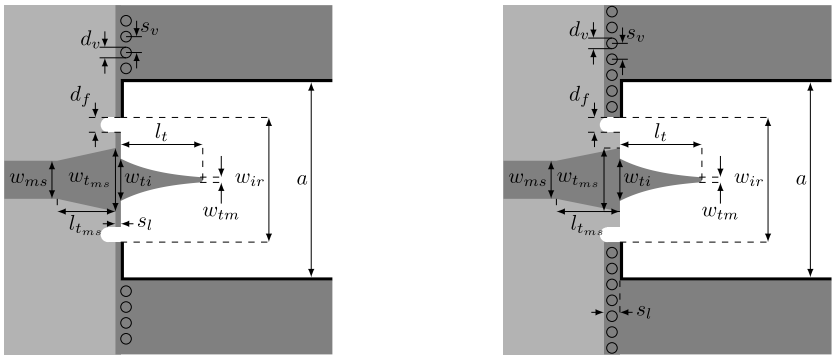


FIGURE 4. (a) Transition from [25]. (b) Slightly modified transition to facilitate cover soldering. In both figures only the top face of the central layer of the transition (without covers) is shown. The dark grey colour indicates the areas where the surface metallisation of the board has not been removed; the light grey colour the areas where the PCB dielectric substrate is exposed without surface metallisation; the white colour the empty areas (no substrate at all); and the metallisation of the board edges is indicated by a thick black line. The underside of this layer is identical, the only difference being that it has no substrate areas exposed (no metallisation).

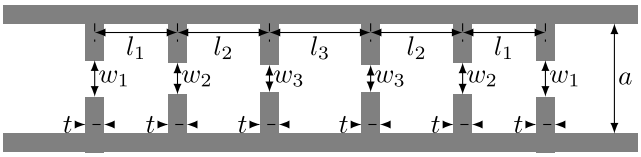


FIGURE 5. Schematic of the 5-cavity ESIW filter.

TABLE 2. Dimensions of the 5-cavity ESIW filter at 13 GHz in mm.

Dim.	Value	Dim.	Value
t	2.0000	w_3	5.4318
a	15.7988	l_1	15.5838
w_1	8.9127	l_2	17.2861
w_2	5.9963	l_3	17.4756

Specifically, a 150 mm long empty waveguide section fed at the inlet and outlet by a transition as shown in Fig. 4(b) was fabricated.

For the second device, a Chebyshev filter of 5th order, 0.01 dB ripple, centered at 13 GHz and with a bandwidth of 300 MHz, has been integrated within an identical device like the mentioned back-to-back. The structure and dimensions of the filter can be seen in Fig. 5 and Table 2.

Figures 6(a), 6(b) and 6(c) show some images of the fabricated devices before and after the soldering of the covers.

Fig. 6(c) clearly shows how the fixation of the cover can be achieved by simply distributing a tin paste line around the contour of the cover. To ensure correct positioning of the covers prior to soldering, only four alignment holes are used in the central layer (as shown in Fig. 6(c)), into which pins are inserted, and removed after the soldering, to act as limits and prevent movement of the cover during the start of soldering.

As mentioned above, both circuits have been produced in two different production series: one with completely metallised covers and the other without re-metallising after mechanising. The manual soldering process is similar in both cases: the cover is aligned with the pins, a line of tin paste is deposited next to the edge of the cover and the soldering iron is passed over to melt the tin paste while the cover is lightly pressed to ensure the flatness of the cover.

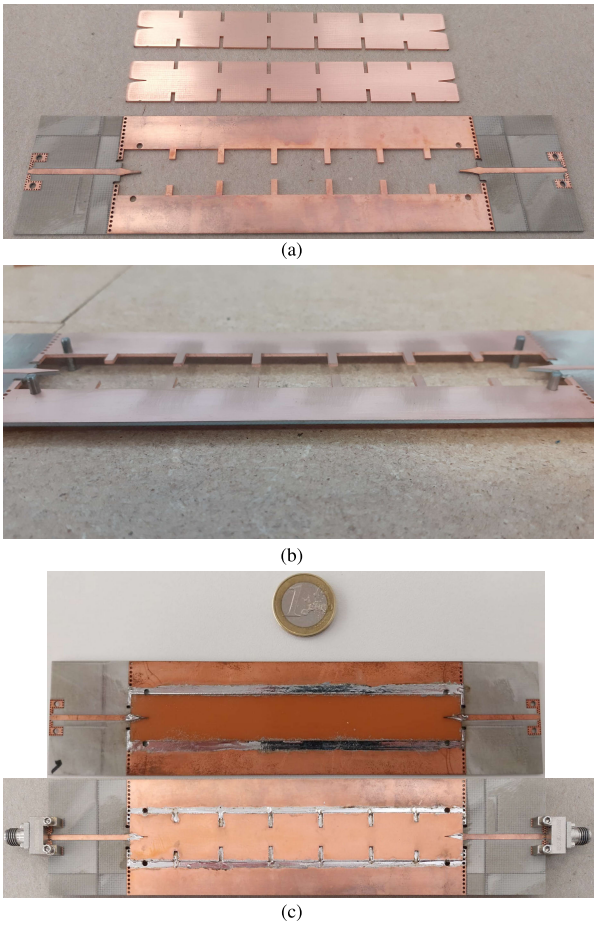
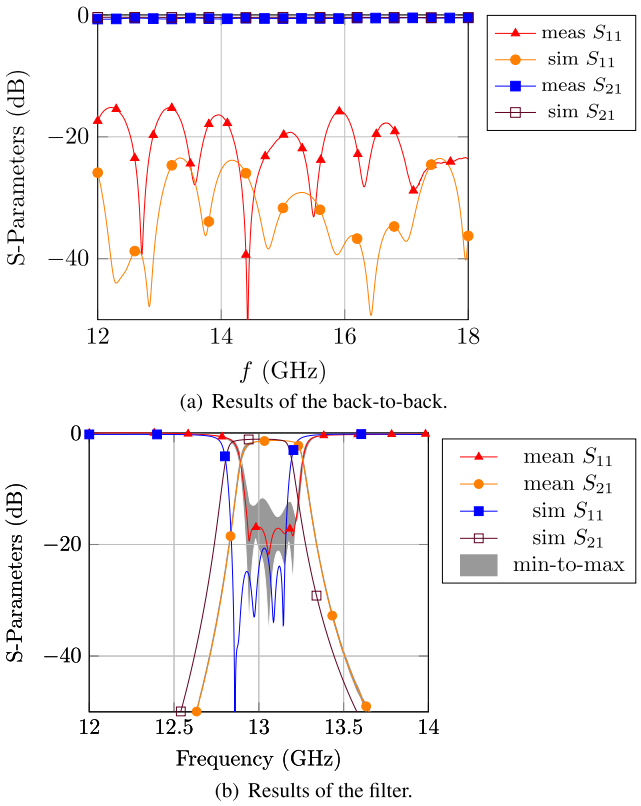


FIGURE 6. (a) Covers and central layer (top view) of the fabricated filter. (b) Detail of the use of the alignment pins. (c) Soldered prototypes of one of the back-to-back and one of the filters fabricated in this work.



(a) Results of the back-to-back.

(b) Results of the filter.

FIGURE 7. Comparison of prototype measurements with simulated results obtained with CST Studio Suite.

In the case of non-metallised covers, a little more expertise is required from the technician, as greater care is needed to ensure connectivity between the cover and the central layer. Whether with metallised or non-metallised covers, the electrical contact obtained is excellent and, consequently, so is the performance of the devices. Although functional circuits can be achieved easily and cost-effectively with both types of covers, the solution with metallised covers is mainly recommended, especially in the case of non-rectangular covers and covers with bends (e.g. in the filter); this is due to the fact that this avoids possible cavities with lack of soldering and facilitates the work of the technicians.

Fig. 7 shows the measurements of the prototypes and the results of the simulations performed with CST Studio Suite 2023. In the measurements, the reference planes in both port 1 and 2 of each prototype have been brought to the start of the microstrip to ESIW transition using a purpose-built microstrip calibration kit as in [25]; in CST, the results have been simulated with the same reference planes. It can be seen that the results agree very well with the measurements. For the back-to-back case, measured results are extremely similar independently of using metallised or non-metallised covers; hence, for the sake of clarity, only the case of non-metallised covers is plotted in Fig.7(a) to be compared with the simulation; maximum measured insertion loss is 0.7 *dB*, which is very low and similar to the simulation, whereas measured return loss is better than 15 *dB*, which is somewhat higher than the simulation, mainly due to the possible unsealed cavities that may remain for using non-metallised covers.

In the case of the filter, after several tests, it has been found that the results are better when the covers are fully metallised, due to the reasons already mentioned. For the three devices manufactured in the filter series with metallised covers, the comparison between the simulation and the average of the measurements is shown in Fig. 7(b), together with the maximum dispersion of measured values of reflection and transmission (shaded in grey). Except for S_{11} in the passband, the scattering of values is imperceptible, indicating a high repeatability of the fabrication and soldering processes. The average measured values and the simulated ones are very similar, taking into account that a slight frequency shift is observed (due to a systematic manufacturing error most probably caused by the oblique cut produced by the laser cutter used to mechanise the ESIW in the central layer; since this cut has a high degree of repeatability, the frequency shift of all the filters is the same, so it can be easily corrected in the design phase and thus obtain filters centered on the desired design frequency).

Once this new manufacturing and soldering method has been validated for ESIW circuits, an analysis of advantages and disadvantages can be made in comparison with the previous soldering methods. The advantages of the first method, that of distributing the tin directly between the different layers, are that good electrical contact is achieved between layers and that the manufacturing process is acceptably fast and economical as there are no metallised soldering vias to be made; on the other hand, it has several disadvantages, such as uncertainty in the thickness of the soldered layers due to possible air bubbles that may remain resilient, low levels of repeatability and reliability due to the uneven distribution of tin paste between the different layers, and frequent overflows of tin inside the cavity, apart from requiring a reflow oven to complete the soldering process. In summary, this initial method, although apparently cheap and fast, is in practice very expensive and ineffective due to the lack of repeatability, which means that several attempts have to be made before a working prototype is achieved. The second method, proposed in [9], has several advantages in that it achieves very good electrical contact between layers, a high degree of repeatability and reliability, as the amount and distribution of tin paste is controllable before the final soldering process, which also gives greater control over the final thickness of the layers; in contrast, the disadvantages of this method are the large number of soldering vias to be drilled and metallised in all the layers, which lengthens the manufacturing time and increases the costs, as well as the need for specific equipment to properly execute the process by means of a high temperature press. Finally, the new method described in this work has the advantages of providing excellent electrical contact between layers, a very high rate of repeatability and reliability, as well as an exact

TABLE 3. Qualitative comparison of different fabrication procedures.

Ref.	Type	Device	f (GHz)	Fabrication	Connectivity	Easiness	Fabric. Time	Fabric. Cost	Weight	Equipment	Repeatability
[this]	**ESIW**	**waveguide / filter**	**13**	**new soldering proc.**	**very good**	**very easy**	**short**	**low**	**low**	**soldering iron**	**high**
[1]	ESIW	filter	11	basic soldering	worst	equivalent	shorter	equivalent	equivalent	reflow oven	much worst
[9]	ESIW	filter	13	soldering vias	equivalent	more difficult	longer	equivalent	equivalent	reflow oven / press	equivalent
[18]	ESIW	waveguide	15	screws	worst	more difficult	longer	more expensive	higher	screwdriver	worst
[19]	ESIW	waveguide	15	screws+soldering	worst	more difficult	longer	more expensive	higher	soldering iron+screwdriver	worst
[13]	ESIW	antenna	11.75	prepeg+vias	worst	more difficult	longer	more expensive	equivalent	press	worst
[20]	AFSIW	waveguide	140	prepeg+soldering	equivalent	more difficult	longer	more expensive	equivalent	press	equivalent

control of the final thickness of the device (which is especially important in multilayer devices [26]), since the tin paste is not deposited between the layers, but by joining them at the edge of the covers to the central layer; although it is not necessary for the covers to be completely metallised, it is recommended that they be metallised to facilitate the soldering process and further ensure electrical connectivity. In addition, there is no need for metallised soldering vias or specific equipment, just a simple laboratory soldering iron is sufficient to carry out the soldering process at room temperature, thus greatly reducing the economic and time costs. The only disadvantage of this new method is the fact of fitting the cover with the minimum possible overlap to the central layer, which is solved by knowing the cutting precision of the mechanising machine and by simple alignment holes to position the cover before proceeding to deposit the tin paste line around the cover.

To make clearer the advantages of this new fabrication process, Table 3 includes a qualitative comparison of devices fabricated according to different procedures. The procedure stated in this work is taken as the comparison reference in terms of connectivity, easiness of fabrication, fabrication time and cost, weight of the device, estimated repeatability and equipment required. Data in the table reveal that this new soldering procedure is the easiest one that provides extremely good connectivity without incrementing the weight of the device, maintaining short fabrication time with low fabrication cost and at the same time guarantees a high degree of repeatability with the only required equipment of a soldering iron.

IV. CONCLUSION

In this work, it has been possible to modify the structure of the covers of an ESIW device so that its assembly by soldering requires as little equipment as possible, in this case, a simple tin soldering iron. The fabricated prototypes provide results comparable to those achieved with more elaborate soldering procedures (multiple metallised vias for guiding the tin) and which require expensive equipment (reflow ovens or presses). This simplification of the ESIW device fabrication process lowers the cost and shortens the fabrication process times, thus making this technology more affordable for development in smaller laboratories, which can then take advantage of the benefits of this technology: high quality devices fully integrated on PCBs, easily fabricated with classical PCB fabrication procedures and with performance results close to those expected for devices developed with classical waveguides.

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