IEEE Access
Multidisciplinary | Rapid Review | Open Access Journal

Received 30 March 2024, accepted 17 April 2024, date of publication 22 April 2024, date of current version 29 April 2024.

Digital Object Identifier 10.1109/ACCESS.2024.3391796

RESEARCH ARTICLE

Finite-Control-Set Model Predictive Control for Single-Phase CHB 5-Level Inverter as an Active Power Filter With Discrete-Time FO-PI DC-Link Controller

ROBERTO MORALES-CAPORAL[1], (Senior Member, IEEE), EDMUNDO BONILLA-HUERTA[1], RAFAEL ORDOÑEZ-FLORES[1], ANDRES A. VALDEZ-FERNANDEZ[2], (Senior Member, IEEE), AND JOSE DE JESUS RANGEL-MAGDALENO[3], (Senior Member, IEEE)

[1]Division of Graduate Studies and Research, Tecnológico Nacional de México–Instituto Tecnológico de Apizaco, Tlaxcala 90300, Mexico
[2]School of Science, Universidad Autónoma de San Luis Potosí, San Luis Potosí 78295, Mexico
[3]Department of Electronics, National Institute of Astrophysics, Optics and Electronics, Puebla 72840, Mexico

Corresponding author: Roberto Morales-Caporal (roberto.mc@apizaco.tecnm.mx)

This work was funded by Tecnológico Nacional de México (TecNM). Project No. 17531.23-P.

ABSTRACT This paper presents a finite-control-set model predictive control (FCS-MPC) with fractional-order proportional-integral (FO-PI) controller to regulate the dc-link voltage of a single–phase cascaded H–bridge (CHB) 5-level inverter working as a shunt active power filter (APF). By using the FCS-MPC scheme in a single–phase CHB multilevel inverter as an APF, it is possible to generate a compensation current that tracks its reference with maximum precision, in addition, it presents a quick dynamic reaction to disturbances. When the compensation current is injected into the electrical system, current harmonic distortions are effectively reduced. To simplify the number of evaluations in the algorithm, the voltages on the dc-link of each H-bridge are equalized by a redundant selection of switching states of the multilevel inverter. The discrete-time model of the single-phase shunt APF, the technique to generate the compensation current reference signal, and the developed FCS-MPC algorithm are explained in detail. Furthermore, to keep the dc-link voltage steady, with minimal disturbance, it is proposed to use a discrete-time FO-PI controller. The effectiveness of the proposed control scheme is investigated in steady-state, as well as dynamic transients caused by sudden load changes. The developed control algorithm is verified through experimental tests conducted on a 5 kVA single-phase CHB 5-level inverter-based shunt APF.

INDEX TERMS Discrete-time control systems, finite control set, fractional order control, model predictive control, multilevel converter, shunt active power filter.

I. INTRODUCTION

Non-linear electrical loads, such as lighting circuits, diode rectifiers, battery chargers, uninterruptible power supplies, voltage source inverters (VSIs), etc., connected to the electrical distribution network, generate harmonic pollution, resulting in a degradation of the power quality, in grid instability, and an increase in system losses [1]. To minimize these unwanted harmonics, it is necessary to include harmonic filters into the power system.

There are different types of harmonic filters on the market that depend on the nominal power and other parameters dependent on the electrical load. In fact, there are two main types of harmonic filters available: passive filters and active power filters (APFs) [2], [3]. What differentiates these two types of harmonic filters are the components used for their operation. Passive harmonic filters are mainly designed with resistors, inductors, and capacitors. While APFs use power electronic devices and digital systems.

The associate editor coordinating the review of this manuscript and approving it for publication was Fabian Khateb.

Nowadays, due to their flexibility, lower weight and volume, APFs are preferable to achieve an effective solution to current harmonic suppression and power factor correction [4]. There are mainly two types of APFs, series and shunt. However, shunt APF, compared to series APF, is the most widely used, because it more effectively suppress harmonic current issues [4], [5].

The shunt APF requires a VSI with capacitors as energy storage to generate and inject a compensation current to the grid, in opposite phase to the current harmonics generated by the non-linear electrical load. The main objective is that the compensation current generated and injected by the shunt APF returns the grid current to a sinusoidal waveform with a very low harmonic content. However, to achieve outstanding power quality improvement with the shunt AFP, a fast-response current controller must be designed so that the filter's current tracks the reference signal of the compensation current with maximum tracking precision.

A. CURRENT CONTROL OF THE SHUNT APF

The conventional solution to control the current of shunt APFs is through the use of a linear proportional-integral (PI) controller [6], [7], [8]. However, it has been documented that this solution is not the most satisfactory for controlling ac signals, particularly during transients. Therefore, to improve the behavior during transients, various researchers have proposed using other types of controllers, such as nonlinear controllers, e.g., the sliding mode control [9], [10], repetitive control [11], [12], [13], deadbeat control [14], [15], [16], model predictive control (MPC) [17], [18], [19], and artificial intelligence (AI) algorithms [20], [21], [22].

The sliding mode control strategy shows fast current loop dynamics, as well as relative ease to be implemented, however, it presents chattering.

The repetitive-based control scheme has the ability to perform selective harmonic compensation and effectively suppresses periodic disturbances, but in the case of non-periodic disturbances its performance decreases.

Even though the deadbeat control method presents very fast current loop dynamics, its response depends on system parameters and can introduce delays during its digital implementation, which can lead to cumulative errors.

The MPC scheme uses a discrete-time model of the system to predict its behavior for at least one sampling period into the future. Afterward, the voltage vector that must be applied by the VSI is the one that minimizes a cost function of the priorities of the control system. Among the main advantages of this algorithm are: 1) system constrains and nonlinearities can be explicitly considered in the optimization, 2) the algorithm considers the power switches in the optimization as constrains on the inputs, consequently, there is no need to use modulators. 3) When MPC is used in a shunt APF, it has the advantage that the current tracks the reference of the compensation current excellently and presents a quick reaction when there are sudden changes in the reference signal [23], [24]. The main drawbacks of this control strategy are that: it depends on the system parameters, and the optimization problem must be solved in real-time.

Lately, current controllers that use AI algorithms for shunt APF have also been introduced. These control methods are very efficient, they have the ability to self-learn and self-adjust. They also show excellent reference current tracking. However, during its design and implementation, a compromise must be found between its performance and its computational burden. Furthermore, for its correct implementation, high-end digital systems must be used.

B. VSI TOPOLOGY FOR THE SHUNT APF

Aiming to use lower capacity power electronic devices and to further improve power quality, in the last decade, the use of multilevel inverter topologies in three-phase APFs has been proposed, but their use can also be extended to single-phase APFs, as demonstrated in this paper.

Multilevel inverters offer numerous advantages as compared to the two-level VSIs [25], [26], [27]. Among the different multilevel inverter topologies, the cascaded H-bridge (CHB) topology is the most attractive due to its lower number of components, higher modularity and hardware scalability [28], [29], [30]. Another advantage of the multilevel inverter topology is that, as more H-bridge cells are connected, the number of voltage levels also increases in a staircase voltage waveform, obtaining a low voltage harmonic distortion at the output of the inverter. However, the number of voltage vectors that the VSI can generate also increases, resulting in a greater number of switching states. Therefore, to reduce the number of calculations necessary for the selection of the appropriate voltage vector to be generated by the VSI in the future sampling period, an optimization criterion must be applied in the MPC algorithm for a limited number of switching states. This optimization criterion in the literature is called finite-control-set (FCS) [31], [32]. The FCS strategy excludes redundant switching states without affecting the tracking accuracy of the reference current signal.

C. COMPENSATION CURRENT REFERENCE SIGNAL

The strategies for generating the compensation current reference signal in a shunt APF can be mainly divided into: direct and indirect methods [5], [24]. Direct methods use circuit analysis to generate the compensation current signal, are difficult to design, and require high-speed analog-to-digital converters (ADCs) for successful implementation. On the other hand, indirect methods must control one of the system parameters, commonly the dc-link voltage. This, for simplicity, is commonly done by means of a PI controller. However, in order to increase the quality of the compensation current reference signal, other advanced control techniques have also been studied. Techniques such as adaptive control [33], [34] and those based on AI algorithms [35], [36].

When the CHB VSI operates in a shunt APF, keeping the voltages on each of the dc-buses at the same value is a great challenge, since these are not generated by an external rectifier circuit designated for this task. The strategies reported by researchers to match dc-bus capacitor voltages can be classified into: 1) exploitation of repetitive switching states and 2) use of PWM signals [37].

In this research, the first strategy has been selected, since no PWM technique is used. For this, the process of increasing or decreasing the voltages of the dc-bus capacitors is considered to be slower than the process of tracking the offset current reference signal.

D. PURPOSE OF THE WORK AND ORGANIZATION

For various reasons, it is desirable to maintain high quality current and voltage waveforms with high power factor in electrical power distribution systems. And researchers continually propose different strategies to achieve high-quality electrical power waveforms, e.g., by installing shunt APFs.

These investigations have primarily been carried out with shunt APFs that use two-level VSIs. However, it has been shown that by using a multilevel inverter topology, power quality is further increased, higher power levels can be operated, and stress on the VSI's components is reduced. Therefore, in the present study, a single-phase CHB 5-level inverter is selected since it is desired to keep the cost, the algorithm complexity, and the computational burden low.

After having exhaustively reviewed of the different current control strategies for shunt APFs, the MPC scheme has been selected, mainly due to its discrete nature and low complexity. Furthermore, with this algorithm, an excellent and quick tracking of ac current is obtained when disturbances occur [38]. Nevertheless, to reduce the number of voltage vectors to be evaluated, it has been proposed to use the FCS technique as an optimization strategy. To do this, the switching states are exploited, so that, the voltages of the capacitors of the CHB multilevel inverter remain balanced, without degrading steady-state and dynamic-state performances.

Besides, in the case of the dc-link voltage control loop, different control strategies were also evaluated, and it was determined to implement a discrete-time PI$^{\lambda}$ controller. This controller shows low sensitivity to external disturbances and a memory effect.

An initial study of the proposed FCS-MPC scheme for single-phase shunt APF was presented in [39], where simulated results can be found. In this paper, the extended study, the digital implementation, and experimental results are presented. In summary, the main contributions of this paper are:

- By using the FCS-MPC scheme in a single-phase CHB inverter, high system dynamics performance is achieved with reduced harmonic distortion and guaranteed stability. (No similar study has been found in the available literature for single-phase shunt APF application).
- By using a multilevel topology, the waveforms of both voltage and current at the output of the inverter are improved. In addition, the stress on the power electronics components is reduced.
- Maintaining optimal dc-link voltage control is crucial in shunt APFs because capacitors are required to mitigate instantaneous active power. In this case, and to be consistent with the discrete nature of the system, it has been proposed to implement a discrete-time PI$^{\lambda}$ controller.
- Due to the self-capacity to maintain the voltage balance on the dc-buses, it is possible to minimize the switching losses and simplify the objectives of the cost function, thus simplifying the algorithm.
- Implementation of the developed algorithm in a prototype of a 5 kVA single-phase CHB 5-level inverter working as shunt APF.

The rest of the paper is organized as follows. In section II, the circuit diagram of the CHB 5-level inverter-based shunt APF and its discrete-time model are introduced. Section III explains the discrete implementation of the designed PI$^{\lambda}$ control for the dc-link, in Section IV, it is analyzed the proposed FCS-MPC scheme and the redundant switching strategy to balance the dc-buses. In Section V, first the experimental system setup is presented, and then the proposed control scheme is demonstrated through experimental results. Finally, the conclusions are given in Section VI.

II. SINGLE-PHASE CASCADED H-BRIDGE 5-LEVEL VSI-BASED SHUNT APF

A. DISCRETE-TIME MODEL

Fig. 1 shows the circuit diagram of the single-phase CHB 5-level VSI operating as a shunt APF. This is built based on two IGBT full H-bridges, each H-bridge has an independent capacitance of similar value, in this case, expressed as C_a and C_b. R_c and L_c represent the equivalent resistance and inductance of the shunt APF and R_s and L_s are the equivalent resistance and inductance of the grid, respectively.

In this electrical circuit, the grid voltage (v_s) supplies a nonlinear load, which consists of a single-phase diode H-bridge rectifier connected to a RC circuit.

The symbols i_c, i_s and i_L represent the compensation, grid and load currents, respectively.

The single-phase shunt APF operates in such a way that the generated i_c is injected into the common coupling point (CCP) to cancel unwanted current harmonics (i_h).

To perform mathematical modeling, the load impedance can be neglected, and only the filter and the grid impedance are considered [17], so that $L_e = L_s + L_c$ and $R_e = R_s + R_c$. Therefore, the mathematical model of the shunt APF can be expressed as

$$v_i = v_s + R_e i_c + L_e \frac{di_c}{dt} \tag{1}$$

To obtain the discrete-time model of the system without increasing the complexity of the algorithm, the simple direct

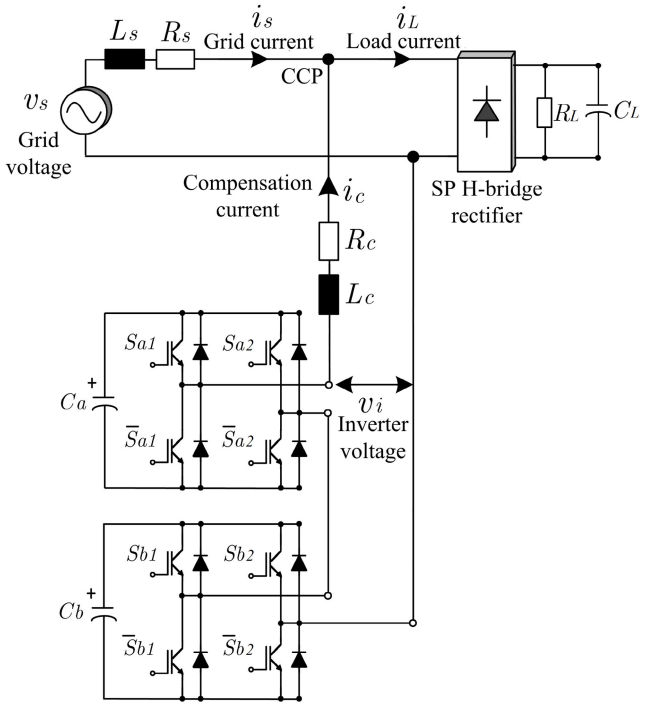

FIGURE 1. Circuit diagram of the single-phase CHB 5-level VSI as shunt APF.

TABLE 1. Output voltage vectors for the single-phase CHB 5-level VSI.

j	(S_a, S_b)	v_{ij}	$i_c > 0$		$i_c < 0$	
			V_{C_a}	V_{C_b}	V_{C_a}	V_{C_b}
1	$(1,1)$	$2V_{dc}$	↓	↓	↑	↑
2	$(0,1)$	V_{dc}	↑	↓	↓	↑
3	$(-1,1)$	0	↓	↓	↓	↓
4	$(1,0)$	V_{dc}	↓	↑	↑	↓
5	$(0,0)$	0	↓	↓	↓	↓
6	$(-1,0)$	$-V_{dc}$	↑	↓	↓	↑
7	$(1,-1)$	0	↓	↓	↓	↓
8	$(0,-1)$	$-V_{dc}$	↓	↑	↑	↓
9	$(-1,-1)$	$-2V_{dc}$	↑	↑	↓	↓

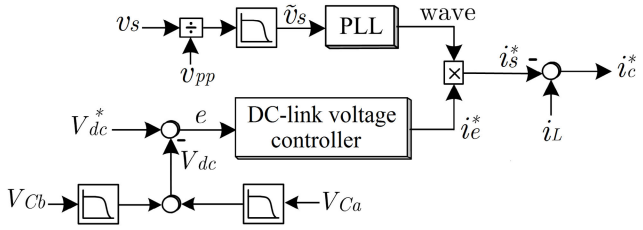

FIGURE 2. Block diagram to generate the i_c^*.

difference expression (forward Euler method) is used for the derivative, since a satisfactory approximation is obtained for first-order systems [38]. Therefore, considering a constant sampling period T_S, the discrete-time model of the system can be written as

$$\frac{i_c[k+1] - i_c[k]}{T_S} = \frac{1}{L_e}\left(v_i[k] - v_s[k] - R_e i_c[k]\right) \tag{2}$$

In (2), the voltage at the output of the inverter (v_i) takes on an implicit value that can be either negative, positive, or zero.

Then, the dynamics of both capacitors can be expressed as

$$C_a \frac{dV_{C_a}}{dt} = i_c \cdot \left(S_{a1} \cdot \bar{S}_{a2} - \bar{S}_{a1} \cdot S_{a2}\right) \tag{3}$$

$$C_b \frac{dV_{C_b}}{dt} = i_c \cdot \left(S_{b1} \cdot \bar{S}_{b2} - \bar{S}_{b1} \cdot S_{b2}\right) \tag{4}$$

Generalizing (3) and (4) to a discrete-time model, results

$$V_{C_x}[k+1] = V_{C_x}[k] - \frac{T_S}{C_x} i_c[k] \cdot \left(S_{x1} \cdot \bar{S}_{x2} - \bar{S}_{x1} \cdot S_{x2}\right) \tag{5}$$

where $x \in \{a, b\}$

B. OUTPUT VOLTAGE OF THE INVERTER

Considering that it is possible to maintain a constant voltage of the same value on the two capacitors, then v_i will show five levels, depending on the combination of the switching signals S_{x1}, S_{x2}, where $x \in \{a, b\}$, in addition $\bar{S}_{x1}$ and $\bar{S}_{x2}$, work complementary. So, v_i can be expressed as

$$v_i = V_{Ca}\left(S_{a1} - S_{a2}\right) + V_{Cb}\left(S_{b1} - S_{b2}\right) \tag{6}$$

following the discrete nature of the VSI, two new switching functions S_a and S_b can be defined as follows

$$S_a, S_b \in \{-1, 0, 1\} \tag{7}$$

With the used single-phase inverter topology, the v_i can be generated with 16 possible voltage vectors j of the 5-level VSI. To reduce the number of switching states of each power device between successive voltage steps and l transitions in case of non-successive l- steps to one, it is applied an optimization criterion [39]. This criterion of limiting the possible voltage vectors available without degrading system performance is called FCS. In this case, the optimization criterion considers that it is sufficient to use only two pairs of reiterative states (0, 1), (1, 0) and $(-1, 0)$, $(0, -1)$ to generate the voltage levels V_{dc} and $-V_{dc}$, respectively. And only three zero voltage vectors $(-1, 1)$, (0, 0) and $(1, -1)$ to obtain zero voltage at the output of the multilevel inverter.

The optimization strategy has the capacity to maintain a balanced voltage across both capacitor, for which the charging current flow is considered, as shown in Table 1. This selection of charge and discharge state of each capacitor will be explained in detail in subsection IV-B. Thus, the sixteen possible switching states are reduced to only nine switching states ($j = 1, \ldots, 9$), as shown in Table 1.

C. GENERATION OF THE COMPENSATION CURRENT SIGNAL

1) STRATEGY TO GENERATE THE I_C^*

Fig. 2 depicts a simplified block diagram of the used strategy to generate the reference signal of the compensation current i_c^*. The active power absorbed by the inverter is controlled by adjusting the amplitude of the active power

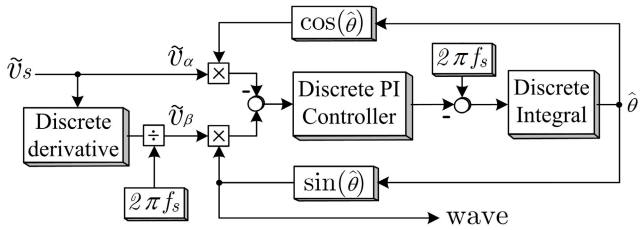

FIGURE 3. Structure of the used single-phase OSG-PLL.

reference signal (i_e^*) (in this case, by a dc-link controller). This amplitude must be synchronized with the v_s signal, with help of a signal obtained from a single-phase phase-locked loop (PLL), in this case, called "wave", in order to obtain a reference signal of the grid current i_s^*. Subsequently, the i_L is added to this signal to generate a suitable i_c^* [5].

Once the dc-link voltage (V_{dc}) (in this case, the addition of V_{Ca} and V_{Cb}) remains at its set level (V_{dc}^*), the generated i_c will be identical to i_h and they will cancel each other.

2) OSG-PLL

The use of the PLL is highly recommended to track the phase angle of the v_s and to match the phase of the i_s, since there is a possibility of grid voltage and frequency distortions e.g., in the case of weak grid condition and unbalanced grid impedance (in three-phase systems), which can lead to instabilities [12], [40]. Therefore, in this work, it has been proposed to use an orthogonal signal generation–based PLL (OSG-PLL) [41]. Figure 3 shows the basic structure of the OSG-PLL, where f_s and $\hat{\theta}$ represent the grid frequency and the estimate phase angle, respectively.

This structure has been selected because when implemented correctly, it produces a very accurate result [41], [42]. However, for its adequate digital implementation, it is necessary to use a numerical approximation to the derived function to obtain a useful orthogonal signal, which, in this case, has been done following the strategy described in [42], as well as to the design of the OSG-PLL's discrete-time PI controller. For the case of discrete integration, the trapezoidal method has been implemented.

The measured v_s must be, as far as possible, free of distor-tion and noise, so it is necessary to have a normalized and filtered $\tilde{v}_s$ signal before its use in the OSG-PLL. It is worth mentioning that, it is necessary to carefully match the order and cutoff frequency of the LPF (typically, a finite impulse response filter is used), to provide a satisfactory compromise between its distortion rejection performance and its speed.

III. DC-LINK VOLTAGE CONTROL

A. PI CONTROLLER

Fig. 4a) shows a simplified block diagram of the V_{dc} control loop for generating the compensation current signal, where the CC block represents the current control loop and the inverter. This block can be represented by a gain of value $H = v_{pp}/2V_{dc}^*$. This is done considering that V_{dc} remains constant with a minimum value of $v_{pp} = v_s\sqrt{2}$ [33].

To simplify the modeling, it is assumed that: 1) the dynamics of the current control loop is significantly faster with respect to the voltage control loop, 2) inverter nonlinearities are neglected.

The $s-$domain transfer function (TF) of the capacitors considering the gain of the power converter (see Fig. 4b), can be expressed by a first order system as

$$P(s) = \frac{H}{C_T s} \tag{8}$$

where $C_T = C_a C_b/(C_a + C_b)$. Likewise, the TF in the $s-$domain of the PI controller has the following form

$$C(s) = K_P + \frac{K_I}{s} \tag{9}$$

being K_P and K_I the controller gains. Then, the TF of the equivalent closed-loop system with the PI is given by

$$\frac{V_{dc}}{V_{dc}^*} = \frac{\frac{K_P H}{C_T}s + \frac{K_I H}{C_T}}{s^2 + \frac{K_P H}{C_T}s + \frac{K_I H}{C_T}} \tag{10}$$

In this second order system, the damping ratio ξ and the natural frequency ω_n can be derived as

$$\begin{cases} \xi = \dfrac{K_P}{2}\sqrt{\dfrac{H}{K_I C_T}} \\ \omega_n = \sqrt{\dfrac{K_I H}{C_T}} \end{cases} \tag{11}$$

gains K_P and K_I can be tuned by using the canonical form of the characteristic equation ($s^2 + 2\xi\omega_n s + \omega_n^2 = 0$). To simplify the study and considering that the dynamics of the V_{dc} does not need to be too fast, a damping ratio of $\xi = 1$ has been selected to obtain an underdamped system without oscillations.

To set the ω_n value, it is common to consider the settling time (t_s) of the step response, which can be approximated by $t_s \approx \frac{3.9}{\xi\omega_n}$ (for 2% tolerance). In order to guarantee a sufficiently fast response of the V_{dc} control loop, in this work, the t_s is adjusted to one and a half periods of the alternating grid signal, i.e., considering a grid frequency of $f_s = 60$ Hz, one and a half periods lasts 25 ms. Thus, a natural frequency of $\omega_n = 157$ rad/s was set.

Since the controller must be implemented discreetly, the Tustin transformation has been applied to (9), resulting in

$$C(z) = \frac{\left(K_P + K_I\frac{T_S}{2}\right) + \left(-K_P + K_I\frac{T_S}{2}\right)z^{-1}}{1 - z^{-1}} \tag{12}$$

by developing the inverse z-transform to (12), the following difference equation is obtained

$$\begin{aligned} u[k] = u[k-1] &+ K_P\left(e[k] - e[k-1]\right) \\ &+ K_I\frac{T_s}{2}\left(e[k] + e[k-1]\right) \end{aligned} \tag{13}$$

where $u[k]$ represents the controller output at the present moment, $u[k-1]$ represents the controller output one

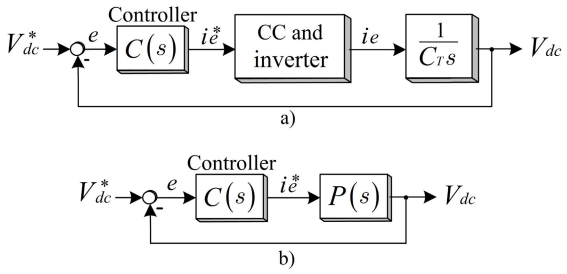

FIGURE 4. Block diagram of the V_{dc} control loop.

TABLE 2. Controller parameters.

Symbol	Parameter	Value
V_{dc}^*	140	V
T_S	70	μs
K_P	0.4396	
K_I	34.51	
λ	0.85	
$f_0(1-\lambda)$	1	
$f_1(1-\lambda)$	$-2(1-\lambda)$	
$f_2(1-\lambda)$	$2(1-\lambda)^2$	
$f_3(1-\lambda)$	$-\frac{4}{3}(1-\lambda)^3-\frac{2}{3}(1-\lambda)$	
$f_4(1-\lambda)$	$\frac{2}{3}(1-\lambda)^4+\frac{4}{3}(1-\lambda)^2$	
$f_5(1-\lambda)$	$-\frac{4}{15}(1-\lambda)^5-\frac{4}{3}(1-\lambda)^3-\frac{2}{5}(1-\lambda)$	

sampling period in the past, $e[k]$ and $e[k-1]$ are the present error and the previous error, respectively.

Performing the corresponding calculations with the values shown in Table 2, and considering the system parameters (see Table 3), and substituting these in (13), results in

$$u[k] = u[k-1] + 0.4396\,(e[k]-e[k-1]) + 0.0012079\,(e[k]+e[k-1]) \quad (14)$$

B. FO-PI CONTROLLER

The $s-$domain transfer function (TF) of the PI^λ controller can be expressed as

$$C(s) = K_P + \frac{K_I}{s^\lambda} \quad (15)$$

with λ being the integral order, and can have a real value between 0 and 2 [43]. To adjust the integral order, it must be considered that the lower its value, the slower the system response will be. On the other side, if λ increases, the system response also increases, but it becomes increasingly oscillatory. In this case, the value of the integral order was adjusted, by trial and error, to a value of $\lambda = 0.85$.

The TF of the PI^λ in $z-$domain when the Tustin transformation is applied to (15), can be expressed as

$$C(z) = K_P + K_I \left(\frac{2}{T_S}\right)^{-\lambda} \frac{1+z^{-1}}{1-z^{-1}} \cdot \sum_{n=0}^{N} f_n\,(1-\lambda)\,z^{-n} \quad (16)$$

where n is the number of memory units, which in this case has been restricted to $N = 5$. The coefficients $f_0(1-\lambda), \ldots, f_5(1-\lambda)$ are calculated as shown in Table 2 [43].

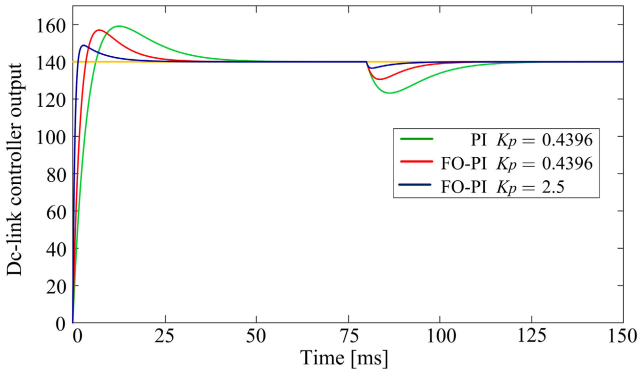

FIGURE 5. Responses of the closed-loop dc-link voltage systems with $V_{dc}^* = 140$ V and $T_S = 70$ μs.

By performing the inverse z-transform to (16), results in the following difference equation

$$u[k] = u[k-1] + K_P\,(e[k]-e[k-1]) + K_I \left(\frac{2}{T_S}\right)^{-\lambda} \cdot \sum_{n=0}^{N} f_n\,(1-\lambda)\,(e[k-n]+e[k-n-1]) \quad (17)$$

There are different methods in the literature for optimal adjustment of the FO-PI's gains, among which are the PSO strategy and genetic algorithms [43]. Nevertheless, it is also possible to perform an initial tuning from the PI control and then experimentally adjust the gains by trial and error [44].

So, in this case, to reduce the complexity of this task and considering that the voltage control loop does not react too quickly to disturbances (although high performance in steady-state is desired), the gains of the FO-PI controller have been tuned with the help of the PI controller. Then, developing the corresponding calculations with the values shown in Table 2, and considering the system parameters (see Table 3) in (17), gives

$$\begin{aligned} u[k] = u[k-1] &+ 0.4396(e[k]-e[k-1]) \\ &+ 0.005629(e[k]+e[k-1]) \\ &- 0.001688(e[k-1]+e[k-2]) \\ &+ 0.0002533(e[k-2]+e[k-3]) \\ &- 0.0005882(e[k-3]+e[k-4]) \\ &+ 0.0001707(e[k-4]+e[k-5]) \\ &- 0.0003631(e[k-5]+e[k-6]) \end{aligned} \quad (18)$$

An experimental adjustment was carried out by increasing the gain K_P, of the PI^λ controller, since, as this gain increases, the sensitivity of the controller to error increases. However, it should be noted that if the gain increases too much, the system tends to become unstable. In this case, it was adjusted to a value of $K_P = 2.5$, thus achieving better performance of the control system, as depicted in Fig. 5.

Fig. 5. shows the responses of the closed loop dc-link voltage systems with $V_{dc}^* = 140$ V and $T_S = 70$ μs (the selection of this sampling time is explained in detail

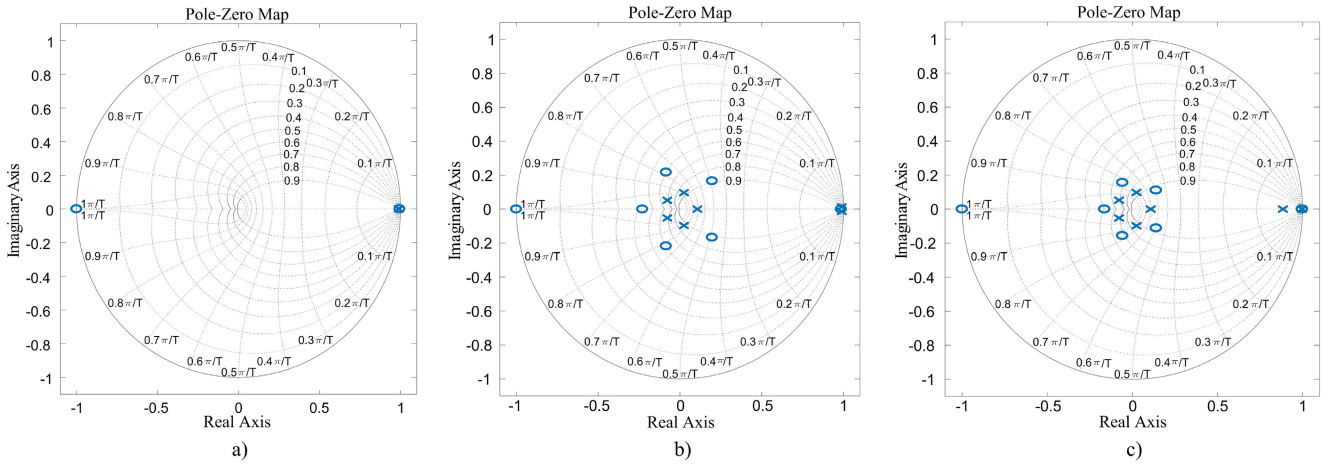

FIGURE 6. Pole-zero maps.

in subsection V-A2). At $t = 80$ ms, a disturbance of the same magnitude is applied, in order to analyze the transient response of the system.

Integral gains were not handled, since higher values of these can cause instability in the system.

C. STABILITY ANALYSIS

1) DISCRETE-TIME PI CONTROLLER

The discrete-time TF of the closed-loop system with the PI controller is as follows

$$\frac{V_{dc}}{V_{dc}^*} = \frac{0.011021 + 0.0000603z^{-1} - 0.010961z^{-2}}{1.011021 - 1.999939z^{-1} + 0.989038z^{-2}} \quad (19)$$

This discrete-time closed-loop system has two poles $\{0.9892, 0.9889\}$ and two zeros $\{-1.0, 0.9945\}$. According to the Nyquist stability criterion for discrete-time systems, this will depend on the location of the poles in the $z-$plane. The stability limit is the unit circle, with the poles within the unit circle being stable. Then, since all poles of (19) lie inside the unit circle (see Fig. 6a), the system is stable.

2) DISCRETE-TIME FO-PI CONTROLLER

The discrete-time TF of the closed-loop system with the PI$^\lambda$, and $K_P = 0.4396$ is given by as in (20), shown at the bottom of the page. This discrete-time TF has seven poles $\{0.9888 + j0.0145, 0.9888 - j0.0145, 0.1064 + j0.0, 0.0241 + j0.0968, 0.0241 - j0.0968, -0.0772 + j0.0521, -0.0772 - j0.0521\}$ and seven zeros $\{0.9849 + j0.0, -1.0 + j0.0, 0.1963 + j0.1665, 0.1963 - j0.1665, -0.2293 + j0.0, -0.0848 + j0.2176, -0.0848 - j0.2176\}$. Since all the poles of (20) are inside the unit circle (see Fig. 6b), the system is stable.

The discrete-time TF of the closed-loop system with the PI$^\lambda$, and $K_P = 2.5$ is derived as in (21), shown at the bottom of the page. This discrete-time TF also has seven poles $\{0.9972 + j0.0, 0.8844 + j0.0, 0.1080 + j0.0, 0.0241 + j0.0979, 0.0241 - j0.0979, -0.0779 + j0.0525, -0.0779 - j0.0525\}$ and also seven zeros $\{0.9973 + j0.0, -1.0 + j0.0, 0.1396 + j0.1113, 0.1396 - j0.1113, -0.1638 + j0.0, -0.0583 + j0.1563, -0.0583 - j0.1563\}$. Since in this discrete-time closed-loop system, all poles lie inside the unit circle (see Fig. 6c), the system is stable.

$$\frac{V_{dc}}{V_{dc}^*} = \frac{0.01113+0.000239z^{-1}-0.01092z^{-2}-0.0000442z^{-3}-0.0000188z^{-4}-0.0000152z^{-5}-0.0000138z^{-6}-0.00000907z^{-7}}{1.01113-1.9998z^{-1}+0.98907z^{-2}-0.0000442z^{-3}-0.0000188z^{-4}-0.0000152z^{-5}-0.0000138z^{-6}-0.00000907z^{-7}} \quad (20)$$

$$\frac{V_{dc}}{V_{dc}^*} = \frac{0.06264+0.000239z^{-1}-0.062437z^{-2}-0.0000442z^{-3}-0.0000188z^{-4}-0.0000152z^{-5}-0.0000138z^{-6}-0.00000907z^{-7}}{1.06264-1.99976z^{-1}+0.937562z^{-2}-0.0000442z^{-3}-0.0000188z^{-4}-0.0000152z^{-5}-0.0000138z^{-6}-0.00000907z^{-7}} \quad (21)$$

IV. FCS-MPC FOR SINGLE-PHASE CASCADED H-BRIDGE 5-LEVEL VSI-BASED SHUNT APF

A. FCS-MPC

At the beginning of each T_S, the digital system acquires the samples of the set of variables to be measured through sensors and ADCs. Then, the i_c^* signal is generated (see Fig. 2), and predicted by a second-order Lagrange extrapolation equation as $i_c^*[k+1] = i_c^*[k-2] - 3i_c^*[k-1] + 3i_c^*[k]$.

Subsequently, the algorithm predicts the behavior of the measured compensation current for each of the nine possible voltage vectors v_i, according to table 1 as follows

$$i_{cj}[k+1] = \left\{ \frac{T_S}{L_e} \left(v_{ij}[k] - v_s[k] - R_e i_c[k] \right) \right\} + i_c[k] \quad (22)$$

Afterward, to select the best voltage vector that will build the compensation current in the next sampling period, closest to the reference signal, a cost function g must be evaluated [45]. So, for a system like the one studied here, the cost function must be able to guarantee the following three conditions [17]: 1) tracking of the reference current with minimum error, 2) constant voltage of the dc-link, and 3) balance in the voltages of dc-buses. To achieve this, the cost function should be expressed as

$$\begin{aligned} g = {} & \gamma_1 \left(i_c^*[k+1] - i_{cj}[k+1] \right)^2 \\ & + \gamma_2 \left(V_{dc}^*[k+1] - \{ V_{Ca}[k+1] + V_{Cb}[k+1] \} \right)^2 \\ & + \gamma_3 \left(V_{Ca}[k+1] - V_{Cb}[k+1] \right)^2 \end{aligned} \quad (23)$$

It is desirable to suppress the second and third objectives of the cost function (23), in order to obtain a reduced cost function and to strengthen the stability of the current control loop. However, this task is not trivial, since the terms associated with the compensation current and the dc-bus voltages are heavily related. Therefore, to simplify the cost function (23), the generation of the compensation current must be carried out considering an appropriate selection of the switching states (the redundant selection of switching states is explained in the following subtopic).

The goal is to ensure that even when a constant dc-link voltage is required, as well as balanced voltage across both capacitors, a redundant switching state can be selected each time. This must be done by considering the charging and discharging of the capacitors, thus eliminating the need for weighting factors to control the voltages on the dc-buses [39]. Following this strategy, it is possible to simplify (23), as

$$g = \left(i_c^*[k+1] - i_{cj}[k+1] \right)^2 \quad (24)$$

A detailed analysis of the stability of power converters controlled with FCS-MPC can be consulted in [46]. Where it is shown that power converters with a cost function similar to (24) produce asymptotically stable control signal responses.

B. REDUNDANT SELECTION OF SWITCHING STATES

This part of the algorithm evaluates the nine voltage vector to decide the possibility of increasing or decreasing the capacitor voltages V_{Ca} and V_{Cb}, in order to maintain the balance between the dc-bus voltages of each H-bridge, as depicted in Table 1.

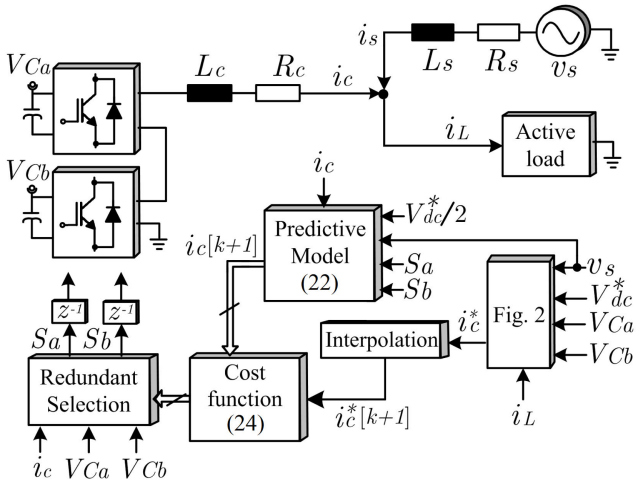

FIGURE 7. Block diagram of the proposed FCS-MPC for single-phase CHB 5-level VSI-based shunt APF.

For example, the FCS-MPC scheme decides that the multilevel inverter should generate an output voltage $v_i = -V_{dc}$ at future time $T_S[k+1]$. Besides, $i < 0$ and $V_{C_b} > V_{C_a}$. Then, there are two redundant switching states that satisfy those conditions, and these are $v_{i6}[k+1]$ and $v_{i8}[k+1]$. So, the optimal switching sate that should be selected to be applied by the VSI in the next sampling period will depend on the state of charge of the capacitors.

In this case, since V_{C_a} must increase, the voltage vector $v_{i8}[k+1]$ must be selected, because this voltage vector will cause that V_{C_a} increases and that V_{C_b} decreases.

In case a zero voltage vector is selected, each zero voltage vector alternates based on the last applied switching state to reduce the stress on the semiconductors.

A block diagram of the proposed FCS-MPC scheme is depicted in Fig 7, and a flowchart diagram of the algorithm is shown in Fig 8.

V. RESULTS

A. EXPERIMENTAL SYSTEM SETUP

1) HARDWARE

The single-phase CHB 5-level inverter was designed and implemented with four half-H-bridge power cells as shown in Fig. 9. Each power cell consists of two discrete devices IGBT-diode (APT80GA60LD40). These are controlled with an isolated, high current gate driver Si8285 by Silicon Labs.

The power cell was designed, considering protection circuits, desaturation circuits and bootstrap circuits to obtain a high-performance power cell. The design and embedding of snubber circuits in the drive circuit has been necessary to suppress the voltage spikes that appear when the IGBTs turn-off. The design, specifications, and laboratory testing of each power cell can be found in [47].

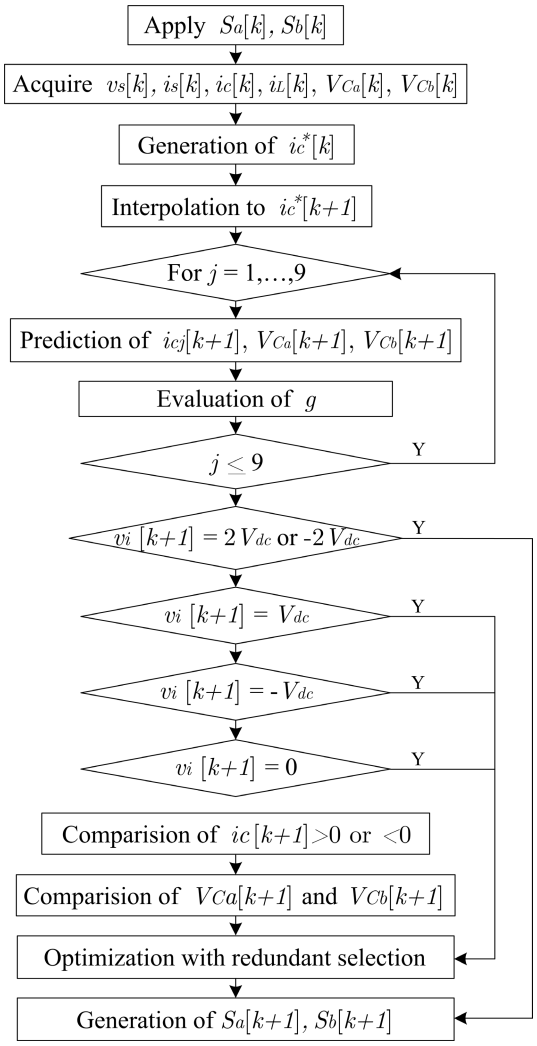

FIGURE 8. Flowchart diagram of the developed algorithm.

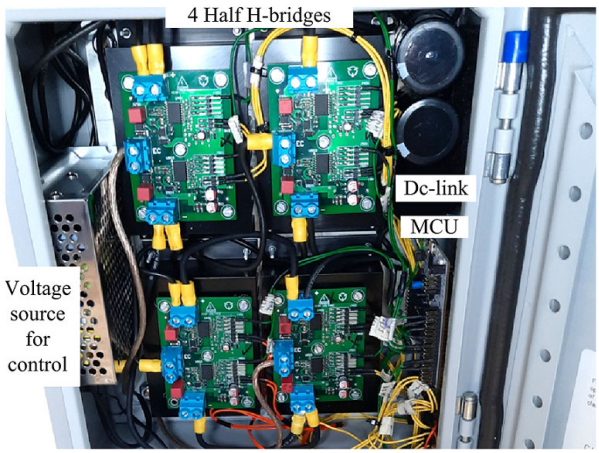

FIGURE 9. The single-phase CHB 5-level inverter.

Furthermore, it has been necessary to use an EMI filter on the grid voltage, a Faraday cage for the compensation inductance, and it was considered to compensate for the dead-time and the voltage drop of the semiconductors according to [48], all of this to keep the current ripple to a minimum.

Current measurements are made using Hall-effect current transducers (LA 100-P/SP13). The measured current values are filtered before the ADCs using passive analog LPFs set at 3.3 KHz. A LeCroy HDO6054 500MHz 4 Channel Oscilloscope is used to capture the waveforms.

It should be mentioned that for safety, since it has been working with a prototype, the grid voltage has been reduced to $v_{pp} = 100\ v$, with the help of a transformer, as can be seen in the experimental system setup of the Fig. 10.

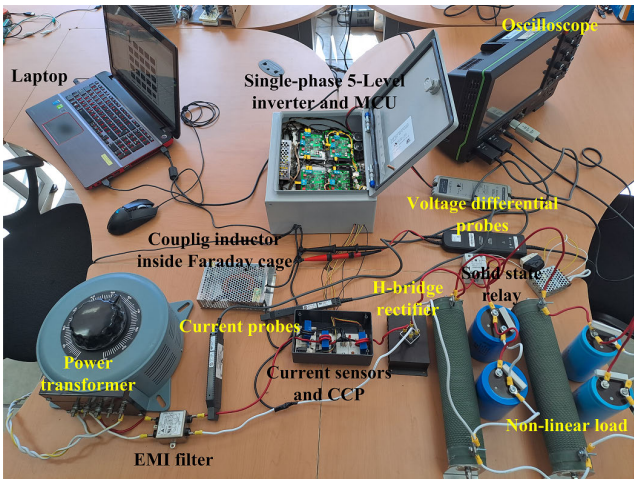

FIGURE 10. The experimental system setup.

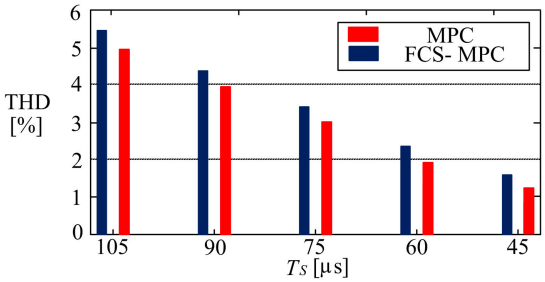

FIGURE 11. THD of the i_S with an active RC load and PI^{λ} controller.

TABLE 3. System parameters.

Symbol	Parameter	Value
$v_{pp} = v_s\sqrt{2}$	Grid voltage	100 v
$C_a = C_b$	Dc-bus capacitor	1000 μF
f_s	Grid frequency	60 Hz
L_s	Grid inductance	0.2 mH
L_c	Coupling inductance	4 mH
R_c	Coupling resistance	0.24 Ω
R_L	Load resistance	20 Ω
C_L	Load capacitance	4700 μF

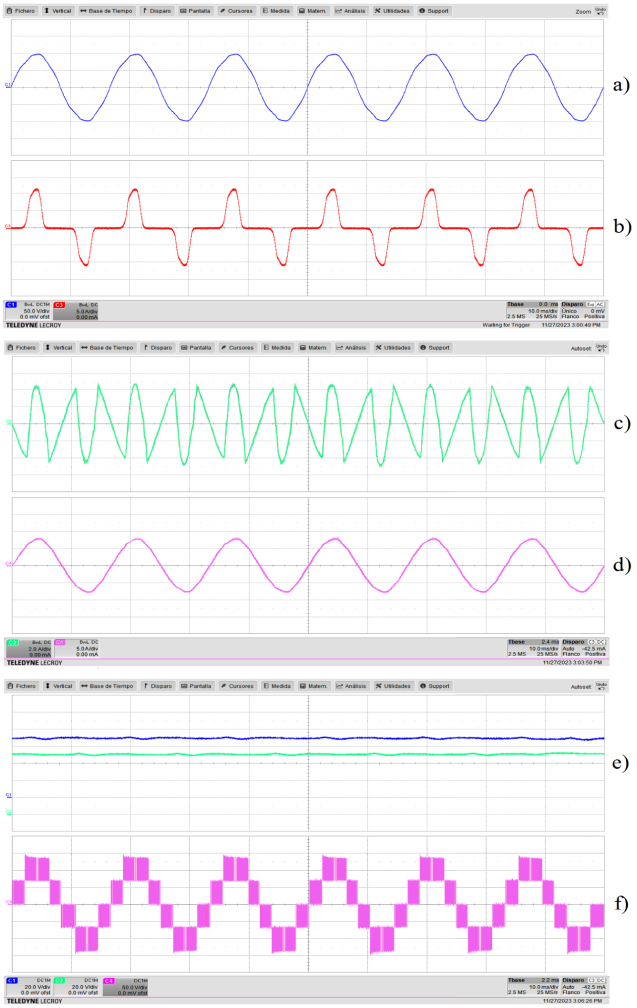

FIGURE 12. Steady-state performance of the developed shunt APF with PI$^{\lambda}$ controller [10 ms/div]. a) Grid voltage [50 V/div], b) load current [5 A/div], c) compensation current [2 A/div], d) grid current [5 A/div], e) dc-link voltage [20 V/div] and f) the inverter voltage [50 V/div].

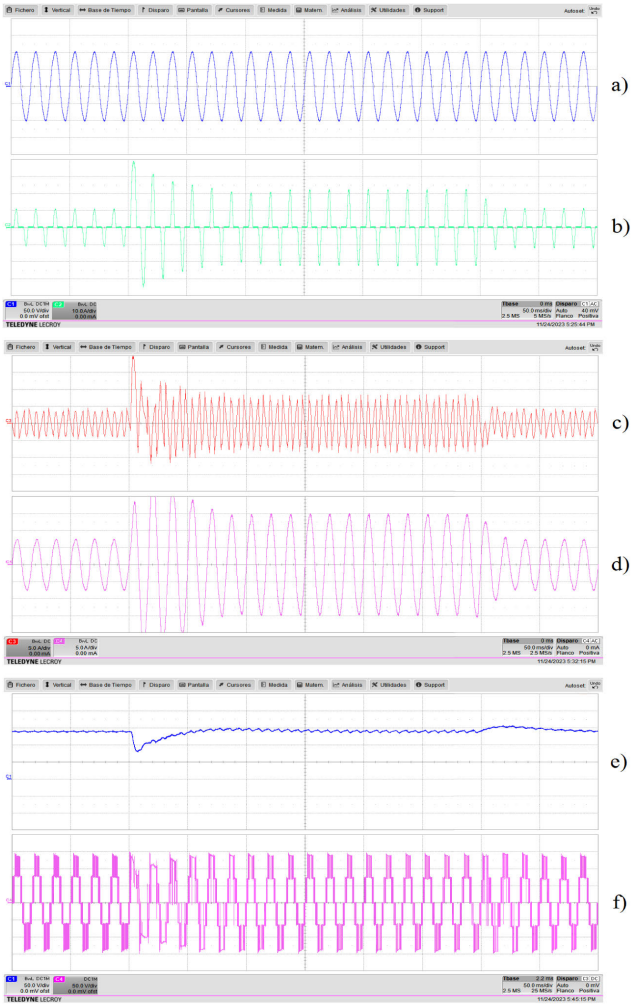

FIGURE 13. Dynamic performance of the developed shunt APF with PI controller [50 ms/div]. a) Grid voltage [50 V/div], b) load current [10 A/div], c) compensation current [5 A/div], d) grid current [5 A/div], e) dc-link voltage [50 V/div] and f) the inverter voltage [50 V/div].

2) DIGITAL IMPLEMENTATION

The developed algorithm has been implemented in a fully digital manner using a cost-effective STM32F439ZI digital system. The STM32F4 series are high-performance real-time MCUs with DSP and FPU instructions. With up to 225 DMIPS/608 CoreMark executing from Flash memory at up to 180 MHz operating frequency. 1 MB Flash memory, 1.4 MB RAM memories, and 6 ADCs with 16-bit [49].

The selected digital system is capable of solving the conventional MPC algorithm, i.e., using the 16 voltage vectors available with the topology of the inverter under study, in a control cycle of $T_S = 48\ \mu$s and the developed FCS-MPC algorithm (using 9 voltage vectors) in $T_S = 36\ \mu$s, both with PI$^{\lambda}$ control.

In FCS-MPC strategies without modulator, switching take place every discrete-time instants $T_S[k]$, $T_S[k+1]$,.... Therefore, it is desirable to have as high a sampling frequency as possible. Besides, the sampling interval not only affects the precision of the discretization, but also the performance of the controller. For example, in APF applications, the total harmonic distortion (THD) of the corrected i_s is a function of T_S, as shown in Fig.11.

On the other hand, for the selection of the appropriate T_S, the maximum switching frequency at which the power converter can operate must also be considered, which in this case is 20 kHz. Although this is the maximum operating frequency, it is advisable for safety to operate at 75% of the maximum frequency. Additionally, with the goal that the THD in the corrected i_s remains below 4% to deal with the IEEE std. 519-2014 [50], the FCS-MPC algorithm has been programmed in a fixed control cycle of $T_S = 70\ \mu$s.

The electrical parameters of the experimental setup are listed in Table 3.

B. EXPERIMENTAL RESULTS

Fig. 12 shows a steady-state experimental result of the developed FCS-MPC algorithm, with the PI$^{\lambda}$ controller and an active RC load. It is observed how the i_s returns to

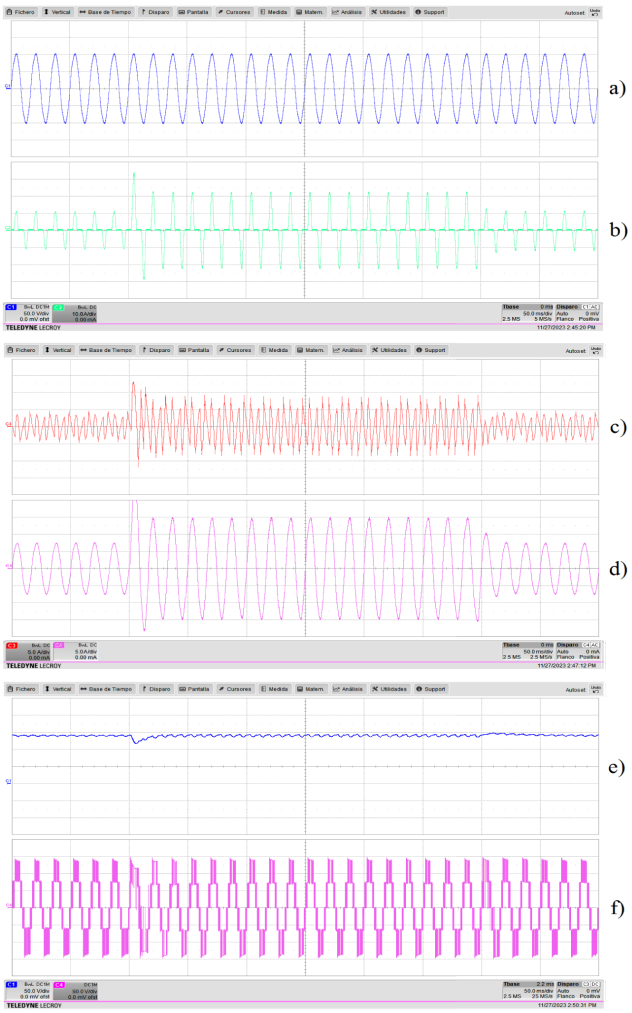

FIGURE 14. Dynamic performance of the developed shunt APF with PI$^{\lambda}$ controller [50 ms/div]. a) Grid voltage [50 V/div], b) load current [10 A/div], c) compensation current [5 A/div], d) grid current [5 A/div], e) dc-link voltage [50 V/div] and f) the inverter voltage [50 V/div].

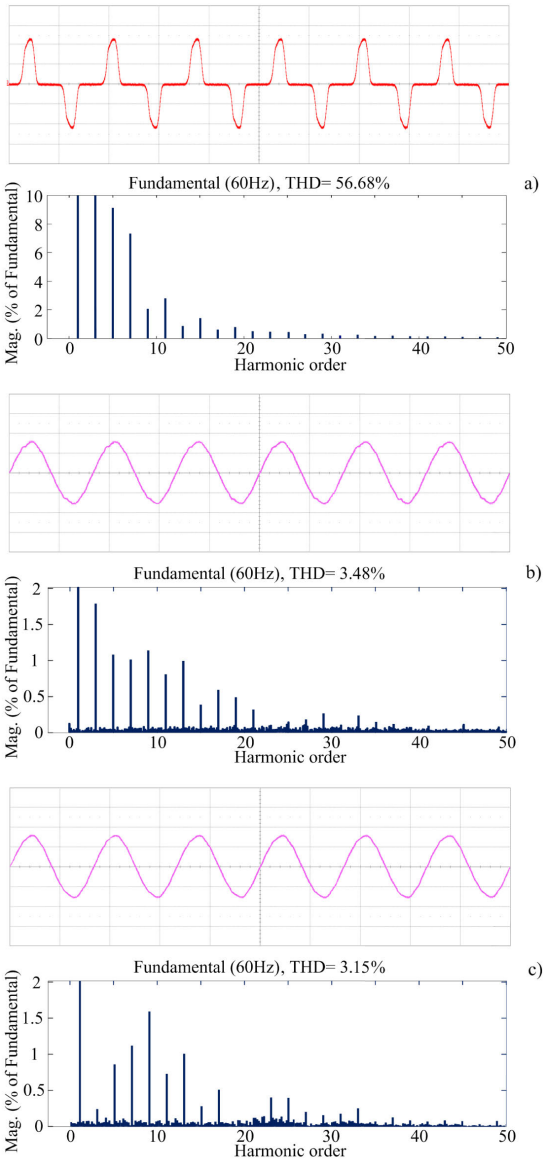

FIGURE 15. Steady-state THD of the i_s. a) Before being compensated [5 A/div], b) after being compensated with the FCS-MPC and PI controller [5 A/div], and c) after being compensated with the FCS-MPC and PI$^{\lambda}$ controller [5 A/div].

its correct waveform excellently. And the voltages on the dc-buses remain at their reference levels without difficulty, in this case $V_{C_a} = V_{C_b} = 70$ V. The five voltage levels generated by the inverter can also be appreciated.

Fig. 13 shows a dynamic experimental result of the system with the classical PI controller, and when the RC load suddenly increases by 100% at $t = 100$ ms, and then decreases by half abruptly at $t = 400$ ms. It can be seen how i_L, i_c and i_s increase rapidly when the load increases. In this case, the maximum overshoot of the corrected i_s reaches up to 26 A.

In the same figure, it is observed that the V_{dc}^* deceases a little when the load increases but returns to its reference value smoothly. When the load decreases, the reverse process occurs, V_{dc}^* shows a small overshoot but returns without setbacks to its adjusted value.

Fig. 14 shows the experimental results of a similar test of the Fig. 13, but with the proposed PI$^{\lambda}$ controller. It can be seen how the currents increase quickly when the load increases. With the PI$^{\lambda}$ controller, the maximum overshoot of the corrected i_s becomes only 22 A.

In the same figure, it is observed that V_{dc}^* presents a decrease with respect to its reference, but much smaller and with a shorter response time than when the PI controller is used. When the additional load is removed, currents decrease in magnitude and the V_{dc}^* shows an almost imperceptible overshoot and quickly returns to its set point.

Fig. 15a shows the THD of the i_s before being corrected by the shunt APF, and this has a value of 56.68%. Fig. 15b shows the THD of the i_s when it is compensated with the FCS-MPC and PI controller. In this case, the i_s contains a distortion of 3.48%. Fig. 15c shows the THD of the same corrected i_s when it is compensated with the FCS-MPC and PI$^{\lambda}$ controller. In this case, the i_s presents a THD of 3.15%.

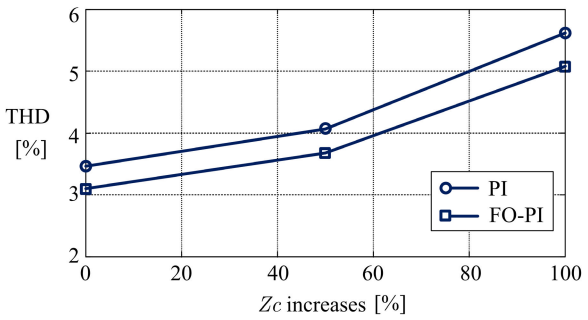

FIGURE 16. Z_c mismatch while FCS-MPC algorithm runs.

TABLE 4. Comparison of performance between PI control and the proposed FO-PI, for closed-loop voltage control.

Variable	with PI	with PI$^\lambda$
Step response (2% tolerance)	25 ms	10 ms
Response time of transient	50 ms	20 ms
Maximum i_s when load increases	26 A	22 A
THD of the corrected i_s	3.48%	3.15%
Tolerance to parametric uncertainty of Z_c	up to 45%	up to 60%
Execution time (STM32F439ZI)	2.5 μs	8.5 μs

In this way, it is verified that the THD has been reduced according to what the IEEE Std. 519-2014 indicates. By using the proposed PI$^\lambda$ controller, it is possible to reduce the harmonic distortion a little more compared to the classic PI controller, because the compensation current reference signal is generated in a more exact way.

C. PARAMETER MISMATCH

As is well known, FCS-MPC scheme require precise parameter values to achieve optimal control. Then, experimentally, the coupling impedance ($Z_c = R_c + j\omega_s L_c$) is varied to obtain the THD of i_s related to the mismatch in the value of Z_c. Fig. 16 shows the THD of i_s that is obtained as Z_c increases, during these tests the FCS-MPC algorithm runs with fixed values of $R_c = 0.24\ \Omega$ and $L_c = 4$ mH.

From these tests, it is deduced that it is possible for the system under study to operate adequately with a Z_c uncertainty of up to 60% with respect to the measured value of the Z_c, when PI$^\lambda$ control is used.

Table 4 summarizes an experimental comparison of the differences when using the different control strategies to generate the i_s^*.

VI. CONCLUSION

A FCS-MPC algorithm for the single-phase CHB 5-Level inverter working as shunt APF was presented. It has been confirmed that it is possible to generate the compensation current very close to its reference value, thanks to an appropriate selection of the voltage vector. The final selection of the voltage vector among the several possible ones is carried out by evaluating a simplified cost function. It has been shown that the cost function can be simplified thanks to the exploitation of switching redundancies and the possibility of maintaining a balanced voltage on the dc-buses.

It was confirmed that the use of a PI$^\lambda$ controller to generate the compensation current reference improves the performance of the system in stable and transient states, which has been designed and implemented completely in discrete-time.

It is important to mention that an adequate design and an appropriate implementation of the hardware have been key, so that the ripple of the currents does not increase further. In this case, an EMI filter at the input, passive filters in signal conditioning, Faraday cage for the Z_c, and even snubber circuits were necessary to successfully keep the current ripple low. An adequate knowledge of the system parameters is necessary, since an inaccuracy of them ($Z_c > 60\%$ for an active RC load and PI$^\lambda$ controller) negatively impacts the prediction of the variables.

REFERENCES

[1] J. S. Subjak and J. S. McQuilkin, "Harmonics-causes, effects, measurements, and analysis: An update," *IEEE Trans. Ind. Appl.*, vol. 26, no. 6, pp. 1034–1042, Nov. 1990.
[2] Y. Wang, P. Chen, J. Yong, W. Xu, S. Xu, and K. Liu, "A comprehensive investigation on the selection of high-pass harmonic filters," *IEEE Trans. Power Del.*, vol. 37, no. 5, pp. 4212–4226, Oct. 2022.
[3] D. Li, T. Wang, W. Pan, X. Ding, and J. Gong, "A comprehensive review of improving power quality using active power filters," *Electr. Power Syst. Res.*, vol. 199, Oct. 2021, Art. no. 107389.
[4] A. Heenkenda, A. Elsanabary, M. Seyedmahmoudian, S. Mekhilef, A. Stojcevski, and N. F. A. Aziz, "Unified power quality conditioners based different structural arrangements: A comprehensive review," *IEEE Access*, vol. 11, pp. 43435–43457, 2023.
[5] Y. Hoon, M. A. M. Radzi, M. A. A. M. Zainuri, and M. A. M. Zawawi, "Shunt active power filter: A review on phase synchronization control techniques," *Electronics*, vol. 8, no. 7, p. 791, Jul. 2019.
[6] A. A. Valdez-Fernandez, G. Escobar, D. U. Campos-Delgado, K. O. Mtepele, and P. R. Martinez-Rodriguez, "A model-based controller for a single-phase n-level CHB multilevel converter," *Int. J. Electr. Power Energy Syst.*, vol. 125, Feb. 2021, Art. no. 106454.
[7] B. Aljafari, K. Rameshkumar, V. Indragandhi, and S. Ramachandran, "A novel single-phase shunt active power filter with a cost function based model predictive current control technique," *Energies*, vol. 15, no. 13, p. 4531, Jun. 2022.
[8] C. Buccella, M. G. Cimoroni, and C. Cecati, "Mitigation technique for cascaded H-bridge multilevel inverters based on pulse active width modulation," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 11, no. 1, pp. 999–1008, Feb. 2023.
[9] M. Ishfaq, W. Uddin, K. Zeb, S. U. Islam, S. Hussain, I. Khan, and H. J. Kim, "Active and reactive power control of modular multilevel converter using sliding mode controller," in *Proc. 2nd Int. Conf. Comput., Math. Eng. Technol. (iCoMET)*, Sukkur, Pakistan, Jan. 2019, pp. 1–5.
[10] B.-Y. Luo, R. K. Subroto, C.-Z. Wang, and K.-L. Lian, "An improved sliding mode control with integral surface for a modular multilevel power converter," *Energies*, vol. 15, no. 5, p. 1704, Feb. 2022.
[11] G. Pandove and M. Singh, "Robust repetitive control design for a three-phase four wire shunt active power filter," *IEEE Trans. Ind. Informat.*, vol. 15, no. 5, pp. 2810–2818, May 2019.
[12] H. Geng, Z. Zheng, T. Zou, B. Chu, and A. Chandra, "Fast repetitive control with harmonic correction loops for shunt active power filter applied in weak grid," *IEEE Trans. Ind. Appl.*, vol. 55, no. 3, pp. 3198–3206, May 2019.
[13] A. A. Valdez-Fernández, G. Escobar, G. A. Catzin-Contreras, M. E. Hernández-Ruíz, and R. Morales-Caporal, "A 6h ± 1 repetitive scheme for the three-phase CHB seven-level converter used in an APF application," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 12, no. 2, pp. 1641–1653, Apr. 2024.
[14] M.-S. Karbasforooshan and M. Monfared, "An improved reference current generation and digital deadbeat controller for single-phase shunt active power filters," *IEEE Trans. Power Del.*, vol. 35, no. 6, pp. 2663–2671, Dec. 2020.

[15] M. Pichan, M. Seyyedhosseini, and H. Hafezi, "A new DeadBeat-based direct power control of shunt active power filter with digital implementation delay compensation," *IEEE Access*, vol. 10, pp. 72866–72878, 2022.
[16] L. Zhou, Z. Zhou, J. Qi, and W. Han, "Hybrid prediction-based deadbeat control for a high-performance shunt active power filter," *IEEE Access*, vol. 11, pp. 11118–11131, 2023.
[17] P. Acuña, L. Morán, M. Rivera, R. Aguilera, R. Burgos, and V. G. Agelidis, "A single-objective predictive control method for a multivariable single-phase three-level NPC converter-based active power filter," *IEEE Trans. Ind. Electron.*, vol. 62, no. 7, pp. 4598–4607, Jul. 2015.
[18] H. Saldías Molina, J. Dixon Rojas, and L. Morán Tamayo, "Finite set model predictive control to a shunt multilevel active filter," *COMPEL, Int. J. Comput. Math. Electr. Electron. Eng.*, vol. 34, no. 1, pp. 279–300, Jan. 2015.
[19] M. Najjar, M. Shahparasti, R. Heydari, and M. Nymand, "Model predictive controllers with capacitor voltage balancing for a single-phase five-level SiC/Si based ANPC inverter," *IEEE Open J. Power Electron.*, vol. 2, pp. 202–211, 2021.
[20] S. Hou, J. Fei, Y. Chu, and C. Chen, "Experimental investigation of adaptive fuzzy global sliding mode control of single-phase shunt active power filters," *IEEE Access*, vol. 7, pp. 64442–64449, 2019.
[21] K. K. Kumar, M. V. Karthik, and K. V. Kumar, "THD reduction in single-phase cascaded H-Bridge multilevel inverter using fuzzy logic controller," in *Proc. Int. Conf. Sustain. Comput. Smart Syst. (ICSCSS)*, Coimbatore, India, Jun. 2023, pp. 1321–1327.
[22] F. Simonetti, A. D'Innocenzo, and C. Cecati, "Neural network model predictive control for CHB converters with FPGA implementation," *IEEE Trans. Ind. Informat.*, vol. 19, no. 9, pp. 9691–9702, Sep. 2023.
[23] P. Karamanakos, E. Liegmann, T. Geyer, and R. Kennel, "Model predictive control of power electronic systems: Methods, results, and challenges," *IEEE Open J. Ind. Appl.*, vol. 1, pp. 95–114, 2020.
[24] R. Morales-Caporal, "Optimal indirect model predictive control for single-phase two-level shunt active power filters," *J. Power Electron.*, vol. 22, no. 1, pp. 84–93, Jan. 2022.
[25] J. Rodriguez, J.-S. Lai, and F. Zheng Peng, "Multilevel inverters: A survey of topologies, controls, and applications," *IEEE Trans. Ind. Electron.*, vol. 49, no. 4, pp. 724–738, Aug. 2002.
[26] H. Abu-Rub, J. Holtz, J. Rodriguez, and G. Baoming, "Medium-voltage multilevel converters—State of the art, challenges, and requirements in industrial applications," *IEEE Trans. Ind. Electron.*, vol. 57, no. 8, pp. 2581–2596, Aug. 2010.
[27] J. Azurza Anderson, G. Zulauf, P. Papamanolis, S. Hobi, S. Miric, and J. W. Kolar, "Three levels are not enough: Scaling laws for multilevel converters in AC/DC applications," *IEEE Trans. Power Electron.*, vol. 36, no. 4, pp. 3967–3986, Apr. 2021.
[28] M. A. Perez, S. Bernet, J. Rodriguez, S. Kouro, and R. Lizana, "Circuit topologies, modeling, control schemes, and applications of modular multilevel converters," *IEEE Trans. Power Electron.*, vol. 30, no. 1, pp. 4–17, Jan. 2015.
[29] B. N. Rao, Y. Suresh, A. K. Panda, B. S. Naik, and V. Jammala, "Development of cascaded multilevel inverter based active power filter with reduced transformers," *CPSS Trans. Power Electron. Appl.*, vol. 5, no. 2, pp. 147–157, Jun. 2020.
[30] P. Sun, Y. Tian, J. Pou, and G. Konstantinou, "Beyond the MMC: Extended modular multilevel converter topologies and applications," *IEEE Open J. Power Electron.*, vol. 3, pp. 317–333, 2022.
[31] J. Rodriguez, M. P. Kazmierkowski, J. R. Espinoza, P. Zanchetta, H. Abu-Rub, H. A. Young, and C. A. Rojas, "State of the art of finite control set model predictive control in power electronics," *IEEE Trans. Ind. Informat.*, vol. 9, no. 2, pp. 1003–1016, May 2013.
[32] P. Karamanakos and T. Geyer, "Guidelines for the design of finite control set model predictive controllers," *IEEE Trans. Power Electron.*, vol. 35, no. 7, pp. 7434–7450, Jul. 2020.
[33] M. Merai, M. W. Naouar, I. Slama-Belkhodja, and E. Monmasson, "An adaptive PI controller design for DC-link voltage control of single-phase grid-connected converters," *IEEE Trans. Ind. Electron.*, vol. 66, no. 8, pp. 6241–6249, Aug. 2019.
[34] J. Zhou, Y. Yuan, and H. Dong, "Adaptive DC-link voltage control for shunt active power filters based on model predictive control," *IEEE Access*, vol. 8, pp. 208348–208357, 2020.
[35] K. Rameshkumar and V. Indragandhi, "Real time implementation and analysis of enhanced artificial bee colony algorithm optimized PI control algorithm for single phase shunt active power filter," *J. Electr. Eng. Technol.*, vol. 15, no. 4, pp. 1541–1554, Jul. 2020.
[36] V. Muneer, G. M. Biju, and A. Bhattacharya, "Optimal machine learning based controller for shunt active power filter by auto machine learning," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 11, no. 3, pp. 3435–3444, Jun. 2023.
[37] G. Farivar, B. Hredzak, and V. G. Agelidis, "Decoupled control system for cascaded H-bridge multilevel converter based STATCOM," *IEEE Trans. Ind. Electron.*, vol. 63, no. 1, pp. 322–331, Jan. 2016.
[38] I. Harbi, J. Rodriguez, E. Liegmann, H. Makhamreh, M. L. Heldwein, M. Novak, M. Rossi, M. Abdelrahem, M. Trabelsi, M. Ahmed, P. Karamanakos, S. Xu, T. Dragicevic, and R. Kennel, "Model predictive control of multilevel inverters: Challenges, recent advances, and trends," *IEEE Trans. Power Electron.*, vol. 38, no. 9, pp. 10845–10868, Sep. 2023.
[39] R. Morales-Caporal, "Finite–control–set model predictive control for a single–phase cascaded H–bridge multilevel converter operating as a shunt active power filter," in *Proc. 20th Int. Conf. Electr. Eng., Comput. Sci. Autom. Control (CCE)*, Oct. 2023, pp. 1–6.
[40] X. Lin, Y. Wen, R. Yu, J. Yu, and H. Wen, "Improved weak grids synchronization unit for passivity enhancement of grid-connected inverter," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 10, no. 6, pp. 7084–7097, Dec. 2022.
[41] Y. Han, M. Luo, X. Zhao, J. M. Guerrero, and L. Xu, "Comparative performance evaluation of orthogonal-signal-generators-based single-phase PLL algorithms—A survey," *IEEE Trans. Power Electron.*, vol. 31, no. 5, pp. 3932–3944, May 2016.
[42] Q. Guan, Y. Zhang, Y. Kang, and J. M. Guerrero, "Single-phase phase-locked loop based on derivative elements," *IEEE Trans. Power Electron.*, vol. 32, no. 6, pp. 4411–4420, Jun. 2017.
[43] F. Merrikh-Bayat, S.-N. Mirebrahimi, and M.-R. Khalili, "Discrete-time fractional-order PID controller: Definition, tuning, digital realization and experimental results," 2014, *arXiv:1405.0144*.
[44] I. Tejado, B. Vinagre, J. Traver, J. Prieto-Arranz, and C. Nuevo-Gallardo, "Back to basics: Meaning of the parameters of fractional order PID controllers," *Mathematics*, vol. 7, no. 6, p. 530, Jun. 2019.
[45] R. Morales-Caporal, O. Sandre-Hernández, and A. A. Valdez-Fernandez, "Model predictive control for single-phase cascaded H-bridge five-level inverter," in *Proc. 19th Int. Conf. Electr. Eng., Comput. Sci. Autom. Control (CCE)*, Nov. 2022, pp. 1–5.
[46] R. P. Aguilera and D. E. Quevedo, "Predictive control of power converters: Designs with guaranteed performance," *IEEE Trans. Ind. Informat.*, vol. 11, no. 1, pp. 53–63, Feb. 2015.
[47] R. Morales-Caporal, J. F. Pérez-Cuapio, H. P. Martínez-Hernández, and R. Cortés-Maldonado, "Design and hardware implementation of an IGBT-based half-bridge cell for modular voltage source inverters," *Electronics*, vol. 10, no. 20, p. 2549, Oct. 2021.
[48] A. Mora, J. Juliet, A. Santander, and P. Lezana, "Dead-time and semiconductor voltage drop compensation for cascaded H-bridge converters," *IEEE Trans. Ind. Electron.*, vol. 63, no. 12, pp. 7833–7842, Dec. 2016.
[49] *STM32H745ZI MCU*. Accessed: Oct. 2023. [Online]. Available: https://www.st.com/en/microcontrollers-microprocessors/stm32f4-series.html
[50] *IEEE Recommended Practice and Requirements for Harmonic Control in Electric Power Systems*, Standard EEE 519-TM-2014, The Inst. Electr. Electron. Engineers, Inc., IEEE Power and Energy Society, Mar. 2014.

ROBERTO MORALES-CAPORAL (Senior Member, IEEE) received the B.E. degree in electromechanical engineering from the Instituto Tecnologico de Apizaco (ITA), Apizaco, México, in 1999, the M.Sc. degree in electrical engineering from the Graduate and Research Department, Superior School of Mechanical and Electrical Engineering (ESIME), National Polytechnic Institute (IPN), Mexico, in 2001, and the Dr.-Ing. degree in electrical engineering from the University of Siegen, Siegen, Germany, in 2007.

From 2001 to 2003, he was a Lecturer with the Interdisciplinary Professional Unit in Engineering and Advanced Technologies (UPIITA), IPN. He is currently a Professor and a Researcher with the Division of Graduate Studies and Research, ITA. His research interests include DSP-based digital control, predictive control of power converters, hardware design, and the IoT.

Prof. Morales-Caporal is a member of the National Research Fellows System Level 2 (SNI-2), CONAHCYT, Mexico.

EDMUNDO BONILLA-HUERTA received the B.Sc. and M.Sc. degrees in computer science from the Instituto Tecnologico de Apizaco (ITA), Apizaco, Tlaxcala, Mexico, in 1994 and 1996, respectively, and the Ph.D. degree in computer science from the University of Angers, Angers, France, in 2008.

He is currently a Professor with the Division of Graduate Studies and Research, ITA. His research interests include optimization, fuzzy logic, machine learning, techniques for microarray data analysis, and bioinformatics.

RAFAEL ORDOÑEZ-FLORES received the B.E. degree in electronics engineering from the Instituto Tecnologico de Apizaco (ITP), Puebla, Mexico, in 1995, the M.Sc. degree in electronics engineering from the National Center for Research and Technological Development (CENIDET), Cuernavaca, Mexico, in 1998, and the D.Sc. degree in electrical engineering from the University of Paris 11, Higher School of Electricity (SUPELEC), Orsay, France, in 2007.

He is currently a Professor with the Division of Graduate Studies and Research, ITA. His research interests include control of power electronics, electrical energy quality, renewable energy, and magnetic induction heating.

ANDRES A. VALDEZ-FERNANDEZ (Senior Member, IEEE) received the Ph.D. degree in control and dynamical systems from the Potosi Institute of Scientific and Technological Research (IPICyT), Mexico, in 2009.

From 2008 to 2012, he was a full-time Professor-Researcher with the Technological Institute of Superior Studies of Irapuato (TecNM-ITESI), Mexico. He is currently a Professor and a Researcher with the School of Sciences, Universidad Autonoma de San Luis Potosí (UASLP), Mexico. His research interests include analysis, modeling, control design, and fault diagnosis of active power filters, inverters, rectifiers, renewable energy systems, and e-mobility systems. He is a member of the National Research Fellows System Level 2 (SNI-2), CONAHCyT, Mexico.

JOSE DE JESUS RANGEL-MAGDALENO (Senior Member, IEEE) received the B.E. degree in electronics engineering and the M.E. degree in electrical engineering on hardware signal processing from Universidad de Guanajuato, Mexico, in 2006 and 2008, respectively, and the Ph.D. degree from Universidad Autónoma de Queretaro, Mexico, in 2011.

He is currently a Full Researcher with the Department of Electronics, National Institute of Astrophysics, Optics and Electronics (INAOE), Mexico. He has authored one book, and more than 190 works published in journals, conferences, and book chapters. His research interests include FPGAs, signal and image processing, and instrumentation. He is a member of the National Research Fellows System Level 2 (SNI-2), CONAHCyT, Mexico. He received the 2018 IEEE I&MS Outstanding Young Engineer Award.