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RESEARCH ARTICLE

Analysis of Soft Switching Conditions for Push-Pull Current Type Bidirectional DC/DC Converter

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ABSTRACT This article first introduces the working principle of a push-pull current type DC/DC converter, analyzes the transient working process of the converter within one working cycle of the control signal, and draws the relevant waveforms of the main parameters of the circuit; Secondly, equivalent circuits are established for each switch in the circuit to achieve soft switching. At the same time, due to the isolation of the DC/DC converter using parasitic parameters of the converter for resonance, the soft switching conditions of the switch are achieved. The main parameters of the resonance process are about the parasitic capacitance of the switch and the transmission inductance of the converter. Therefore, based on the soft switching implementation process of each switch, the influence relationship between the parameter design of parasitic capacitance and transmission inductance on the soft switching is derived; Finally, the software simulation and prototype experimental platform are built to verify that the derived soft switching conditions can serve as the theoretical basis for the parameter design of push-pull current type DC/DC converters.

INDEX TERMS Bidirectional, DC/DC converter, push-pull type, soft switch.

I. INTRODUCTION

In recent years, bidirectional DC/DC converters have been widely used in renewable energy power generation systems, electric vehicles, uninterruptible power supplies and other industrial fields [1], [2], [3], [4]. The voltage of energy storage devices, such as batteries and super capacitors, is generally relatively low. It is necessary to solve the problem of voltage mismatch between energy storage devices and DC bus through high voltage gain isolated bidirectional DC/DC converter. At the same time, the voltage of the energy storage device changes continuously in the process of charging and discharging, and its variation range is wide. Therefore, as the interface of energy storage device, DC/DC converter needs to meet the following requirements and have the following characteristics: 1) It can realize bidirectional power transmission; 2) High efficiency; 3) Suitable for wide voltage range; 4) Low current ripple at battery side [5], [6], [7], [8]. Realizing the soft switching state of each switch for the converter is an important approach to ensure the high efficiency of the converter. Therefore, many experts and scholars have done a lot of research work.

After analyzing the power return phenomenon in the traditional phase-shift control of isolated bidirectional full bridge DC/DC converter and the influence of return power on current stress, [9] proposed the extended phase-shift control of bidirectional full bridge DC/DC converter for microgrid power distribution. Compared with the traditional phase-shift control, the extended phase-shift control not only expands the regulation range of transmission power, but also increases the flexibility of regulation, reduces the current stress and improves the transmission efficiency of the system. Reference [10] proposed a modulation scheme of dual active bridge (DAB), which can reduce the effective value of current in a

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wide range of operating conditions by adjusting PWM signal and relatively simple controller structure. Reference [11] proposed a novel interleaved high conversion ratio bidirectional DC/DC converter based on switched capacitor and coupled inductor. The series connected switched capacitor and inductor module improved the voltage conversion ratio and reduced the voltage stress of the switch. The module with switched capacitor and inductor in series can realize the soft charge and discharge of switched capacitor, and can realize the automatic current sharing on the inductor; The interleaving structure of switched capacitor is adopted, which can reduce the current ripple at the low voltage side and realize the application of high power. Reference [12] reduced the current ripple by increasing the low-voltage side coupling inductance, but limited the turns of other windings, thus limiting the voltage gain of the converter. Reference [13] separated the low-voltage side filter inductor from the coupling inductor to reduce the current ripple at the low-voltage side, but the voltage stress of all switches was higher than that of the high-voltage side voltage. When analyzing the soft switching of double half bridge DC/DC converter, [14] considered the relationship between input inductance, phase shift angle and duty cycle. References [15] and [16] proposed a high voltage rise DC/DC converter with active clamping circuit to provide ZVS for power switches. The active clamp circuit not only absorbs the leakage energy of the magnetic device, but also leaks the current through the anti-parallel diode of the main switch before the arrival of the grid signal. However, due to the series connection of the coupling inductor and the input DC power supply, high input current ripple is generated in these circuits, which is the main disadvantage of the converter. Reference [17] used synchronous rectifier switches to replace diodes to achieve ZVS conduction of switches. At the same time, the zero DC bias of the coupling inductor can obtain smaller magnetic size and lower core loss, but the voltage gain is not high, and the voltage stress of the output diode is large. Reference [18] used resonant topology and phase shift control method to achieve soft switching. However, the implementation was difficult and the control is complex. Reference [19] used the PPS control method to expand the soft switching range of the converter by increasing the auxiliary inductance. However, the increase of the auxiliary inductance will increase its current RMS, which not only increases the conduction loss of the switch, but also reduces the maximum transmission power. Therefore, it is necessary to consider the trade-off between wide range and high efficiency and high power. In addition, when the converter proposed in [18] and [19] changes in a wide gain range, ZVS is difficult to achieve, and with the increase of circulating current, the efficiency will be further reduced. Reference [20] proposed a soft switching bidirectional DC/DC converter with large transformation ratio. Through a special structure, the converter makes use of the leakage inductance energy to turn on the diode of the switch within the dead time, and realizes the zero voltage turn-on of the switching device. However, the realization of soft switching requires the leakage inductance of the coupling inductor to meet certain conditions. Reference [21] had constructed an accurate soft switching model including all harmonic components for the dual active bridge converter, so as to realize the soft switching parameter design of all switches. However, this method is only applicable to the single phase-shift control, but not applicable to the more complex phase-shift strategy. Reference [22] proposed a high voltage gain and wide range soft switching Bidirectional DC/DC converter topology. The resonant cavity, composed of the leakage inductance of the coupling inductance and the resonant capacitor can not only control the leakage inductance energy, but also suppress the change of the resonant current, which can realize soft switching under full load conditions within a wide voltage range at the low voltage side. References [23] and [24] proposed a DC/DC converter structure based on a single switch coupled inductor, which had low input current ripple and ZCS performance. In these converters, the regenerative passive clamping circuit helps to recover the energy of the leaking inductor. Reference [25] proposed a new improved Y-source step-up DC/DC converter with ZVS characteristics. In this topology, higher voltage gain is achieved by reducing the turn ratio of the secondary and tertiary sides of the coupled inductor. References [26] and [27] introduced two new step-up DC/DC converters using low input current ripple. These topologies operate with Low Reverse Recovery under ZVS conditions. The boost half bridge current mode bidirectional isolated DC/DC converter proposed in [28] can eliminate the high voltage spike at the low voltage side without introducing a clamping circuit. On the basis of [28] and [29] introduced the secondary side of the transformer into the center tap and adds a half bridge. The hybrid phase-shift plus PWM control is adopted. All switches can realize ZVS switching within the full load range, reducing the switching loss and improving the efficiency of the converter. The topology of current mode bi-directional isolated dc/dc converter proposed in [28] and [29] is shown in Figure1 and Figure 2.

In this paper, the working process of the converter is divided into 12 working modes. On this basis, this paper will comprehensively analyze the realization conditions of soft switching from the aspects of circuit working mode, parasitic capacitance, dead time, excitation inductance and so on. The soft switching conditions of the converter are derived, and the soft switching characteristics of the converter under all 12 operating modes are given, which provides the basis for the design of circuit parameters of push-pull current mode bidirectional DC/DC converter.

II. THE WORKING PRINCIPLE OF THE CONVERTER

A. OVERVIEW OF CONVERTER TOPOLOGY

The topology of the push-pull current source bidirectional DC/DC converter designed in this paper is shown in Figure 3. For the similarity of the bidirectional working process of the converter, this paper only takes the forward working process

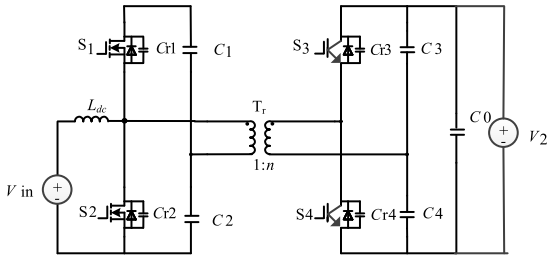


FIGURE 1. Topology proposed in [28].

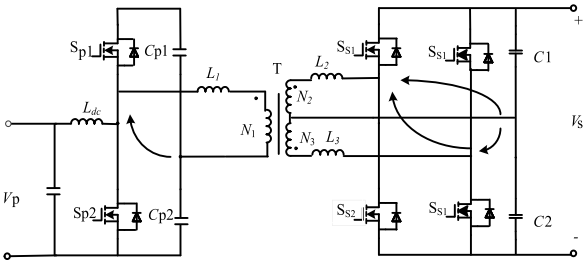


FIGURE 2. Topology proposed in [29].

as an example, that is, the energy is transmitted from the low voltage side to the high voltage side. In Figure 3, V_1 and V_2 represent the low-voltage input voltage and high-voltage output voltage of the topology, respectively. On the low-voltage side, S_1 and S_2 form the main switches of the push-pull circuit, and S_3 and S_4 are two active clamp switches connected to the clamp capacitor C_s, and the input inductance L is connected to the transformer center tap to form a current type input. On the high-voltage side, S_5 and S_6 form an active voltage doubling circuit, where L_s is the leakage inductance on the secondary side of the transformer. The converter can achieve bidirectional power transmission; the cascade design of Boost circuit and push-pull transformer improves transmission efficiency; the clamp capacitor ensures that the input voltage can vary over a wide range; the series inductance L on the battery side can reduce the input current ripple. The arrow directions in the topology represent the positive reference directions of the quantity, with v_{ab} being defined as the voltage before the transmission inductance L_s and v_{cd} as one after the transmission inductance L_s.

According to Figure 3, on the low-voltage side, S_1 and S_2 are main switches, and the duty cycle of each switch is D. the turn-on pulse phase of S_1 switch is 180 ° ahead of that of S_2 switch; S_3 and S_1 are complementary conduction, S_4 and S_2 are complementary conduction. On the high voltage side, the turn-on pulse phase of S_1 is ahead of S_5, which is defined as φ is the phase shift ratio between S_1 and S_5, that is, the phase angle difference (i.e., phase shift angle) between S_1 and S_5 divided by 2π; The duty cycle D of switches S_5 and S_6 is fixed at 0.5, so the symmetry of active voltage doubling can be realized. The capacitances of voltage doubling capacitors C_1 and C_2 are same and the withstand voltages are same. The

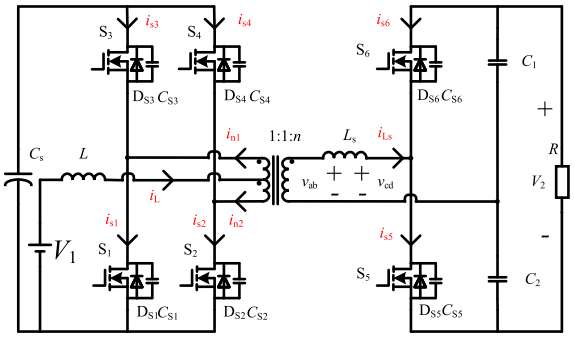


FIGURE 3. Topology of push pull current type bidirectional DC/DC converter.

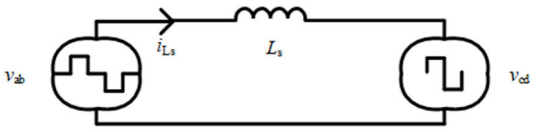


FIGURE 4. Equivalent transmission circuit of converter.

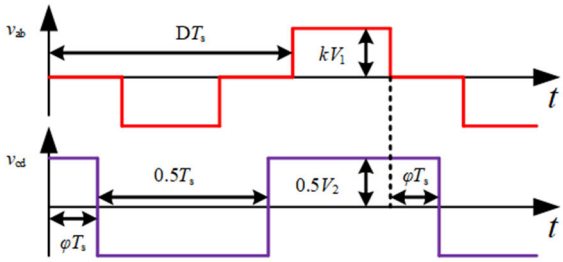


FIGURE 5. Primary and secondary voltage waveforms of converter.

transformer ratio is 1:1:n, i_{n1} and i_{n2} are the current of the two windings on the primary side of the transformer.

The equivalent transmission circuit of the push-pull current type bidirectional DC/DC converter is shown in Figure 4, the primary and secondary side voltage waveforms are shown in Figure 5. i_{Ls} represents the transmission current of the transmission inductance L_s. It can be seen from Figure 4 and Figure 5 that the ratio of V_{cd} to V_2 is 0.5. Therefore, in order to reduce the circulating power of the circuit. By adjusting the PWM pulse, the positive and negative amplitudes of v_{ab} and v_{cd} are equal respectively, so the primary and secondary side voltages match.

According to the one cycle current balance principle of input boost inductor, it can be obtained that

$$V_1 D + (V_1 - V_{C_s})(1 - D) = 0 \tag{1}$$

It can be seen that the voltage V_{Cs} of the clamping capacitor at the original side is

$$V_{C_s} = \frac{V_1}{1 - D} \tag{2}$$

When the circuit enters steady-state operation, the amplitude of the voltage on both sides of the transmission inductance at

the secondary side of the transformer are

$$V_{ab} = \frac{nV_{C_s}}{2} = \frac{n}{2(1-D)}V_1 = kV_1 \tag{3}$$

$$V_{cd} = \frac{V_2}{2} \tag{4}$$

In order to reduce the circulating power, the square wave voltage amplitude on both sides of the transmission inductor L_S is equal by PWM adjustment. The equation is as follows:

$$\frac{nV_1}{2}\frac{1}{1-D} = \frac{V_2}{2} \tag{5}$$

Then the voltage conversion ratio of input voltage V_1 and output voltage V_2 can be obtained as

$$\frac{V_2}{V_1} = \frac{n}{1-D} \tag{6}$$

According to the current KCL characteristics and ampere turns characteristics of the transformer

$$i_{n_1} + i_{n_2} = i_L \tag{7}$$

$$i_{n_1} \times N_1 - i_{n_2} \times N_2 + i_{L_s} \times N_3 = 0 \tag{8}$$

Set the turn ratio relationship as

$$N_1 : N_2 : N_3 = 1 : 1 : n \tag{9}$$

By combining (7), (8) and (9), the following can be solved

$$i_{n_1} = \frac{i_L - ni_{L_s}}{2} \tag{10}$$

$$i_{n_2} = \frac{i_L + ni_{L_s}}{2} \tag{11}$$

The converters proposed in [28] and [29] are current mode isolated bidirectional DC/DC converters. The comparison for topology proposed have and ones in [28] and [29], as given in Table 1:

TABLE 1. Comparison of key circuit parameters.

Comparison Parameters	Proposed in References [28]	Proposed in References [29]	Proposed in this Paper
Number of switches	4	6	6
High voltage side voltage	116V	400V	700V
Transmission Ratio	3-4	7-13	6-12
Applicable Power	Low	Medium	High

B. ANALYSIS OF CONVERTER WORKING PRINCIPLE

According to duty cycle D and shift ratio φ, the converter can be divided into 12 operating modes, as shown in Table 2. The "+" in the working mode number indicates the forward transmission of power, that is, the energy flows from the low-voltage side to the high-voltage side; "−" indicates the reverse transmission of power, that is, the energy flows from the high-voltage side to the low-voltage side. The working state between $0< D <1/2$ and $1/2< D <1$ is slightly different, which has been distinguished in mode division. Taking the A+ mode with $D>1/2$ as an example, this paper analyzes the specific working state of the converter, and the analysis process of other modes is similar.

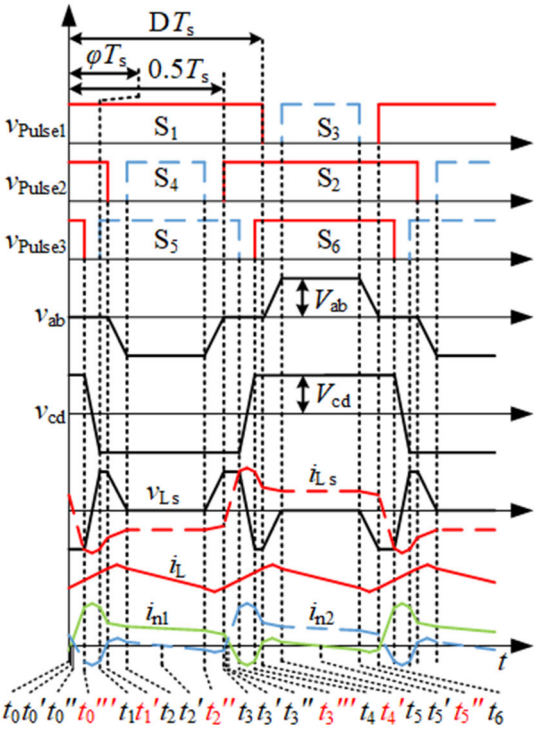


FIGURE 6. Key waveforms of the converter in a switching cycle.

TABLE 2. 12 working modes shift down compared to φ range.

Duty Cycle	Power Flow Direction	Phase Shift Ratio	Operating Mode
$0<D<1/2$	$P<0$	$-1/2<\varphi<D-1/2$	E-
	$P<0$	$D-1/2<\varphi<D/2-1/4$	D-
	$P>0$	$D/2-1/4<\varphi<0$	D+
	$P>0$	$0<\varphi<D$	E+
	$P>0$	$D<\varphi<D/2+1/4$	F+
	$P<0$	$D/2+1/4<\varphi<1/2$	F-
$1/2<D<1$	$P>0$	$-1/2<\varphi<D/2-3/4$	C+
	$P<0$	$D/2-3/4<\varphi<D-1$	C-
	$P<0$	$D-1<\varphi<0$	B-
	$P<0$	$0<\varphi<D/2-1/4$	A-
	$P>0$	$D/2-1/4<\varphi<D-1/2$	A+
	$P>0$	$D-1/2<\varphi<1/2$	B+

In the working state of the push-pull current type bidirectional DC/DC converter, there are 18 working stages in a switching cycle. The time period t_0-t_6 is one cycle of the converter. The waveform in a switching cycle of the push-pull current DC/DC converter is shown in Figure 6, and the modal analysis is carried out as follows.

Stage 1 (t_0-t_0'): Before t_0, switch S_2 and S_6 are turned on, C_{S1} and C_{S3} are resonant with L_S, and the working state is t_5'' - t_6(Stage 18). At t_0, the resonance between C_{S1}, C_{S3} and L_S ends, D_{S1} is turned on, and the zero voltage turn-on of switch S_1 is realized. The secondary circuit state of the

transformer does not change, and the current i_{Ls} is positive and i_{s6} is negative.

Stage 2 ($t_0\prime$ -$t_0\prime\prime$): At $t_0\prime$, i_{n1} rises from negative to zero, and then increases positively.

Stage 3 ($t_0\prime\prime$ - $t_0\prime\prime\prime$): At $t_0\prime\prime$, the transmission inductance current i_{Ls} drops to zero, then becomes negative and continues to decrease. The boost inductance current i_L, i_{s1}, i_{s2}, i_{s6}, i_{n1}, and i_{n2} at the input side are all positive.

Stage 4 ($t_0\prime\prime\prime$ - t_1): At $t_0\prime\prime\prime$, switch S_6 turned off, parasitic capacitances C_{S5} and C_{S6} of S_5 and S_6 resonate with transmission inductance L_s, voltage v_{CS5} at C_{S5} decreases from V_2, and voltage v_{CS6} at C_{S6} rises from zero. Until t_1, v_{CS6} rises to V_2, v_{CS5} drops to zero, and the resonance process ends.

Stage 5 (t_1- $t_1\prime$): At t_1, the resonance process ends and a drive signal is added to the switch S_5. Since the inductive current i_{Ls} cannot change suddenly, the transmission inductive current i_{Ls} forms a loop through the parasitic diode of the switch S_5, realizing the zero voltage conduction of S_5.

Stage 6 ($t_1\prime$ - t_2): At $t_1\prime$, switch S_2 is turned off. At this time, the capacitance C_{S2} and C_{S4} resonate with the inductance L_s, the voltage v_{CS2} at C_{S2} rises from zero, and the voltage v_{CS4} at C_{S4} decreases from V_{Cs}. Until t_2, v_{CS2} rises to V_{Cs}, v_{CS4} drops to zero, and the resonance ends.

Stage 7 (t_2- $t_2\prime$): At t_2, the driving signal S_4 is added to S_4 for conduction. Since the inductive current i_{n2} cannot change suddenly, the parasitic diode of switch S_4 is used for freewheeling, and the switch S_4 realizes zero voltage switch-on.

Stage 8 ($t_2\prime$ - $t_2\prime\prime$): The current i_{S4} of switch S_4 changes from negative to zero, and then becomes positive and continues to increase.

Stage 9 ($t_2\prime\prime$ - t_3): At $t_2\prime\prime$, the switch S_4 is turned off. At this time, C_{S2} and C_{S4} resonate with the transmission inductance L_s, the voltage v_{CS4} at C_{S4} rises from zero, and the voltage v_{CS2} at C_{S2} falls from V_{Cs}. Until t_3, v_{CS4} rises to V_{Cs}, v_{CS2} drops to zero, and the resonance process ends. At t_3, S_2 is turned on, and the DC/DC converter operates for half a cycle.

The time period t_3-t_6 is the second half of the cycle, and its working stage is similar to t_0-t_3 working stage, so it will not be repeated here.

III. ANALYSIS OF SOFT SWITCHING PROCESS

Through the analysis of the working principle in the previous section, it can be found that the push-pull current source DC/DC converter realizes zero voltage switching on at the moments of switching on and off of the switch. The parasitic capacitance of the switch resonates with the transformer transmission inductance L_s, and when the opposite the bridge arm is turned on, the voltage of the switch drops to zero, making the reverse parallel diode conductive. By analyzing the resonant process, the soft switching conditions of push-pull DC/DC converter can be deduced, which need to meet the following requirements: (1) the current direction of the switch is negative at the opening time; (2) The energy in the transmission inductor can fulfill the demand of parasitic capacitor charging and discharging. The resonant modes of push-pull current type DC/DC converter are stage 4 ($t_0\prime\prime$ - t_1), stage 6 ($t_1\prime$ - t_2), stage 9 ($t_2\prime\prime$ - t_3), stage 13 ($t_3\prime\prime\prime$ - t_4), stage 15 ($t_4\prime$ - t_5), and stage 18 ($t_5\prime\prime$ - t_6). At $t_0\prime\prime\prime$ in stage 4, the switch S_6 is turned off, and then S_5 realizes zero voltage switching on; in stage 6, switch S_2 is turned off at $t_1\prime$, and then S_4 realizes zero voltage switching on; S_4 is turned off at $t_2\prime\prime$ in stage 9, and then S_2 realizes zero voltage switching on; at $t_3\prime\prime$ in stage 13, S_5 is turned off, and then S_6 realizes zero voltage switching on; S_1 is turned off at $t_4\prime$ in stage 15, and then S_3 realizes zero voltage switching on; S_3 is turned off at $t_5\prime\prime$ in stage 18, and then S_1 realizes zero voltage switching on.

In the push-pull current type DC/DC converter, the operation stages of bridge arms S_1 and S_2, S_3 and S_4, S_5 and S_6 are completely symmetrical, and there is no lead and lag phenomenon. Therefore, as long as the zero voltage switching on of switches S_1, S_3 and S_5 are realized, the zero voltage switching on of all switches can be realized. Therefore, the soft switching analysis will be carried out for switch S_1 (stage 18), S_3 (stage 15), and S_5 (stage 4).

In the soft switching analysis, the ratio of the equivalent transmission inductance $L_s\prime$ to the original transmission inductance L_s is 1: n^2; The ratio of the equivalent voltage doubling capacitor voltage $V_{C1}\prime$ to the original voltage doubling capacitor voltage V_{C1} is 1: n.

A. SOFT SWITCHING ANALYSIS OF SWITCH S_1

At $t_5\prime\prime$, the switch S_3 is turned off. At this time, C_{S1} and C_{S3} resonate with the transmission inductance L_s, the voltage v_{CS3} at C_{S3} rises from zero, and the voltage v_{CS1} at C_{S1} decreases from V_{Cs}. Until t_6, v_{CS3} rises to V_{Cs}, v_{CS1} drops to zero, and the resonance process ends. The Zero voltage switch-on circuit of S_1 is shown in Figure 7. According to the switch-on process, the S_1 zero voltage switch-on equivalent circuit is shown in Figure 8.

The following formula can be listed by the equivalent circuit

$$\begin{cases} v_{CS3} + v_{CS1} = V_{Cs} \\ L_s' \dfrac{di_{Ls}'}{dt} = V_{C1}' - v_{CS1} \\ i_3 = C_{S3} \dfrac{dv_{CS3}}{dt} \\ i_1 = C_{S1} \dfrac{dv_{CS1}}{dt} \\ i_1 = i_3 + i_{Ls}' \end{cases} \tag{12}$$

Due to the symmetry of switching devices,

$$C_{S1} = C_{S3} = C_r \tag{13}$$

Solve the above equation and obtain

$$\frac{d^2 i_{Ls}'}{dt^2} + \frac{1}{2C_r L_s'} i_{Ls}' = 0 \tag{14}$$

At time $t_5\prime\prime$, the switch S_3 is turned off, and according to the steady-state process, the initial value I_{Ls3} of the current $i_{Ls}\prime$

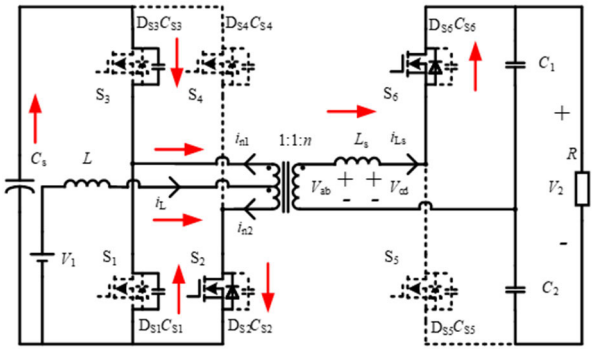


FIGURE 7. Zero voltage switch-on circuit of S_1.

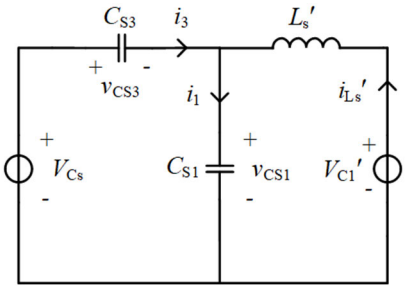


FIGURE 8. Zero voltage switching on equivalent circuit of S_1.

can be obtained as

$$I_{Ls3} = I_{n1}(t_5'') = -\frac{\frac{V_2}{n}}{4Lf_s}(1 - D)(D - \frac{1}{2}) < 0 \tag{15}$$

By combining the above two equations, it can be concluded that

$$i_{Ls}'(t) = I_{Ls3}\cos[\frac{1}{\sqrt{2L_s'C_r}}(t - t_5'')] \tag{16}$$

$$v_{CS1}(t) = V_{C1}' + I_{Ls3}\sqrt{\frac{L_s'}{2C_r}}\sin[\frac{1}{\sqrt{2L_s'C_r}}(t - t_5'')] \tag{17}$$

In the formula, $Z_r = \sqrt{\frac{L_s'}{2C_r}}$ is the characteristic impedance of the resonant circuit, and $\omega_r = \frac{1}{\sqrt{2L_s'C_r}}$ is the resonant frequency, the instantaneous value of voltage v_{CS1} is

$$v_{CS1}(t) = V_{C1}' + I_{Ls3}Z_r\sin[\omega_r(t - t_5'')] \tag{18}$$

The variation of voltage v_{CS1} on switch S_1 can be analyzed by (18). When $\omega_r(t - t_5'') = \pi/2$, the voltage v_{CS1} reaches its minimum value,

$$V_{CS1min} = V_{C1}' + I_{Ls3}Z_r \tag{19}$$

In order to achieve zero voltage switching on of switch S_1, the voltage at S_1 should be reduced to zero at the end of stage 18, so D_{S1} can conduct, that is $V_{CS1min} < 0$,

$$Z_r > \frac{V_{C1}'}{-I_{Ls3}} \tag{20}$$

It can also be written as

$$\sqrt{\frac{L_s'}{2C_r}} > \frac{V_{C1}'}{-I_{Ls3}} \tag{21}$$

The above analysis process shows that when the transmission inductance is fixed, the smaller the parasitic capacitance C_r, the easier for S_1 to achieve soft switching in a certain range.

When the parasitic capacitor is charged and discharged, the current will drop at the slope V_{C1}'/L_s'; When C_{S1} is too small, the voltage v_{CS1} will drop to zero in advance, but at this time, the drive signal does not come, which makes the parasitic capacitor C_{S1} lose the opportunity of soft switching when charged. Therefore, it is necessary to design the dead time T_d to make the voltage v_{CS1} meet the minimum requirement without causing the capacitor C_{S1} to be recharged. Usually, the dead time $T_d = T_r/4$, where $T_r = 2\pi/\omega_r$ is the resonant period.

B. SOFT SWITCHING ANALYSIS OF SWITCH S_3

At t_4', switch S_1 is turned off. At this time, the capacitors C_{S1} and C_{S3} resonate with the inductance L_s, the voltage v_{CS1} on C_{S1} rises from zero, and the voltage v_{CS3} on C_{S3} decreases from V_{Cs}. Until t_5, v_{CS1} rises to V_{Cs}, v_{CS3} drops to zero, and the resonance ends. The circuit of S_3 to realize zero voltage switching on is shown in Figure 9, and its equivalent circuit is shown in Figure 10.

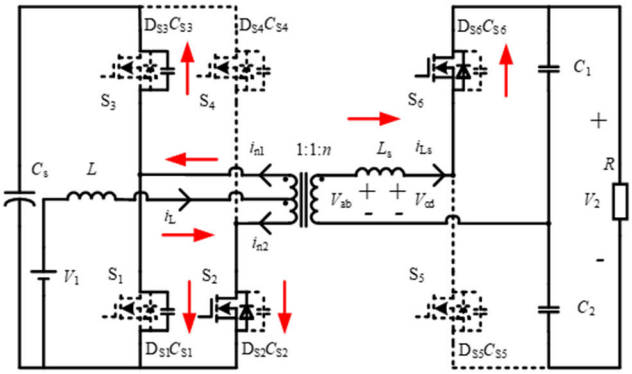


FIGURE 9. Zero voltage switch-on circuit of S_3.

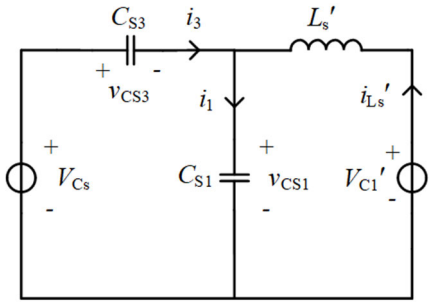


FIGURE 10. Zero voltage switch-on equivalent circuit of S_3.

The following formula can be listed by the equivalent circuit

$$\begin{cases} v_{CS3} + v_{CS1} = V_{Cs} \\ L_s' \dfrac{di_{Ls}'}{dt} = V_{C1}' - V_{Cs} + v_{CS3} \\ i_1 = C_{S1} \dfrac{dv_{CS1}}{dt} \\ i_3 = C_{S3} \dfrac{dv_{CS3}}{dt} \\ i_3 = i_1 - i_{Ls}' \end{cases} \tag{22}$$

Due to the symmetry of switching devices,

$$C_{S1} = C_{S3} = C_r \tag{23}$$

At time t_4', the switch S_1 is turned off, and according to the steady-state process, the initial value I_{Ls1} of the current i_{Ls}' can be obtained

$$I_{Ls1} = I_{n1}(t_4') = \frac{\frac{V_2}{n}}{4Lf_s}(1 - D)(D - \frac{1}{2}) > 0 \tag{24}$$

By combining the above two equations, it can be concluded that

$$v_{CS3}(t) = V_{Cs} - V_{C1}' - I_{Ls1} Z_r \sin[\omega_r(t - t_4')] \tag{25}$$

The variation of voltage v_{CS3} on switch S_3 can be analyzed by (25). When $\omega_r(t - t_4') = \pi/2$, the voltage v_{CS3} reaches its minimum value V_{CS3min}. In order to achieve zero voltage switching of switch S_3, the voltage at S_3 should be reduced to zero at the end of stage 15, so D_{S3} can conduct,that is $V_{CS3min} < 0$,

$$Z_r = \sqrt{\frac{L_s'}{2C_r}} > \frac{V_{Cs} - V_{C1}'}{I_{Ls1}} \tag{26}$$

The above analysis process shows that when the transmission inductance is fixed, the smaller the parasitic capacitance C_r, the easier for S_3 to achieve soft switching in a certain range.

When the parasitic capacitor is charged and discharged, the current will drop at the slope (V_{C1}' -V_{Cs})/L_s', and when C_{S3} is too small, the voltage v_{CS3} will drop to zero in advance, but at this time, the drive signal does not come, which makes the parasitic capacitor C_{S3} lose the opportunity of soft switching when charged. Therefore, it is necessary to design the dead time T_d to make the voltage v_{CS3} meet the minimum requirement without causing the capacitor C_{S3} to be recharged.

C. SOFT SWITCHING ANALYSIS OF SWITCH S_5

At t_0'' ', switch S_6 is turned off. At this time, the capacitors C_{S5} and C_{S6} resonate with the inductance L_s, the voltage v_{CS5} on C_{S5} decreases from V_2, and the voltage v_{CS6} on C_{S6} rises from zero. Until t_1, v_{CS6} rises to V_2, v_{CS5} drops to zero, and the resonance ends. The circuit of S_5 to realize zero voltage switching on is shown in Figure 11, and its equivalent circuit is shown in Figure 12.

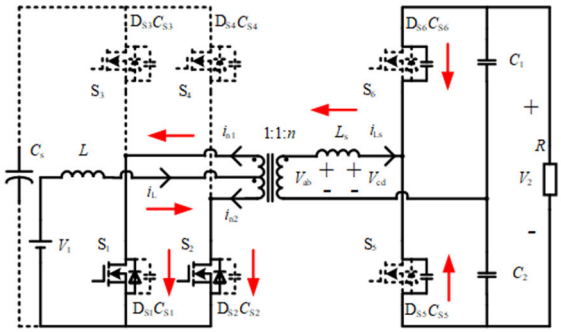


FIGURE 11. Zero voltage switch-on circuit of S_5.

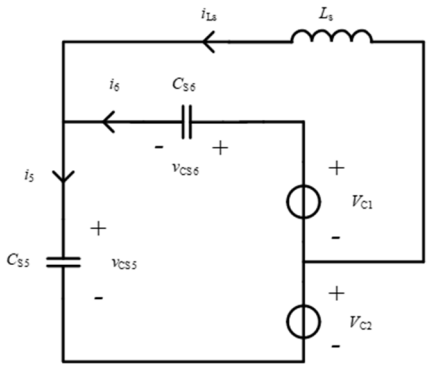


FIGURE 12. Zero voltage switch-on equivalent circuit of S_5.

The following formula can be listed by the equivalent circuit

$$\begin{cases} v_{CS5} + v_{CS6} = V_{C2} + V_{C1} \\ L_s \dfrac{di_{Ls}}{dt} = V_{C2} - v_{CS5} \\ i_6 = C_{S6} \dfrac{dv_{CS6}}{dt} \\ i_5 = C_{S5} \dfrac{dv_{CS5}}{dt} \\ i_5 = i_6 + i_{Ls} \end{cases} \tag{27}$$

Due to the symmetry of switching devices,

$$C_{S5} = C_{S6} = C_r \tag{28}$$

At time t_0' '', the switch S_6 is turned off, and according to the steady-state process, the initial value I_{Ls6} of the current i_{Ls} can be obtained

$$I_{Ls6} = I_{Ls}(t_0''') = \frac{V_2}{2L_s f_s}(\frac{1}{4} - \frac{D}{2}) < 0 \tag{29}$$

By combining the above two equations, it can be concluded that

$$v_{CS5}(t) = V_{C2} + I_{Ls6} Z_r \sin[\omega_r(t - t_0''')] \tag{30}$$

The variation of voltage v_{CS5} on switch S_5 can be analyzed by (30). When $\omega_r(t - t_0''') = \pi/2$, the voltage v_{CS5} reaches its minimum value V_{CS5min}. In order to achieve zero voltage switching of switch S_5, the voltage at S_5 should be reduced

to zero at the end of stage 4, so D_{S5} can conduct,that is $V_{CS5min} < 0$,

$$Z_r = \sqrt{\frac{L_s}{2C_r}} > \frac{V_{C2}}{-I_{Ls6}} \tag{31}$$

The above analysis process shows that when the transmission inductance is fixed, the smaller the parasitic capacitance C_r, the easier for S_5 to achieve soft switching in a certain range.

When the parasitic capacitor is charged and discharged, the current will drop at the slope V_{C2}/L_s, and when C_{S5} is too small, the voltage v_{CS5} will drop to zero in advance, but at this time, the drive signal does not come, which makes the parasitic capacitor C_{S5} lose the opportunity of soft switching when charged. Therefore, it is necessary to design the dead time T_d to make the voltage v_{CS5} meet the minimum requirement without causing the capacitor C_{S5} to be recharged.

The above is the analysis of the soft switching implementation process of the converter in A+ mode. Similarly, the soft switching characteristics of all switches in all 12 operating modes of the converter are shown in Table 3.

TABLE 3. Soft switching characteristics of switches in 12 working modes.

Duty Cycle	$S_{1,2}$	$S_{3,4}$	$S_{5,6}$	Operating Mode
D<1/2	Hard-switched	ZVS	ZVS	D+E+F+
	ZVS	Hard-switched	ZVS	D-E-F-
D>1/2	ZVS	ZVS	ZVS	A+B+C+A-B-C-

It can be seen from table 3 that all switches of the converter can realize soft switching under six operating modes with duty cycle $D > 1/2$. While duty cycle $0 < D < 1/2$, S_1 and S_2 are hard switching during forward power transmission; S_3 and S_4 are hard switching during reverse power transmission. Through the design of the transformer turn ratio, the converter can operate in the duty cycle $D > 1/2$ mode, which can realize the zero voltage switching of all switches and improve the efficiency of the converter.

D. INFLUENCE OF EXCITATION INDUCTANCE ON SOFT SWITCHING

When analyzing the working principle of the system, it is generally considered that the value of transformer excitation inductance L_m is very large, and its influence on the circuit is ignored. However, the excitation inductance L_m of the transformer in the actual system is not infinite, and its size will have a certain impact on the soft switching characteristics of the converter. This section describes this problem. Figure 13 shows the transformer equivalent model in the actual system. The boost inductance L and transmission inductance L_S remain unchanged, and the inductance L_{m1} and L_{m2} are the excitation inductance of the two windings on the primary side. The currents i_{p1} and i_{p2} are the converted currents from the secondary current to the primary side.

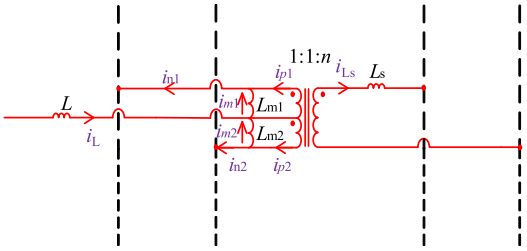


FIGURE 13. Equivalent model of push pull transformer in actual system.

In the actual equivalent model of push-pull transformer shown in Figure 13, the inductance currents meet the following relationship:

$$\begin{cases} i_{n1} + i_{n2} + i_{m1} - i_{m2} = i_L \\ i_{p1} \times N_1 - i_{p2} \times N_2 + i_{Ls} \times N_3 = 0 \\ i_{p1} + i_{m1} = i_{n1} \\ i_{p2} - i_{m2} = i_{n2} \\ i_{m1} = i_{m2} \end{cases} \tag{32}$$

According to formula (32),

$$\begin{cases} i_{p1} = (i_L - n i_{Ls})/2 \\ i_{p2} = (i_L + n i_{Ls})/2 \\ i_{p1} + i_{m1} = i_{n1} \\ i_{p2} - i_{m2} = i_{n2} \\ i_{m1} = i_{m2} \end{cases} \tag{33}$$

From (33), it can be seen that the values of primary winding currents i_{n1} and i_{n2} are related to excitation inductance currents i_{m1} and i_{m2}. Since the soft switching characteristics of the primary side switch are related to the winding current value, the excitation inductance currents i_{m1} and i_{m2} will also affect the soft switching conditions of the primary side switch.

Figure 14 is the key waveform diagram considering the excitation inductance in A+ mode. As the influence of excitation inductance on the circuit waveform is mainly considered, time division in Figure 14 is slightly different from that in Figure 6. By analyzing the operation process of the circuit, it can be seen that during t_0-t_2 and t_3-t_5, the switches S_1 and S_2 are turned on at the same time. At this time, the primary winding voltage is zero, and the excitation inductance currents i_{m1} and i_{m2} remain unchanged. During t_2-t_3, the switches S_1 and S_4 are turned on at the same time. At this time, the primary winding voltage is the clamping capacitor voltage V_{Cs}, and the excitation inductance currents i_{m1} and i_{m2} increase along a positive direction. During t_5-t_6, the switches S_2 and S_3 are turned on at the same time. At this

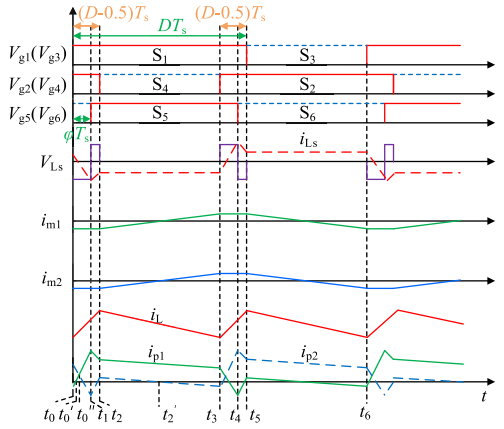


FIGURE 14. Key waveform of A+ mode considering excitation inductance.

time, the primary winding voltage is the negative clamping capacitor voltage V_{Cs}, and the excitation inductance currents i_{m1} and i_{m2} first decrease along the positive direction and then increase along the reverse direction.

Since the excitation currents i_{m1} and i_{m2} are completely symmetrical in the first and second half cycles, the following boundary conditions can be obtained:

$$i_{m1}(t_0) = -i_{m1}(t_3) \tag{34}$$

The excitation currents at t_0 and t_3 are equal in magnitude and opposite in direction. According to this relationship and the working principle of the converter, the expressions of excitation inductance currents i_{m1} and i_{m2} can be solved,

$$\begin{aligned} i_{m1}(\theta) &= i_{m2}(\theta) \\ &= \frac{V_{cs}}{2L_m f_s} \times \begin{cases} D-1 & 0 < \theta < D - \frac{1}{2} \\ 2\theta - D & D - \frac{1}{2} < \theta < \frac{1}{2} \\ 1-D & \frac{1}{2} < \theta < D \\ -2\theta + D + 1 & D < \theta < 1 \end{cases} \end{aligned} \tag{35}$$

where L_m is the value of the overall excitation inductance of the primary winding

From Figure 14 and (35), it can be seen that at t_0, switch S_1 is turned on, and the direction of excitation inductance current i_{m1} and winding current i_{n1} are along the same direction, which is conducive to the realization of soft switching. At t_5, the switch S_3 is turned on, and the excitation inductance current i_{m1} and winding current i_{n1} are along the same direction, which is conducive to the realization of soft switching. Therefore, in the soft switching characteristics of the system, the excitation current is always conducive to the realization of the soft switching process. In the actual parameter design of push-pull transformer, the excitation current can be appropriately increased by appropriately reducing the value of excitation inductance L_m, so as to accelerate the charging and discharging process of parasitic capacitor of switch and create conditions for zero voltage switching on.

IV. ANALYSIS OF SIMULATION RESULTS

In this paper, PISM software is used to simulate the working process of the circuit, and the simulation parameters are shown in Table 4.

TABLE 4. System parameters.

Quantity	Symbol	Value
Input voltage	V_1	96V
Output voltage	V_2	700V
Input inductance	L	100μH
Transmission inductance	L_s	80μH
Clamping capacitor	C_s	220μF
Voltage doubling capacitor	C_1	220μF
Voltage doubling capacitor	C_2	220μF
Output resistance	R	490Ω
Transformation ratio	n	3
Switching frequency	f_s	50kHz

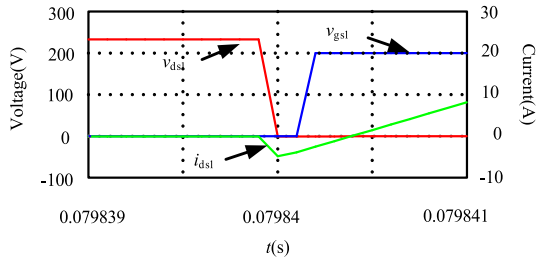


FIGURE 15. The simulation waveform of switch S_1 turned on.

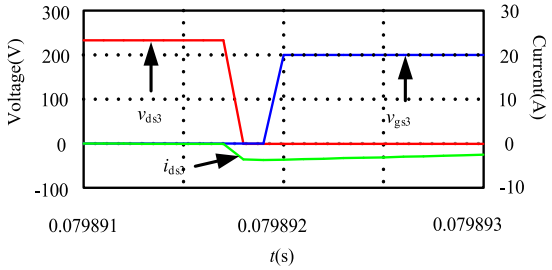


FIGURE 16. The simulation waveform of switch S_3 turned on.

A. SIMULATION ANALYSIS OF SOFT SWITCHING IN A+MODE

The simulation waveform of switch S_1 turned on is shown in Figure 15. It can be seen that the current i_{ds1} is always negative before the drain source voltage v_{ds1} drops to zero at the turn-on time of the switch, indicating that the current has been flowing through the parasitic diode of switch S_1, and that switch S_1 has realized zero voltage switch-on.

According to the soft switching process analysis of switch S_1, after substituting the corresponding values, it can be obtained that $I_{Ls3} = -5$A, $L_s{}' = 8.89\mu$H, $V_{C1}{}' = 116.67$V, and according to (21), C_r <8.17nF. The parasitic capacitance of switch S_1 is 60pF, which is within the numerical range

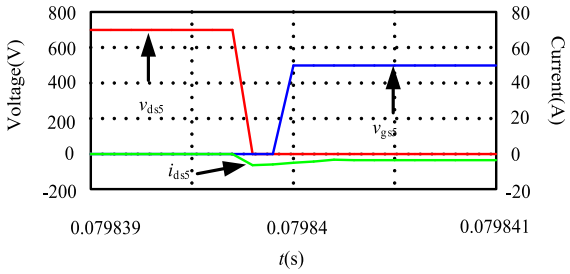


FIGURE 17. The simulation waveform of switch S_5 turned on.

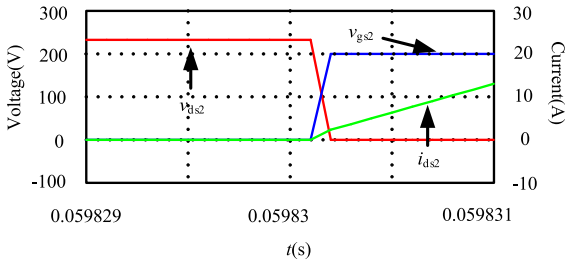


FIGURE 18. The simulation waveform of S_2 turned on when 0.1μF parasitic capacitor was added.

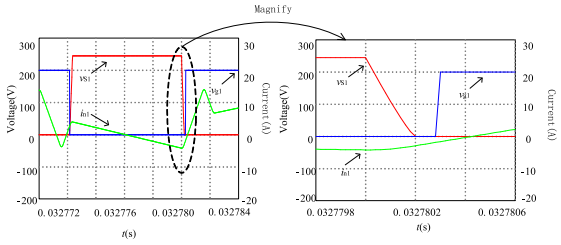


FIGURE 19. Simulation waveform of S_1 when excitation inductance is 500μH.

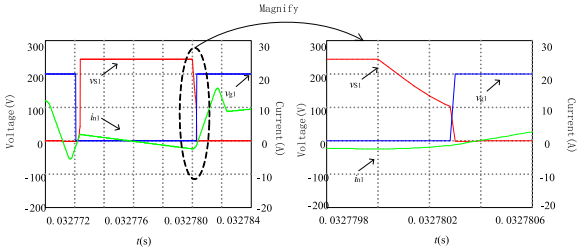


FIGURE 20. Simulation waveform of S_1 when excitation inductance is 1000μH.

of soft switching parasitic capacitance. Therefore, switch S_1 achieves soft switching.

The simulation waveform of switch S_3 turned on is shown in Figure 16. It can be seen that the current i_{ds3} is always negative before the drain source voltage v_{ds3} drops to zero at the turn-on time of the switch, indicating that the current has been flowing through the parasitic diode of switch S_3, and that switch S_3 has realized zero voltage switch.

According to the soft switching process analysis of switch S_3, after substituting the corresponding values, it can be obtained that $I_{Ls1} = 5.07$A, $L_s\prime = 8.89\mu$H, $V_{C1}\prime = 116.67$V, and according to (26), C_r <8.4nF. The parasitic capacitance of switch S_3 is 120pF, which is within the numerical range of soft switching parasitic capacitance. Therefore, switch S_3 achieves soft switching.

The simulation waveform of switch S_5 turned on is shown in Figure 17. It can be seen that the current i_{ds5} is always negative before the drain source voltage v_{ds5} drops to zero at the turn-on time of the switch, indicating that the current has been flowing through the parasitic diode of switch S_5, and that switch S_5 has realized zero voltage switch-on.

According to the soft switching process analysis of switch S_1, after substituting the corresponding values, it can be obtained that $I_{Ls6} = -7$A, $L_s = 80\mu$H, $V_{C2} = 350$V, and according to (31), C_r <16nF. The parasitic capacitance of switch S_5 is 130pF, which is within the numerical range of soft switching parasitic capacitance. Therefore, switch S_5 achieves soft switching.

B. THE INFLUENCE OF PARASITIC CAPACITANCE ON SOFT SWITCHING

On the basis of achieving zero voltage switch-on for each switch in the previous section, 0.1μF parasitic capacitance is added to the switch S_2. The simulation waveform of the turn-on time is shown in Figure 18.

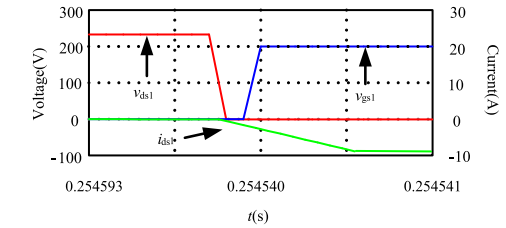
It can be seen from Figure 18 that after 0.1μF parasitic capacitor is connected in parallel at the switch, the drive signal v_{gs2} has been added between grid and source before the drain source voltage v_{ds2} of the switch drops to zero. The drain current i_{ds2} flows through the switch with a positive value, causing the voltage and current to form an overlapping region at the turn-on time, and resulting in the turn-on loss.

From the above research, it can be seen that the parasitic capacitance range of the switch is C_r <8.166nF, and that the parasitic capacitance at the switch should be within this range, otherwise the push-pull current type DC/DC converter will not be able to form zero voltage switch-on, resulting in losses during the turn-on process and affecting the service life of the switch.

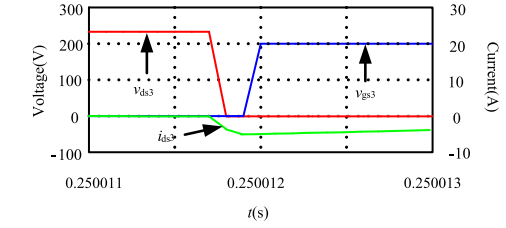
C. THE INFLUENCE OF EXCITATION INDUCTANCE ON SOFT SWITCHING

In this section, the influence of excitation inductance on soft switching is simulated, and the simulation parameters are consistent with Table 4. Figure 19 shows the simulation waveform of switching on process of switch S_1 in A+ mode, when the excitation inductance is 500μH. Figure 20 shows the simulation waveform of switching on process of switch S_1 in A+ mode, when the excitation inductance is 1000μH.

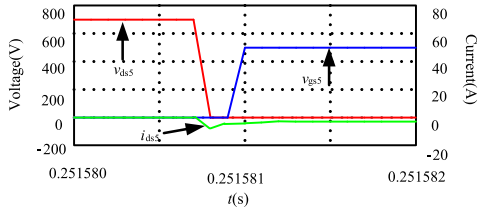
By comparison, it can be found that, when the excitation inductance is 500μH, the winding current i_{n1} at the opening time of switch S_1 is -3A, and that the parasitic capacitance is charged and discharged within the dead time. Before the drive signal V_{g1} arrives, the drain source voltage of switch has been reduced to zero, realizing zero voltage switching. When the excitation inductance is 1000μH, the winding current



a) The simulation waveform of switch S_1 turned on under light load



b) The simulation waveform of switch S_3 turned on under light load



c) The simulation waveform of switch S_5 turned on under light load

FIGURE 21. The simulation waveform of switch S_1,S_3 and S_5 turned on under light load.

i_{n1} at the opening time of the switch is -2A, which is less than the winding current when the excitation inductance is 500μH. During the dead time, the charging and discharging of parasitic capacitance cannot be completed, and the switch S_1 cannot realize zero voltage switching.

D. SOFT SWITCHING SIMULATION UNDER LIGHT LOAD

In the design of soft switch, it is not easy to realize soft switch due to small current under light load. Therefore, this section verifies the realization of soft switch under light load. The rated power of the converter designed in this paper is 3kW, and it is generally considered as light load when the output power is 10% of the rated power. Therefore, this section gives the soft switching condition when the output power is 0.3kw, as shown in Figure 21. Adjust the Output resistance R from 490Ω to 1633Ω.

It can be seen from the simulation waveform that the current is always negative before the drain source voltage drops to zero at the turn-on time of the switches, indicating that the current has been flowing through the parasitic diode of switches, and that switches has realized zero voltage switch-on.

V. EXPERIMENTAL VALIDATION

The photo of the experimental platform is shown in Figure 22. The circuit parameters are listed in Table 4. Figure 23 shows the soft switching waveform of S_1. Excitation inductance of single transformer is 500μH, the switch junction capacitance is 288pF and the dead time is 200ns. When the switch is turned off, the drain source voltage V_{ds1} is clamped at 245V by the clamping capacitor. When the drive signal is turned on, the drain source voltage of the switch has dropped to zero, and the current of the switch is less than zero, then the current flows through the anti-parallel diode. This shows that the switch S_1 achieves zero voltage switching. The soft switching process of S_3 is similarly to that of S_1. Figure 24 shows the soft switching waveform of S_3.

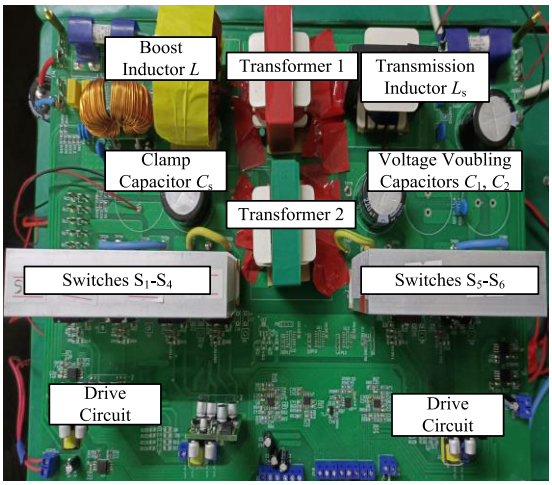
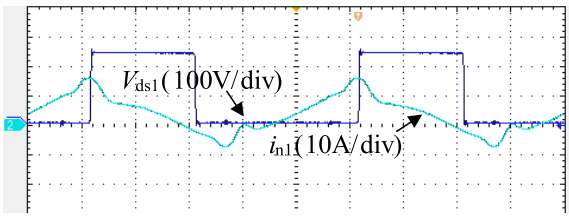
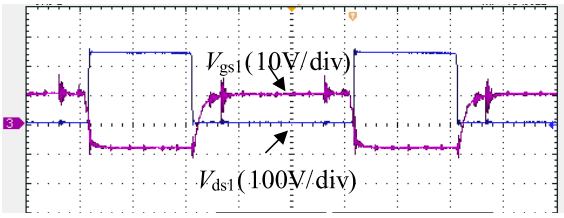


FIGURE 22. Main circuit board of the experimental platform.



a) Drain source voltage and current of S_1



b) Drain source voltage and drive voltage of S_1

FIGURE 23. Soft switching experimental waveform of S_1.

Figure 25 shows the soft switching waveform of S_5. Single transformer excitation inductance is 500μH, the switch junction capacitance is 200pF and the dead time is 200ns. When the switch is turned off, the drain source voltage V_{ds5} is clamped at 700V by the clamping capacitor. When the driving signal is turned on, the drain source voltage of the switch has dropped to zero, then the current flows through the anti-parallel diode. This shows that the switch S_5 has realized zero

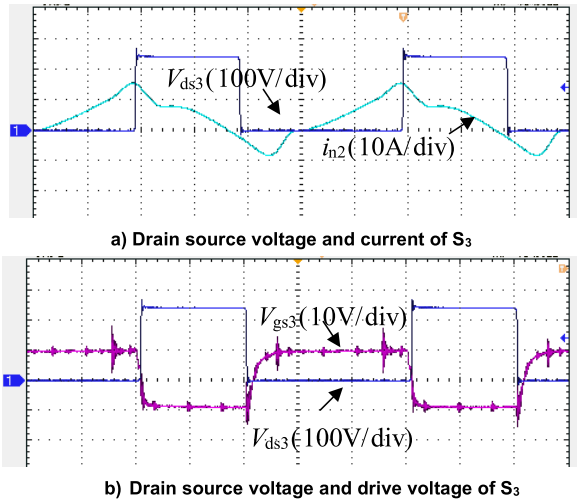


FIGURE 24. Soft switching experimental waveform of S_3.

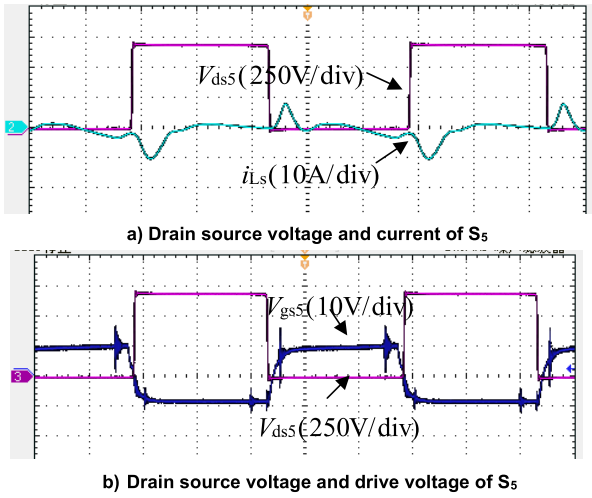


FIGURE 25. Soft switching experimental waveform of S_5.

voltage switching. The spike of the driving pulse is caused by the switching action of other switches during the operation of the system.

VI. CONCLUSION

The push-pull current-mode bidirectional DC/DC converter designed in this paper adopts a topology in which a boost circuit is cascaded with a push-pull transformer. This design enables bidirectional power transmission, and is suitable for a wide voltage input range, and has a small current ripple on the battery side. Firstly, this paper analyzes the operating modes of the converter and takes the A+ mode as an example to analyze the soft switching process of the converter. Secondly, by establishing an equivalent circuit of the switching transient of the switch, the influence of the dead time, parasitic capacitance, and excitation inductance on soft switching is analyzed, and the conditions for achieving soft switching in the converter are obtained. The soft switching characteristics under all 12 operating modes of the converter are also given. Finally, based on the analyzed soft switching conditions, suitable circuit parameters are selected to simulate and experimentally verify the DC/DC converter. The results show that the push-pull isolated DC/DC converter can achieve soft switching of all switches by applying the soft switching conditions proposed in this paper, which verifies the correctness and effectiveness of theoretical analysis.

REFERENCES

[1] M. Wu, N. Hou, W. Song, and W. Jiang, "Direct power balance control scheme of the input-independent-output-parallel operated full-bridge isolated DC–DC converters," *Proc. CSEE*, vol. 38, no. 5, pp. 1329–1337, May 2018, doi: 10.13334/j.0258-8013.pcsee.171291.

[2] X. Yu, C. Tu, F. Xiao, and B. Liu, "Transient DC bias mechanism and suppression strategy of the three-port isolated DC–DC converter," *Trans. China Electrotech. Soc.*, vol. 35, no. 9, pp. 1962–1972, 2020, doi: 10.19595/j.cnki.1000-6753.tces.190384.

[3] S. S. Chakraborty and K. Hatua, "Modeling with beat frequency dynamics and phase-frequency control design for a dual-bridge series resonant converter," *IEEE Trans. Ind. Electron.*, vol. 69, no. 8, pp. 7952–7962, Aug. 2022, doi: 10.1109/TIE.2021.3109532.

[4] J. Ding, S. W. Zhao, and H. Yin, "A new type of soft switch isolated DC/DC converter with high step-up," *Adv. Technol. Electr. Eng. Energy*, vol. 39, no. 6, pp. 18–25, Jun. 2020, doi: 10.12067/ATEEE1908021.

[5] R. Wu, B. Wang, Y. Zou, B. Fan, L. Li, and Z. Zhu, "Energy router interface model based on bidirectional flow control for intelligent park," in *Proc. 43rd Annu. Conf. IEEE Ind. Electron. Soc.*, Beijing, China, Oct. 2017, pp. 7771–7776.

[6] L. Zhen, L. Penghua, S. Wanxing, D. Songhuai, D. Qing, and L. Zhipeng, "Research on a household energy router for energy internet," in *Proc. 13th IEEE Conf. Ind. Electron. Appl. (ICIEA)*, Wuhan, China, May 2018, pp. 952–957.

[7] K. Wang, X. Liu, L. Zhao, Y. Zhou, and D. Xu, "Research on structure and energy management strategy of household energy router based on hybrid energy storage," in *Proc. IEEE Power Energy Soc. Innov. Smart Grid Technol. Conf. (ISGT)*, Washington, DC, USA, Feb. 2019, pp. 1–5.

[8] Y. Qin, H. Hua, and J. Cao, "Short-term energy cache regulation for energy router: A robust H-infinity approach," in *Proc. IEEE Int. Conf. Energy Internet (ICEI)*, Nanjing, China, May 2019, pp. 161–166.

[9] B. Zhao, Q. Yu, and W. Sun, "Extended-phase-shift control of isolated bidirectional DC–DC converter for power distribution in microgrid," *IEEE Trans. Power Electron.*, vol. 27, no. 11, pp. 4667–4680, Nov. 2012, doi: 10.1109/TPEL.2011.2180928.

[10] W. Choi, K.-M. Rho, and B.-H. Cho, "Fundamental duty modulation of dual-active-bridge converter for wide-range operation," *IEEE Trans. Power Electron.*, vol. 31, no. 6, pp. 4048–4064, Jun. 2016, doi: 10.1109/TPEL.2015.2474135.

[11] Y.-F. Wang, L.-K. Xue, C.-S. Wang, P. Wang, and W. Li, "Interleaved high-conversion-ratio bidirectional DC–DC converter for distributed energy-storage systems—Circuit generation, analysis, and design," *IEEE Trans. Power Electron.*, vol. 31, no. 8, pp. 5547–5561, Aug. 2016, doi: 10.1109/TPEL.2015.2496274.

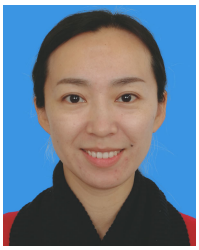
[12] A. R. N. Akhormeh, K. Abbaszadeh, M. Moradzadeh, and A. Shahirinia, "High-gain bidirectional quadratic DC–DC converter based on coupled inductor with current ripple reduction capability," *IEEE Trans. Ind. Electron.*, vol. 68, no. 9, pp. 7826–7837, Sep. 2021, doi: 10.1109/TIE.2020.3013551.

[13] M. Packnezhad and H. Farzanehfard, "Bidirectional soft-switching converter with reduced current ripple at low-voltage side," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 9, no. 4, pp. 4668–4675, Aug. 2021, doi: 10.1109/JESTPE.2020.3020778.

[14] H. Daneshpajooh, A. Bakhshai, and P. Jain, "Design of DC–DC converter with phase shift and duty cycle control for full range soft switching," in *Proc. IEEE 33rd Int. Telecommun. Energy Conf. (INTELEC)*, Amsterdam, The Netherlands, Oct. 2011, pp. 1–6.

[15] J. Jalili, S. M. M. Mirtalaei, M. R. Mohammadi, and B. Majidi, "Correction to: A ZVS high step-up converter based on an integrated boost-cuk topology," *Electr. Eng.*, vol. 104, no. 2, p. 817, Apr. 2022, doi: 10.1007/s00202-021-01450-y.

[16] S. Shabani, M. Delshad, R. Sadeghi, and H. H. Alhelou, "A high step-up PWM non-isolated DC–DC converter with soft switching operation," *IEEE Access*, vol. 10, pp. 37761–37773, 2022, doi: 10.1109/ACCESS.2022.3163146.
[17] Y. Zheng, B. Brown, W. Xie, S. Li, and K. Smedley, "High step-up DC–DC converter with zero voltage switching and low input current ripple," *IEEE Trans. Power Electron.*, vol. 35, no. 9, pp. 9416–9429, Sep. 2020, doi: 10.1109/TPEL.2020.2968613.
[18] W. Chen, K. Liu, J. Zhao, and C. Jin, "Dynamic improvement for phase-shift LLC resonant converter based on disturbance observer," *Energy Rep.*, vol. 9, pp. 1018–1025, Mar. 2023, doi: 10.1016/j.egyr.2022.11.115.
[19] H. Jeong, M. Kwon, and S. Choi, "Analysis, design, and implementation of a high gain soft-switching bidirectional DC–DC converter with PPS control," *IEEE Trans. Power Electron.*, vol. 33, no. 6, pp. 4807–4816, Jun. 2018, doi: 10.1109/TPEL.2017.2738705.
[20] Z. Hosseinzadeh, N. Molavi, and H. Farzanehfard, "Soft-switching high step-up/down bidirectional DC–DC converter," *IEEE Trans. Ind. Electron.*, vol. 66, no. 6, pp. 4379–4386, Jun. 2019, doi: 10.1109/TIE.2018.2863216.
[21] X. Tian, C. Wang, G. Sa, J. Hong, and P. Wang, "An accurate model for soft-switching analysis of three-port DC–DC converter," *J. Power Supply*, vol. 18, no. 4, pp. 94–101, Jul. 2020, doi: 10.13234/j.issn.2095-2805.2020.4.94.
[22] F. Yuan, R. Hao, X. You, P. Xiang, and C. Jingxian, "A high voltage gain wide range soft switching bidirectional DC–DC converter," *Chin. J. Electr. Eng.*, vol. 43, no. 19, pp. 7626–7639, Oct. 2023, doi: 10.13334/j.0258-8013.pcsee.221292.
[23] S. Hasanpour, Y. P. Siwakoti, and F. Blaabjerg, "Analysis of a new soft-switched step-up trans-inverse DC/DC converter based on three-winding coupled-inductor," *IEEE Trans. Power Electron.*, vol. 37, no. 2, pp. 2203–2215, Feb. 2022, doi: 10.1109/TPEL.2021.3103978.
[24] M. Mahmoudi, A. Ajami, E. Babaei, and J. Soleimanifard, "Theoretical and experimental evaluation of SEPIC-based DC–DC converters with two-winding and three-winding coupled inductors," *Int. J. Circuit Theory Appl.*, vol. 50, no. 11, pp. 3891–3910, Jun. 2022, doi: 10.1002/cta.3359.
[25] Y. Guan, Y. Cheng, T. Yao, Y. Wang, W. Wang, and D. Xu, "A high-performance DC–DC converter with soft switching characteristic and high voltage gain," *IEEE Trans. Power Electron.*, vol. 37, no. 10, pp. 12279–12288, Oct. 2022, doi: 10.1109/TPEL.2022.3172904.
[26] A. Mirzaee and J. S. Moghani, "Coupled inductor-based high voltage gain DC–DC converter for renewable energy applications," *IEEE Trans. Power Electron.*, vol. 35, no. 7, pp. 7045–7057, Jul. 2020, doi: 10.1109/TPEL.2019.2956098.
[27] M. R. S. de Carvalho, E. A. O. Barbosa, F. Bradaschia, L. R. Limongi, and M. C. Cavalcanti, "Soft-switching high step-up DC–DC converter based on switched-capacitor and autotransformer voltage multiplier cell for PV systems," *IEEE Trans. Ind. Electron.*, vol. 69, no. 12, pp. 12886–12897, Dec. 2022, doi: 10.1109/TIE.2022.3142432.
[28] F. Z. Peng, H. Li, G.-J. Su, and J. S. Lawler, "A new ZVS bidirectional DC–DC converter for fuel cell and battery application," *IEEE Trans. Power Electron.*, vol. 19, no. 1, pp. 54–65, Jan. 2004, doi: 10.1109/TPEL.2003.820550.
[29] S. Xiaofeng, W. Xiaoying, and S. Yanfeng, "A current mode bi-directional isolated DC–DC converter with zero voltage switching in the full power range," *Acta Electrotechn. Sinica*, vol. 33, no. 10, pp. 1–12, May 2018, doi: 10.19595/j.cnki.1000-6753.tces.161132.



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