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RESEARCH ARTICLE

A 28-GHz–195-dB FoM$_A$ 3.72-GHz/V Class-B/C Nested-*gm* VCO With Coupled Tail Filtering in a 65-nm CMOS

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ABSTRACT This paper introduces a class-B/C nested-*gm* voltage-controlled oscillator (VCO) with coupled tail filtering in the 28 GHz band. The addition of only two cross-coupled NMOSs duplicates the *gm* to boost the transconductance. This topology exhibits the characteristics of coupled VCOs, such as when two VCOs are interconnected through a transformer. The core area is minimized by implementing a tail-filtering inductor for a secondary harmonic filter in same space with the primary transformer. The proposed VCO is fabricated with a 65-nm CMOS process, an output frequency of 25.4–29.12 GHz, and a K_{VCO} of 3.72 GHz/V. It has a supply voltage of 1 V and consumes 16.8 mW of power. It exhibits a phase noise of –105.34 dBc/Hz with a 1 MHz offset. The proposed VCO has a core area of 0.06 mm^2. The figure of merit (FoM), FoM according to the area, and FoM according to K_{VCO} are –182.37, –194.96, and –192.66 dB, respectively.

INDEX TERMS Area saving, CMOS, class-B/C, high VCO gain, gm boosting, LC tank, nested gm, noise filtering, phase noise, VCO.

I. INTRODUCTION

LC voltage-controlled oscillators (VCOs) are essential in wireless communication and sensor applications to generate the variable frequencies required for signal transmission and reception. In particular, frequency-modulated continuous wave (FMCW) radar applications require high-gain VCOs that output wide frequency signals in one channel for high-distance resolution. VCO performance requires a pure signal to ensure the precision of the frequency output under low power consumption and to improve the efficiency of the device by reducing noise within the system. Therefore, VCO designs employ phase noise and power consumption as a figure of merit (FoM). In this process, the FoM for integration density and that for VCO gain (K_{VCO}) are defined as FoM$_A$ and FoM$_{KVCO}$, respectively. These FoMs are benchmarks in wireless communication, radar, and sensor technologies that require continuous frequency control and efficient power consumption.

The Lesson equation is generally used to determine the phase noise in VCOs. Phase noise is defined using various parameters, including the resonator's output frequency (f_{OUT}), LC tank inductance (L), noise factor (F), oscillation amplitude (V_A), and quality factor (Q). While L, f_{OUT}, and F are proportional to the phase noise, Q and V_A are inversely proportional. This equation describes how resonator characteristics and loading quality factors affect VCO phase noise at different frequency offsets from the carrier frequency.

In a VCO, an effective negative *gm* is essential for stable and controlled oscillations. This characteristic counteracts the inherent positive resistance within LC tank circuits. By providing negative transconductance, the VCO compensates for

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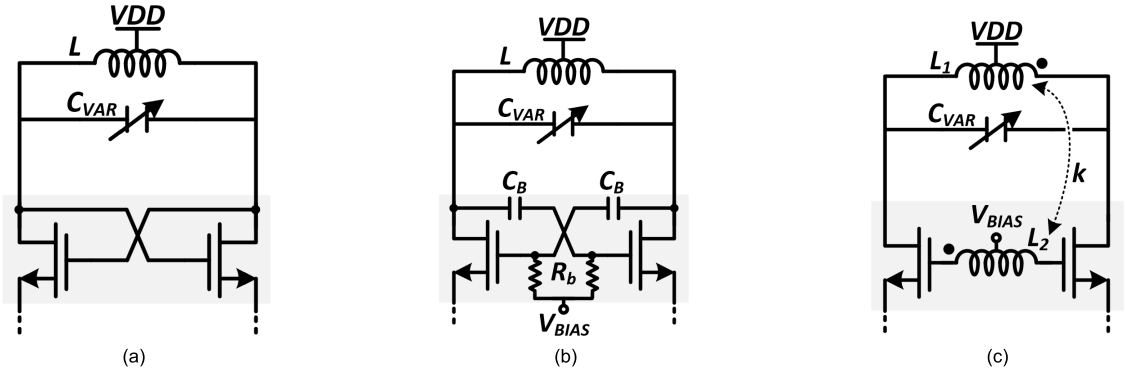


FIGURE 1. Overview of effective negative conductance (gm) topologies: (a) class-B VCO, (b) a DC decoupling class-C VCO, and (c) a transformer-coupled class-C VCO.

the loss of the tank circuit, ensuring continuous oscillation. This negative *gm* is crucial in regulating the amplitude of the oscillation signal and stabilizing the oscillation frequency, contributing to the overall stability of the VCO.

Fig. 1 illustrates an effective negative *gm* topology. Fig. 1(a) presents cross-coupled NMOS transistors in a class-B VCO configuration [1], [2], [3], [4], [5], [6], [7], [8], [9], [10], [11], [12], [13]. These transistors are biased to operate near the cut-off region, enabling the AC to generate oscillation waveforms. Cross-coupling between these components improves the linearity and frequency stability to ensure consistent output signals. Fig. 1(b) and (c) present a VCO with class-C operation. In the VCO design shown in Fig. 1(b), a DC decoupling capacitor removes the DC bias in the signal path, and only an AC component can pass through [14], [15], [16], [17], [18], [19], [20], [21], [22], [23], [24], [25], [26], [27], [28], [29], [30], [31], [32], [33], [34], [35], [36], [37]. This component ensures that the VCO operates in a way that prevents any unwanted DC interference from affecting the output signal. However, it results in a low Q and high F because high resistance is required to apply the common-mode DC bias voltage (V_{BIAS}). Therefore, a phase noise drop is inevitable according to the Lesson equation.

Fig. 1(c) shows that, in the class-C operation, the transformer feedback involves the integration of the transformer with the resonant LC tank. This feedback mechanism directs energy back into the tank, helping to improve the resonance and maintain the oscillation [38], [39], [40], [41], [42], [43], [44], [55], [56]. In a transformer-coupled VCO, the phase noise can be affected by the transformer's mutual inductance (k). Nonlinearity or fluctuations in the transformer characteristics, such as loss or coupling fluctuations with the frequency, can produce phase noise that affects the output signal quality of the VCO. As a result, it is essential to design a transformer with a high k and Q. In addition to these designs, class-F VCOs have been developed that employ both differential-mode (DM) and common-mode (CM) resonances by shaping impulse sensitivity functions (ISFs), dramatically improving phase noise performance [50], [51], [52], [53].

Several techniques have been developed to suppress the phase noise of LC VCOs. For example, VCO tail filtering has been designed to suppress secondary harmonics. This method implements inductor LH and capacitor CH between the negative *gm* and AC ground. The LC tank suppresses even harmonics with high impedance to the second harmonic frequency [10], [11], [12], [29], [36], [44], [49]. As the LC configuration of the tail, the node touching the negative *gm* falls to a voltage lower than the ground and secures the V_{DS} of the core MOSFET, increasing the output power of the VCO. This tail harmonic filtering technique reduces the phase noise but requires a greater area due to the additional inductor. This area issue can be solved by coupling the tail filtering inductor to a primary inductor with a low k [12].

Another useful technique is *gm* boosting, which can be achieved in two ways: (1) the current paths can be arranged at the gates of two cross-coupled MOSFETs [27], [28], [29], [30], [31], [32], [33], [41], [42] or (2) the current paths can be arranged in parallel with two other MOSFETs [8], [9], [36], [43]. These methods increase the oscillation amplitude of the output signal and support rapid start-up. This approach is suitable for class-C VCO structures with a low oscillation start-up power consumption because it reduces the core current. This technique also reduces the phase noise by increasing the signal amplitude according to the Lesson equation but requires additional total power consumption.

Dual-core coupling VCOs that integrate two oscillators interconnected through a coupling network have also been developed [45], [46], [47], [48], [54]. Typically, the primary core acts as the primary oscillator generating the main signal, while the secondary core adjusts the frequency by synchronizing with the primary core through a coupling network. Dual-core coupling VCOs offer a wider frequency tuning range (FTR) and lower phase noise. However, this design is complicated by the synchronization between the two cores, which requires sophisticated calibration, resulting in greater design complexity and lower integration efficiency.

A VCO controls the output frequency by constructing a varactor whose capacitance changes depending on the input voltage. As the varactor size increases, K_{VCO} increases to

produce a wide FTR, but the output frequency sensitivity increases depending on the input voltage of the VCO. This also affects the Q of the core, resulting in low phase noise for the VCO [49]. Previous studies on VCOs have reduced the phase noise by increasing the Q while constructing a small varactor that is insensitive to changes in frequency but is characterized by a narrow FTR. These VCOs implement a parallel capacitor bank to implement multiple channels and expand the practical FTR. The VCO proposed in the present study is an FMCW radar application target with a continuously broad FTR that implements only a large varactor without a capacitor bank. The proposed VCO thus has a novel structure with low phase noise despite the Q loss.

The proposed VCO implements a coupled tail-filtering technique with a coupled VCO to reduce the area and utilizes a class-C nested-*gm* topology to boost the *gm* and thus suppress the phase noise. In this topology, where two VCOs are interconnected, only two cross-coupled NMOSs are added to the transformer-coupled class-C VCO. The proposed VCO supports class-B/C mode by adjusting the bias voltage to the secondary inductor. Configuring a tail-filtering inductor as a transformer is thus advantageous for wide-band impedance, exhibiting a low k with the other two inductors. The proposed LC tank of the VCO achieves a frequency range of 25.40–29.12 GHz and a K_{VCO} of 3.72 GHz/V because it only employs a varactor without a capacitor bank.

The remainder of this paper is structured as follows. Section II describes the concept and circuit diagram of the proposed nested-*gm* class-B/C VCO with coupled tail filtering. The measurement results and conclusions are then presented in Sections III and IV, respectively.

II. PROPOSED DESIGN IMPLEMENTATION

Fig. 2 presents a block diagram of the proposed class-B/C nested-*gm* VCO. Two LC banks and an effective negative *gm* are employed with tail filtering. The two VCOs are interconnected, supplying voltage for each core. The proposed VCO operates in class-B mode if the internal voltage is equal to the supply voltage (i.e., $V_{INT} = V_{DD}$) and operates in class-C mode if the internal voltage is less than the supply voltage (i.e., V_{INT}<V_{DD}). Because both VCOs must oscillate during regular operation, V_{INT} cannot be zero, and the voltage may fall to the minimum oscillation condition. The nested *gm* in the proposed VCO has the effect of an overlapping *gm* via the effective negative *gm* bound to two stages. The *gm*-boosting techniques described in previous studies add current to the core, but the nested-*gm* approach employed in the proposed VCO multiplies the effective gm_1 and gm_2 using a two-stage common-source amplifier. Two LC tanks are coupled to each other and have one resonance frequency. Using tail filtering, the second harmonics are suppressed to reduce the phase noise.

Fig. 3 displays a circuit diagram of the proposed class-B/C nested-*gm* VCO with coupled tail filtering. M1 and M2 are cross-coupled by transformers L1 and L3, and L1 and two C_{var} pairs are employed as primary LC tanks. In addition,

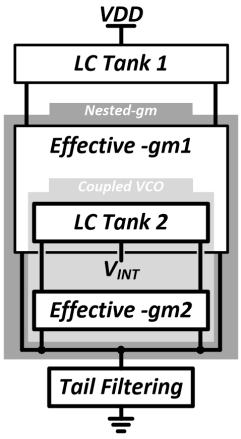


FIGURE 2. Block diagram of the proposed VCO.

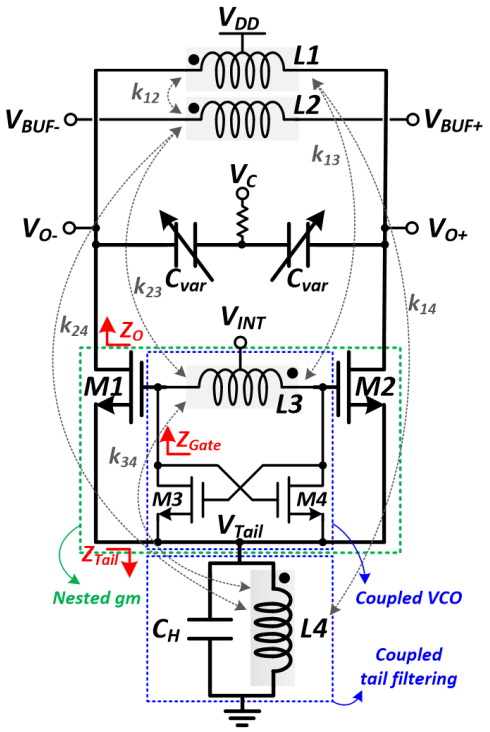


FIGURE 3. Schematic of the proposed class-B/C nested-gm VCO with coupled tail filtering.

M3 and M4 are cross-coupled, and the parasitic capacitors of M1–4 and L3 are employed as secondary LC tanks in the coupled VCO. The oscillation signal is sent back to L1 via L3, and the resonance signal is generated due to the negative *gm* of M3 and M4. In L3, M1 and M2 amplify the output signal swing; therefore, the proposed design can reduce the VCO phase noise. Second harmonic tail filtering is implemented as C_H and L4 and as a transformer coupled to the other inductors with a low k. The control voltage (V_C) determines the capacitance of C_{var} so that the VCO oscillation frequency can be adjusted. L2 is used to transfer the VCO output signal to the buffer for measurement. L2 is also implemented as a

transformer so that the input impedance of the buffer does not affect the VCO core.

The sinewave has harmonic properties. The phase noise of the VCO is reduced by eliminating the second harmonic, which is an even number that affects signal interference. The differential fundamental signals ($f_{O+/-}$) of the VCO are mixed at the source of the VCO core MOSFET, resulting in a second harmonic signal ($2f_O$). The LC tail filter is configured on this node to filter out $2f_O$. However, the secondary harmonic frequency also shifts because the VCO outputs a frequency that changes according to the input voltage. Previous studies have solved this by externally adjusting C_H or the LC tank in the tail filtering unit with a switch to suppress $2f_O$ and thus meet the target frequency. The proposed VCO employs L4 as a transformer and designs the impedance (Z_{Tail}) of the tail filtering node to exhibit a wide-band characteristic. When two inductors with different resonant frequencies are grouped into low k transformers, they exhibit wideband impedance characteristics [12]. Fig. 4(a) presents the simulation results for the impedance viewed from each node. In the circuit for the proposed VCO, Z_O and Z_{Gate} have high impedance at f_O, while Z_{Tail} exhibits resonant characteristics at f_O and $2f_O$. Fig. 4(b) displays the transient simulation results for the proposed VCO. V_{Tail} oscillates to $2f_O$ with a common-mode voltage close to zero due to tail filtering. The resistance of L4 encounters a high current and has a common-mode voltage greater than zero. As a result, the amplitude of the proposed output signal from the VCO increases while V_{Tail} has a voltage lower than zero. Fig. 4(c) presents the ISF, g_{ds}, g_m, and g_m/g_{ds} transient simulation results for the primary VCO and the coupled VCO.

Fig. 5 shows the layout of the proposed nested-*gm* VCO. According to the circuit diagram in Fig. 3, the primary inductor L1 is configured with the highest and thickest metal layer M9 to obtain a high Q [35]. The L2 and L3 inductors are composed of metals M8 and M7, respectively, to maintain a high k. L4 is located far from the core inductors to obtain a low k. Table 1 presents the results of the proposed VCO parameters obtained from the simulation. L1, L2, L3, and L4 obtain 124.2, 197.0, 167.3, and 139.2 pH, respectively, while Q1, Q2, Q3, and Q4 are 25, 9, 12, and 2, respectively. A coupling factor of around 0.8 is obtained from L1, L2, and L3, which are near the center, while a value of about 0.25 is observed from L4, which is far from the center. The transformers use high-layer metals M7–9, and C_{var} is located close to the core MOSFETs of M1–4.

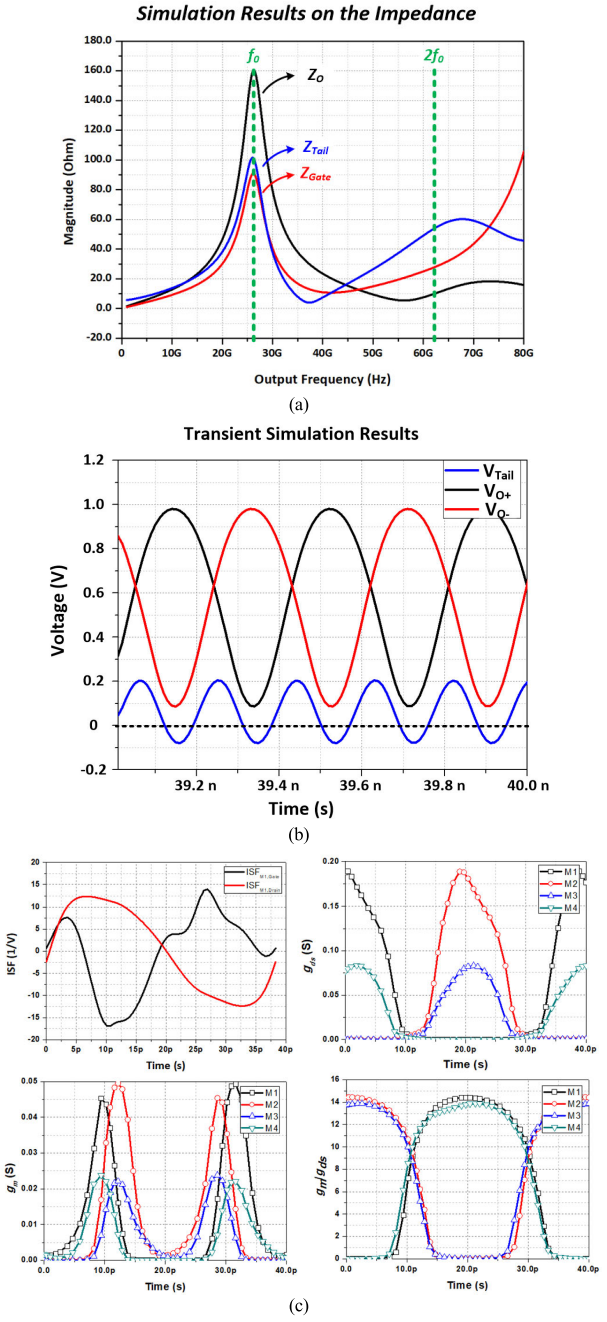


FIGURE 4. Simulation results for (a) the impedance of the proposed VCO, (b) the transient voltage, and (c) the ISF, g_{ds}, g_m and g_m/g_{ds}.

III. MEASUREMENT RESULTS

Fig. 6 presents die micrographs of the proposed nested-*gm* VCO with coupled tail filtering fabricated using a 65 nm CMOS process. The proposed VCO core occupies an area of 0.06 mm^2. The measurement equipment measures the phase noise and spectrum of the proposed VCO with a signal source analyzer and a PXA signal analyzer. A transformer and a buffer amplifier are configured in the VCO core according to the specifications of the measurement equipment, and an on-chip current mode logic frequency divider is configured to output a frequency that is eight times lower than VCO outputs.

Fig. 7 presents the measurement results for the phase noise of the proposed nested-*gm* VCO. Specifically, Fig. 7(a) displays the measurement results for the signal output to an on-chip divider, showing that –123.4 dBc/Hz is obtained at a 1 MHz offset with a 3.64 GHz carrier, while –105.3 dBc/Hz, which is the conversion data, is obtained with a 29.12 GHz carrier. Fig. 7(b) and (c) present the measurement and

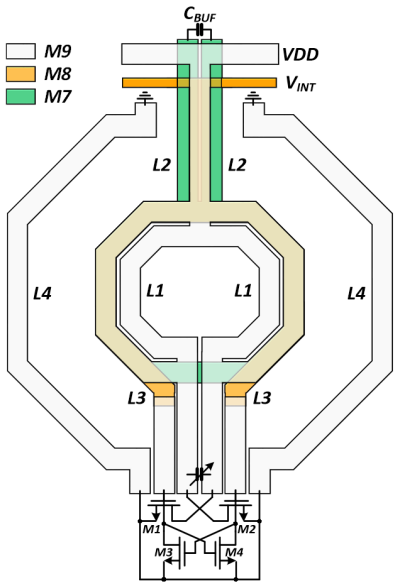


FIGURE 5. Layout of the proposed nested-gm VCO with coupled tail filtering.

TABLE 1. Proposed VCO parameters.

Parameter	Value	Parameter	Value
L1	124.2 pH	k_{12}	0.87
L2	197.0 pH	k_{13}	0.83
L3	167.3 pH	k_{14}	0.28
L4	139.2 pH	k_{23}	0.78
Q1	25	k_{24}	0.21
Q2	9	k_{34}	0.25
Q3	12	-	-
Q4	2	-	-

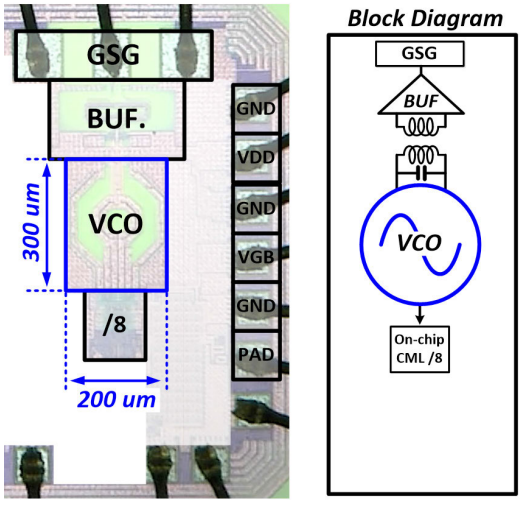
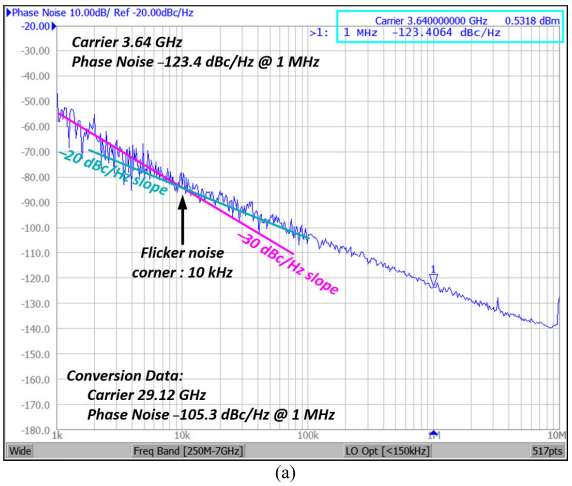
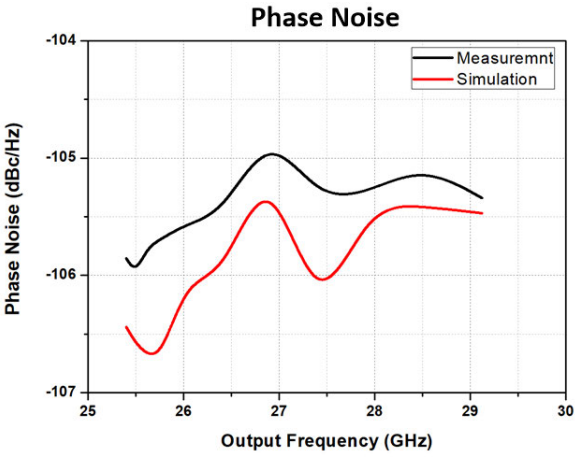


FIGURE 6. Die micrographs and die block diagram.

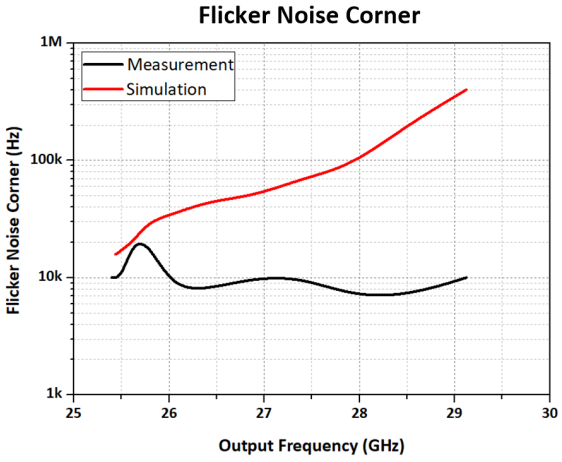
simulation results for the phase noise and the flicker noise corner, respectively. In a non-ideal environment, unexpected



(a)



(b)



(c)

FIGURE 7. Phase noise results for the proposed VCO (a) at a carrier frequency of 3.64 GHz, (b) simulation and measurement data, and (c) flicker phase noise corner.

RLC between the printed circuit board (PCB) and chip and process-voltage-temperature (PVT) variation reduces the phase noise performance by less than 1 dBc/Hz. Furthermore, an unexpected parasitic effect in the electromagnetic (EM) and corner simulations in the VCO circuit impacts all the

TABLE 2. Performance summary and comparison table.

References	Unit	This work	TICAS-II [13]	TMTT [35]	VLSI [42]	JSSC [53]	JSSC [54]
Year	-	**2024**	2022	2023	2023	2024	2024
Technology	-	**65 nm CMOS**	65 nm CMOS	90 nm SiGe BiCMOS	65 nm CMOS	65 nm CMOS	65 nm CMOS
Topology	-	**Nested-*gm*, Coupled tail filtering**	Coupled tail filtering	Tail filtering	*gm*-boosting	Class-F	Dual core coupled VCO
Supply Voltage	V	**1**	1	1.8	1	0.6	0.54
Output Frequency	GHz	**25.4–29.12**	4.2–4.6	27.9–28.8	19.43–20.62	12.3–15.2	11.5–14.3
Cap-Bank Bit-Width	bit	**0**	2	4	2	6	-
K_{VCO}	GHz/V	**3.72**	0.06	0.28^	0.6	0.072	0.06
Power	mW	**16.8**	7.4	24.7	23.6	9.6	5.6
Area	mm^2	**0.06**	0.52	0.09	-	0.06	0.065
Phase Noise @ 1MHz	dBc/Hz	**–105.34**	–126.3	–109.5	–102.05	–118	–119.2
FoM	dB	**–182.37**	–190.5	–185.2	–174.35	–180	–192.8
FoM_A	dB	**–194.96**	–193.34	–195.65	-	–192.2	–204.6
FoM_{KVCO}	dB	**–192.66**	–166.06	–174.07	–169.91	–157.14	–168.36

^Estimated K_{VCO} for the frequency range overlaps by 50%

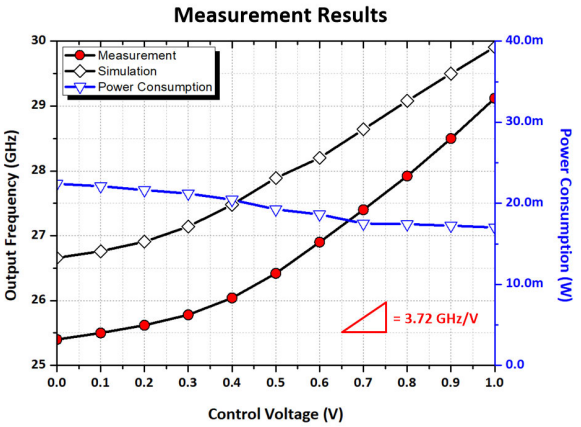


FIGURE 8. Measurement results for the power consumption and output frequency.

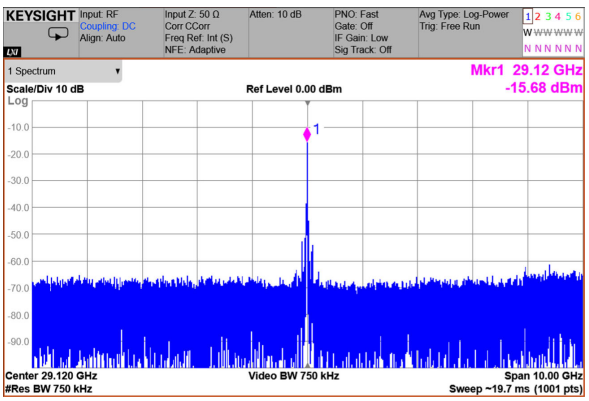


FIGURE 9. Measurement results for the power spectrum.

factors of the Lesson equation. In addition, depending on the output frequency range and voltage bias condition of VCO,

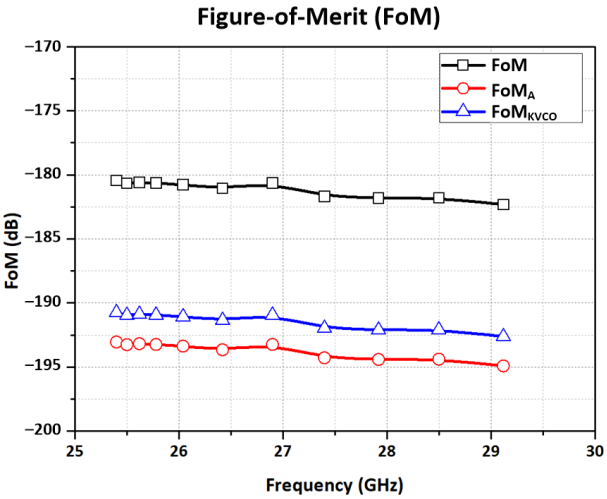


FIGURE 10. FoMs calculated using the measured data.

the measurement results of the phase noise and the flicker noise corner differ from the simulation.

Fig. 8 presents the measured power consumption and output frequency of the proposed VCO. The value of C_{var} decreases as V_C increases, and consequently the power consumption decreases. The VCO output frequency according to the input voltage V_C is 25.40–29.12 GHz, and K_{VCO} is 3.72 GHz/V. At the highest output frequency of 29.12 GHz, 16.8 mW of power is consumed, and the supply voltage is 1 V. The output frequency of the proposed VCO is about 1 GHz lower even though EM data, PVT variation, and parasitic capacitance are considered in the simulation. Fig. 9 presents the output spectrum measurement results, with –15.68 dBm obtained at 29.12 GHz.

Fig. 10 presents the FoMs for the proposed VCO based on the measurement results. The equations for the FoM, FoM_A

and FoM_{KVCO} are as follows:

$$FoM = \mathcal{L}(\Delta f) - 20log(\frac{f_{out}}{\Delta f}) + 10log(\frac{P_{DC}}{mW}), \quad (1)$$

$$FoM_A = FoM - 10log(\frac{Area}{mm^2}), \quad (2)$$

$$FoM_{KVCO} = FoM - 20log(K_{VCO} \cdot \frac{V}{GHz}) \quad (3)$$

In equations (1), (2), and (3), Δf is the offset frequency $\mathcal{L}(\Delta f)$ is the phase noise, f_{OUT} is the output frequency, P_{DC} is the power consumption, and K_{VCO} is the gain of VCO. Table 2 presents a performance summary and comparison with state-of-the-art LC VCOs.

IV. CONCLUSION

The class-B/C VCO proposed in this article demonstrates low phase noise, a high K_{VCO}, and a small area due to its use of a nested-*gm* topology and coupled tail filtering. The proposed VCO is fabricated using a 65-nm RF CMOS process. This VCO adds two cross-coupled NMOSs to produce a structure where the coupled VCO and *gm* overlap to increase the signal amplitude. The phase noise is reduced by removing the secondary harmonic via LC tail filtering. This L is composed of a transformer to reduce the chip area. It has a large impedance in a wide frequency band due to the coupling of different frequencies. By reducing the gate voltage of the core MOSFET, the proposed VCO improves the FoM through the class-C operation. The proposed nested-gm VCO has an output frequency of 25.40–29.12 GHz and a K_{VCO} of 3.72 GHz/V without a capacitor bank. The supply voltage is 1 V, the power consumption is 16.8 mW, and the area is 0.06 mm^2. The FoM according to power, area, and K_{VCO} is –182.37, –194.96, and –192.66 dB, respectively.

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