IEEE Access
Multidisciplinary ⋮ Rapid Review ⋮ Open Access Journal

Received 20 March 2024, accepted 12 April 2024, date of publication 18 April 2024, date of current version 26 April 2024.

Digital Object Identifier 10.1109/ACCESS.2024.3391027

RESEARCH ARTICLE

Performance Investigation of Source Extension Approach on III–V Vertical Tunnel FET

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ABSTRACT A triple-metal-gate stacked III–V vertical tunnel field-effect transistor (TM-GS-VTFET) structure is examined. There are two different TM-GS-VTFETs: Device-A, which uses a source pocket, and Device-B, which uses a new source extension approach. Source pocket-engaged TFETs are recognized for their enhanced ON-state current (I_{ON}) and subthreshold swing compared to traditional TFETs. However, they may require more complex fabrication procedures. The source extension strategy alters the electric-field distribution and decreases the tunneling barrier width near the source side. This boosts the tunneling rate and increases the device functioning. The simulation was performed using the Silvaco Technology Computer-Aided Design (TCAD) tool. Various analog and radio-frequency (RF) parameters were examined. The I_{ON} in Device-B was found to be 234.03 μA/μm, the OFF-state current (I_{OFF}) was 1.52 $\times$ 10^{-14}A/μm, Sub-threshold swing (SS) was 28.58 mV/decade, and the transconductance (gm) was 245.28 μS/μm. The RF frequency parameter such as cutoff frequency (f_T), oscillating frequency (f_{max}), and Gain Bandwidth Product (GBP) were 152.45 GHz, 830 GHz and 25.16 GHz respectively. It was observed that Device-B exhibited 11 times higher I_{ON}, 3.2 times higher GBP, and 3.15 times higher fmax than Device-A. The utilization of this source extension technique has proven to be advantageous for achieving enhanced analog and RF properties in TFETs.

INDEX TERMS TFET, stacked gate, source extension, source pocket, tunneling, GaSb, InP.

I. INTRODUCTION

The Complementary metal-oxide-semiconductor (CMOS) technology used to construct most current electronic devices has come a long way in the last four decades. CMOS technology has proven to be a valuable tool for implementing ideas owing to its reliability, low cost, and low energy consumption. However, the boundaries imposed by the laws of physics have been exceeded, leading to unfavorable performance in devices operating at the nanoscale [1]. When the dimensions of metal-oxide-semiconductor field-effect transistor (MOSFET) devices are scaled down, an increase in leakage or off-state current is observed due to Drain-Induced Barrier Lowering (DIBL) and other short-channel effects [2]. The MOSFET subthreshold slope is greater than 60 mV/decade even at room temperature. Consequently, researchers are actively seeking the next digital paradigm shift. Most portable electronic equipment can be adjusted to meet consumer requirements with only a handful of technological outliers, making them inefficient in terms of space, time, and resource utilization. MOSFETs are frequently employed in both digital and analog configurations. The short-channel effect becomes readily apparent if the MOSFET device is shrunk to a size of less than a nanometer [3]. The short-channel effect leads to many issues such as decreased device performance, increased leakage current, punch-through, and drain-induced barrier lowering (DIBL) [4]. The fabrication procedure for a TFET is similar to that for a conventional CMOS device [11]. TFET offer a more favorable alternative to MOSFET to address these issues.

TFETs are preferable to MOSFETs because of their higher I_{ON}/I_{OFF} ratios [6]. According to these findings, the I_{ON}/I_{OFF} ratio of the TFET can be improved by operating it at lower voltages. TFETs use band-to-band tunneling (BTBT) as the mechanism for injecting carriers, which can result in a sub-threshold swing (SS) value at ambient temperatures steeper

The associate editor coordinating the review of this manuscript and approving it for publication was Huamin Li.

than 60mV/decade [7]. As the operating speed of the device increased, the impact of short-channel effects decreased, the SS value was less than 60 mV/decade, the on/off current ratio increased, and the reduction in leakage current enabled the feasibility of low-power applications.

In source pocket-based TFET, the tunneling barrier is modulated by introducing a strongly doped source pocket close to the source [9]. This can increase the tunneling probability and enhance device performance. Source pocket-involved Tunnel FETs are recognized for their enhanced ON-state current and subthreshold swing compared with traditional Tunnel FETs [10]. However, these methods require complex procedures. Source extension-based TFETs extend the source region beyond the gate edge to alter the electric field distribution and decrease the tunneling barrier width near the source side [11]. This boosts the pace of tunneling and promotes device function [12]. Tunnel FETs based on source extension are recognized for their straightforward fabrication and ability to enhance the ON-state current and subthreshold swing [13].

Section II briefly describes the TM-GS-VTFET structural models obtained by varying the channel and drain lengths and the energy band profiles. In Chapter III, analog device parameters such as drain current (I_{ON}), transconductance (g_m), Transconductance Generation Factor (TGF), surface potential (Ψ), electric field (E), and tunnel path characteristics are analyzed. Chapter IV discusses radio frequency (RF) parameters, such as Gate-to-Drain Capacitance (C_{GD}), Gate-to-Source Capacitance (C_{GS}), cut-off frequency (f_T), gain bandwidth product (GBP), Frequency of Oscillation (f_{max}), and Intrinsic Gate Delay (τ_{int}). The Dynamic Power Dissipation (P_{dyn}) transit time (τ) is followed by a conclusion.

II. DEVICE STRUCTURE

A Cross-sectional schematic of the TM-GS-VTFET with a GaSb source pocket (Device-A) and the TM-GS-VTFET with source extension (Device-B) is shown in Figure 1. The length and thickness of the device were 65 and 30 nm, respectively. The parameters used in the TM-GS-VTFET are listed in Table 1, and the properties of GaSb and InP used in the simulation are listed in Table 2.

TABLE 1. Device parameters.

Parameters	Value
Source (N_A) P+ type	1×10^{20} cm^{-3}
Drain (N_D) N+ type	5×10^{18} cm^{-3}
Channel (N_A) P type	1×10^{16} cm^{-3}
Channel thickness	10 nm
Dielectric thickness	1 nm
Gate M1 work function	4.2 eV
Gate M2 work function	4.6 eV
Gate M3 work function	4.2 eV

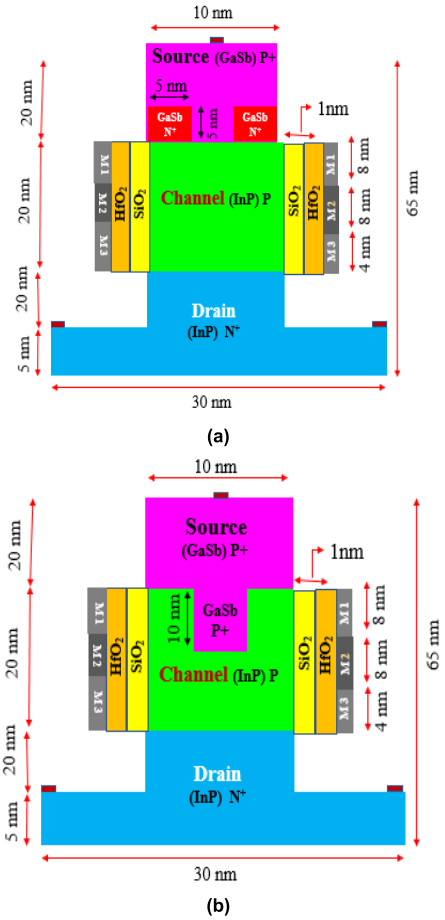

FIGURE 1. Cross-sectional schematic of (a) TM-GS-VTFET with source pocket (Device-A), (b) TM-GS-VTFET with Source Extension (Device-B).

TABLE 2. Material properties.

Parameters	GaSb	InP
Energy band-gap (eV)	0.726	1.34
Dielectric constant	15.69	12.5
Hole mobility (cm2/V-s)	1000	200
Electron mobility (cm2/V-s)	3000	5400
Electron affinity (eV)	4.06	4.38
Effective Electron Mass	0.041mo	0.08mo
Effective Hole Mass	0.4mo	0.6mo

An energy-band diagram illustrates the interplay between the energy levels of the source and drain regions, and the existence of an energy barrier within the channel. When energy levels line up in a manner that allows electric current to flow more easily, a phenomenon known as tunneling effect [13]. The energy-band diagram illustrates the interplay between the energy levels of the source and drain regions and the existence of an energy barrier within the channel [14]. In addition, this analysis can enhance subthreshold qualities [15]. Changing the material parameters and gate voltage allows the tunneling characteristics to be adjusted [16], [17].

Source-pocket-enabled TFETs also involve modifications to the source region; however, in this case, a "pocket" is introduced within the source region. This pocket was designed to enhance the electric field and facilitate efficient carrier tunneling. Source pocket-enabled TFETs introduce pockets with specific doping characteristics within the source region. The purpose of pocket doping, which generated a useful electric field, was to optimize tunneling. The tunneling mechanism is affected by the pocket in the source region, which enhances the electric field and promotes more effective band-to-band tunneling [18].

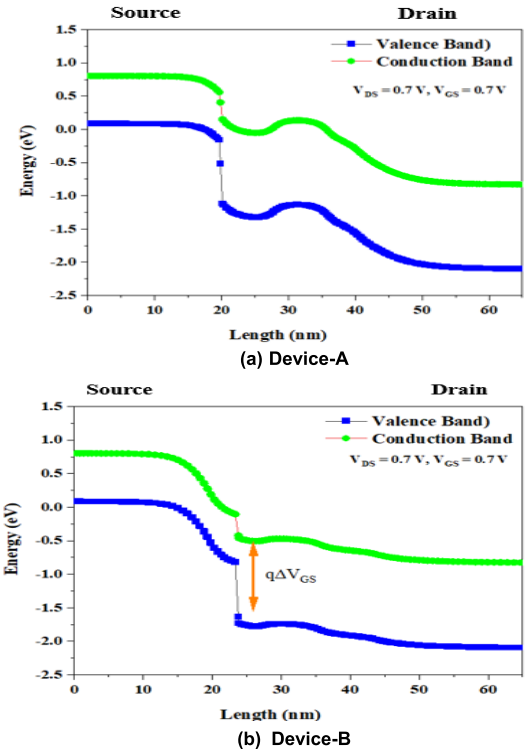

FIGURE 2. Energy band diagram.

In source-extended TFETs, the source region extends physically into the channel. This innovation enhances the overall performance of the device by reducing the travel distance of the carriers to the tunnel, thereby increasing the probability of tunneling. The source extension method mainly involves optimizing doping profiles. This approach ensures a seamless link between source and channel domains. The overall device performance can be improved by reducing the tunneling distance and increasing tunneling probability.

The inclusion of a GaSb pocket source layer in Device-A results in the incorporation of an extra energy barrier for electrons at the junction between the source and channel, Due to this GaSb pocket source, an energy barrier facilitates the selective filtration of electrons with energies near the uppermost region of the valence band. as shown in Figure-2. Such energy levels cause electrons to transition into the channel material InP's conduction band with a greater bend. Hence enhancing the operational efficiency of TFET, the Fermi level of the GaSb pocket source can be altered by varying the V_{GS}. In Device-B, the GaSb source extension creates an additional energy barrier at the source-channel junction. This barrier facilitates the sorting of electrons based on their respective energy levels illustrated in the energy band diagram. In GaSb, electrons with energies near the top of the valence band have a better chance of breaking through the barrier and entering the conduction band of the InP channel. This phenomenon boosts the TFET's ON-current by allowing electrons with greater energies to pass through the barrier more easily. Higher energy electrons are more likely to be chosen due to the energy filtering effect, and only those with sufficient energy can tunnel and contribute to the device's current. This results in a reduction of the leakage current [19]. When the ON-current increases, the TFET can better switch other circuit components since it can handle a more significant drive current. The subthreshold swing (SS) can potentially be reduced by extending the GaSb source. The SS metric assesses a TFET performance transitioning between its ON and OFF states [20]. Reduced power consumption and increased efficiency are attributed to the smaller SS, which necessitates a lower gate voltage and facilitates faster device activation.

III. RESULTS AND DISCUSSION-ANALOG PARAMETER

A. ON-STATE CURRENT (I_{ON})

The electrical conductivity of a device depends on its I_{ON}. A direct correlation exists between the I_{ON} and transconductance of the device (g_m). Increasing the g_m improves amplification and analog quantities [21].

$$I_D \propto \exp\left[-\frac{4\sqrt{2\,\mathrm{m}^*}E_g^{*\frac{3}{2}}}{3|e|\hbar\left(E_g^* + \Delta\Phi\right)}\sqrt{\frac{\varepsilon_{Si}}{\varepsilon_{ox}}t_{ox}t_{Si}}\right]\Delta\Phi \qquad (1)$$

where $\Delta\Phi$ -Tunneling window, m$*$ is the effective mass, q is the charge of an electron, $\hbar$ - Reduced Plank's constant, E_g^* - Effective bandgap, λ is the tunneling width, and t_{si}, t_{ox}, ε_{si} and ε_{ox} are the thickness and permittivity of silicon and oxide, respectively.

The I_{ON} for Device-A and Device-B were 26.82 μA and 26.82 μA respectively as shown in Figure 3. Device-B demonstrated superior performance because of the source extension technique, which reduced the tunneling distance and enhanced the concentration and velocity of the electrons in the J_{SC} region. Applying a positive V_{GS} causes the Fermi level in the source region to move downwards. Consequently, the convergence of the source and the channel generates a powerful electric field. The electric field induces a modification in the energy bands of InP, which serves as the channel material. The conduction band edge of InP is in alignment with or near the valence band edge of the GaSb source. This configuration facilitates the movement of electrons from the source to the channel by creating an energy barrier. When the energy level of the GaSb source reaches a sufficient magnitude, the electrons undergo quantum mechanical tunneling to enter the InP channel. The InP channel enables efficient electron conduction towards the drain as a result of the drain voltage (V_{DS}). The application of the source extension approach resulted in improved energy-filtering operations,

during decrease in SS, which in turn enhanced Device-B's current.

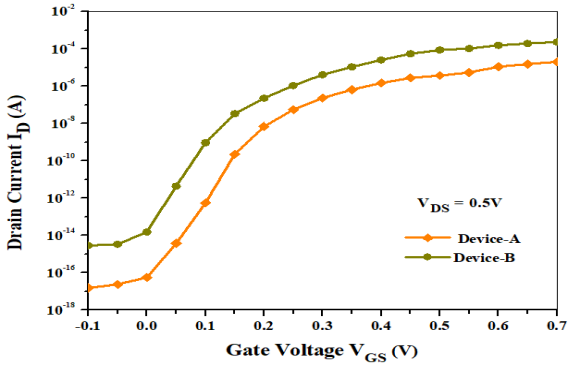

FIGURE 3. Transfer characteristics.

The I_{OFF} values for Device-A and Device-B were 5.6×10^{-17}A/μm and $1{,}52 \times 10^{-14}$A/μm. The source pocket in Device-A plays an important role in I_{OFF} reduction. The source pocket can affect SS by influencing the tunneling characteristics and carrier injection into the channel. The SS of Device-A and Device-B were 24.56 mv/decade and 28.58 mV/decade respectively.

B. TRANSCONDUCTANCE (g_m)

Evaluation of the performance of a TFET is often based on its transconductance, which quantifies its ability to convert changes in voltage into corresponding changes in current [22]. The primary application of this device is to quantify the level of amplification gain. The mathematical expression is as follows:

$$g_m = \frac{\partial I_D}{\partial V_{GS}} \tag{2}$$

The tunneling process and g_m can be improved through meticulous design of the tunneling barrier and selection of appropriate source/channel materials. Furthermore, manipulation of the gate structure has the potential to affect the tunneling process, thereby influencing the transconductance.

Figure 4 illustrates the g_m for Device-A and Device-B were 86.74 μS/μm and 245.28 μS/μm respectively. Due to Source channel materials such as GaSb and InP, source extension and drain extension in Device-B, improved transconductance was achieved. A device exhibiting a higher transconductance characteristic is capable of establishing a channel with enhanced transfer efficiency, rendering it highly suitable for utilization in analogue applications.

C. TRANSCONDUCTANCE GENERATION FACTOR (TGF)

TGF provides further insights into TFETs' ability of TFETs to withstand subthreshold dips that are far steeper than those achievable with ordinary MOSFETs, which is a major benefit. A higher TGF value indicates a more effective conversion of gate-source voltage changes into I_{ON} changes, reflecting a more responsive and efficient transistor. In the proposed method, source extension can affect the tunneling probability,

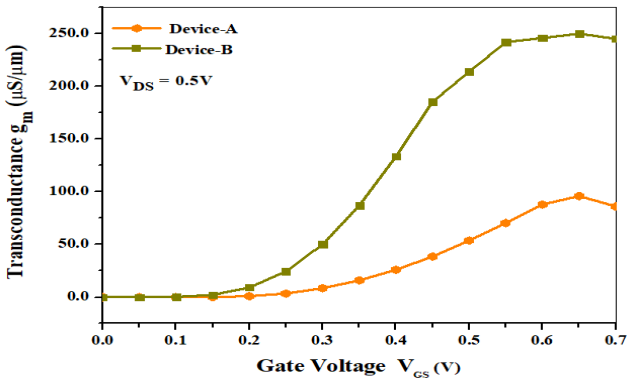

FIGURE 4. Transconductance.

carrier injection, and overall device performance. By influencing these factors, the source extension contributes to the TGF of the device as illustrated in Transconductance Generation Factor Figure 5.

The mathematical expression is given as;

$$TGF = \frac{g_m}{I_D} \tag{3}$$

Device-A contains two highly doped GaSb source pockets positioned in proximity to the top and bottom gate terminals. The source pockets are engineered to provide a concentrated supply of charge carriers, they offer improved TGF between 0.1 and 0.35 volts. A more precise and manageable activation state may be available from source pockets. Device-B incorporates the source extension within the width range of 13 nm to 17 nm. Because of this, source extensions can cause the sub-threshold slope to be steeper and the enhancement of TGF after 0.3 V.

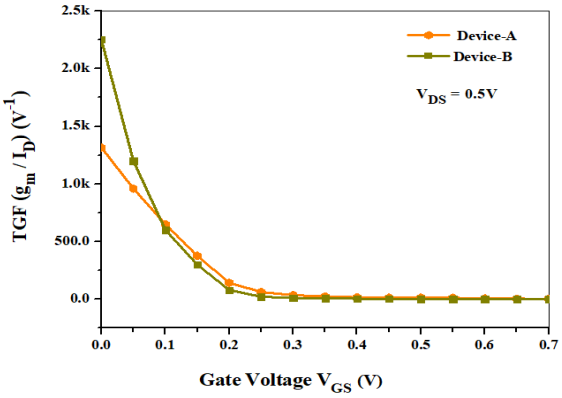

FIGURE 5. Transconductance generation factor (TGF).

D. SURFACE POTENTIAL (Ψ)

The management of energy-band alignment is governed by the surface potential at the interface between GaSb and InP. Band alignment must be carefully constructed for the valence band of the channel material (InP) to align properly with the conduction band of the source material (GaSb). This phenomenon facilitates efficient electron tunneling. Variations in the surface potential influence the height of the energy barrier between the source and channel.

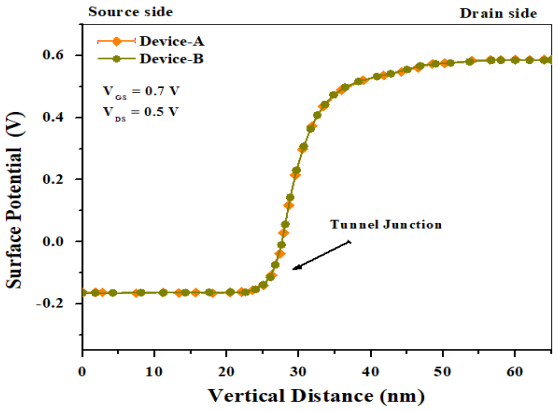

FIGURE 6. Surface potential.

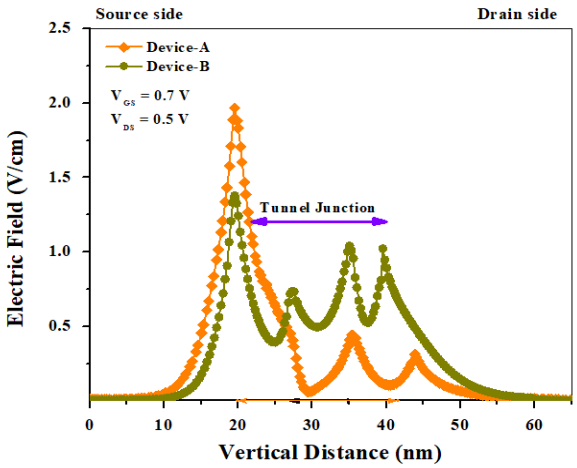

FIGURE 7. Electric field.

Figure 6 shows that an increase in the energy barrier can alter the tunneling rate owing to an increase in surface potential. Reducing the energy barrier height, which facilitates electron flow, is a fundamental way to increase the TFET performance. Optimizing the on/off current ratio, reducing ambipolar conduction, and increasing the subthreshold swing are just a few of the device performance goals that can be achieved by manipulating the surface potential profile. Reduced power consumption is a major benefit of using TFETs because of their ability to efficiently manage steep subthreshold slopes. The surface potential plays a crucial role in achieving a steep subthreshold slope by allowing rapid changes in the current flow in response to fluctuations in gate voltage.

E. ELECTRIC FIELD

Analyzing the electric field distribution in a TFET is essential for providing significant attention to the device structure. A TFET generally consists of three primary parts: source region, tunneling barrier, and drain area. The tunneling barrier in a TFET is of great importance because of its capacity to control the tunneling probability, which affects device characteristics. The electric field generally demonstrates its maximum strength near the contact point between the source and the channel. A tunneling barrier is a physical boundary that separates the source and channel areas, wherein the electric field attains its maximum intensity, and is mostly concentrated inside this specific region. A strong electric field enhances the movement of charge carriers through the barrier. The electric field of a TFET is crucial for enabling tunneling, as shown in Figure 7. The application of a robust electric field across the channel region enhances tunneling probability. This reduces the source voltage required for TFETs to operate, thereby reducing their power requirements and improving their performance at low voltages.

In the tunneling junction spanning the range of 20–40 nm, Device-B exhibited a higher electric field than Device-A.

F. TUNNEL PATH

The energy bands and Fermi levels in a TFET must be precisely managed to facilitate electron transport from the source to channel. This was performed using V_{GS}, which shifts the Fermi levels of the source and channel materials. Controlling the energy bands and Fermi levels of the TFET allows more efficient electron transport from the source to the channel. This was achieved by applying the V_{GS}. Therefore, the Fermi levels in the source and channel materials shifted to different positions. The application of a positive V_{GS} resulted in a downward shift of the Fermi level within the source region. Consequently, this establishes a pronounced electric field at the junction between the source and the channel. This electric field altered the energy bands of the InP channel material.

The conduction band edge in InP exhibits proximity to or alignment with the valence band edge of the GaSb source. Because of this configuration, the energy barrier facilitates the movement of electrons from the source towards the channel. Electrons in the GaSb source quantum-mechanically tunnel into the InP channel when they possess sufficient energy to cross the energy barrier. Once the electrons are in the InP channel, the drain voltage (V_{DD}) enables them to flow effortlessly into the drain.

Figure 8 illustrates the features of the tunneling process in Device-A and Device-B considering the influence of the BTBT (band-to-band tunneling) electron and hole tunneling mechanisms. The diagram includes information on the electron concentration and total current density. The results indicate that compared to the other devices, Device-B shows dominance and better tunneling characteristics.

IV. RESULTS AND DISCUSSION-RF PARAMETER

A. GATE-TO-DRAIN CAPACITANCE (C_{GD}) AND GATE-TO-SOURCE CAPACITANCE (C_{GS})

The gate-to-source (C_{GS}) and gate-to-drain (C_{GD}) capacitances of TFET devices behave differently depending on V_{GS} when compared to standard thermionic MOSFETs. C_{GD} in TFETs is primarily used to display the overall gate capacitance. In the active state of the transistor, the capacitance between the gate and source exhibits a significantly reduced value owing to the reliance of the TFET current on the diminishing barrier at the source-channel junction. Figure 9 shows the capacitance of the proposed device.

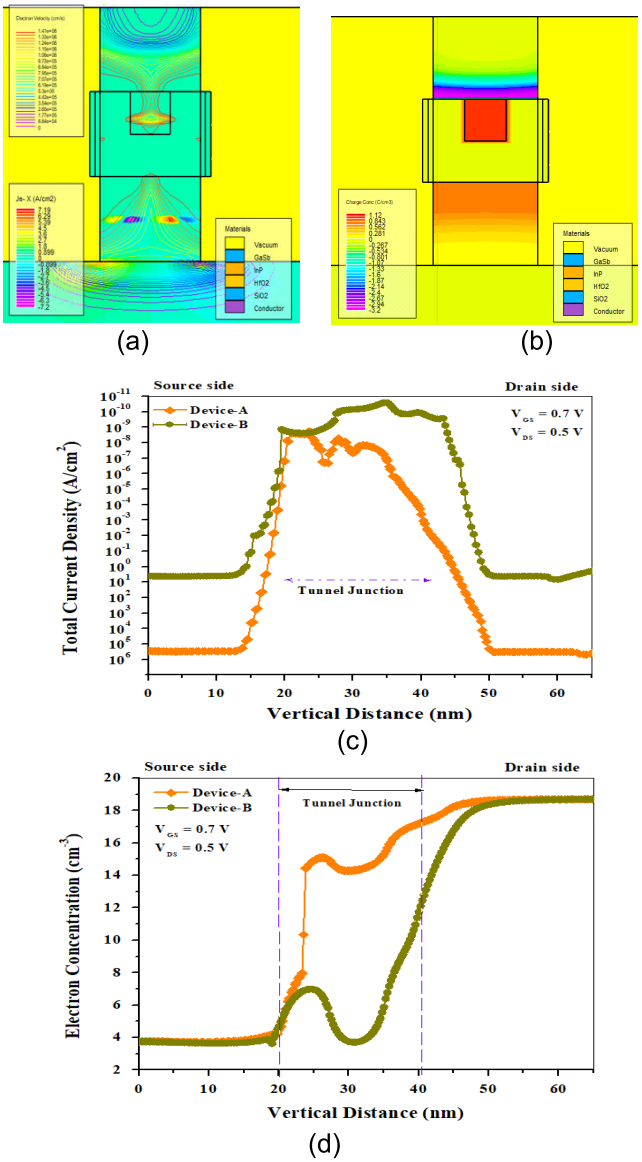

FIGURE 8. (a) e-Velocity, (b) Charge concentration, (c) Electron concentration and (d) Total current density.

B. CUT-OFF FREQUENCY (f_T)

The cutoff frequency (f_T) of a TFET is influenced by various factors, including device geometry, material properties, and operational parameters. The f_T of the TFET can be increased through meticulous design of the bandgap of the device. Most TFETs are fabricated using materials characterized by narrow bandgaps, such as III-V compounds. The doping patterns within the TFET structure also have an impact on f_T. The composition and concentration of dopants in the source, channel, and drain regions have a significant impact on the tunneling mechanism, thus influencing f_T, which is mathematically defined as

$$f_T = \frac{g_m}{2\pi\,(C_{GS} + C_{GD})} \tag{4}$$

Figure 10 shows the f_T for Device-A and Device-B were determined to be 50.34 GHz and 152.45 GHz respectively. Device-B exhibited lower C_{GS} (155 aF) and C_{GD} (134 aF)

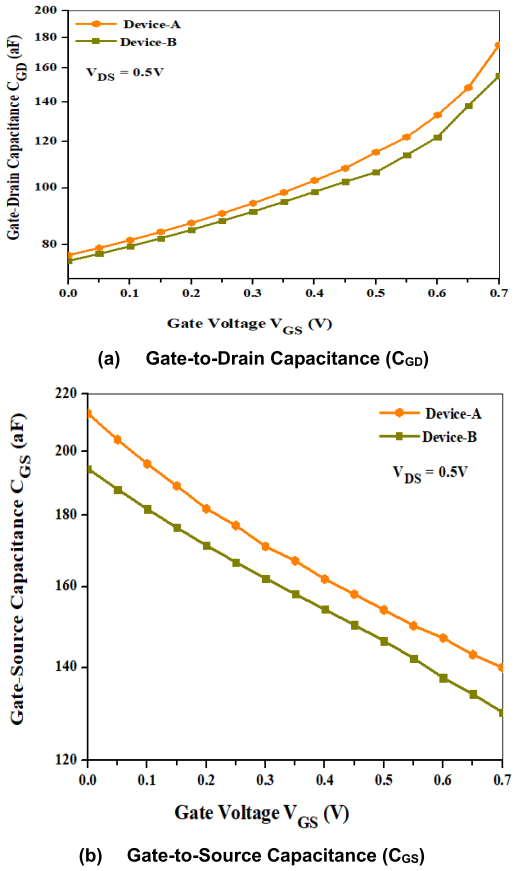

FIGURE 9. Proposed device capacitance (a) & (b).

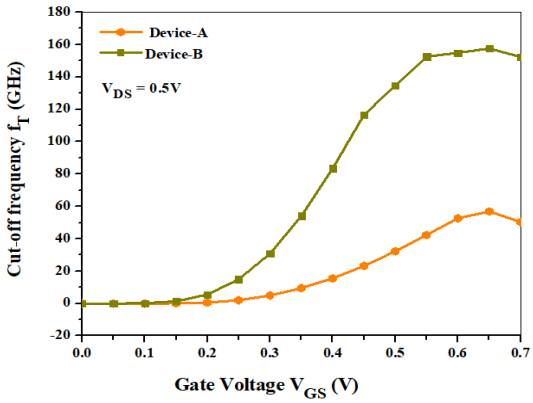

FIGURE 10. Cut-off frequency.

values than Device-A. Furthermore, the gate-to-source transconductance (g_m) for Device-B was measured to be 245.28 μS/μm. The f_T value of Device-B is greater than that of Device-A.

C. GAIN BAND-WIDTH PRODUCT (GBW)

TFETs that possess a high gain-bandwidth product (GBP) can swiftly switch and respond to input signals. This characteristic renders them suitable for applications that require rapid transition periods, such as pulse shaping and high-speed data transmission. A larger GBP facilitates the amplification of signals at lower power levels, which is advantageous

for low-power or battery-operated devices that prioritize the power efficiency.

$$GBP = \frac{g_m}{10 \times 2\pi C_{GD}} \tag{5}$$

Figure 11 shows that Device-B had a GBP value of 25.16 GHz, whereas Device-A had a GBP value of 7.82 GHz. Device-B has a GBP that is 3.2 times more than that of Device-A. Consideration of GBP is essential when examining high-frequency transients. The GBP device exhibited an optimal performance in applications requiring high-speed operation and low-bias conditions. A significant level of importance was attributed to the high GBP in circuit applications such as RF amplifiers, which necessitates rapid speed and minimal input bias current.

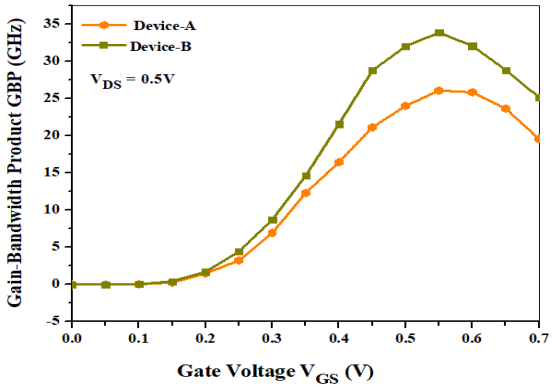

FIGURE 11. Gain bandwidth product.

D. MAXIMUM OSCILLATION FREQUENCY (f_{max})

Examining the maximum oscillation frequency (f_{max}) is an important part of understanding how TFETs work because it shows the highest frequency at which these devices can work as oscillators or amplifiers. Because of its direct relationship with the speed and general performance of TFET, fmax is crucial for high-frequency applications. The fmax value of the TFET is proportional to its switching speed.

The frequency at which power gain equals one is known as the f_{max}.

$$f_{max} = \frac{g_m}{2\pi C_{gs}\sqrt{4\left(g_{ds} + g_m \frac{C_{gd}}{C_{gs}}\right)(R_s + R_{ch} + R_g)}} \tag{6}$$

$$f_{max} = \frac{f_T}{\sqrt{8\pi C_{gd} R_{gd}}} \tag{7}$$

$C_{gs\ and}$ C_{gd}- Gate-to-source and Gate-to-drain capacitances, respectively; g_{ds} - output conductance; and R_s, R_{ch} and R_g are the source, channel, and gate resistances, respectively.

Figure 12 shows that f_{max} for Device-B was 830 GHZ, whereas that for Device-A is 264 GHZ. Device-B has 3.15 times higher f_{max} compare with Device-A. The device's ability to perform high-speed digital operations and immediate signal processing is particularly useful in today's electronics, because it facilitates faster switching. TFETs with larger fmax values allow for faster data transmission and reception. These devices can facilitate wireless communication and high-velocity data transfers. Devices with high f_{max} values are required in the RF circuits for signal generation and amplification. RF front-end components, including low-noise amplifiers, mixers, and frequency synthesizers, can benefit from the use of TFETs with high fmax.

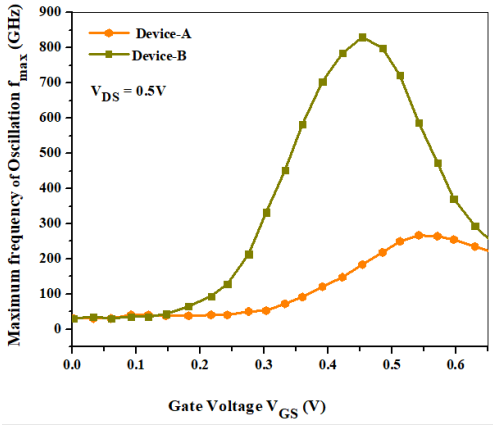

FIGURE 12. Maximum oscillating frequency.

E. INTRINSIC GATE DELAY (τ_{int})

Determining the intrinsic gate delay (τ_{int}) is a reliable method to assess the operational speed of a device. The significance of parasitic gate capacitance (C_{GG}) and I_{ON} should not be underestimated. Changes in I_{ON} had the greatest impact on the intrinsic gate delay. It is given in (8);

$$\tau_{int} = \frac{C_{gg} X V_{DD}}{I_D} \tag{8}$$

Figure 13 shows that τ_{int} of Device-B was 0.388 ps, whereas Device-A was 4.87 ps.

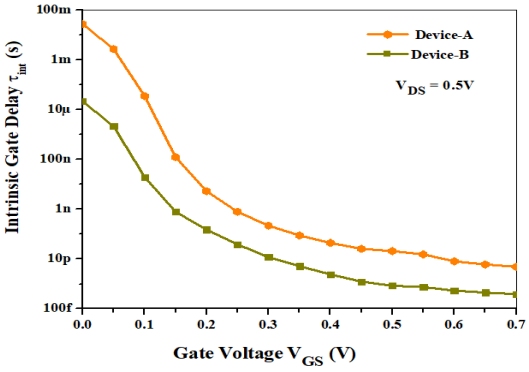

FIGURE 13. Intrinsic gate delay.

F. DYNAMIC POWER DISSIPATION (PDYN)

$$P_{dyn} = C_{gg} V_{DD}^2 f \tag{9}$$

where f represents the operating frequency, and C_{gg} is the total gate capacitance (sum of C_{GD} and C_{GS}). The Figure 14 shows P_{dyn} of Device-A and Device-B were recorded as 0.133 nW and 0.125 nW respectively as shown in Figure 14 dynamic power dissipation. Device-B exhibited a lower

TABLE 3. Performance comparison between TM-GS-VTFET with literature review papers [22], [23], [24], [25].

Ref.	Source Material	Channel Material	Dielectric Material	I_{ON} (μA)	I_{ON} / I_{OFF}	SS (mV/dec)	Channel Length (nm)	g_m μS/μm	Structure
Bijesh et al. (2013)	GaAsSb	InGaAs	$Al_2O_3\backslash HfO_2$	740	-	-	200	700	Vertical
A. Lemtur et al. (2018)	AlGaSb	GaAsP	HfO_2	12.8	10^{12}	19.7	30	96.4	GAA
Hu Liu et al. (2019)	InGaAs	InAlAs	$HfO_2\backslash SiO_2$	16.7	10^{10}	<60	50	69.3	Planar
A. Bhattacharyya et al. (2020)	InAsSb	InAsSb	$HfO_2\backslash SiO_2$	40.5	10^{9}	20.3	20	300	Planar
In this work (Device-A)	GaSb	InP	$HfO_2\backslash SiO_2$	20.14	10^{11}	24.56	20	86.74	Vertical
In this work (Device-B)	GaSb	InP	$HfO_2\backslash SiO_2$	234.03	10^{10}	28.58	20	245.2	Vertical

dynamic power consumption. Reducing the dynamic power consumption of the device is extremely important to avoid an excessive temperature rise and subsequent performance decline.

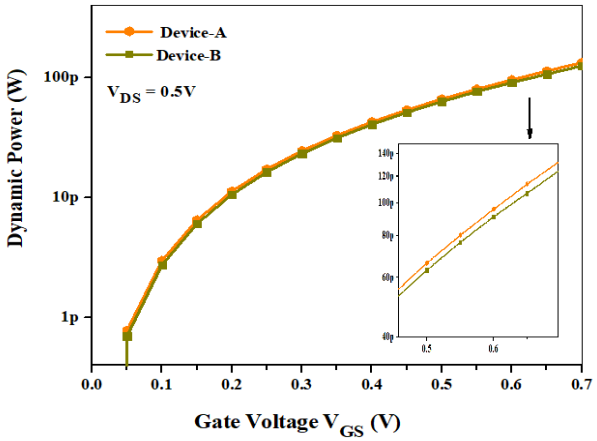

FIGURE 14. Dynamic power dissipation.

G. TRANSIT TIME (τ)

The subthreshold slope of a TFET is directly related to its transit time (τ). The TFET was designed to have a subthreshold drop that is significantly steeper than that of a normal MOSFET. When the tunneling time was short, the subthreshold slopes were high. This allows the TFET to quickly change from ON to OFF. For high-speed performance, the tunneling time should be short. The expression for τ is

$$\tau = \frac{1}{2\pi f_T} \tag{10}$$

The τ values of Device-A and Device-B were 3.16 ps and 1.04 ps respectively. The change over time of Device-B was relatively low, as shown in Figure 15. A TFET with decreased tunneling time has the potential to transition from an active state to an inactive state more rapidly. This attribute makes it particularly appropriate for digital applications that require fast performance. The capacity of the device to transition between states at a faster rate has the potential to improve energy efficiency by reducing the power loss during these transitions, resulting in faster tunneling times.

The performance of the TM-GS-VTFET with Source extension (Device-B) was compared with that of the existing

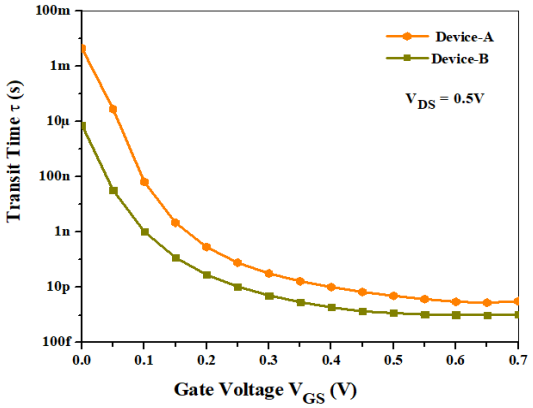

FIGURE 15. Transit time.

literature review, as presented in Table 3. In their studies, the authors Bijesh et al., and Bhattacharyya et al. have demonstrated increased I_{ON} values.

However, these investigations revealed a large channel length, high SS value, and noticeably low I_{ON}/I_{OFF} ratio. However, regarding the I_{ON} and I_{ON}/I_{OFF} ratios, subthreshold swing (SS), moderate transconductance (g_m), and shorter channel length, Device-B performed better.

Both the study conducted by Bhattacharyya et al. and this study employed the same heterogeneous dielectric material HfO_2/SiO_2. Bhattacharyya et al. employed a doping-less charge plasma TFET in their study, whereas our research specifically investigated a vertical TFET. The utilization of the source extension technique in Device-B resulted in an enhanced energy band alignment. The simulation outcomes showed improvements in I_{ON} efficiency as well as in other measured parameters such as transconductance (g_m), subthreshold swing (SS), and the ratio of I_{ON} to I_{OFF} values. These observed values are in close proximity to those reported by Bhattacharyya et al.

V. CONCLUSION

The present study focuses on the analysis of the Triple Metal-Gate Stacked- III-V Vertical Tunnel Field Effect Transistor (TM-GS-VTFET) through a source pocket and source extension approach. The source extension alters the electric field distribution in the device, decreasing the tunneling barrier width close to the source side, and increasing the tunneling

rate. Consequently, this enhances the on-state current and subthreshold swing properties. In the TM-GS-VTFET with source extension approach, the I_{ON} was measured to be 234.03 μA, while the OFF-current (I_{OFF}) was found to be 1.52×10^{-14} A. Additionally, the sub-threshold swing was determined to be 28.58 mV/decade, the g_m value was calculated to be 245.28 μS/μm, and the device exhibited excellent electric field characteristics and an efficient tunnel path. The RF results indicate the cutoff frequency (f_T) at 152.45 GHz. The GBP value was determined to be 25.16 GHz, while the fmax value reached 830 GHz. In addition, the transit time (τ) was found to be 1.04 picoseconds. Applications that demand high-speed operation and improved analog/RF performance are well-suited to TM-GS-VTFETs designed using a source extension method.

REFERENCES

[1] M. Saravanan and E. Parthasarathy, "A review of III-V tunnel field effect transistors for future ultra low power digital/analog applications," *Microelectron. J.*, vol. 114, Aug. 2021, Art. no. 105102.

[2] T. Yu, W. Lü, Z. Zhao, P. Si, and K. Zhang, "Negative drain-induced barrier lowering and negative differential resistance effects in negative-capacitance transistors," *Microelectron. J.*, vol. 108, Feb. 2021, Art. no. 104981.

[3] R. Saha, R. Goswami, and D. K. Panda, "Analysis on electrical parameters including temperature and interface trap charges in gate overlap Ge source step shape double gate TFET," *Microelectron. J.*, vol. 130, Dec. 2022, Art. no. 105629.

[4] P. Raut, U. Nanda, and D. K. Panda, "Analytical drain current model development of twin gate TFET in subthreshold and super threshold regions," *Microelectron. J.*, vol. 135, May 2023, Art. no. 105761.

[5] A. Bhardwaj, P. Kumar, B. Raj, and S. Anand, "Design and performance optimization of dopingless vertical nanowire TFET using gate stacking technique," *J. Electron. Mater.*, vol. 51, no. 7, pp. 4005–4013, Jul. 2022.

[6] K. N. Priyadarshani and S. Singh, "Ultra sensitive label-free detection of biomolecules using vertically extended drain double gate $Si_{0.5}Ge_{0.5}$ source tunnel FET," *IEEE Trans. Nanobiosci.*, vol. 20, no. 4, pp. 480–487, Oct. 2021.

[7] S. A. Ahmad and N. Alam, "Design of a triple pocket multi-gate material TFET structure for low-power applications," *Semicond. Sci. Technol.*, vol. 36, no. 2, Feb. 2021, Art. no. 025015.

[8] T. Ashok and C. K. Pandey, "Demonstration of a novel dual-source elevated-channel dopingless TFET with improved DC and analog/RF performance," *Microelectron. J.*, vol. 144, Feb. 2024, Art. no. 106071.

[9] Y. Shao, M. Pala, D. Esseni, and J. A. del Alamo, "Scaling of GaSb/InAs vertical nanowire Esaki diodes down to sub-10-nm diameter," *IEEE Trans. Electron Devices*, vol. 69, no. 4, pp. 2188–2195, Apr. 2022.

[10] V. Vijayvargiya, B. S. Reniwal, P. Singh, and S. K. Vishvakarma, "Impact of device engineering on analog/RF performances of tunnel field effect transistors," *Semicond. Sci. Technol.*, vol. 32, no. 6, Jun. 2017, Art. no. 065005.

[11] *ATLAS User's Manual*, Silvaco Int., Santa Clara, CA, USA, 2018.

[12] M. Karbalaei, D. Dideban, and H. Heidari, "A simulation study of the influence of a high-k insulator and source stack on the performance of a double-gate tunnel FET," *J. Comput. Electron.*, vol. 19, no. 3, pp. 1077–1084, Sep. 2020.

[13] W. Gonçalez Filho, E. Simoen, R. Rooyackers, C. Claeys, N. Collaert, J. A. Martino, and P. G. D. Agopian, "Analog design with line-TFET device experimental data: From device to circuit level," *Semicond. Sci. Technol.*, vol. 35, no. 5, May 2020, Art. no. 055025.

[14] C. N. Macambira, P. G. D. Agopian, and J. A. Martino, "Evaluation of dielectrically modulated and fringing field tunneling field effect transistor biosensors devices," *ECS J. Solid State Sci. Technol.*, vol. 10, no. 7, Jul. 2021, Art. no. 077001.

[15] K. R. N. Karthik and C. K. Pandey, "Design and investigation of a novel gate-all-around vertical tunnel FET with improved DC and analog/RF parameters," *ECS J. Solid State Sci. Technol.*, vol. 11, no. 11, Nov. 2022, Art. no. 111007.

[16] J. L. Padilla, C. Medina-Bailón, C. Navarro, C. Alper, F. Gamiz, and A. M. Ionescu, "Analysis of the heterogate electron–hole bilayer tunneling field-effect transistor with partially doped channels: Effects on tunneling distance modulation and occupancy probabilities," *IEEE Trans. Electron Devices*, vol. 65, no. 1, pp. 339–346, Jan. 2018.

[17] J. Wu and Y. Taur, "Reduction of TFET OFF-current and subthreshold swing by lightly doped drain," *IEEE Trans. Electron Devices*, vol. 63, no. 8, pp. 3342–3345, Aug. 2016.

[18] P. Sharma, J. Madan, R. Pandey, and R. Sharma, "RF analysis of double-gate junctionless tunnel FET for wireless communication systems: A non-quasi static approach," *J. Electron. Mater.*, vol. 50, no. 1, pp. 138–154, Jan. 2021.

[19] S. Hussain, N. Mustakim, and J. K. Saha, "Linearity performance and distortion analysis of carbon nanotube tunneling FET," *J. Electron. Mater.*, vol. 50, no. 3, pp. 1496–1505, Mar. 2021.

[20] A. B. Tawseef, M. Mustafa, and M. R. Beigh, "Study of short channel effects in n-FinFET structure for Si, GaAs, GaSb and GaN channel materials," *J. Nano-Electron. Phys.*, vol. 7, p. 03010, Jan. 2015.

[21] M. Saravanan and E. Parthasarathy, "Impact of pocket layer on linearity and analog/RF performance of InAs-GaSb vertical tunnel field-effect transistor," *J. Electron. Mater.*, vol. 52, no. 4, pp. 2772–2779, Apr. 2023.

[22] R. Bijesh, H. Liu, H. Madan, D. Mohata, W. Li, N. V. Nguyen, D. Gundlach, C. A. Richter, J. Maier, K. Wang, T. Clarke, J. M. Fastenau, D. Loubychev, W. K. Liu, V. Narayanan, and S. Datta, "Demonstration of $In_{0.9}Ga_{0.1}As/GaAs_{0.18}Sb_{0.82}$ near broken-gap tunnel FET with I_{ON}=740μA/μm, G_M=700μS/μm and gigahertz switching performance at V_{DS}=0.5V," in *IEDM Tech. Dig.*, Dec. 2013, p. 28, doi: 10.1109/IEDM.2013.6724708.

[23] A. Lemtur, D. Sharma, P. Suman, J. Patel, D. S. Yadav, and N. Sharma, "Performance analysis of gate all around GaAsP/AlGaSb CP-TFET," *Superlatt. Microstruct.*, vol. 117, pp. 364–372, May 2018.

[24] H. Liu, L.-A. Yang, Z. Jin, and Y. Hao, "An $In_{0.53}Ga_{0.47}As/In_{0.52}Al_{0.48}As$ heterojunction dopingless tunnel FET with a heterogate dielectric for high performance," *IEEE Trans. Electron Devices*, vol. 66, no. 7, pp. 3229–3235, Jul. 2019.

[25] A. Bhattacharyya, M. Chanda, and D. De, "$GaAs_{0.5}Sb_{0.5}/In_{0.53}Ga_{0.47}As$ heterojunction dopingless charge plasma-based tunnel FET for analog/digital performance improvement," *Superlatt. Microstruct.*, vol. 142, Jun. 2020, Art. no. 106522.

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