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RESEARCH ARTICLE

Theoretical Comparison, Real-Time Emulation, and Experiment Validation of DC/DC Converter for Fuel Cell Electric Vehicle

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ABSTRACT In this study, an Interleaved Boost Converter constructed with six cascade parallel connected phases is proposed for Fuel Cell Electric Vehicle (FCEV). Silicon Carbide (SiC) semiconductors are selected help gain high efficiency, high compactness and better thermal ability. Inverse coupled inductors are used to reduce the volume, weight and core losses of magnetic components. The proposed topology reduces significantly the AC amplitude of fuel cell current and therefore the operating life of the Proton Exchange Membrane Fuel Cell (PEMFC) can be extended. Hardware-in-the-Loop (HIL) real-time emulation of the proposed converter has been addressed. Finally, a 1kW prototype of the proposed converter has been established and experiments have been launched for the validation. Depending on theoretical comparison analysis, HIL real-time verification and experimental validation, the PEMFC system combined with the proposed converter can own high reliability, high system efficiency and high compactness.

INDEX TERMS Fuel cell electric vehicle, proton exchange membrane fuel cell, hardware-in-the-loop real-time emulation, DC/DC converter.

I. INTRODUCTION

As one of the most significant facts affecting our quality of life, it is an urgent need to decrease transportation-related greenhouse gas emissions. New generation of transports, which are based on clean energy, are required to be developed and replace the traditional fossil fuels-based transportations. Technologies based on hydrogen energy are increasingly thought to be the ideal answers to resolve this problem [1]. Fuel cell electric vehicles, or FCEVs, are regarded as a very promising and ecologically beneficial technology to transform the present method of transportation. Some automakers, including Nissan, Toyota, and Hyundai, have already begun to manufacture FCEVs [2].

Proton Exchange Membrane Fuel Cell (PEMFC) is the most suitable type of fuel cell for automotive applications [3]. As a high-current low-voltage power source, PEMFC system's output voltage must be increased to approximately a few hundred volts (400V∼700V) to be suitable with vehicle powertrains. Consequently, in order to function as a power conditioning unit between the PEMFC and the motor drive system, a DC/DC boost converter is required. Zhang et al. [4] proposed a diode-capacitor based non-isolated DC/DC converter as a simple and low-cost solution for achieving high step-up voltage regulation in fuel cell generation. Saravanan and Babu [5] proposed a high static gain DC/DC converter which is derived from SEPIC converter by introducing a voltage-doubler circuit. Delshad and Farzanehfard [6] presented a novel active soft-switching push-pull current fed converter with high voltage gain ratio. Vinnikov and Roasto [7] presented a Quasi Z-source Buck-

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TABLE 1. PEMFC specifications of Ballard®FCvelocity®-9SSL.

Symbol	Parameter	Value
P_N	Rated Power (beginning of life)	21.0 kW
I_{FC_N}	Rated Current	300 A
V_{FC_N}	Voltage	70.2 V
N_{cell}	Number of Cells	110
p_{H2}	Fuel Pressure	1.2 bar(g)
p_{O2}	Oxidant Pressure	1.0 bar(g)
T_{amb}	Ambient Temperature (operating)	-25~+75 °C

Boost inverter (Q-ZSI). Although these converters obtained either high voltage gain ratio or relatively high efficiency, the major drawback was that the input current ripple was still high which can decrease the fuel cell stack's lifespan [8]. Interleaved Boost Converter (IBC) has been developed for its low input current ripple feature, relatively simple construction and low current stress for power components [9], [10], [11], [12].

Hardware-in-the-Loop (HIL) real-time validation can help reduce the developing period and research cost [13]. Furthermore, HIL test is a necessary step before the establishment of experiment test-bench. Because it is a useful method for confirming the control strategy, particularly in the event of a malfunction, and because it lowers the risk that may arise in a real experiment [14].

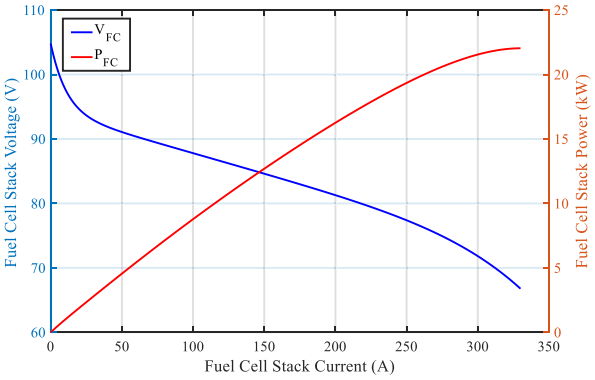
Silicon Carbide (SiC) semiconductors have better efficiency and thermal performance than Silicon (Si) semiconductor. Fewer power losses contribute to gain better thermal performance of powertrain in a FCEV. Meanwhile, the inductors, which are inverse coupled and constructed in cyclic cascade structure, can reduce inductors' volume and weight. Hence, SiC semiconductors and inverse coupled inductors are used in this work.

The manuscript is organized as follow: in section II, the modeling process of the selected PEMFC in our study is presented; section III presents a general theoretical comparison analysis of the fuel cell stack current ripple, the estimation of magnetic component volume and the converter's efficiency are mainly focused; in section IV, HIL real-time validation of the proposed IC-IBC is detailed; after that, section V presents the experimental results of a 1kW prototype of IC-IBC; the last section VI is where the manuscript ends.

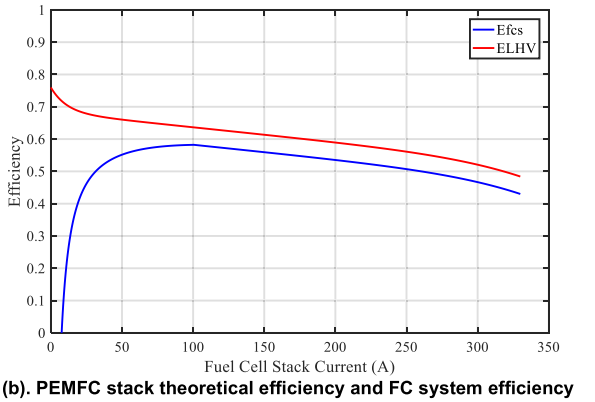
II. MODELING PROCESS OF PEMFC

The primary power source of an FCEV is a fuel cell stack, which transforms chemical energy contained in hydrogen straight into electrical energy. The stack voltage can be expressed as a function of parameters, for example, stack current, reactant pressures, membrane humidity, etc. [15]. In this study, the fuel cell model is based on Ballard® FCvelocity®-9SSL PEMFC and the parameters are as presented in Table 1 [16].

According to the literatures [15], [16], [17], [18], and [19], PEMFC polarization curve, stack efficiency and FC system



(a). PEMFC polarization curve



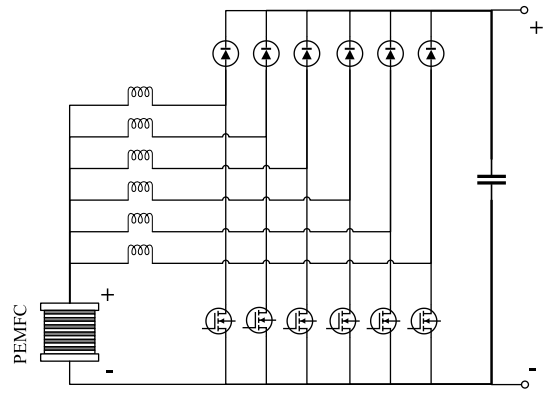
(b). PEMFC stack theoretical efficiency and FC system efficiency

FIGURE 1. Ballard® FCvelocity®-9SSL performance.

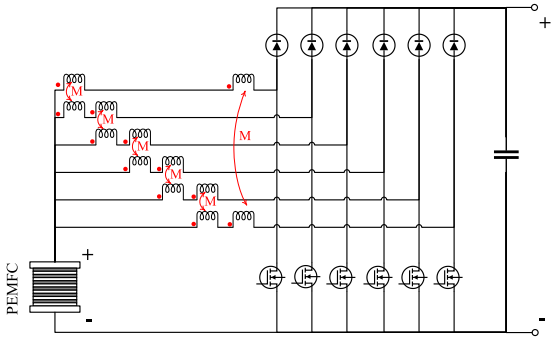
efficiency have been obtained depending on the Appendix A and presented as FIGURE 1. In FIGURE 1(b), the legend "E_{fcs}" represents fuel cell system efficiency and the legend "E_{LHV}" represents low heat value efficiency which is the fuel cell stack efficiency. It can be observed that the maximum efficiency of the fuel cell system is 58% when the fuel cell stack current reaches 100A. At the nominal power (300A), the system efficiency is 47% while the theoretical efficiency is 52%. Overall, the fuel cell system reaches high efficiency in the linearity range.

III. COMPARATIVE ANALYSIS OF THE PROPOSED CONVERTER

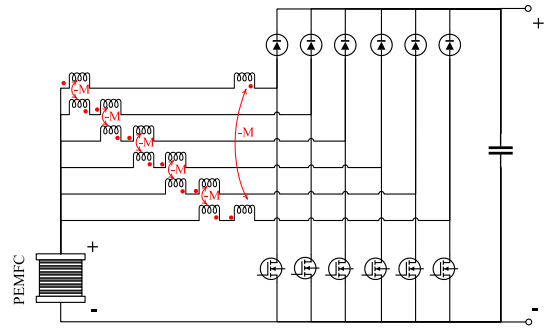
Benefitting from the interleaved architecture, IBC owns features such as low input current ripple, low component electric stress, high redundancy and other advantages [17]. In this study, a six-phase IBC is designed in order to decrease component electric stress and input current ripple furthermore [18]. Meanwhile, both direct coupled inductor and inverse coupled inductor are taken into consideration to find out which coupled mode can help to reduce converter's volume, weight and power losses. As presented in TABLE 2, the proposed IC-IBC has been comparatively analyzed with UC-IBC and DC-IBC. The constructure of these two control groups are described in the table. And the topologies are illustrated by FIGURE 2. The converter specifications required in this study are presented in Table 3.



(a) 6-phase Interleaved Boost Converter (UC-IBC)



(b) 6-phase IBC: direct coupled inductor (DC-IBC)



(c) 6-phase IBC: inverse coupled inductor (IC-IBC)

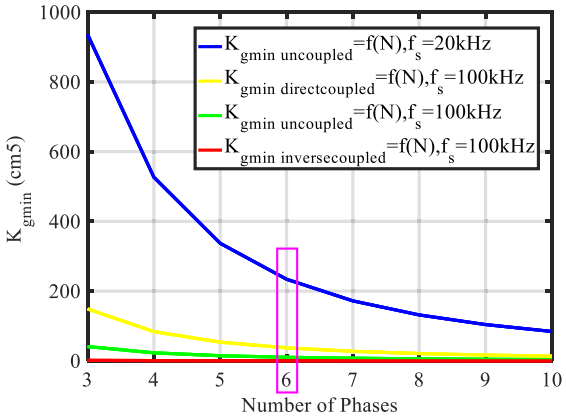
FIGURE 2. Three power converters for the comparative analysis done in this study.

TABLE 2. The characteristics of three converters in our study.

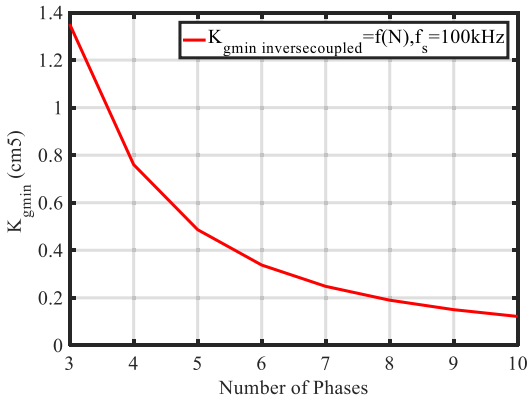
	Topology	Coupled Inductor	MOSFET & Diode	Phases
UC-IBC DC-IBC IC-IBC	Interleaved Boost Converter	Uncoupled Direct coupled Inverse coupled	SiC Semiconductor	6

A. COMPARISON ANALYSIS OF INDUCTOR VOLUME

Inductor's volume and weight affect the compactness of power converter a lot. To settle this issue, inductors in coupled structure are attractive to be used [20].



(a). Relationship between K_{gmin} and N



(b) Zoom of K_{gmin} for IC-IBC

FIGURE 3. Comparison of minimum core geometric constant among each topology.

TABLE 3. The specifications of DC/DC converters in our study.

Parameter	Symbol	Value	Unit
Input voltage	V_{in}	70	V
Nominal power	P_N	21	kW
Output voltage	V_{out}	350	V
Inductor current ripple	$\triangle i_L$	20%*I_L	A
	UC-IBC (f_{s1})	100	kHz
Switching frequency	DC-IBC (f_{s2})	100	kHz
	IC-IBC (f_{s3})	100	kHz

The effective electrical size of magnetic cores can be described by the core geometrical constant K_g [19], which can be calculated by equation (1) and (2) for uncoupled inductor core and coupled inductor core separately.

$$K_{g\ \min\_uncoupled} = \frac{\rho_{cu} \times L^2 \times I_{Lmax}^2}{B_{sat}^2 \times K_u \times R_L} \quad (1)$$

$$K_{g\ min\_coupled} = \frac{\rho_{cu} \times L_M^2 \times i_{M,sat}^2 \times (I_{L1} + I_{L2})^2}{B_{sat}^2 \times K_u \times P_{cu\_tot}} \quad (2)$$

In both equations, the wire effective resistivity ρ_{cu} is $1.724*10^{-6}$ Ω-cm, the saturation flux density B_{sat} is 0.2 Tesla and the winding fill factor K_u is 0.4. For UC-IBC, the induc-

tance is 56μH and the maximum inductor current is 55A. For DC-IBC and IC-IBC, the magnetizing inductances are the same that equals 56μH. The DC flux of inverse coupled inductor will be partially or totally canceled depending on the configuration of core. Hence, the maximum magnetizing current of IC-IBC is 5A, and 110A for DC-IBC.

According to FIGURE 3, the more interleaved phase used, the smaller core geometrical constant achieved. In FIGURE 3.(a), the blue curve and the green curve separately stands for UC-IBC combined with switching frequency of 20kHz and 100kHz. When the switching frequency increases, K_{gmin} of magnetic component decreases dramatically. When the switching frequency reaches 100kHz, the minimum core geometric constant of DC-IBC is the highest while the value of IC-IBC is the smallest. UC-IBC is between these two boundaries. The zoom of K_{gmin} for IC-IBC has been presented in FIGURE 3 (b). IC-IBC owns the minimum core geometric constant compared with other topologies, thus inductors with inverse coupled structure is more attractive for converters to help decrease total volume and weight in FCEV.

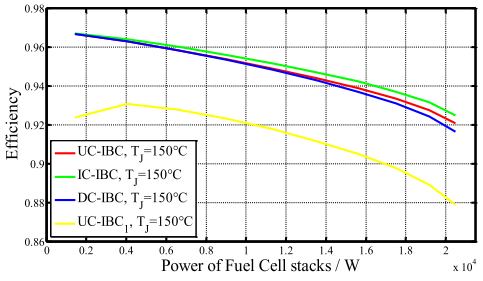
B. COMPARISON ANALYSIS OF CONVERTER EFFICIENCY

In order to satisfy high switching frequency requirement and reduce power losses, discrete SiC MOSFETs (CREE® C2M0025120D) and SiC Schottky diodes (CREE® C4D40120D) are used. Compared with the traditional Si semiconductor, SiC semiconductor can be applied in high switching frequency field benefiting from that lower switching losses can be achieved. Meanwhile, the utilization of SiC semiconductor can help achieve better thermal performance of the converter. The temperature rise can be kept at a low level because the power loss is lower than the use of Si semiconductor. Considering the silicon Schottky diode, the reverse recovery power loss is relatively high which can reduce converter's efficiency. For the SiC diode, its reverse recovery current is almost zero and the reverse recovery power loss can be neglected. In order to clearly explain how SiC semiconductor influences converter's efficiency, UC-IBC based on Si MOSFET (IXFB150N65 × 2, IXYS Corporation) and Si Schottky diode (IDW75D65D1, Infineon Technologies) has also been designed and analyzed. However, high switching frequency (100kHz in our study) is not suitable for the conventional Si semiconductor in real application; hence, the switching frequency of UC-IBC based on Si semiconductor is selected as 20kHz. In the following part, UC-IBC1 symbolizes UC-IBC based on the conventional Si semiconductors.

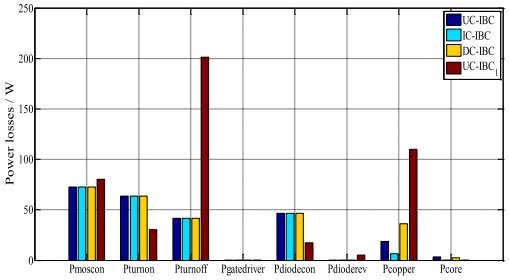
In order to analyze converter's efficiency, magnetic component of each converter has been designed and the specifications are summarized in Table 4. The quantity of core is for single phase of each converter. Obviously, direct coupled structure and low switching frequency lead to the increase of core volume and weight as the designed cores for DC-IBC and UC-IBC$_1$.

TABLE 4. Inductor's specifications (single phase).

Converter	Core	Quantity	Single Core Volume & Weight
UC-IBC	Toroid, MPP 60µ	1	91400 mm^3, 790g
DC-IBC	Toroid, MPP 26µ	4	91400 mm^3, 790g
IC-IBC	Toroid, MPP 60µ	1	21300 mm^3, 180g
UC-IBC$_1$	Toroid, MPP 14µ	1	407000 mm^3, 3000g



(a). Efficiency curves in whole power range of PEMFC @ Tj=150℃



(b). Single phase power losses distributions @ PFC=21kW & Tj=150℃

FIGURE 4. Efficiency curves and single phase power losses of UC-IBC, IC-IBC and DC-IBC.

The calculation processes of each component's power losses have been given by in Appendix C. Concerning the real application, during the design process, it is essential to determine each component's maximum power losses in the worst-case scenario. Because semiconductors' parameters change a lot with the junction temperatures, The datasheet indicates that for semiconductors, the worst-case temperature is 150°C for the junction temperature (T_j).

The efficiency of each converter has been calculated as presented in FIGURE 4.(a). The efficiency of IC-IBC is the highest and its maximum value is over 96.5%. At the nominal power, the efficiency of IC-IBC and DC-IBC are 92.12% and 91.20%, separately. The efficiency of UC-IBC is between IC-IBC and DC-IBC. However, in the low power range, the difference among the efficiencies of each topology is not significant. It is evident that the efficiency of UC-IBC$_1$ is the lowest in the whole range. At the nominal power, the efficiency is only 87.8% and its maximum efficiency is lower than 93%.

Figure 4 (b) shows the power losses distribution of the single phase for these four converters so that one may

comprehend how the power losses of each component affect the converter's efficiency.

From FIGURE 4.(b), it can be found that:

1) UC-IBC$_1$ obtains the highest switching losses, especially during the turn-off period of Si MOSFET. This is a main drawback of the conventional Si MOSFET compared with SiC MOSFET.

2) Varying inductors have varying power losses. Because of its small core size, IC-IBC achieves the lowest copper losses and core losses. For UC-IBC$_1$, the length of winding increases and its copper losses is the highest. The magnetic fluxes of DC-IBC are superimposed inside the magnetic core because the inductors are coupled directly; hence, a bigger magnetic core is requested and P_{copper} of DC-IBC also increases.

Therefore, compared with the conventional Si semiconductor, SiC semiconductor helps a lot to reduce the switching losses. At the same time, high switching frequency can be applied benefiting from the use of SiC semiconductor. Hence, the proposed topology achieves the highest efficiency and the most compact structure.

C. THEORETICAL ANALYSIS OF FUEL CELL SYSTEM EFFICIENCY BASED ON DIFFERENT CONVERTERS

Considering the influence of power converter's losses, the fuel cell system efficiency can be calculated as (14) [15]:

$$\eta'_{sys} = \eta_{FC} \times \eta_{aux} \times \eta_{conv} \tag{3}$$

The obtained fuel cell system efficiency curves of IC-IBC, DC-IBC, UC-IBC and UC-IBC$_1$ are illustrated in FIGURE 5. PEMFC system combined with IC-IBC owns the highest efficiency in the whole range. At the nominal power, the system efficiency is around 43%; the maximum system efficiency is around 55.8%. For the system combined with either UC-IBC or DC-IBC, although its efficiency is lower than the system combined with IC-IBC, there is no very big difference among these three systems. Due to the converter UC-IBC$_1$ obtains the lowest efficiency, the PEMFC system also has the lowest system efficiency compared with other three s (41% at the nominal power; 53% at the maximum point). Therefore, IC-IBC can improve not only converter's efficiency but also PEMFC system's efficiency, which is important for the fuel economy. In Figure 5, the green curve of UC-IBC's efficiency is very close to the red and blue curves. Hence, the fuel cell system efficiency is zoomed at the nominal operating point to make the result clearer to understand.

D. SIMULATION ANALYSIS OF THE PROPOSED CONVERTER

As the inductor of each phase is coupled with the other two adjacent phases, a schematic diagram to illustrate the possible waveforms of the inductor currents has been presented in FIGURE 6 based on the modeling process of proposed converter which is detailed in Appendix B. The inverse coupled inductor's current waveform is compared with the

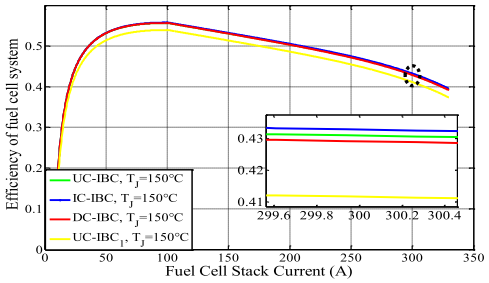


FIGURE 5. Comparison analysis of PEMFC system efficiency based on IC-IBC, DC-IBC and UC-IBC.

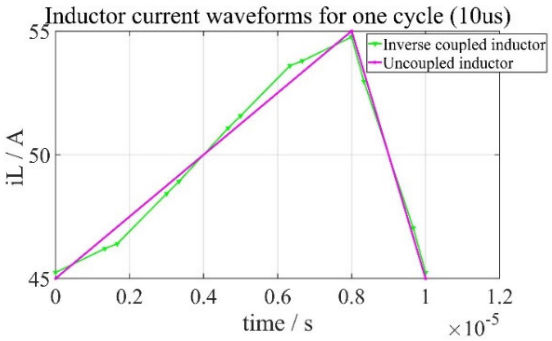


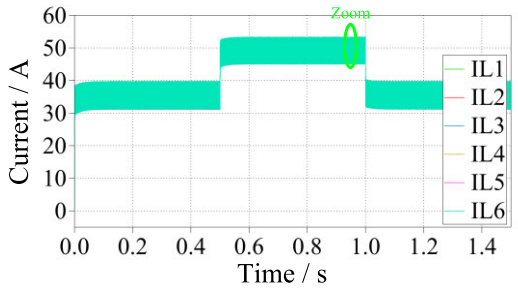
FIGURE 6. The comparison of inductor current waveforms of IBC based on inverse coupled inductor and uncoupled inductor.

current waveform of uncoupled inductor. Obviously, the one based on inverse coupled inductor owns more variations due to the aspect of inductor coupling. The variation is strongly influenced by the coupling mode, coupling coefficient and duty cycle. In this research, the inductor of each phase is coupled with the other two adjacent phases. And in this example, the coupling coefficient is set as -0.5 and the duty cycle is set as 0.8 to satisfy the voltage gain requirement.

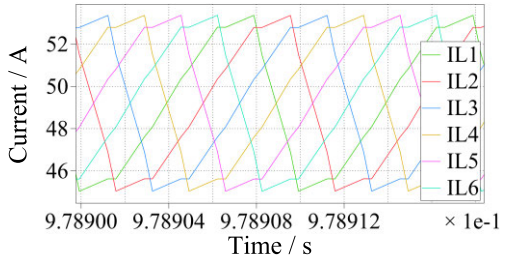
To verify the analysis of inductor current operation process, simulations have also been done under the environment of PLECS software. The simulation results are given as FIGURE 7. The simulation has been done under load variation condition. According to the results in FIGURE 7.(a) & (c), the inductor currents of each phase have been well controlled, and the DC bus voltage have been well regulated around the reference value 350V. Furthermore, as presented in FIGURE 7.(b), the inductor waveforms meet well with the theoretical analysis as shown in FIGURE 6. Hence, the theoretical analysis for the application of inverse coupled inductor structure to the proposed converter topology has been verified.

IV. HARDWARE-IN-THE-LOOP REAL-TIME VALIDATION OF IC-IBC

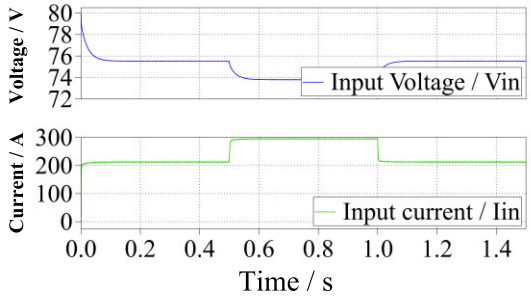
Hardware-in-the-Loop is treated as a useful way to validate a new converter topology or converter's control strategy [21]. In this section, the proposed IC-IBC, which shows significant interests for FCEV application, has been verified by HIL real-time emulation. MicroLabBox from dSPACE GmbH has



(a). Inductor current variation of each parallel phase under loading and unloading period



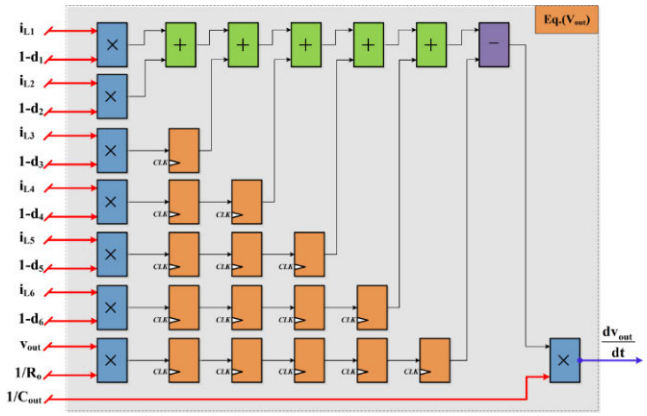
(b). Zoom of inductor current waveforms in (a)



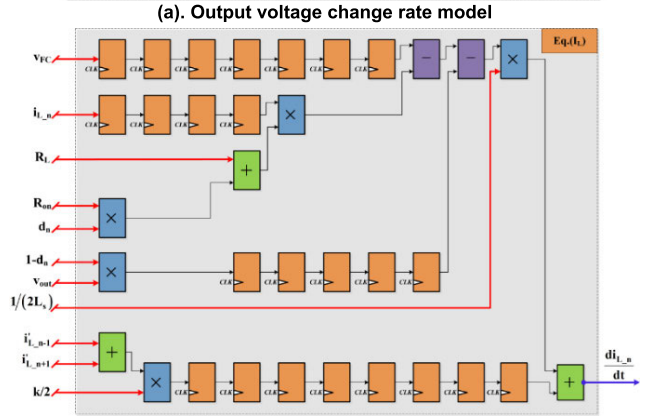
(c). DC bus voltage variation under loading and unloading period

FIGURE 7. The comparison of inductor current waveforms of IBC based on inverse coupled inductor and uncoupled inductor.

been used as the platform [22]. Inside the real-time emulator, a real-time processor of NXP (Freescale) QorlQ P5020, dual-core, 2 GHz exists to ensure its real-time solving ability. Meanwhile, a Xilinx® Kintex®-7 series FPGA is integrated to increase the equipment's hardware resources and improve its logical operation performance. No doubt that dSPACE MicroLabBox is typically employed as a Rapid Control Prototype (RCP). Meanwhile, this platform can also be used as a HIL platform which has been done in our research. During this study, we successfully modeled the proposed topology in FPGA of MicroLabBox, and the control strategy and PEMFC model are developed in real-time processor of MicroLabBox. The HIL validation and converter modeling process are presented in the diagrams of FIGURE 8 and FIGURE 9. According to this process, the proposed topology and the control strategy can both be validated based on high switching frequency before experimental tests on a small-scale test bench.



(a). Output voltage change rate model



(b). Inductor current change rate model

FIGURE 8. Converter and controller HIL modeling processes of IC-IBC.

A. HIL MODELING PROCESS OF THE PROPOSED CONVERTER

Because high switching frequency is required by the proposed IC-IBC, the real-time model is implemented in MicroLab-Box's FPGA module. The small signal model of converter is used aiming to verify the control strategy.

The proposed converter model is constructed by output voltage model and inductor current model. Each model consists two parts: variation rate model of sensed property and integrator model. The integrator model is realized by the adder and register of FPGA. The variation rate models are derived from the state-space equation of IC-IBC given by Appendix B, and are illustrated by FIGURE 8.(a) and (b) separately.

As the precision of logical operation is important to make sure the correctness of FPGA model, the registers are constructed in pipeline structure to improve FPGA program's response [23]. The output voltage variation rate is taken as an example to detail how to ensure FPGA model's latency. In FIGURE 8.(a), the latency of multiply operation is set as three clock periods while one clock period for add operation. iL_1*(1)-d_1), iL_2*(1)-d_2) and iL_3*(1)-d_3) are implemented in parallel. Then, the sum of iL_1*(1)-d_1) and iL_2*(1)-d_2) will be added to iL_3*(1)-d_3). Therefore, the calculation procedure is synchronized and the timing sequence disorder is avoided.

The identical approach is also applied to other loops and the timing synchronization of each model is realized.

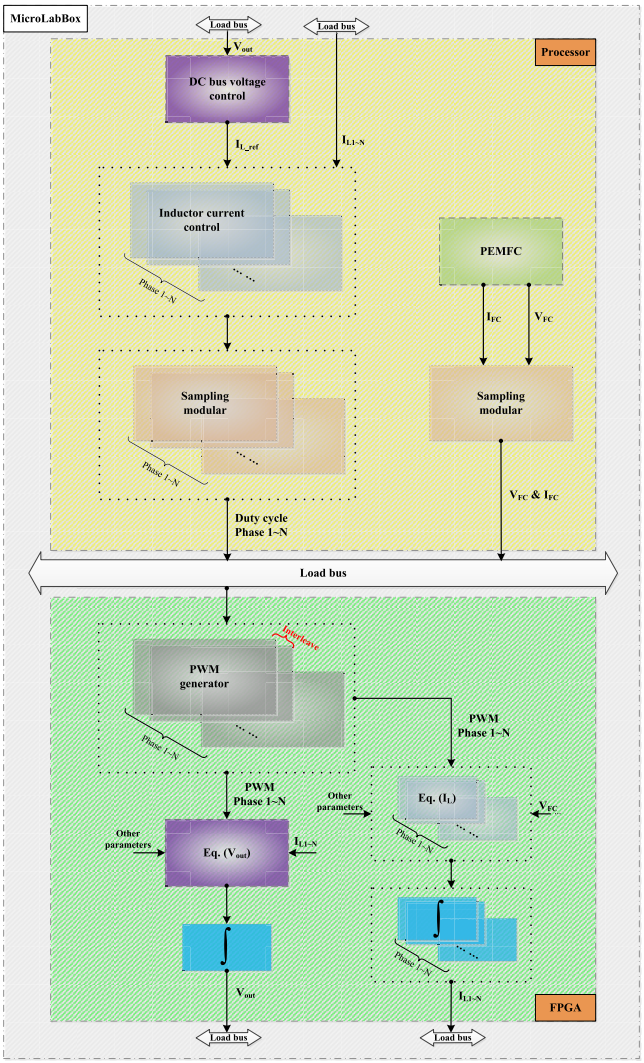
Since the AC component of inductor current is no more an ideal triangular wave, the inductor current equation of IC-IBC is more complicated as in FIGURE 8. (b). The coupling coefficient (k), the self-inductance (L_s), and the change rate of neighbor phase's current (i'_{L_n-1} and i'_{L_n+1}) are taken into consideration.

B. IC-IBC HIL REAL-TIME VALIDATION

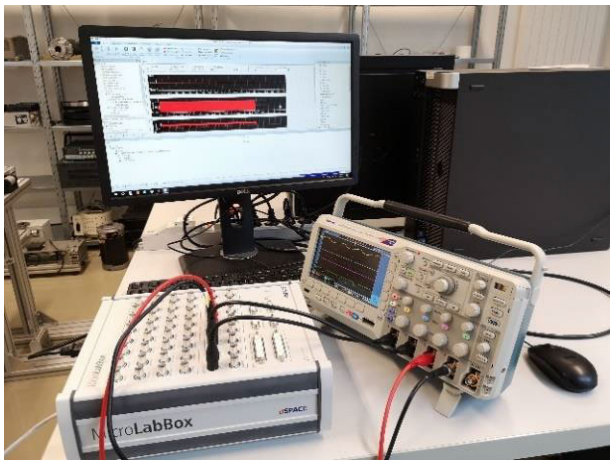
The diagram of MicroLabBox for real time HIL validation is presented as FIGURE 9.(a) and the HIL real-time validation platform used in this study is given in FIGURE 9.(b). The system construction can be detailed as two parts. "(V_{out})" and "(I_L)" have been analyzed in detail previously. The PEMFC and controller models are realized in the real-time processor, and the converter model is implemented in FPGA. Host computer sets the controller parameters and load parameters through monitoring the visual interface based on dSPACE ControlDesk. The time step of HIL model is set as 10us to meet the requirement of model precision.

Depending on the analysis in previous subsection, the real-time validation results are given as follow.

The results are as in FIGURE 10.(a)∼(c) for light load condition and FIGURE 10.(d)∼(f) for full load condition. As presented in FIGURE 10, DC bus output voltage, inductor current, fuel cell voltage and current have been achieved by HIL validation. From these results we can find that the converter output voltage is stabilized around 350VDC which the specification requirement, and no matter at light load or full load condition, the DC bus voltage can be well regulated. The voltage gain ratio reaches 4.04 under light load and 4.86 under full load. It is possible to reduce the voltage gain ratio in order to achieve higher converter efficiency (maximum as 96.5%) and PEMFC system efficiency (maximum as 55.8%). Hence, the correctness of the proposed topology and the control strategy have been verified. As presented in FIGURE 10 (c) & (f), the AC component of the inverse coupled inductors' current waveforms are detailed. To be emphasized here, due to the quantitative limitation of oscilloscope channel, only the current waveforms from phase 1 to phase 4 are shown. Obviously, these waveforms of HIL validation are identical with the theoretical analysis result and simulation result. The coupling coefficient is set as −0.5 and the duty cycle is set as 0.8 to satisfy the voltage gain requirement. According to the HIL validation results, the fuel cell current ripple can be kept blow 7% in the whole power range which satisfy the operation requirement of fuel cell stack. The fuel cell current ripples, 6.21% for light load and 1.6% for full load, are all kept lower than the limitation 10% [8]. Hence, the fuel cell stack lifespan is possible to be extended based on the proposed IC-IBC. The inductor current ripple and the fuel cell current ripple. As detailed previously, fuel cell current ripple is closely related to the lifespan of fuel cell stack. Therefore, a six-phase interleaved boost converter which is proposed in this study can reduce input current ripple significantly and is promising to extend its operating duration.

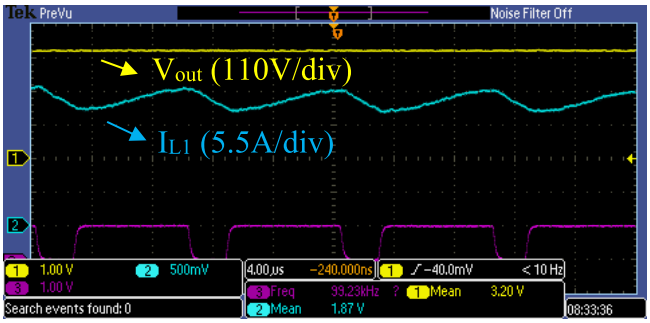


(a). Implementation of controller and DC/DC converter models inside the

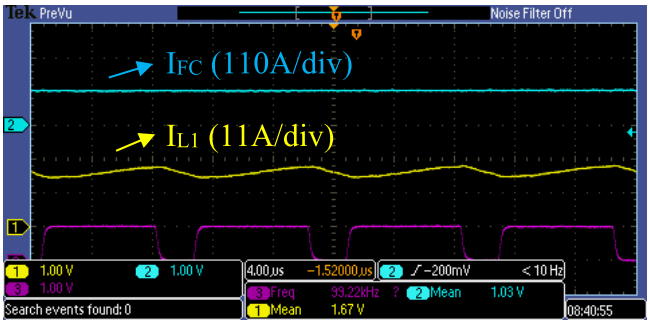


(b). HIL real-time validation platform: MicroLabBox from dSPACE GmbH

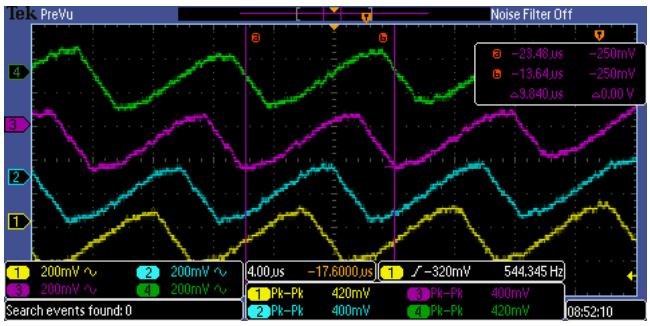
FIGURE 9. The realization and detail of IC-IBC HIL real-time validation.



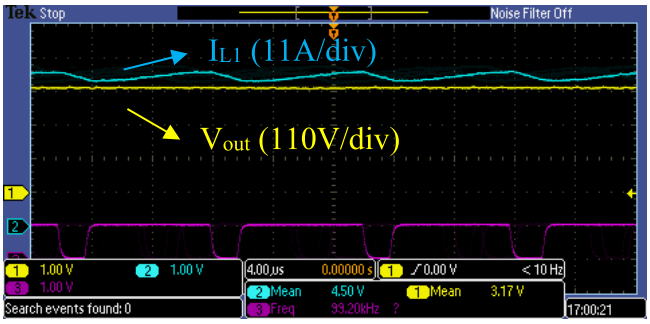
(a). Vout (yellow), L1 (blue) and PWM1 (purple) signals



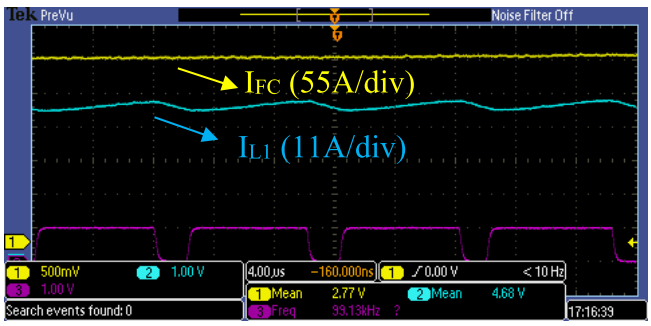
(b). IFC (blue), IL1 (yellow) and PWM1 (purple) signals



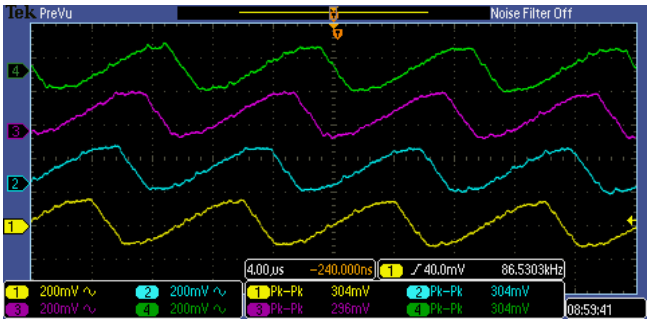
(c). AC component of IL1 (yellow, 2.2A/div), IL2 (blue, 2.2A/div), IL3 (purple, 2.2A/div), and IL4 (green, 2.2A/div) signals



(d). Vout (yellow), IL1 (blue) and PWM1 (purple) signals



(e). IFC (yellow), IL1 (blue) and PWM1 (purple) signals



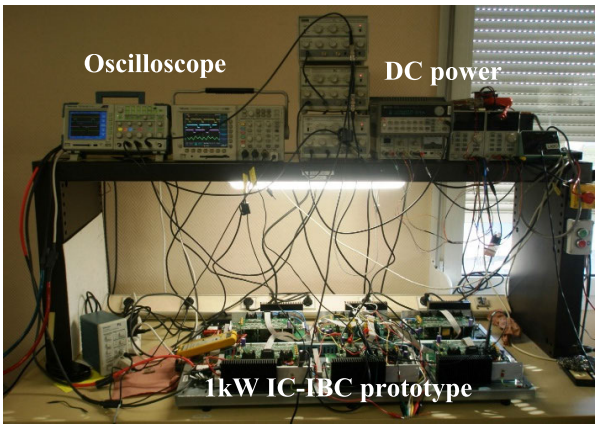
(f). AC components of IL1 (yellow, 2.2A/div), IL2 (blue, 2.2A/div), IL3 (purple, 2.2A/div), and IL4 (green, 2.2A/div) signals

FIGURE 10. HIL real time validation results of IC-IBC at different load conditions: light load (c)~(e) while full load (f)~(h).

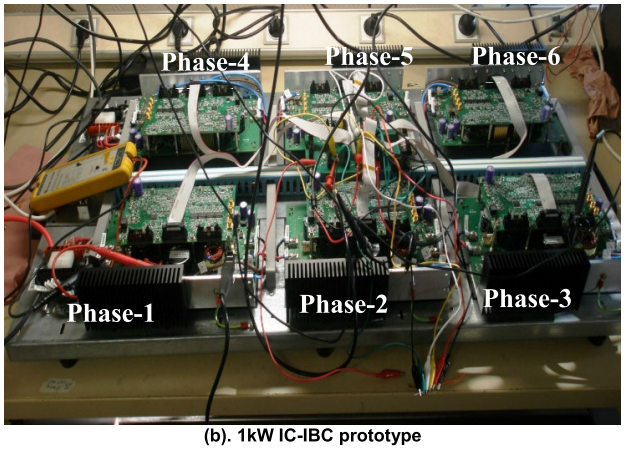
V. EXPERIMENTAL VALIDATION

In order to verify the proposed topology for PEMFC application, a 1kW prototype has been designed and tested in laboratory. The nominal input voltage and output voltage are 12V and 24V, respectively. The output voltage can be set between 20V and 80V by tuning the duty cycle. The switching frequency is set as 66kHz due to the limitation of test platform. The inductor current ripple is set as 10%*I_L. The magnetizing inductance is 116μH. The SiC MOSFETs (C3M0065090D) of CREE® are used as the power switches. In the prototype, the diodes are also replaced by the selected SiC MOSFET in order to reduce the reverse recovery power losses. Two power switches are connected in parallel to reduce the conduction losses at each branch, thus, four SiC MOSFETs exist in a single phase of the converter. The output filter capacitor is 300μF and the ESR is 2.4mΩ. The experiment test platform and the detail of the prototype are presented in FIGURE 11.

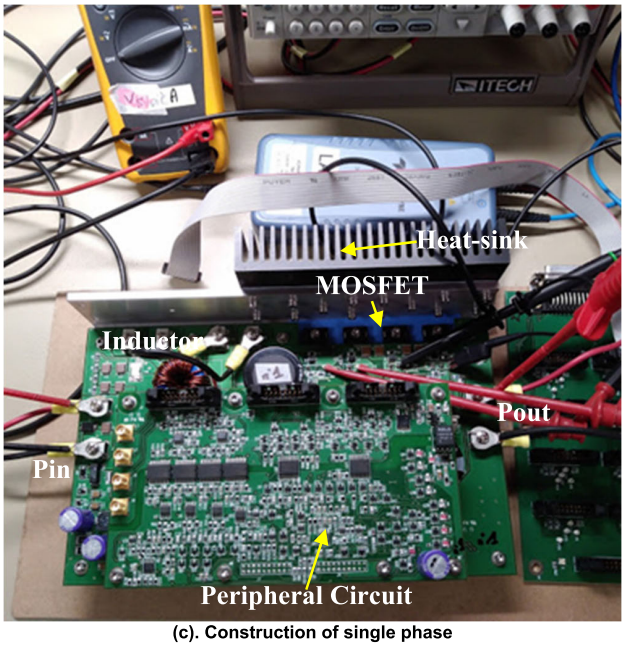
The validation results are illustrated in FIGURE 12. A group of typical operating conditions is given that the input voltage is 12.5V and the output voltage is 25.0V. Three power levels are tested to verify the prototype, 280W, 625W and 890W. At each condition, the DC bus voltage and inductor current are well controlled. Since there is a limitation of oscilloscope's channels, only the drain-source voltages of Phase-1~3 and the inductor current of Phase-1 are recorded. In FIGURE 12 (a), the inductor current of Phase-1 is denoted by the green curve. It can be found clearly that inductor current pulses six times during one switching cycle, which corroborate the theoretical analysis and HIL validation



(a). Test condition

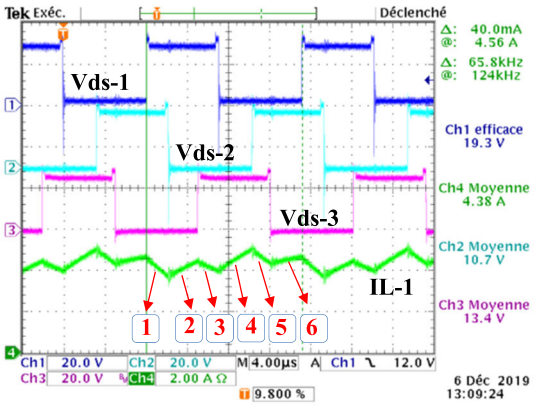


(b). 1kW IC-IBC prototype

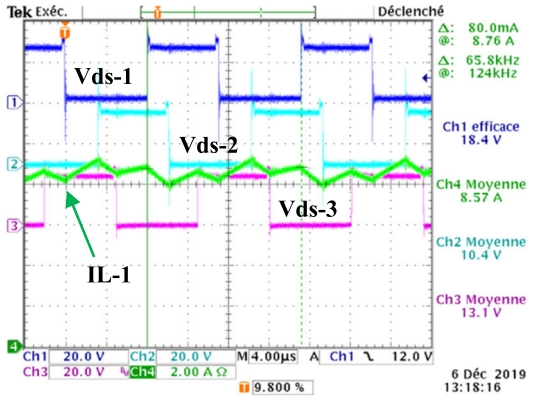


(c). Construction of single phase

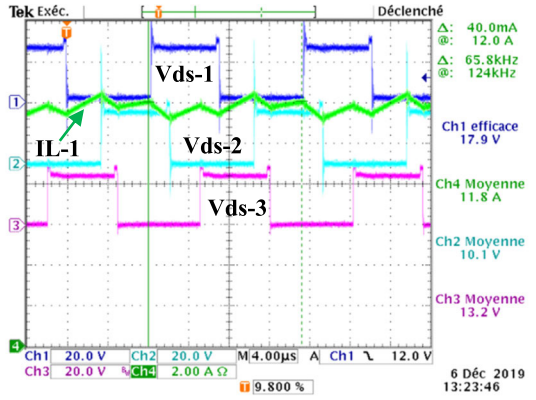
FIGURE 11. Experimental validation of the proposed 6-phase IC-IBC by a 1kW prototype.



(a). Vin=12.54V Iin=22.4A Vout=25.45V Iout=10.01A fs=66kHz Ton=8.4μs



(b) Vin=12.51V Iin=50.0A Vout=23.63V Iout=22.85A fs=66kHz Ton=8.4μs



(c) Vin=12.57V Iin=71.2A Vout=23.11V Iout=32.00A fs=66kHz Ton=8.7μs

FIGURE 12. Experimental results of the IC-IBC prototype.

presented in previous sections. As explained previously in section III, the inductor current waveform of the proposed topology is strongly influenced by the coupling mode, coupling coefficient and duty cycle. Because the experiment platform is a down scale prototype, which is 1kW at the nominal operating point, the converter's specifications differ from the theoretical analysis. The coupling mode is still inverse coupled with adjacent phases and the main differences are explained as follow: 1) the duty cycle of the converter is set around 0.5 which can satisfy the two times voltage gain ratio requirement; 2) the coupling coefficient is set as negative 0.9 which is negative 0.5 during the simulation and HIL validation. According to our previous research [9], higher coupling coefficient can lead to higher input current ripple.

Although the input current ripple is increased, it is still kept blow 10% and will not lead to negative effectiveness to the fuel cell.

VI. CONCLUSION

A six-phase IBC has been proposed for FCEV application in this study. Benefiting from the interleaved structure and inverse coupled inductor, the proposed converter has significantly reduced the fuel cell current ripple and the fuel cell stack lifespan can therefore be extended. Depending on the comparative analysis with two other topologies, the volume, weight and core losses of magnetic component have been dramatically decreased by the use of inverse coupled inductor based on the cascade structure. Thanks to SiC semiconductor, high switching frequency has been applied. Moreover, the switching losses, reverse recovery losses and conduction losses have been reduced significantly. Hence, the efficiency of the proposed IC-IBC has been increased and more compact magnetic component has been selected. The PEMFC system based on IC-IBC has achieved relative high efficiency, and thus, its hydrogen consumption rate is possible to be reduced. The proposed IC-IBC has been validated by real-time HIL. Obviously, the verification results coincide with the theoretical analysis. At last, the topology is validated by a 1kW prototype. Hence, the novelty of this research can be concluded as follow: 1) a new DC/DC power converter topology is proposed for FCEV application to achieve low input current ripple, low electrical stress on components and a more compact structure; 2) a much more rigorous verification process is used in this study to confirm the correctness and effectiveness of theoretical analysis, design process and validation results. In the future study, the compactness and efficiency of IC-IBC prototype will be focused to improve the performance of system.

APPENDIX A
PEMFC MODEL AND EFFICIENCY CALCULATION

In (A.1), v_{cell} stands for single cell terminal voltage and v_{FC} stands for stack voltage.

$$\begin{cases} v_{cell} = E - v_{act} - v_{ohm} - v_{cons} \\ v_{FC} = v_{cell} \times N_{cell} \end{cases} \tag{A.1}$$

E stands for the cell Nernst voltage in (A.2).

$$E = 1.229 - 0.85 \times 10^{-3} \times \left(T_{fc} - T_0\right) + 4.3085 \times 10^{-5} \times T_{fc} \times \left[ln\left(p_{H_2}\right) + \frac{1}{2} \cdot ln\left(p_{O_2}\right)\right] \tag{A.2}$$

The cell activation loss can be obtained by (A.3).

$$v_{act} = v_0 + v_a \times \left(1 - e^{-c_1 \times j_{fc}}\right) \tag{A.3}$$

The cell ohmic loss can be obtained by (A.4).

$$\begin{cases} v_{ohm} = j_{fc} \times R_{ohm} \\ R_{ohm} = \dfrac{t_m}{\sigma_m} \end{cases} \tag{A.4}$$

The concentration loss can be obtained by (A.5).

$$v_{conc} = j_{fc} \times (c_2 \times \frac{j_{fc}}{j_{max}})^{c_3} \tag{A.5}$$

For the auxiliary system of PEMFC, the power required by air compressor can be obtained as (A.6).

$$P_{cp} = \frac{C_p \times T_{amb}}{\eta_{mec} \times \eta_{mot}} \times \left[\left(\frac{p_{sm}}{p_{atm}}\right)^{\frac{\gamma-1}{\gamma}} - 1\right] \times \dot{m_{air,in}} \tag{A.6}$$

The compressor air flow rate which can be obtained by (A.7).

$$\dot{m_{air,in}} = \frac{S_{O_2}}{r_{O_2}} \times \frac{I_{FC}}{4F} \times M_{air} \times N_{cell} \tag{A.7}$$

The air compressor efficiency can be obtained by (A.8).

$$\eta_{cp} = \frac{P_{FC} - P_{cp}}{P_{FC}} \times 100\% = \frac{P_{net}}{P_{FC}} \times 100\% \tag{A.8}$$

The voltage efficiency of a fuel cell (ηFC) is presented by (A.9).

$$\eta_{FC} = \eta_{LHV} = \frac{v_{cell}}{1.254} \tag{A.9}$$

Then, the fuel cell system efficiency can be calculated as (A.10).

$$\eta_{sys} = \eta_{FC} \times \eta_{aux} \tag{A.10}$$

APPENDIX B
IC-IBC MODELING PROCESS

The general formula of State-Space Equation for three converters is presented as

$$\begin{cases} K \cdot \dfrac{dx\,(t)}{dt} = A \cdot x\,(t) + B \cdot u\,(t) \\ y\,(t) = C \cdot x\,(t) + E \cdot u\,(t) \end{cases} \tag{B.1}$$

In equation (B.1), K is a constant matrix, which is one of the coefficients of converter's state-space equation. When the converter topology exchanges, the matrix will also be modified. As presented by (B.2), u(t) stands for the input variables; y(t) stands for the output variables; x(t) stands for the state variables which contains the inductor current and capacitor voltage.

$$\begin{cases} x\,(t) = \left[\, i_{L1}\,(t) \cdots i_{LN}\,(t)\ v_o\,(t) \,\right]^T_{(N+1)\times 1} \\ u\,(t) = \left[\, v_{in}\,(t)\ 0 \,\right]^T \\ y\,(t) = i_{in}\,(t) \end{cases} \tag{B.2}$$

As presented by (B.3) and (B.4), as shown at the top of the next page, A, B, C and E are the constant matrix consists of the duty cycle, inductor resistance and semiconductor's conduction resistance.

K is the constant matrix consist the inductor value, mutual inductor value and capacitor value. The main difference between each converter's State-Space Equation is due to the specific value. As presented by (B.5), K1 stands for the matrix

$$A=\begin{bmatrix} -(R_L+D_1\times R_{on}) & 0 & \dots & 0 & -D'_1 \\ 0 & -(R_L+D_2\times R_{on}) & \dots & 0 & -D'_2 \\ \dots & \dots & \dots & \dots & \dots \\ 0 & 0 & \dots & -(R_L+D_N\times R_{on}) & -D'_N \\ D'_1 & D'_2 & \dots & D'_N & -\dfrac{1}{R_o} \end{bmatrix}_{(N+1)\times(N+1)} \tag{B.3}$$

$$\begin{cases} B=\begin{bmatrix} 1 & -D' \\ 0 & 0 \end{bmatrix} \\ C=\begin{bmatrix} 1 & 1 & \dots & 1 & 0 \end{bmatrix}_{1\times(N+1)} \\ E=\begin{bmatrix} 0 & 0 \end{bmatrix} \end{cases} \tag{B.4}$$

for UC-IBC. K2 given by (B.6) stands for the matrix for the proposed IC-IBC.

$$K_1=\begin{bmatrix} L_1 & 0 & \dots & 0 & 0 \\ 0 & L_2 & \dots & 0 & 0 \\ \dots & \dots & \dots & \dots & \dots \\ 0 & 0 & \dots & L_N & 0 \\ 0 & 0 & \dots & 0 & C \end{bmatrix}_{(N+1)\times(N+1)} \tag{B.5}$$

$$K_2=\begin{bmatrix} 2L_1 & -M & 0 & \dots & -M & 0 \\ -M & 2L_2 & -M & \dots & 0 & 0 \\ 0 & -M & 2L_3 & \dots & 0 & 0 \\ 0 & 0 & \dots & 2L_{N-1} & -M & \dots \\ -M & 0 & \dots & -M & 2L_N & 0 \\ 0 & 0 & 0 & \dots & 0 & C \end{bmatrix}_{(N+1)\times(N+1)} \tag{B.6}$$

APPENDIX C
POWER CONVERTER POWER LOSSES CALCULATION

TABLE 5. The calculation process of converter's power losses.

Symbol	Parameter	Calculation Process
P_{on_switch}	Power switch conduction losses	$(1/N^2)\times I^2_{in\_rms}\times D\times R_{on\_mos}$
P_{turnon_switch}	Power switch turn-on losses	$\frac{f_s\times(E_{test\_on}\times V_{switch})}{(V_{switch\_test\_on}\times I_{switch\_test\_on})}\times\left(\frac{I_{in}}{N}\right)$
$P_{turnoff\_switch}$	Power switch turn-off losses	$f_s\times\frac{(E_{test\_off}\times V_{switch})}{(V_{switch\_test\_off}\times I_{switch\_test\_off})}\times\left(\frac{I_{in}}{N}\right)$
P_{gate_driver}	Power switch gate driver losses	$Q_{gate\_mos}\times V_{gs}\times f_s$
P_{on_diode}	Diode conduction losses	$(I_{in_{ave}}/N)\times(1-D)\times V_F+(1/N^2)\times I^2_{in\_rms}\times(1-D)\times R_{on\_diode}$
P_{rev_diode}	Diode reverse recovery losses	$0.5\times V_{rev}\times Q_{rev}\times(V_{rev}/V_R)\times f_s$
P_{copper}	Inductor copper losses	$(1/N^2)\times I^2_{in\_rms}\times R_L$
P_{core}	Inductor core losses	$K_{fe}\cdot(\Delta B)^{\beta}\cdot A_c\cdot l_m$

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