

Received 20 March 2024, accepted 4 April 2024, date of publication 10 April 2024, date of current version 19 April 2024.

Digital Object Identifier 10.1109/ACCESS.2024.3387108

## RESEARCH ARTICLE

# Optimizing Low Noise Amplifiers: A Two-Stage Approach for Improved Noise Figure and Stability

MOHAMMAD ZAID<sup>1</sup>, (Member, IEEE), PURNIMA KUMARI<sup>2</sup>,  
AHTISHAM PAMPORI<sup>1</sup>, (Member, IEEE),  
MOHAMMAD SAJID NAZIR<sup>1</sup>, (Member, IEEE), UMAKANT GOYAL<sup>2</sup>, (Member, IEEE),  
MEENA MISHRA<sup>2</sup>, AND YOGESH SINGH CHAUHAN<sup>1</sup>, (Fellow, IEEE)

<sup>1</sup>Department of Electrical Engineering, Indian Institute of Technology Kanpur (IIT Kanpur), Kanpur 208016, India

<sup>2</sup>Solid State Physics Laboratory, Defence Research and Development Organization, Delhi 110054, India

Corresponding author: Mohammad Zaid (mzaid@iitk.ac.in)

**ABSTRACT** This study introduces a new design for a low noise amplifier (LNA) consisting of two stages taking advantage of the inherent lossy properties of the input matching components. By doing this, the design balances the minimum noise figure (NF) and stability, eliminating the complexities and challenges introduced by feedback networks. Furthermore, the integration of the low-pass filter (LPF) into the design as a noise-matching network ensures improved performance across both the amplifier stages. A comprehensive analytical study is also introduced to delve deep into the relationship between critical LNA parameters, such as stability and noise figures, and the internal resistance of input-matching inductors. Two C-band LNAs are compared in terms of stability using indigenous  $0.25\mu\text{m}$  GaN technology. The designs are substantiated by fabricating two LNA MMICs for a 5-7 GHz frequency range, having a minimum NF of 1.3 dB and 1.5 dB, with a gain of 15 dB and 16 dB at 6 GHz, respectively. The study reveals that using the proposed approach, there is an overall improvement in NF of 0.2 dB within the frequency of operation. The work entails a way to remove the feedback network in the LNA leading to an improved NF.

**INDEX TERMS** C-band, GaN, low-noise amplifier (LNA), low pass filter (LPF), noise figure (NF).

## I. INTRODUCTION

With the advent of 5G, wireless communication systems development has become rampant. Wireless communication systems' complexity has evolved significantly in going from the 2nd Generation (2G) to the 5th Generation (5G) technology. 5G NR wireless systems are cutting-edge networks that use smaller cells to connect more devices than 4G cells. From smart city appliances and robots to autonomous and networked cars, this technology has many uses. 5G New Radio (NR) Generation wireless systems are more efficient networks as they use smaller and more efficient cells, making the interconnection between cells easy [1].

The associate editor coordinating the review of this manuscript and approving it for publication was Bilal Khawaja<sup>1</sup>.

While the 3rd Generation Partnership Project (3GPP) has categorized 5G into two distinct frequency ranges, FR1 (sub-6 GHz) and FR2 (over 24 GHz), it is a widespread fallacy to solely associate 5G with the high-frequency band. An essential obstacle in the journey towards worldwide implementation of 5G is the development of diverse wireless elements inside the FR1 and FR2 frequency bands. Therefore, it is crucial to possess the ability to build wireless components within the FR1 band efficiently. The FR1 band encompasses lower frequencies, resulting in longer wavelengths, which allows for extensive coverage and plays a crucial role in ensuring improved connectivity. Therefore, the development of RF components in the FR1 band has made notable progress in the present period [2], [3].

The effectiveness of these systems heavily depends on the effective amplification of weak signals picked up by

antennas. The LNA, a critical element responsible for amplifying the received signals, is at the center of the transceiver chain. The key feature of an LNA is its capacity to boost signal power without degrading the signal-to-noise ratio, leading to enhanced system sensitivity, range, and performance. [4], [5]. Typically, the LNA being the initial active stage of a microwave receiver system, its noise-gain performance affects the overall NF of the receiver, necessitating careful optimization during the design phase [6], [7]. Apart from providing an excellent NF, the LNA must also be highly rugged. Therefore, the choice of process technology used in the design of an LNA is also vitally important [8], [9], [10].

With its large bandgap, high breakdown field, high peak and saturation carrier velocity, and good thermal conductivity, AlGaIn/GaN high electron mobility transistor (HEMT) devices have become the technology of choice for high-power microwave electronics [11], [12], [13], [14], [15], [16], [17], [18]. Apart from being the technology of choice for next-generation high-power and high-frequency applications, they also show excellent noise characteristics for the design of LNA [19], [20]. When used in the transmitter/receiver front-end design, GaN HEMTs contribute to the integration of high-power amplifiers (HPAs) and LNAs in the same epitaxial material, thereby eliminating the receiver protection circuitry [19], [20].

Because of the high inherent ruggedness of GaN devices, the LNA can be designed without a limiter circuit to sustain high input power levels compared to other design technologies like GaAs. As a result of removing the limiter from the chain, the resulting LNA has a lower NF and less complex circuitry [1], [19], [21], [22], [23]. One of the principal characteristics of LNA design using GaN technology is the inherent linearity of the GaN devices. Thus, if HPA and  $T/R$  switches can be designed using the same GaN technology as the LNA, a fully integrated  $T/R$  module with low noise, high linearity, and high power amplification can be developed [24], [25].

The primary goal of LNA design is to achieve both minimum NF and maximum stable gain [26]. Traditionally, there is a trade-off between maximizing gain and minimizing NF. As a result, it is critical to understand how to achieve a low NF while maintaining constant gain. Different topologies and stabilization techniques are employed in an LNA to achieve stability, each with merits and demerits. The most prevalent and commonly used LNA topology is the common source (CS) topology. Compared to the common gate topology, a common source LNA's gain and noise performance are superior. However, due to the Miller effect, the amplifier's bandwidth is typically narrow [27]. Using the proper feedback or matching circuits, a common source design may be employed in wideband applications [28]. In a wideband LNA, inductor degeneration (LS) feedback is used to bring the minimum noise impedance ( $Z_{opt}$ ) closer to the maximum power gain impedance ( $Z_{in}$ ),

**TABLE 1. Important Process Parameters of the 0.25  $\mu\text{m}$  GaN technology.**

Parameter	Typical Value
Active Device	HEMT
Gate Length	0.25 $\mu\text{m}$
$I_{ds} - Sat$	1000mA/mm
Breakdown Voltage	>100 V
Cut-off Frequency	40 GHz
Pinch-off Voltage	-3.4 V
Wafer Thickness	100 $\mu\text{m}$

while resistive feedback (RF) increases the stability of the LNA [29], [30].

In this work, we provide an in-depth analytical comparison of two distinct LNAs. Our analysis uncovers a vital link between the stability, NF, and internal resistance features of the lossy inductors used as matching components in the LNA design. The method of using the inductor's internal resistance for stabilization improves the LNA's overall NF (0.2 dB in our case) without significantly affecting its gain. Solid State Physics Laboratory (SSPL) developed indigenous 0.25  $\mu\text{m}$  GaN technology, which is employed in the design and fabrication of the LNA. Section II gives a brief introduction to the process technology and the choice of device used for the design of the LNA. Section III consists of an in-depth analysis of the effect of the internal resistance on the stability, gain, and NF. Results of the fabricated LNA are discussed in section IV and finally, the paper is concluded in section V.

## II. MMIC DESIGN

### A. PROCESS TECHNOLOGY

The production begins with a Silicon Carbide (SiC) substrate that's 100  $\mu\text{m}$  thick, chosen for its impressive heat conductivity and its compatibility with GaN materials. The molecular Beam Epitaxy (MBE) technique is used to grow layers of GaN, AlGaIn, and GaN on the substrate. After these layers have been developed, a gate, with a width of 0.25  $\mu\text{m}$ , is etched onto the semi-insulating SiC substrate using electron beam lithography. In this design, the drain and source electrodes of the device are formed through an ohmic contact, ensuring low contact resistance and optimal current flow. To achieve short gate length and low gate resistance, optical lithography defines the 0.25  $\mu\text{m}$  ODgate. The U-groove ODgate etching is formed by using a silane based solution that terminates on GaN cap etching stop layer incorporated into the epitaxial material structure and followed by a metal deposition and lift-off sequence to form the 0.25  $\mu\text{m}$  T-gate of the transistor. To safeguard the wafer,  $\text{Si}_3\text{N}_4$  passivation layer is laid down using plasma-enhanced chemical vapor deposition (PE-CVD), and fluorine ion implantation is utilized to separate active devices.

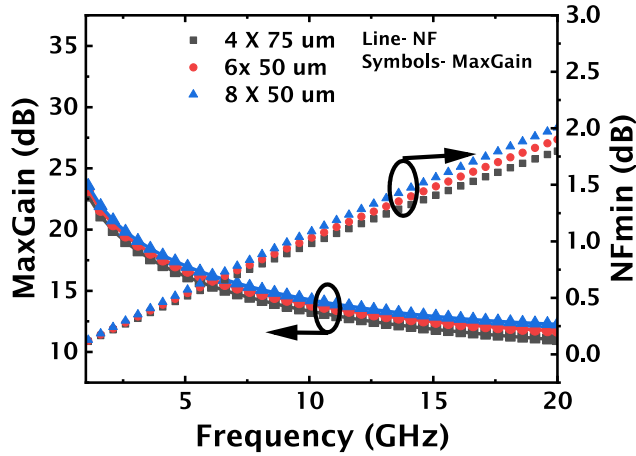


FIGURE 1. Variation of minimum NF and maximum gain with change in device width and the number of fingers for three different devices with frequency (bias current of 48 mA).

**B. DEVICE SIZE SELECTION**

The primary challenge in Low-Noise Amplifier (LNA) design is achieving simultaneous noise matching and gain matching. It is feasible to engineer an LNA with a significantly low NF, but this often leads to a compromise in gain performance. The selection of the input device is critical in LNA design. To maintain robustness against high input power levels, the device size must be sufficiently large, ensuring high input power survivability and a minimal  $NF_{min}$ . Equation (1) illustrates that an input device with elevated NF and diminished gain will adversely affect the overall NF of the LNA.

$$NF = NF_1 + \frac{NF_2 - 1}{Ga_1} + \frac{NF_3 - 1}{Ga_1 * Ga_2} + \dots \quad (1)$$

The device choice for the design of this particular LNA is based on the noise parameters measurements. The measurement was carried out for bias of 48 mA, 96 mA, and 144 mA. The drain was biased at a voltage of 10 volts, while the gate was varied from -5 volts to -3 volts. The selection of the three points was based on the criteria of NFmin and gain. The decision was made not to select low-bias current due to its inadequate gain. The three positions, namely 48mA, 96mA, and 144mA, were selected because the NFmin at these specific points exhibited a difference of around 0.2 dB. Choosing too many bias currents nearby results in unnecessary additional labor, as it does not significantly affect the minimum noise figure (NFmin) or the optimal noise impedance.

Three devices having a width and number of fingers as  $4 \times 75 \mu m$ ,  $6 \times 50 \mu m$  and  $8 \times 50 \mu m$  were fabricated and the NF and gain of the devices were measured for each, and the data was analyzed. The device having the dimensions  $4 \times 75 \mu m$  showed the minimum NF while providing a sufficient maximum gain which is what is required according to Equation (1). The measured NF and maximum gain for all the device sizes is as shown in Fig. 1.

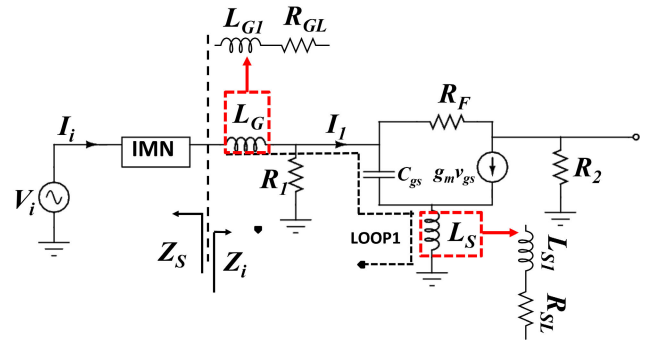


FIGURE 2. Small signal equivalent of the LNA with resistive feedback and representing Miller effect. The feedback capacitor is not shown to simplify the analysis.

**III. DETAILED THEORETICAL ANALYSIS**

**A. EFFECT OF INTERNAL RESISTANCE ON THE STABILITY**

The stability of a two-port network is usually determined by two critical parameters,  $K$  - factor and  $\mu$  - factor, defined in (2) and (4), respectively.

$$K = \frac{1 - |S_{11}|^2 - |S_{22}|^2 + |\Delta|^2}{2 |S_{12}S_{21}|} \quad (2)$$

where

$$\Delta = S_{11}S_{22} - S_{12}S_{21} \quad (3)$$

and

$$\mu = \frac{1 - |S_{11}|^2}{|S_{22} - S_{11}^*| + |S_{21}S_{12}|} \quad (4)$$

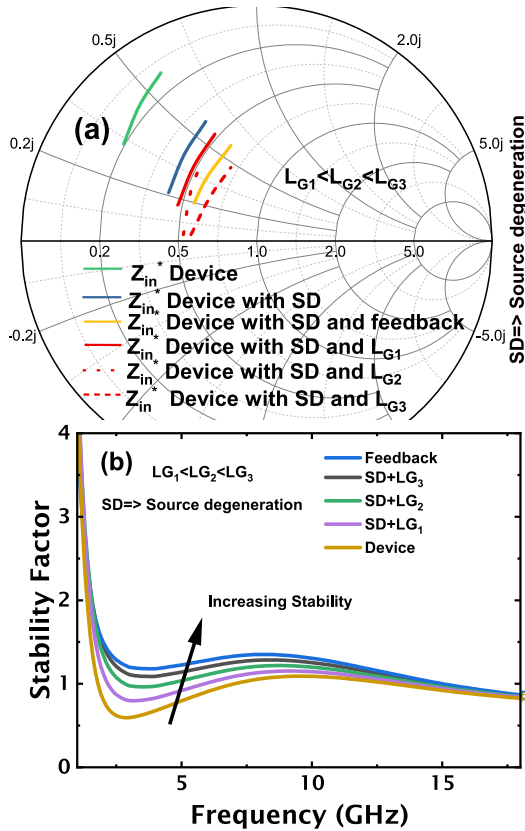
For a two-port network to be unconditionally stable, the K-factor and  $\mu$ -factor must be greater than 1 and 0, respectively [31], [32]. As can be seen from (4), for the  $\mu$ -factor to be greater than 0,  $|S_{11}|$  must be less than 1. In terms of input impedance  $Z_{in}$  and characteristic impedance  $Z_0$ ,  $|S_{11}|$  can be written as (5).

$$|S_{11}| = \frac{Z_{in} - Z_0}{Z_{in} + Z_0} \quad (5)$$

Thus, for  $|S_{11}|$  to be less than 1, the value of  $Z_{in}$  must be real and positive. To see the dependence of  $Z_{in}$  on the feedback as in [33], we apply KVL in the input loop 1 of the circuit shown in Fig. 2. The feedback resistor  $R_F$  present in the common source topology can be divided into two parts using Miller's theorem as  $R_1$  and  $R_2$ , calculated as  $R_1 = R_F / (1 - A_v)$  and  $R_2 = R_F (1 - 1/A_v)$ . Using KVL in loop-1 (see Fig. 2), we get,

$$v_i = j\omega L_G I_i - \frac{kI_i (j\omega L_G + R_1)}{j\omega C_{gs} R_1} - \frac{k v_i}{j\omega C_{gs} R_1} \quad (6)$$

$$Z_{in} = \frac{-\omega^2 C_{gs} L_G - (1 + j\omega L_S g_m - \omega^2 L_S C_{gs}) \left( \frac{j\omega L_G}{R_1} + 1 \right)}{j\omega C_{gs} + \frac{1 + j\omega g_m L_S - \omega^2 L_S C_{gs}}{R_1}} \quad (7)$$



**FIGURE 3.** (a)  $Z_{in}^*$  of the LNA for the first stage for different variations of the device from 5-8 GHz. The plot shows that a high inductor value at the input provides similar characteristics of  $Z_{in}^*$  as feedback can achieve. (b) the variation of the stability factor of the LNA for different geometry variations of the device. The plot shows that stability can be achieved using a higher inductor value at the input instead of feedback.

The value of  $Z_{in}$  without the feedback resistor can be written as:

$$Z_{in} = \frac{-\omega^2 C_{gs} L_G - (1 + j\omega L_S g_m - \omega^2 L_S C_{gs})}{j\omega C_{gs}} \quad (8)$$

Equations (7) and (8) can be rewritten by replacing the inductors along with their internal resistances, as given by (9) and (10), shown at the bottom of the next page.

Here,  $R_{GL}$  and  $R_{SL}$  are the internal resistance of the gate and drain inductance  $L_G$  and  $L_S$  respectively.

Expression of  $Z_{in}$  given in (10), implies the addition of feedback tends to increase the value of  $Z_{in}$ . From (9) it is clear that the same increase in the value of  $Z_{in}$  can be obtained by properly tuning the inductors  $L_G$  and  $L_S$  (source degeneration (SD)) such that they offer a high internal resistance, which is the ultimate goal for which feedback is employed. Thus, the feedback resistor that controls the input impedance of the LNA, and in turn, the stability of the circuit can be eliminated and the same control can be provided by the proper tuning of the lossy inductors at the cost of reduced stability as shown in Fig. 3 (b). Further, we observe from the Smith chart shown in Fig. 3 (a) that the gain matching becomes relatively easy if one applies feedback, as the  $Z_{in}^*$  moves closer to the 50  $\Omega$

point. The same trend can be achieved by using a large value of the input inductor.

### B. EFFECT OF INTERNAL RESISTANCE ON THE GAIN

Applying KVL in loop-1 of the LNA shown in Fig. 4 we get the relationship between  $v_i$  and  $v_{gs}$  as:

$$v_i = v_{gs} + j\omega g_m v_{gs} L_S \quad (11)$$

$$v_{gs} = \frac{v_i}{1 + j\omega g_m L_S} \quad (12)$$

Applying KCL at node-1 of the LNA shown in Fig. 10 gives us,

$$\frac{v_{out} - v_i}{R_F} + g_m v_{gs} + \frac{v_{out}}{Z_L} = 0 \quad (13)$$

Replacing the value of  $v_{gs}$  from (12) into (14) we get,

$$\frac{v_{out} - v_i}{R_F} + g_m \frac{v_i}{1 + j\omega g_m L_S} + \frac{v_{out}}{Z_L} = 0 \quad (14)$$

(14) can be written in terms of  $v_{out}$  and  $v_i$  as:

$$v_{out} \left[ \frac{1}{R_F} + \frac{1}{Z_L} \right] = v_i \left[ \frac{1}{R_F} + \frac{g_m}{1 + j\omega g_m L_S} \right] \quad (15)$$

The gain of the LNA can be simply written as the ratio of  $v_{out}$  and  $v_i$  as:

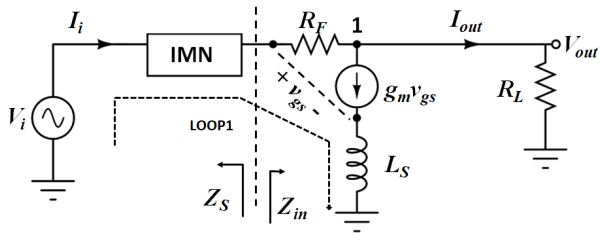
$$Gain = \frac{v_{out}}{v_i} = \frac{\left[ \frac{1}{R_F} + \frac{g_m}{1 + j\omega g_m L_S} \right]}{\left[ \frac{1}{R_F} + \frac{1}{Z_L} \right]} \quad (16)$$

From (16) it is clear that as the feedback increases (the value of  $R_F$  reduces) the gain of the LNA decreases. Therefore, feedback also affects the gain of the LNA.

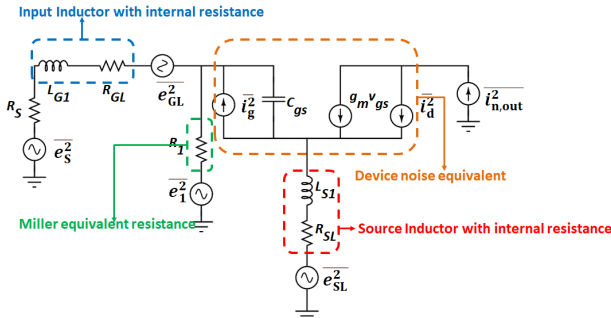
### C. EFFECT OF INTERNAL RESISTANCE ON THE NF

The influence of the inductor's internal resistance on the NF is discernible when analyzing the small-signal equivalent circuit of the LNA, particularly one that employs a resistive feedback inductive source degeneration topology, as depicted in Fig. 5. This intrinsic resistance has implications for the LNA's overall performance, and thus, understanding its role within this circuit configuration becomes vital. The expression for the NF can be derived and modified accordingly, using the expression of the NF of the circuit in Fig. 5 as (17) [34]. The first term of the equation encompasses noise introduced by all resistive components within the LNA, including the inductor's intrinsic resistance. The subsequent three terms respectively denote noise arising from gate and drain currents. The final triad of terms predominantly rests on device dimensions and biases, rendering them less susceptible to modifications. In contrast, the initial term is highly influenced by matching parameters, thereby exerting a significant influence on the LNA's NF.

Here  $R_1$  is the Miller equivalent of the feedback resistor at the input of the LNA and  $Z_{eq}$  is the Thevenin's equivalent resistance as seen from the source. As can be observed in (17), to achieve a low NF, the value of  $Z_{eq}$  should be as low as possible. From the expression of  $Z_{eq}$  given in (18), it is



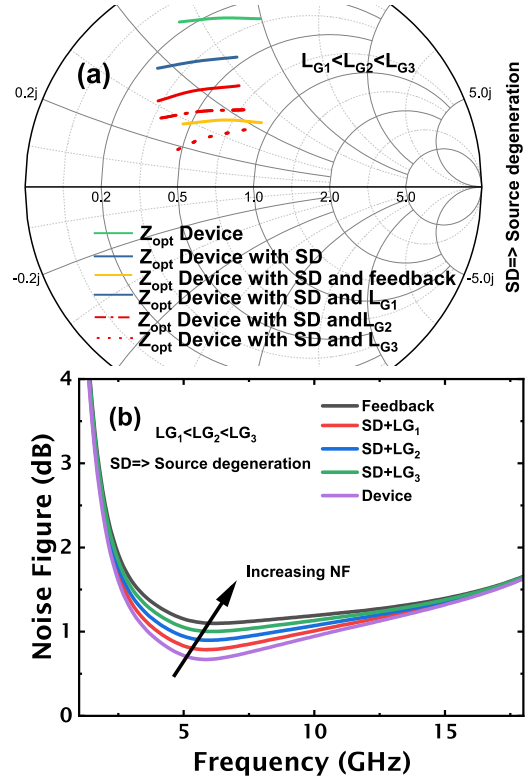
**FIGURE 4.** Small signal equivalent circuit of the LNA MMIC to derive the feedback resistor's dependence on the LNA's gain.



**FIGURE 5.** Small signal equivalent schematic of the resistive feedback inductive source degenerated low noise amplifier for noise calculation. The internal parasitics of the device have not been considered.

evident that as the value of  $R_1$  is increased or the feedback is reduced, the value of  $Z_{eq}$  reduces. Thus, it is important to avoid feedback for achieving a low overall NF of the LNA. This fact is also proven by plotting the  $Z_{opt}$  of the common source LNA on a Smith chart shown in Fig. 6 (a). The value  $Z_{opt}$  moves closer to the center of the Smith chart for either feedback or a high value of gate inductor. However, from Fig. 6 (b) it is evident that the value of NF increases much more when feedback is used than a high input inductor value. The analysis suggests that for stability and the lowest NF, it is better to leverage internal resistances in the gate and drain inductors rather than feedback. Removing resistive feedback simplifies the LNA's design and improves its NF.

$$F = 1 + \frac{1}{R_S} \left\{ R_{GL} + R_{SL} + |Z_{eq}|^2 \frac{|i_g^2|}{4kT\Delta f} + \left| \frac{1 + j\omega C_{gs} Z_{eq}}{g_m} \right|^2 \frac{|i_d^2|}{4kT\Delta f} - 2 \operatorname{Re} \left[ Z_{eq} \left( \frac{1 + j\omega C_{gs} Z_{eq}}{g_m} \right)^* \frac{i_g^* i_d}{4kT\Delta f} \right] \right\} \quad (17)$$



**FIGURE 6.** (a)  $Z_{opt}$  of the LNA for the first stage for different variations of the device from 5-8 GHz. The plot shows that a high-value inductor at the input provides similar characteristics of  $Z_{opt}$  as feedback can achieve. (b) Shows the variation of the minimum NF of the LNA for different variations of the device. The plot shows that the NF for the topology with feedback is the worst.

The value of  $Z_{eq}$  is derived separately for the resistive feedback topology shown in Fig. 2 as:

$$Z_{eq} = R_S + R_{GL} + \frac{\omega^2 R_1 R_{SL} L_S^2}{(R_1 + R_S)^2 + \omega^2 L_S^2} + j\omega \left[ L_G \frac{R_1 R_{SL} L_S}{(R_1 + R_{SL})^2 + \omega^2 L_S^2} \right] \quad (18)$$

$Z_{eq}$  is the equivalent impedance of the circuit shown in Fig. 5 seen from the source. And,  $i_g$  and  $i_d$  can be written as:

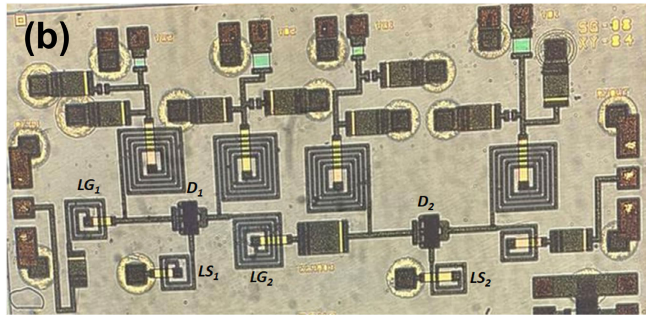
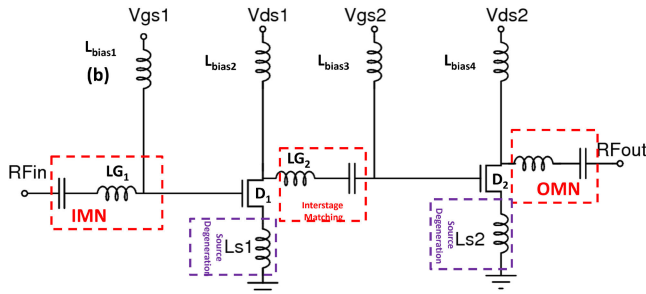
$$|i_g^2| = R \frac{\omega^2 C_{gs}^2}{g_m} 4kT\Delta f \quad (19)$$

$$|i_d^2| = P g_m 4kT\Delta f \quad (20)$$

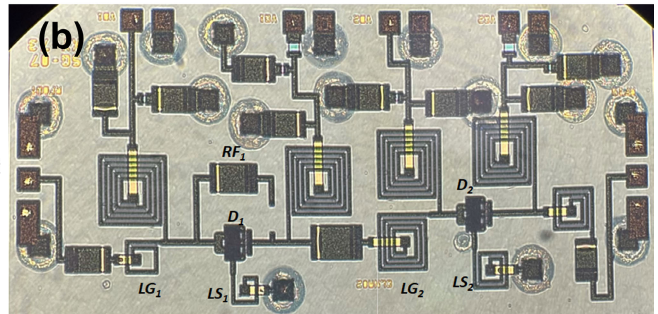
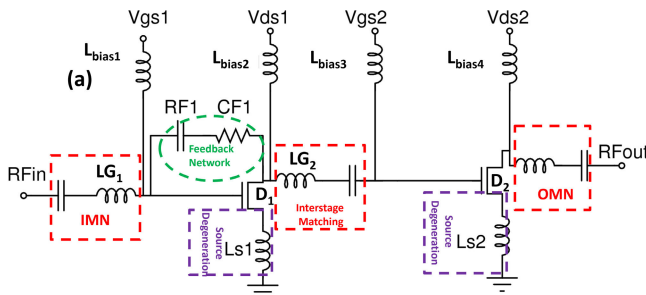
where R and P are the coefficients of gate and drain noise, respectively.

$$Z_{in} = \frac{-\omega^2 C_{gs} (L_{G1} + R_{GL}) - (1 + j\omega (L_{S1} + R_{SL}) g_m - \omega^2 (L_{S1} + R_{SL}) C_{gs})}{j\omega C_{gs}} \quad (9)$$

$$Z_{in} = \frac{-\omega^2 C_{gs} (L_{G1} + R_{GL}) - (1 + j\omega (L_{S1} + R_{SL}) g_m - \omega^2 (L_{S1} + R_{SL}) C_{gs}) \left( \frac{j\omega (L_{G1} + R_{GL})}{R_1} + 1 \right)}{j\omega C_{gs} + \frac{1 + j\omega g_m (L_{S1} + R_{SL}) - \omega^2 (L_{S1} + R_{SL}) C_{gs}}{R_1}} \quad (10)$$



**FIGURE 7.** (a) Schematic of the designed C-band LNA MMIC having a high value of input inductor but no feedback. (b) Micrograph of the fabricated C-band MMIC LNA having a high value of input inductor but no feedback. The total chip size was  $3.2 \times 1.6 \text{ mm}^2$ .



**FIGURE 8.** (a) Schematic of the designed C-band LNA MMIC having a low value of input inductor but with feedback. (b) Micrograph of the fabricated C-band LNA MMIC having a low value of input inductor but with feedback. The total chip size was  $3.2 \times 1.6 \text{ mm}^2$ .

**TABLE 2.** Comparison table showing the various components and vital parameters of the two fabricated LNA MMICs.

	LNA1	LNA2
$LG_1$ (nH)	0.79	0.54
$LS_1$ (nH)	0.64	0.52
$D_1$ ( $\mu\text{m}$ )	$4 \times 75$	$4 \times 75$
$LG_2$ (nH)	1.03	1.09
$LS_2$ (nH)	0.56	0.58
$D_2$ ( $\mu\text{m}$ )	$4 \times 75$	$4 \times 75$
$S_{11}$ (dB)	$< -8$	$< -8$
$S_{22}$ (dB)	$< -10$	$< -10$
Gain (dB)	16	15
NF (dB)	1.3	1.5

#### IV. RESULTS AND DISCUSSION

In this section, we analyze the performance of the two fabricated LNAs. Fig. 7 shows the schematic and micrograph of the fabricated LNA without feedback (LNA1), using  $0.25 \mu\text{m}$  GaN technology and Fig. 8 shows the schematic and micrograph of the fabricated LNA with feedback (LNA2). Both the LNAs use LPF matching networks for input matching. The LPF matching is the simplest matching network comprising a capacitor and a series inductor. Since the device is inherently capacitive, the inductor of the LPF helps in canceling the reactive part of the device, which further leads to a good matching at the input. The measurements are performed using a DC probe card specifically designed to measure the intended LNA. Since stability is an essential part

of the design of commercial amplifiers (usually defined by their  $K$  - factor and  $\mu$  - factor values) [31], it is imperative to ensure the stability of the designed LNAs. The designed amplifiers have an overall stability factor of  $K > 1$  and  $\mu > 0$  from DC - 18 GHz as can be seen from Fig. 9 (c) and Fig. 10 (c), respectively.

S-parameter measurements are done from 5-7 GHz with a 100 MHz step size using Keysight PNA-X N5244A. The device in the first stage of the first LNA1 is biased at an operating point  $V_{gs}$ ,  $V_{ds}$ , and  $I_{ds}$  of  $-4 \text{ V}$ ,  $10 \text{ V}$ , and  $48 \text{ mA}$ , respectively. The device for the second stage of the first LNA is biased at an operating point  $V_{gs}$ ,  $V_{ds}$ , and  $I_{ds}$  of  $-3 \text{ V}$ ,  $10 \text{ V}$ , and  $96 \text{ mA}$ , respectively. The device in the second stage has a slightly higher drain current as the second stage mainly contributes to the overall gain of the LNA.

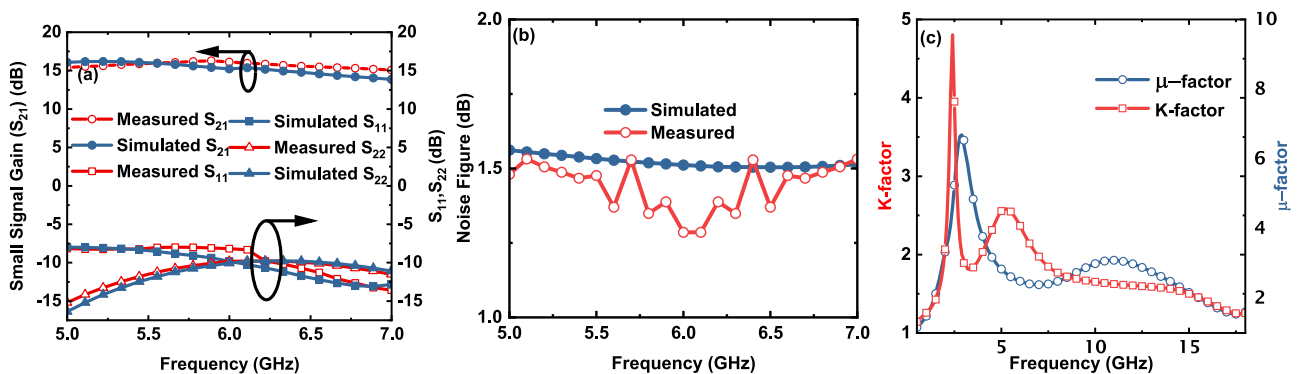
Fig. 9 (a) depicts the comparison of the simulated and measured S-parameters. As can be seen from Fig. 9 (a) the LNA1 has a gain greater than 15 dB with a deviation of  $\pm 1 \text{ dB}$ , an input and output return loss of greater than 10 dB for a frequency range of 5-7 GHz.

Further, on-wafer noise measurements are done for a frequency range of 5-7 GHz with a step size of 100 MHz. Fig. 9 (b) compares the simulated and measured NF for the specified frequency range. The simulated and measured NF are in close agreement with each other. The minimum measured NF is 1.3 dB at a frequency of 6 GHz.

The device in the first stage of the second LNA2 was biased at an operating point  $V_{gs}$ ,  $V_{ds}$ , and  $I_{ds}$  of  $-4 \text{ V}$ ,  $10 \text{ V}$ , and  $48 \text{ mA}$ , respectively. The device for the second stage of the

**TABLE 3.** Performance analysis of our proposed LNAs with other state-of-the-art contemporary LNA designs operating in C-Band.

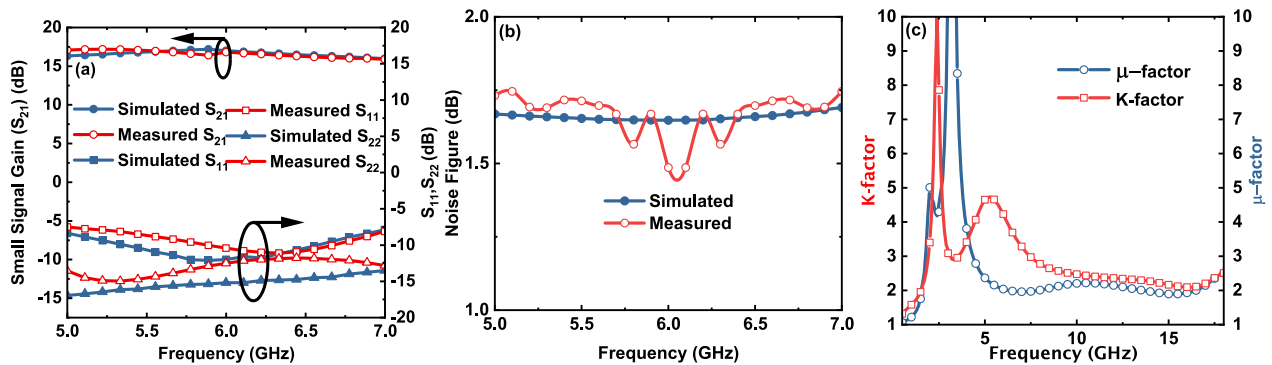
References	Frequency (GHz)	NF (dB)	Gain (dB)	IRL/ORL (dB)	Topology	Process	Area (mm <sup>2</sup> )
[37]	2.4/5	2	17	>10	1-stage	0.15μm p-HEMT	1
[38]	3.1-10.6	>2	>15	>8	-	0.18μm CMOS	1.6
[39]	2-12	>3	16.5-19.5	>10	CG-CS	40nm CMOS	0.092
[40]	2.2/5.5	3.1	11	>10	2-stage cascaded	0.18μm CMOS	-
[41]	1-12.5	1.5-2.4	23.6	>8	2-stage cascaded	0.15μm GaAs pHEMT	0.75
[42]	2-40	2-2.6	15.2	>6	3-stage distributed	0.15μm GaAs pHEMT	1.88
[43]	0.1-20	3.1-5.8	28.6	>10	3-stage cascode	0.15μm GaAs pHEMT	1.53
[44]	0.1-23	2.7-4	27.4	>5	3-stage cascode	0.15μm GaAs pHEMT	1.36
[45]	0.1-12.3	1.9-3.5	12.3	>8	1-stage CG-CS	GaAs HBT	1.07
[46]	3.2-14.7	1.3-2.5	34	>5	3-stage CS with FB	0.15μm GaAs pHEMT	2
[47]	4-42.5	3.6	13	>6	cascode	0.25μm GaAs HEMT	2.4
[48]	8-12	1.5-2.8	18	>6	2-stage cascaded	0.25μm GaAs HEMT	1.21
[49]	6.5-16.5	2	12.5	>6	2-stage cascaded	0.25μm GaAs HEMT	-
[50]	5-6	2.4	31	>5	3-stage CS with FB	0.25μm GaN HEMT	NA
[51]	5.7-6.7	3.2	8	>5	3-stage CS with FB	0.25μm GaN HEMT	12
[52]	5-6	5.5	12	>5	3-stage CS with FB	0.25μm GaN HEMT	49
This work (LNA1)	5-7	1.3-1.5	15	>8	2-stage cascaded	0.25μm GaN HEMT	5.1
This work (LNA2)	5-7	1.5-1.7	16	>8	2-stage cascaded	0.25μm GaN HEMT	5.1



**FIGURE 9.** Simulated and on-wafer measured performance of the C-band GaN MMIC LNA without feedback (LNA1) (a) S-parameters, (b) NF, and (c) Stability factor (K-factor and μ-factor). The on-wafer noise measurements are done using a dedicated probe card. The minimum NF for this LNA is 1.3 dB @ 6GHz.

first LNA was biased at an operating point  $V_{gs}$ ,  $V_{ds}$ , and  $I_{ds}$  of -3V, 10 V, and 96 mA, respectively.

Fig. 10 (a) depicts the comparison of the simulated and measured S-parameters and Noise figures, respectively.



**FIGURE 10.** Simulated and on-wafer measured performance of the C-band GaN MMIC LNA with feedback (LNA2) (a) S-parameters, (b) NF, and (c) Stability factor (K-factor and  $\mu$ -factor). The on-wafer noise measurements are done using a dedicated probe card. The minimum NF for this LNA is 1.5 dB @ 6GHz.

As can be seen from Fig. 10 (a) the LNA2 has a gain greater than 16 dB with a deviation of  $\pm 1$  dB, and input return loss of greater than 10 dB for a frequency of 5-7 GHz.

Fig. 10 (b) compares the simulated and measured NF for the specified frequency range. The simulated and measured NF are in close agreement with each other. The minimum measured NF is 1.5 dB at a frequency of 6 GHz.

As can be seen from Fig. 9 (b) and Fig. 10 (b) there are fluctuations in the measured NF of the LNA. Measured S-parameter and noise data served as the foundation for the design of the LNA that was carried out in this work. It is important to note that the wafer that is measured for standalone devices is distinct from the wafer that was measured for circuits. There are differences between the estimated model of the device and the real device. These differences are caused by variances in the process as well as different wafers. Because of this, the model tends to underestimate the data at some locations. This is the reason that at some point in the plot, the NF of the fabricated LNA is better than the simulated LNA.

Table 2 lists the values of the various matching parameters used for the implementation of the two LNAs MMIC. Table 2 also displays the different measured parameters at a frequency of 6 GHz. It is evident from Table 2 that the LNA without feedback (LNA1) has a better noise performance in terms of NF. LNA1 has an improvement of 0.2 dB in the overall NF as compared to LNA2. Table 3 shows a detailed comparative performance analysis of the state-of-the-art LNAs from the literature with the designed LNAs. The designed LNAs achieved competitive RF performance. As can be seen from Table 3 the designed LNAs provide the best gain and NF for other GaN-based LNAs designed for the same frequency range. Thus, it can be inferred that by properly leveraging the inherent lossy nature of the matching components one can achieve a better NF with sufficient gain.

## V. CONCLUSION

In this study, we successfully designed and fabricated two distinct LNAs, leveraging the inherent lossy nature of input-matching components. This novel approach eliminated the conventional necessity for a feedback network,

simplifying the overall design. Our analytical investigation underscored that the integration of a high inductor value in the input matching network and the employment of source degeneration over feedback not only reduces complexity but also notably improves the NF. Moreover, this strategy illuminated the possibility of achieving simultaneous gain and noise matching. Utilizing 0.25  $\mu\text{m}$  GaN technology for fabrication, the proposed LNAs have showcased state-of-the-art performance, laying a robust foundation for future advancements in low-noise amplifier design.

## ACKNOWLEDGMENT

The authors would like to thank the entire fabrication and characterization team from DRDO-SSPL, Delhi, and GAETECH, Hyderabad, for fabricating, measuring, and characterizing all the devices and circuits. They would also like to thank Raghvendra Dangi from the Nano-Laboratory, IIT Kanpur, for his helpful contributions throughout the project.

## REFERENCES

- [1] D. Choudhury, "5G wireless and millimeter wave technology evolution: An overview," in *IEEE MTT-S Int. Microw. Symp. Dig.*, May 2015, pp. 1–4.
- [2] M. Zada, I. A. Shah, and H. Yoo, "Integration of sub-6-GHz and mm-wave bands with a large frequency ratio for future 5G MIMO applications," *IEEE Access*, vol. 9, pp. 11241–11251, 2021.
- [3] J. J. M. Rubio, R. Quaglia, A. Piacibello, V. Camarchia, P. J. Tasker, and S. Cripps, "3–20-GHz GaN MMIC power amplifier design through a COU compensation strategy," *IEEE Microw. Wireless Compon. Lett.*, vol. 31, no. 5, pp. 469–472, May 2021.
- [4] S. Shinjo, K. Nakatani, K. Tsutsumi, and H. Nakamizo, "Integrating the front end: A highly integrated RF front end for high-SHF wide-band massive MIMO in 5G," *IEEE Microw. Mag.*, vol. 18, no. 5, pp. 31–40, Jul. 2017.
- [5] D. Pepe, I. Chlis, and D. Zito, "Transformer-based input integrated matching in cascode amplifiers: Analytical proofs," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 65, no. 5, pp. 1495–1504, May 2018.
- [6] E. Limiti, W. Ciccognani, and S. Colangeli, "Characterization and modeling of high-frequency active devices oriented to high-sensitivity subsystems design," in *Microwave De-Embedding*, G. Crupi and D. M.-P. Schreurs, Eds. Oxford, U.K.: Academic Press, 2014, ch. 3, pp. 97–150. [Online]. Available: <https://www.sciencedirect.com/science/article/pii/B9780124017009000033>
- [7] Y. Wang, J. Duster, and K. Kornegay, "Design of an ultra-wideband low noise amplifier in 0.13  $\mu\text{m}$  CMOS," in *Proc. IEEE Int. Symp. Circuits Syst.*, Jun. 2005, pp. 5067–5070.
- [8] S. Joo, T.-Y. Choi, and B. Jung, "A 2.4-GHz resistive feedback LNA in 0.13- $\mu\text{m}$  CMOS," *IEEE J. Solid-State Circuits*, vol. 44, no. 11, pp. 3019–3029, Nov. 2009.



- [9] S. Zandian, H. Khosravi, and A. Bijari, "Design and heuristic optimization of a CMOS LNA for ultra-wideband receivers," in *Proc. 27th Iranian Conf. Electr. Eng. (ICEE)*, Apr. 2019, pp. 243–248.
- [10] H. Khosravi, A. Bijari, N. Kandalafi, and J. Cabral, "A low power concurrent dual-band low noise amplifier for WLAN applications," in *Proc. IEEE 10th Annu. Inf. Technol., Electron. Mobile Commun. Conf.*, Oct. 2019, pp. 1118–1123.
- [11] S.-E. Shih, W. R. Deal, D. M. Yamauchi, W. E. Sutton, W.-B. Luo, Y. Chen, I. P. Smorchkova, B. Heying, M. Wojtowicz, and M. Siddiqui, "Design and analysis of ultra wideband GaN dual-gate HEMT low-noise amplifiers," *IEEE Trans. Microw. Theory Techn.*, vol. 57, no. 12, pp. 3270–3277, Dec. 2009.
- [12] U. K. Mishra, P. Parikh, and Y.-F. Wu, "AlGaIn/GaN HEMTs—An overview of device operation and applications," *Proc. IEEE*, vol. 90, no. 6, pp. 1022–1031, Jun. 2002.
- [13] U. K. Mishra, S. Likun, T. E. Kazior, and Y.-F. Wu, "GaN-based RF power devices and amplifiers," *Proc. IEEE*, vol. 96, no. 2, pp. 287–305, Feb. 2008.
- [14] A. U. H. Pampori, S. A. Ahsan, R. Dangi, U. Goyal, S. K. Tomar, M. Mishra, and Y. S. Chauhan, "Modeling of bias-dependent effective velocity and its impact on saturation transconductance in AlGaIn/GaN HEMTs," *IEEE Trans. Electron Devices*, vol. 68, no. 7, pp. 3302–3307, Jul. 2021.
- [15] A. U. H. Pampori, S. A. Ahsan, and Y. S. Chauhan, "Modeling the impact of dynamic fin-width on the I–V, C–V and RF characteristics of GaN fin-HEMTs," *IEEE Trans. Electron Devices*, vol. 69, no. 5, pp. 2275–2281, May 2022.
- [16] M. S. Nazir, P. Kushwaha, A. Pampori, S. A. Ahsan, and Y. S. Chauhan, "Electrical characterization and modeling of GaN HEMTs at cryogenic temperatures," *IEEE Trans. Electron Devices*, vol. 69, no. 11, pp. 6016–6022, Nov. 2022.
- [17] M. Zaid, A. Pampori, R. Dangi, and Y. Singh Chauhan, "S-band GaN based power amplifier with symmetric matching network," in *Proc. IEEE 9th Uttar Pradesh Sect. Int. Conf. Electr., Electron. Comput. Eng. (UPCON)*, Dec. 2022, pp. 1–4.
- [18] M. Zaid, A. Pampori, and Y. S. Chauhan, "16 Watt S-band GaN based power amplifier using replicating stages," in *Proc. IEEE 9th Uttar Pradesh Sect. Int. Conf. Electr., Electron. Comput. Eng. (UPCON)*, Dec. 2022, pp. 1–4.
- [19] S. Colangeli, A. Bentini, W. Ciccognani, E. Limiti, and A. Nanni, "GaN-based robust low-noise amplifiers," *IEEE Trans. Electron Devices*, vol. 60, no. 10, pp. 3238–3248, Oct. 2013.
- [20] S. Mao, R. Xu, B. Yan, and Y. Xu, "An improved noise modeling method using a quasi-physical zone division model for AlGaIn/GaN HEMTs," *IEEE Trans. Electron Devices*, vol. 70, no. 4, pp. 1835–1842, Apr. 2023.
- [21] S. Shekhar, J. S. Walling, S. Aniruddhan, and D. J. Allstot, "CMOS VCO and LNA using tuned-input tuned-output circuits," *IEEE J. Solid-State Circuits*, vol. 43, no. 5, pp. 1177–1186, May 2008.
- [22] Ç. Yagbasan and A. Aktug, "Robust X-band GaN LNA with integrated active limiter," in *Proc. 13th Eur. Microw. Integr. Circuits Conf. (EuMIC)*, Sep. 2018, pp. 237–240.
- [23] C. Trantarella and P. Blount, "Low noise GaN amplifiers with inherent overdrive protection," *Microw. J.*, vol. 58, pp. 78–88, Dec. 2015.
- [24] A. M. E. Abounemra, M. Helaoui, and F. M. Ghannouchi, "A high gain and high linear 0.25  $\mu\text{m}$  GaN HEMT based monolithic integrated C-band low noise amplifier," in *Proc. IEEE Int. Electromagn. Antenna Conf. (IEMANTENNA)*, Oct. 2019, pp. 016–019.
- [25] L. Pace, S. Colangeli, W. Ciccognani, P. E. Longhi, E. Limiti, R. Leblanc, M. Feudale, and F. Vitobello, "Design and validation of 100 nm GaN-On-Si Ka-band LNA based on custom noise and small signal models," *Electronics*, vol. 9, no. 1, p. 150, 2020. [Online]. Available: <https://www.mdpi.com/2079-9292/9/1/150>
- [26] C.-T. Fu, C.-N. Kuo, and S. S. Taylor, "Low-noise amplifier design with dual reactive feedback for broadband simultaneous noise and impedance matching," *IEEE Trans. Microw. Theory Techn.*, vol. 58, no. 4, pp. 795–806, Apr. 2010.
- [27] S. A. Saleh, M. Ortmanns, and Y. Manoli, "A comparative study of CMOS LNAs," in *Proc. 18th Eur. Conf. Circuit Theory Design*, Aug. 2007, pp. 76–79.
- [28] W. Chang, G.-I. Jeon, Y.-R. Park, S. Lee, and J.-K. Mun, "X-band low noise amplifier MMIC using AlGaIn/GaN HEMT technology on SiC substrate," in *Proc. Asia-Pacific Microw. Conf.*, Nov. 2013, pp. 681–684.
- [29] S. T. Nicolson and S. P. Voinescu, "Methodology for simultaneous noise and impedance matching in W-band LNAs," in *Proc. IEEE Compound Semiconductor Integr. Circuit Symp.*, Nov. 2006, pp. 279–282.
- [30] M. Thompson and J. K. Fidler, "Determination of the impedance matching domain of impedance matching networks," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 51, no. 10, pp. 2098–2106, Oct. 2004.
- [31] B. Razavi, *RF Microelectronics* (Communications Engineering and Emerging Technologies Series). Upper Saddle River, NJ, USA: Prentice-Hall, 2011.
- [32] D. M. Pozar, *Microwave Engineering*, 3rd ed. Hoboken, NJ, USA: Wiley, 2005. [Online]. Available: <https://cds.cern.ch/record/882338>
- [33] N. Bajpai, P. Maity, M. Shah, A. Das, and Y. S. Chauhan, "An ultra-low noise figure and multi-band re-configurable low noise amplifier," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 70, no. 3, pp. 1006–1016, Mar. 2023.
- [34] B. Razavi, *Design of Analog CMOS Integrated Circuits*. Boston, MA, USA: McGraw-Hill, 2003.
- [35] X. Bi, Z. Feng, S. Guan, Z. Cao, Y. Mei, J. Li, Z. Zhang, and Q. Xu, "An L- and C-band radiometer utilizing distributed active hot and cold loads with 156% fractional bandwidth," *IEEE Trans. Microw. Theory Techn.*, vol. 70, no. 3, pp. 1841–1855, Mar. 2022.
- [36] Y.-J. Lin, S. S. H. Hsu, J.-D. Jin, and C. Y. Chan, "A 3.1–10.6 GHz ultra-wideband CMOS low noise amplifier with current-reused technique," *IEEE Microw. Wireless Compon. Lett.*, vol. 17, no. 3, pp. 232–234, Mar. 2007.
- [37] Z. Liu and C. C. Boon, "A 0.092-mm<sup>2</sup> 2–12-GHz noise-cancelling low-noise amplifier with gain improvement and noise reduction," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 69, no. 10, pp. 4013–4017, Oct. 2022.
- [38] J.-X. Chou, C.-H. Wei, and Y.-S. Lin, "Compact dual-band LNA design using a bridged-T coil-based matching network," in *Proc. IEEE Int. Symp. Radio-Freq. Integr. Technol. (RFIT)*, Aug. 2021, pp. 1–3.
- [39] X. Yan, J. Zhang, H. Luo, S.-P. Gao, and Y. Guo, "A compact 1.0–12.5-GHz LNA MMIC with 1.5-dB NF based on multiple resistive feedback in 0.15- $\mu\text{m}$  GaAs pHEMT technology," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 70, no. 4, pp. 1450–1462, Apr. 2023.
- [40] G. Nikandish and A. Medi, "A 40-GHz bandwidth tapered distributed LNA," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 65, no. 11, pp. 1614–1618, Nov. 2018.
- [41] K.-P. Ahn, R. Ishikawa, and K. Honjo, "Low noise group delay equalization technique for UWB InGaP/GaAs HBT LNA," *IEEE Microw. Wireless Compon. Lett.*, vol. 20, no. 7, pp. 405–407, Jul. 2010.
- [42] J. Hu, K. Ma, S. Mou, and F. Meng, "Analysis and design of a 0.1–23 GHz LNA MMIC using frequency-dependent feedback," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 66, no. 9, pp. 1517–1521, Sep. 2019.
- [43] J. Hu, K. Ma, S. Mou, and F. Meng, "A seven-octave broadband LNA MMIC using bandwidth extension techniques and improved active load," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 65, no. 10, pp. 3150–3161, Oct. 2018.
- [44] Y. Wang, C.-C. Chiong, J.-K. Nai, and H. Wang, "A high gain broadband LNA in GaAs 0.15- $\mu\text{m}$  pHEMT process using inductive feedback gain compensation for radio astronomy applications," in *Proc. IEEE Int. Symp. Radio-Frequency Integr. Technol. (RFIT)*, Aug. 2015, pp. 79–81.
- [45] M. Sakalas and P. Sakalas, "Design of a wideband, 4–42.5 GHz low noise amplifier in 0.25  $\mu\text{m}$  GaAs pHEMT technology," in *Proc. IEEE BiCMOS Compound Semiconductor Integr. Circuits Technol. Symp. (BCICTS)*, Nov. 2020, pp. 1–4.
- [46] M. He, Y. Peng, and B. Li, "A reconfigurable low noise amplifier for X/Ku band," in *Proc. Int. Conf. Microw. Millim. Wave Technol. (ICMMT)*, May 2018, pp. 1–3.
- [47] L. He, J. Hu, and B. Gao, "A 6.5–16.5 GHz low noise amplifier based on GaAs pHEMT," in *Proc. IEEE 3rd Int. Conf. Circuits Syst. (ICCS)*, Oct. 2021, pp. 144–149.
- [48] K.-C. He, M.-T. Li, C.-M. Li, and J.-H. Tarn, "Parallel-RC feedback low-noise amplifier for UWB applications," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 57, no. 8, pp. 582–586, Aug. 2010.
- [49] R. Giofrè, W. Ciccognani, S. Colangeli, M. Feudale, C. Lanzieri, G. Polli, A. Salvucci, A. Suriani, M. Vittori, and E. Limiti, "A C-band GaN single chip front-end for SAR applications," in *Proc. IEEE Radio Wireless Symp. (RWS)*, Jan. 2020, pp. 162–164.
- [50] C. Andrei, O. Bengtsson, R. Doerner, S. A. Chevtchenko, and M. Rudolph, "Robust stacked GaN-based low-noise amplifier MMIC for receiver applications," in *IEEE MTT-S Int. Microw. Symp. Dig.*, May 2015, pp. 1–4.



**MOHAMMAD ZAID** (Member, IEEE) received the B.Tech. and M.Tech. degrees in electronic engineering from the Zakir Hussain College of Engineering and Technology, Aligarh Muslim University. He is currently pursuing the Ph.D. degree with Indian Institute of Technology Kanpur (IIT Kanpur), specializing in the field of RF circuit design, with a particular emphasis on GaN-based power amplifier design. In power amplifier design, his research primarily focuses on creating highly efficient and reliable GaN-based power amplifiers. In low noise amplifier design, his designs strive to reduce the NF. His current research interest includes significant advancements in RF circuit design.



**PURNIMA KUMARI** received the B.Tech. degree from NIT Allahabad and the M.Tech degree from Indian Institute of Technology (IIT) Delhi, showcasing her exceptional academic prowess. She is currently a Distinguished Scientist with the Solid State Physics Laboratory (SSPL), a prominent research and development establishment under the Defense Research and Development Organization (DRDO), India.



**AHTISHAM PAMPORI** (Member, IEEE) received the bachelor's degree in electronics and communications engineering from NIT Srinagar. He is currently pursuing the Ph.D. degree with Indian Institute of Technology Kanpur (IIT Kanpur), with a focus on the characterization and modeling of GaN HEMT RF devices. He is a Postdoctoral Researcher with UC Berkeley under Prof. Chenming Hu. His research interests include modeling and characterization of GaN HEMTs and their applications in RF systems. He was a recipient of the prestigious Prime Minister's Research Fellowship (PMRF).



**MOHAMMAD SAJID NAZIR** (Member, IEEE) received the bachelor's degree in electronics and communication engineering from NIT Srinagar. He is currently pursuing the Ph.D. degree with Indian Institute of Technology Kanpur (IIT Kanpur). His research interests include GaN modeling, characterization, and design of circuits for RF applications. He was a recipient of the prestigious Prime Minister's Research Fellowship (PMRF).



**UMAKANT GOYAL** (Member, IEEE) received the B.Tech. degree (Hons.) in electronics and electrical communication engineering from IIT Kharagpur, in 2003, and the M.E. degree in microelectronics from IISc Bengaluru, in 2009. In 2003, he joined the Defence Research and Development Organization (DRDO) as a Sc-B. He is currently a Senior Scientist with the Solid State Physics Laboratory (SSPL), DRDO. He is working in the field of high-power GaAs and GaN-based MMIC design catering frequency applications up to the Ku band. His research interests include device modeling and PDK development. He was a recipient of the Alumni Gold Medal from IISc Bengaluru.



**MEENA MISHRA** received the M.Sc. degree in electronics from Jamia Millia Islamia and the Ph.D. degree in artificial neural network modeling of pseudomorphic high electron mobility transistor (PHEMT). She is currently a Distinguished Scientist and the Visionary Director with the Solid State Physics Laboratory (SSPL), Defence Research and Development Organization (DRDO), with a prolific career dedicated to the advancement of high-frequency device design and the meticulous development of low noise amplifiers. Her illustrious journey in the realm of technology and electronics has been punctuated by significant contributions that have left an indelible mark on the field. This groundbreaking research has been instrumental in redefining the boundaries of high-frequency device design and amplification techniques.



**YOGESH SINGH CHAUHAN** (Fellow, IEEE) is currently a Professor with Indian Institute of Technology Kanpur, India. He is also the developer of several industry-standard models, such as the ASM-HEMT Model, BSIM-BULK (formerly BSIM6), BSIM-CMG, BSIM-IMG, BSIM4, and BSIM-SOI Models. His research group is involved in developing compact models for GaN transistors, FinFET, Nanosheet/Gate-All-Around FETs, FDSOI transistors, Negative Capacitance FETs, and 2D FETs. He has published more than 250 papers in international journals and conferences. His research interests include characterization, modeling, and simulation of semiconductor devices. He is a member of Indian National Young Academy of Science (INYNAS). He is the Founding Chairperson of the IEEE Electron Devices Society U.P. Chapter. He received the Ramanujan Fellowship, in 2012, the IBM Faculty Award, in 2013, the P. K. Kelkar Fellowship, in 2015, the CNR Rao Faculty Award, the Humboldt Fellowship, and the Swarnajayanti Fellowship, in 2018. He is the Chair of the IEEE-EDS Compact Modeling Technical Committee. He has served in the technical program committees of the IEEE International Electron Devices Meeting (IEDM), IEEE International Conference on Simulation of Semiconductor Processes and Devices (SISPAD), IEEE European Solid-State Device Research Conference (ESSDERC), IEEE Electron Devices Technology and Manufacturing (EDTM), IEEE International Conference on VLSI Design, and International Conference on Embedded Systems. He is an Editor of IEEE TRANSACTIONS ON ELECTRON DEVICES and the Distinguished Lecturer of the IEEE Electron Devices Society.

...