IEEE Access
Multidisciplinary | Rapid Review | Open Access Journal

Received 20 March 2024, accepted 2 April 2024, date of publication 9 April 2024, date of current version 18 April 2024.

Digital Object Identifier 10.1109/ACCESS.2024.3386747

RESEARCH ARTICLE

A Single Source Quadruple Boost Nine-Level Switched-Capacitor Inverter With Reduced Components and Continuous Input Current

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ABSTRACT The multilevel inverter (MLI) serves as a pivotal class of power electronic converters, well-suited for high-power applications at medium voltage levels, ensuring superior power quality. While designing an MLI, there is a motif among the number of components, voltage stress on the semiconductor devices, and its voltage-boosting ability. A single source nine-level switched-capacitor based novel inverter with reduced components has been proposed in this paper. The proposed H-bridge based switched capacitor inverter topology employs nine switches, two capacitors, two diodes, and one DC source. The inverter has a quadruple voltage boost and the ability to draw continuous input current from the DC supply and self-voltage balance with a voltage ripple of less than 5%. A comprehensive study of performance parameters, design consideration, and loss analysis of the proposed inverter is also incorporated. A level-shifted pulse width modulation technique is implemented to operate the inverter for unity to 0.5 lagging load power factors and $1 - 0.2$ modulation indices. The dynamic responses of the proposed switched capacitor inverter topology are obtained through MATLAB simulation for analysis and further validated by hardware prototype.

INDEX TERMS Continuous input current, reduced components, switched capacitor, voltage stress, voltage boost.

I. INTRODUCTION

Multilevel inverters (MLIs) are employed in various applications of medium and high power systems like electric drive systems, grid interface, static reactive power compensation, HVDC transmission, electric vehicle, renewable energy, active power filter [1]. MLIs provide almost sinusoidal output voltage, which includes lesser total harmonic distortion. Therefore, the size of the required filter at the output reduces the system's overall size and cost. The voltage stresses on the switches and diodes are also lower due to the higher number of small voltage steps. At the same time rate of change of voltage, i.e., $\frac{dv}{dt}$, is also lesser, which reduces the effects of parasitic capacitance in the device [2]. Moreover, MLI can operate at a lower switching frequency (in the kilohertz range), reducing switching losses and electromagnetic interference.

In recent times, switched-capacitor-based multilevel inverters (SC-MLIs) have gained attention over other types of multilevel inverters because of their ability to self-balance the capacitors' voltage, increase voltage gain, and reduce the required DC sources. Several SC-MLIs have been developed that address these features in [2], [3], [4], [5], [6], [7], [8], [9], [10], [11], [12], [13], [14], [15], [16], [17], [18], [19], [20], [21], [22], [23], [24], [25], [26], [27], [28], and [29]. The three-level inverter reported in [3] and [4] draws the continuous input current from the DC supply. However, they have incorporated an additional inductor, capacitor, and

The associate editor coordinating the review of this manuscript and approving it for publication was Poki Chen.

switch to achieve the continuous current. In [2], a five-level inverter with nine switches and one capacitor has been developed. This inverter possesses duplex voltage gain. The seven-level inverters have been discussed in [5], [6], [7], and [8] and incorporated three capacitors. In [5], the charging time of the capacitors has been made independent of the load. The authors in [6] have developed the inverter by cascading a five-level ANPC inverter and a three-level T-type converter (TTC). The voltage gain of 1.5 has been achieved by integrating the TTC with the H-bridge in [7] and the new ANPC inverter in [8]. Another seven-level inverter has been developed to reduce current stress in [9], which has incorporated one additional half-bridge with an inductor that increases the component count.

References [10], [11], [12], [13], [14], [15], [16], [17], [18], [19], [20], [21], [22], [23], [24], [25], [26], [27], and [28] address the nine-level switched-capacitor (SC) inverters. In [10], the SC-based cascaded MLI has been developed to reduce the spike in the capacitors' current. However, it employs fourteen switches and four capacitors with an auxiliary circuit for charging the SCs. Twelve switches have been incorporated in developing nine-level inverters in [11], [12], and [13]. Based on eleven switches, nine-level inverters have been designed in [14], [15], [16], and [17]. The number of switches has been further reduced by one in [18], [19], and [20] i.e., only ten switches. Nine switches have been employed in [21], [22], and [23] to design the nine-level inverters but at the cost of more diodes and capacitors. The nine-level inverter topology reported in [24], [25], and [26] employs only eight switches while the voltage gain is just twofold to the input voltage. References [27] and [28] are able to develop nine-level output with quadrupled voltage gain. Nevertheless, two out of eight switches are bidirectional switches in [27] and have higher component counts, including diodes and capacitors in [28].

Therefore, a nine-level inverter topology with the following key contributions has been presented in this paper.

1) Lesser number of components employed
2) Quadruple voltage boosting
3) Better DC utilization as the input current is continuous
4) Operate under a wider range of load power factors
5) Operate for a wide variation of modulation index
6) Satisfactory operation under a dynamic change in load or input sides
7) Lesser capacitors' voltage ripple
8) Better efficiency

The remnant of the paper is organized as follows: The proposed topology's operation and control strategy are presented in Section II. Design and Description have been discussed in section III. A detailed analysis and comparison with the existing topology are included in section IV. Thereafter, Section V addresses the obtained results and their discussion. The article ended in section VI with the conclusion.

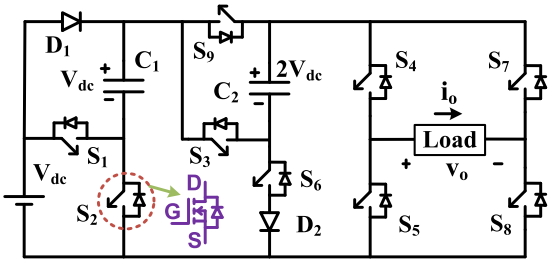

FIGURE 1. Circuit diagram of the proposed inverter topology.

II. OPERATION AND CONTROL STRATEGY

A. MODELING OF THE PROPOSED INVERTER TOPOLOGY

Fig. 1 illustrates the circuit model of the proposed single-source nine-level switched capacitor based novel quadruple boost inverter with reduced components count. The inverter comprises of a DC voltage source (V_{dc}), nine switches (S_1, S_2, ..., S_9), two diodes (D_1 and D_2) and two switched capacitors (C_1 and C_2). Both the diodes are fast recovery diodes. The load is connected as per the circuit diagram in Fig. 1. Moreover, the load current's direction and the voltage's polarity across the load have also been indicated.

The switched capacitors C_1 and C_2 can be charged up to V_{dc} and $2V_{dc}$ respectively. The charging path of C_1 is through D_1 and S_2 while C_2 is getting charge through S_1, body diode of switch S_9, S_6 and D_2. C_1 can be charged by the DC source (V_{dc}) alone while C_2 is charged by the DC source (V_{dc}) along with the capacitor C_1 connected in series.

The maximum blocking voltage or voltage stress (MVS) and maximum rate of change of voltage (MRCV) across the switches are crucial facets of an MLI topology. Both MVS and MRCV across the switches S_1, S_2, diodes D_1 and D_2 are V_{dc} while across switches S_3 and S_9 are $2V_{dc}$. MVS of S_4, S_5, S_7 and S_8 is $4V_{dc}$ while MRCV is $2V_{dc}$ for S_4, S_7 and V_{dc} for S_5, S_8. Further, S_6 has MVS is $2V_{dc}$ and MRCV is V_{dc}.

B. WORKING OPERATION OF THE PROPOSED MLI

The working operation of the proposed inverter topology has been elaborately explained with voltage levels. The nine levels of the output voltage (v_o) are generated as 0, $\pm V_{dc}$, $\pm 2V_{dc}$, $\pm 3V_{dc}$ and $\pm 4V_{dc}$. In all the level generation, as shown in Fig. 2, the current conducting path through which the load is connected is indicated in red, while the charging path of the capacitor is highlighted in green. The capacitor C_1 gets charged when $v_o = \pm V_{dc}$, $\pm 3V_{dc}$ and discharged at $v_o = 0$, $\pm 2V_{dc}$, $\pm 4V_{dc}$ while C_2 gets charged when $v_o = 0$, $\pm 2V_{dc}$ and discharged at $v_o = \pm 3V_{dc}$, $\pm 4V_{dc}$ which can be observed in Table 1. The operation of the inverter in the positive half cycle is as follows:

$v_o = 0^-$ *level* : The load is disconnected from the source and capacitors for this level generation. The load current ($i_o = 0$ for UPF load) is circulating in the negative direction for lagging PF load through the path S_5 and S_8's body diode depicted in Fig. 2(a).

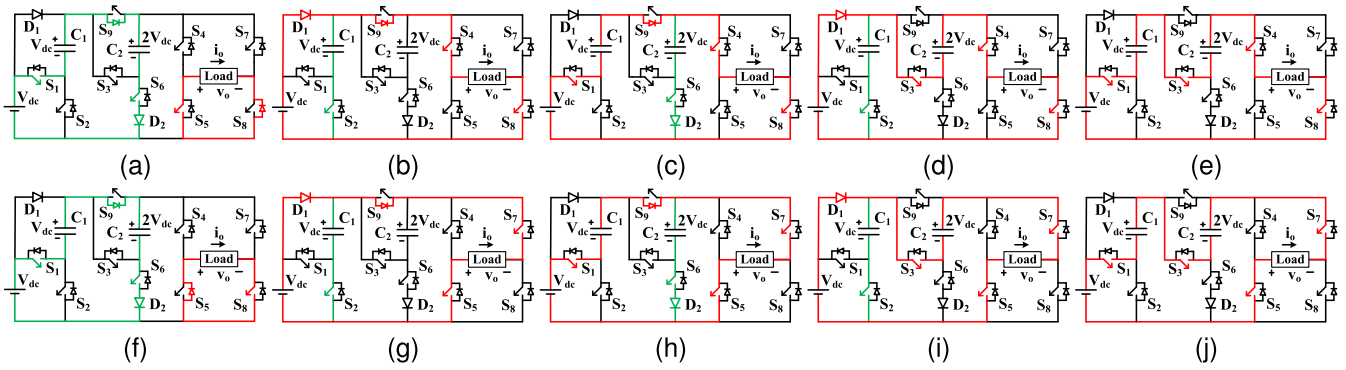

FIGURE 2. Operation of the proposed MLI for generating different voltage levels under the respective level generation of the output voltage. (a) $v_o = 0^-$. (b) $v_o = +V_{dc}$. (c) $v_o = +2V_{dc}$. (d) $v_o = +3V_{dc}$. (e) $v_o = +4V_{dc}$. (f) $v_o = 0^+$. (g) $v_o = -V_{dc}$. (h) $v_o = -2V_{dc}$. (i) $v_o = -3V_{dc}$. (j) $v_o = -4V_{dc}$.

TABLE 1. Switching state, output voltage, and capacitor's state of the Proposed inverter.

S_1	S_2	S_3	S_4	S_5	S_6	S_7	S_8	S_9	v_o	C_1	C_2
1	0	1	1	0	0	0	1	0	$+4Vdc$	↓	↓
0	1	1	1	0	0	0	1	0	$+3Vdc$	↑	↓
1	0	0	1	0	1	0	1	0	$+2Vdc$	↓	↑
0	1	0	1	0	0	0	1	1	$+Vdc$	↑	–
1	0	0	0	1	1	0	1	0	0^+	↓	↑
1	0	0	0	1	1	0	1	0	0^-	↓	↑
0	1	0	0	1	0	1	0	1	$-Vdc$	↑	–
1	0	0	0	1	1	1	0	0	$-2Vdc$	↓	↑
0	1	1	0	1	0	1	0	0	$-3Vdc$	↑	↓
1	0	1	0	1	0	1	0	0	$-4Vdc$	↓	↓

↑, ↓, and – indicate the capacitor's charging, discharging, and idle state respectively.

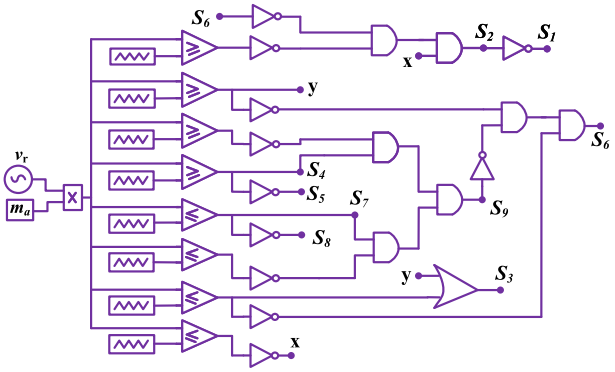

FIGURE 3. Logic circuit diagram for gate pulses generation.

$v_o = +V_{dc}$ *level* : The load is getting driven by the source alone through the path D_1, S_9's body diode, S_4 and S_8 as represented in Fig. 2(b).

$v_o = +2V_{dc}$ *level* : The load receives power from the series combination of V_{dc} and C_1 through the path formed by S_1, the body diode of S_9, S_4, and S_8 as shown in Fig. 2(c). Therefore, the output voltage is $V_{dc} + V_{c1}$.

$v_o = +3V_{dc}$ *level* : The load is connected to V_{dc} and capacitor C_2 through D_1, S_3, S_4 and S_8 which is depicted in the Fig. 2(d). The output voltage appear as $V_{dc} + V_{c2}$.

$v_o = +4V_{dc}$ *level* : The series combination V_{dc}, C_1 and C_2 feed the power to the load through the path S_1, S_3, S_4 and S_8 which is shown in Fig. 2(e). The output voltage is $V_{dc} + V_{c1} + V_{c2}$.

Similarly, the inverter can operate in the negative half cycle, facilitated by the H-bridge acting as the polarity-generating component, which can be perceived by Fig. 2(f) to (j) and Table 1.

C. CONTROL STRATEGY

This paper adopted the level-shifted phase deposition pulse width modulation (PDPWM) method to generate the switches' gate pulses. Compared to fundamental frequency-based switching techniques, this PWM technique has a propensity to lower the harmonics in the load voltage. Fig. 3 shows the 50 Hz sinusoidal reference signal ($v_r = V_{pr} sin\omega t$) has been compared with all the triangular carrier signals whose peak-to-peak amplitude is one and frequency is 5 kHz. The pulses are generated by the comparison, which has been given to the logical circuit in Fig. 3 to acquire the required pulses as per the switching states of the switches as shown in Table 1.

The amplitude of the N-Level inverter's output voltage is directly proportional to the modulation index (m_a), and it can be expressed as (1).

$$m_a = \frac{2V_{pr}}{(N-1)V_{ppc}} \tag{1}$$

where V_{ppc} indicates the peak-to-peak value of the carrier signal.

III. DESIGN AND DESCRIPTION

A. PERFORMANCE PARAMETERS

1) VOLTAGE RIPPLE AND CAPACITORS SELECTION

Often in SCMLI, a very short duration is available for charging the switched capacitors. Various voltage levels may be achieved by discharging the capacitors' voltage. The selection of the capacitors mainly depends on capacitor voltage ripple, discharging time, operating frequency, and inverter application. The capacitor's voltage ripple needs to be maintained within the permissible limit, which provides

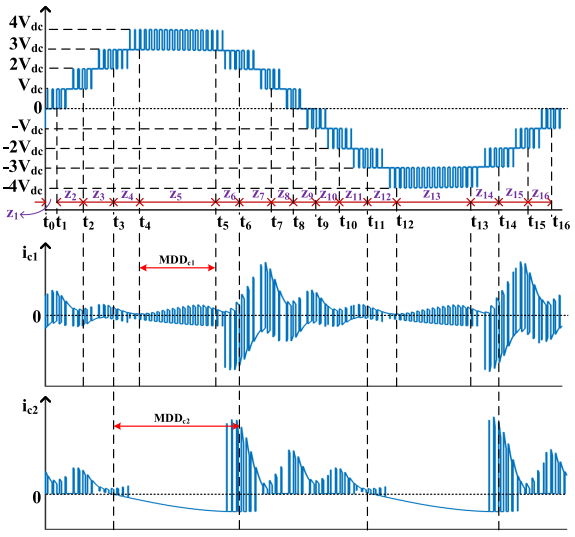

FIGURE 4. Pictorial view of the maximum discharging duration of both capacitors.

the load voltage fluctuation within the licit limit, lesser power losses, and higher inverter efficiency. The longest discharging time needs to be considered for capacitor selection, and the charge stored in the capacitor can be expressed as follows.

$$Q_{cn} = \int_{t_{d1n}}^{t_{d2n}} I_{op} Sin(2\pi f_o t) dt \tag{2}$$

where Q_{cn} indicates the amount of charge stored in n^{th} capacitor, t_{d1n} to t_{d2n} is the maximum discharging duration (MDD) of n^{th} capacitor, I_{op} represents the peak value of the load current, while f_o denotes the load frequency. The maximum value of 'n' is 2 in this paper.

Now, the capacitance can be found as

$$C_n = \frac{Q_{cn}}{\Delta V_{cn}(\%) \times V_{cn}} \tag{3}$$

where V_{cn} represents the voltage across the n^{th} capacitor while ΔV_{cn} is the allowable ripple in V_{cn}.

Fig. 4 shows the maximum discharging duration for the capacitors C_1 and C_2 are t_4 to t_5 and t_3 to t_6 respectively. These instants of time can be found as [30]

$$t_3 = \frac{sin^{-1}(\frac{5}{8})}{2\pi f_0} \tag{4}$$

$$t_4 = \frac{sin^{-1}(\frac{7}{8})}{2\pi f_0} \tag{5}$$

$$t_5 = \frac{\pi - sin^{-1}(\frac{7}{8})}{2\pi f_0} \tag{6}$$

$$t_6 = \frac{\pi - sin^{-1}(\frac{5}{8})}{2\pi f_0} \tag{7}$$

The minimum capacitance of C_1 and C_2 are required for $I_op = 1.3$ A and $\Delta V_c = 4\%$ which have been evaluated by using (2) to (7).

$$C_{1min} = \frac{Q_{c1}}{\Delta V_{c1}} = 3230.9\ \mu F$$

$$C_{2min} = \frac{Q_{c2}}{\Delta V_{c2}} = 2605.04\ \mu F$$

2) TOTAL STANDING VOLTAGE (TSV)

It is the summation of the blocking voltage of all the semiconductor devices incorporated into the inverter, which can be found by (8).

$$TSV(p.u.) = \frac{1}{V_{o_{max}}} \sum_{n=1}^{N_D} V_{bmax,D_n} \tag{8}$$

where $V_{o_{max}}$ represents the maximum output voltage of the inverter and V_{bmax,D_n} indicates the maximum blocking voltage of the n^{th} device while N_D is the total number of devices.

3) LOSS ANALYSIS

The total losses that occur in the system are the combination of various types of losses, which are described below.

a: CONDUCTION LOSSES (P_{CON})

The average conduction losses of all the switches, capacitors, and diodes can be found by (9), (10), and (11), respectively.

$$P_{s,con} = \sum_{z_n=1}^{N_z} \left(\frac{R_{ON_{sn}}}{T_0} \int_{t_u}^{t_v} I_{r_{sn}}^2\, dt \right) \tag{9}$$

where N_z and T_0 are the total numbers of operating zones in one cycle and time period of the load current, respectively, $R_{ON_{sn}}$ is the ON state resistance of $s_n{}^{th}$ switch while t_u and t_v are the starting time and ending time of the particular $z_n{}^{th}$ zone respectively while $I_{r_{sn}}$ represents the RMS (root mean square) current flowing through $s_n{}^{th}$ switch.

$$P_{cap,con} = \sum_{n_z=1}^{N_z} \left(\frac{R_{esr_{cn}}}{T_0} \int_{t_u}^{t_v} I_{r_{cn}}^2\, dt \right) \tag{10}$$

where $R_{esr_{cn}}$ indicates the equivalent series resistance of the $c_n{}^{th}$ capacitor.

$$P_{d,con} = \sum_{n_z=1}^{N_z} \left(\frac{V_{ON_{d_n}}}{T_0} \int_{t_u}^{t_v} I_{a_{d_n}} dt \right) \tag{11}$$

where $V_{ON_{d_n}}$ is the ON state voltage drop of the d_n^{th} diode and $I_{a_{d_n}}$ indicates the average current of the d_n^{th} diode.

Now, the conduction losses (P_{con}) of the inverter can be expressed as

$$P_{con} = P_{s,con} + P_{cap,con} + P_{d,con} \tag{12}$$

TABLE 2. Praformance Comparision with the existing single source nine-level SCMLIs.

MLI	N_s	N_c	N_d	N_{BSW}	TSV_s $(p.u.)$	TSV_d $(p.u.)$	V_g	MVS_s $(p.u.)$	PF Range	C (mF)	f_s (kHz)	$V_{dc} \rightarrow V_{o_{max}}$ (V)	η_m (%)
[13]	12	3	0	0	6	0	4	1	1-0.862	4.3, 2.2, 1.1	20	$80 \rightarrow 320$	96.4
[15]	11	2	0	0	6.5	0	2	1	1-0.998	2.2×2	0.05-0.2	$190 \rightarrow 380$	94.8
[16]	11	2	0	1	8.5	0	2	1	1-0.494	4.7×2	5	$100 \rightarrow 200$	–
[17]	11	2	0	0	5.5	0	2	0.5	1-0.846	4.7×2	2.5	$160 \rightarrow 320$	–
[21]	9	4	4	1	5.25	0	1	1	1-0.303	0.47×4	2.5	$200 \rightarrow 200$	97.3
[22]	9	4	4	0	5.25	0.75	4	0.75	1-0.45	1.0×3, 3.3	10	$100 \rightarrow 400$	95.2
[26]	8	2	1	0	5.5	–	2	1	1-0.982	3.3, 2.2	4	$100 \rightarrow 200$	96.3
[27]	8	2	1	2	6	–	2	1	1-0.876	1.0×2	–	$200 \rightarrow 400$	95
[28]	8	3	3	0	5.75	–	4	1	1-0.976	3.3×3	4	$80 \rightarrow 320$	93
[29]	10	2	3	0	5.75	–	4	1	1-0.954	2.2×2	5	$50 \rightarrow 200$	96.25
[P]	9	2	2	0	6	0.5	4	1	1-0.5	3.3×2	5	$31 \rightarrow 124$	96.95

$V_g = V_{o_{max}}/V_{dc}$, and η_m indicates the maximum efficiency of the inverter, while '–' shows that the information is not included in the respective article.

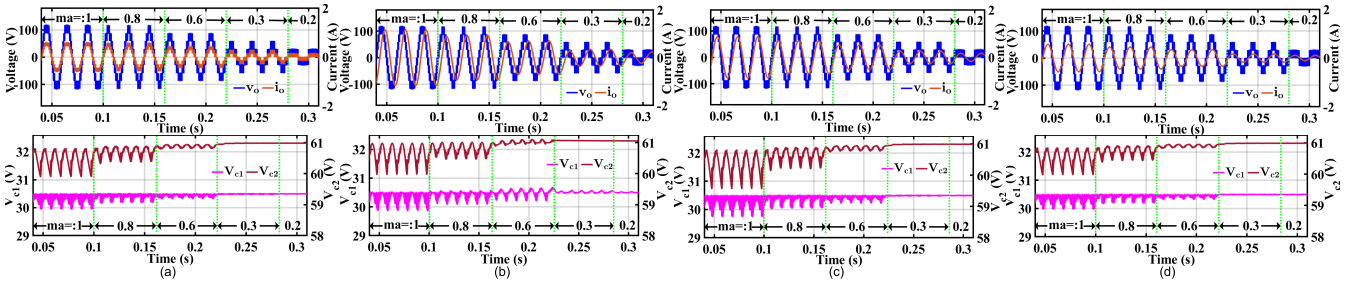

FIGURE 5. Inverter's output voltage, output current, and capacitors voltage waveforms for the step change in m_a under the loading condition of (a) $Z_o =$ 200 Ω, (b) $Z_1 =$ 50 Ω + 275 mH, (c) $Z_2 =$ 120 Ω + 185 mH, and (d) $Z_3 =$ 200 Ω + 150 mH.

b: SWITCHING LOSSES (P_{SW})

Due to the overlap between the current and voltage during switching-ON/OFF operation, switches undergo switching losses. It happens due to the non-ideal switching characteristics of the power electronic switches. The variation of voltage and current is considered linear during ON/OFF for the evaluation of switching losses, and the average switching losses can be found by (13).

$$P_{sw} = f_{sw} \times \left[\sum_{n_s=1}^{N_s} \left\{ \sum_{T_{sw}} \frac{1}{6} \left(V_{ON} I_{ON} T_{ON} + V_{OFF} I_{OFF} T_{OFF} \right) \right\} \right] \quad (13)$$

where f_{sw} is the switching frequency, $T_{sw} = \frac{1}{f_{sw}}$. V_{ON} and I_{ON} represent the transition voltage and current respectively during switching ON while V_{OFF} and I_{OFF} during switching OFF. T_{ON} and T_{OFF} indicate the switch turning ON and turning OFF duration, respectively.

Capacitor ripple losses ($P_{cap,ripp}$): The amount of energy dissipated in the capacitor during charging of the capacitor and the charging path is excluded from the load is qualified as capacitor ripple loss. The losses mainly depend on the operating frequency and capacitance of the capacitor. It can be evaluated as

$$P_{cap,ripp} = (1/2)(2f_o) \sum_{n=1}^{N_c} C_n \Delta {V_{c_n}}^2 \quad (14)$$

where C_n is the capacitance and ΔV_{c_n} denotes the ripple voltage of n^{th} capacitor.

4) EFFICIENCY (η_{MLI})

The efficiency of the MLI can be defined as the total power achieved at the output terminal of the inverter with respect to the input power.

The total losses of the inverter can be found by adding the aforementioned losses. Out of these losses, conduction losses and ripple losses are significant losses. Therefore, by reducing these two losses, the efficiency of the MLI can be enhanced. The efficiency of the MLI can be evaluated as

$$\eta_{MLI} = \frac{P_{O_{MLI}}}{P_{O_{MLI}} + P_{con} + P_{sw} + P_{cap,ripp}} \quad (15)$$

where $P_{O_{MLI}}$ represents the output power of the MLI.

IV. DETAILED ANALYSIS AND COMPARISON WITH EXISTING NINE-LEVEL TOPOLOGY

This section includes a comparative assessment to highlight the positive attributes of the proposed topology over other state-of-the-art structures of the nine-level inverter. Table 2 shows the quantitative and qualitative comparison. In which N_s, N_c, N_d and N_{BSW} are the total number of switches, capacitors, diodes, and number of bidirectional switches out of N_s respectively. Moreover, the 'PF Range' indicates the range of power factor of the load for which the inverter can operate satisfactorily. 'C' and f_s represent the total capacitance used in the inverter and the frequency of the carrier signals, respectively.

The SCMLIs reported on [15], [16], and [17] don't require any diode and bidirectional switches to generate the nine-level output voltage, while the switch count is more

than the proposed inverter topology. The voltage gain attained by them is only twofold the input voltage. The capacitance of capacitors in [16] and [17] is approximately twice that of the proposed inverter. The inverter discussed in [13], [22], and [29] shares a quadruple boosting capability akin to the proposed inverter. However, [13] uses twelve switches and three capacitors of different capacitance. On the other hand, the inverter presented in [22] integrates nine switches, four capacitors, and four diodes while [29] incorporated ten switches, two capacitors, and three diodes, surpassing the component count of the proposed inverter.

From Table 2, it is clearly observed that the topologies developed in [26], [27], and [28] have utilized eight switches. In addition to that, [26] uses only one diode and has a lesser TSV. Nevertheless, it is limited by its narrow operating range of load power PF ($1 - 0.982$) as well as its voltage boosting capability is only twofold. The operating range of load PF in [27] has been extended ($1 - 0.876$), and the size of the capacitor is also reduced. However, two out of the total eight switches are bidirectional switches, and the voltage gain is just two. The inverter suggested in [28] achieves a quadruple voltage gain similar to the proposed inverter. However, this topology requires an extra diode and capacitor. Additionally, it has a narrower operating range of load PF, with values of $1 - 0.976$ lagging, and the capacitor size is notably large. Reference [21] has a larger PF range than all other topologies presented in Table 2. However, it employs four capacitors and four diodes, and one of the nine switches is bidirectional, which indicates a higher number of components inclusion. Moreover, it has minimum TSV_s $(p.u)$, which is evident due to its absence of voltage-boosting capability.

Hence, the proposed SCMLI has a remarkable enhancement in the context of a reduction in the components count, voltage boosting capability, and operating range of load power factor.

V. RESULT AND DISCUSSION

The MATLAB simulation and experimental results have been presented in this section. The proposed nine-level switched capacitor inverter has been tested in two types of dynamic cases to verify its stability under sudden changes. Firstly, there is a step change in modulation index (1 to 0.8, 0.6, 0.3, and 0.2) under different loading conditions, then the load is varied in steps ($Z_1 = 50\ \Omega + 275$ mH to $Z_2 = 120\ \Omega + 185$ mH and $Z_3 = 200\ \Omega + 150$ mH) under different modulation index. Hereafter the Simulation and corresponding experimental results have been elaborately analysed in the following subsections.

A. MATLAB SIMULATION RESULTS AND ANALYSIS

This part of the paper discusses the working performances of the proposed topology through MATLAB simulation. The source voltage is considered as 31 V while the capacitance of both the switched capacitors (C_1 and C_2) is taken as 3.3 mF. The capacitors C_1 and C_2 can charge up to 31 V and 62 V, respectively.

The waveforms of output voltage (v_o), load current (i_o), and capacitor voltages (V_{c1} and V_{c2}) for step change in modulation index (m_a) from 1 to 0.8, 0.6, 0.3 and 0.2 at the respective loads Z_o (200 Ω), Z_1 (50 Ω + 275 mH), Z_2 (120 Ω + 185 mH) and Z_3 (200 Ω + 150 mH) are shown in Fig. 5. The value of m_a is kept 1 till 0.1 s, and from there onwards, it reduces by 0.2 in every 0.06 s till the m_a reaches 0.6 during the step change in m_a. Further, m_a has been decreased to 0.3 at 0.22 s and 0.2 at 0.28 s. It is observed in Fig. 5 and 6 that irrespective of the load, the peak value of the inverter's output voltage (v_o) is 122 V for the value of m_a at unity and 0.8. However, the root mean square (RMS) value is 86.63 V and 69.56 V at unity and 0.8 modulation index. Further, the peak value of the output voltage reduces to 91.5 V, 61.5 V, and 30.5 V at m_a of 0.6, 0.3, and 0.2, respectively.

It can be perceived from Fig. 5(a) that the v_o and i_o are in phase due to purely resistive load $Z_o = 200\ \Omega$ at UPF. The peak value of i_o is 0.61 A for the modulation index $1 - 0.8$. However, the RMS values are 0.43 A at the modulation index of 1 and 0.35 A at 0.8. While 0.46 A, 0.31 A, and 0.15 A are the peak values at respective m_a of 0.6, 0.3, and 0.2. The ripple voltages of the capacitor (C_1) are 0.56 V, 0.32 V, 0.19 V, and 0.05 V for the m_a of 1, 0.8, 0.6 and 0.3 respectively. While the respective ripple voltages of the capacitor (C_2) are 0.93 V, 0.54 V and 0.15 V for the m_a of 1, 0.8 and 0.6.

The voltage v_o at the output terminal of the inverter and current i_o through the load $Z_1 = 50\ \Omega + 275$ mH at 0.5 lagging PF is shown in Fig. 5(b). It observed that the load current i_o is sinusoidal, and it lags the load voltage by 60°. The peak value of load current is 1.22 A for the modulation index of 1 while 0.97 A at 0.8 modulation index. The load current further decreases to 0.73 A, 0.36 A, and 0.24 A for the m_a of 0.6, 0.3, and 0.2 respectively, which can be perceived in Fig. 5(b). For this load, the ripple voltages in V_{c1} are 0.66 V, 0.5 V, 0.48 V and 0.11 V at the m_a of 1, 0.8, 0.6 and 0.3 respectively. While the respective ripple voltages in V_{c2} are 1.02 V, 0.56 V, and 0.17 V corresponding to the modulation index of 1, 0.8 and 0.6 which can be identified in Fig. 5(b).

For the load $Z_2 = 120\ \Omega + 185$ mH at 0.9 lagging PF, the load current lags behind the inverter's output voltage by 25.84° as perceived in Fig. 5(c). The peak value of i_o is 0.91 A for the modulation index of 1 while 0.73 A at 0.8 modulation index. It can also be witnessed that the load current further reduces to 0.55 A, 0.27 A, and 0.18 A for m_a of 0.6, 0.3, and 0.2, respectively. Under this loading condition, ripple voltages across C_1 are 0.76 V, 0.46 V, 0.29 V, and 0.06 V for m_a of 1, 0.8, 0.6 and 0.3 respectively which can be observed in Fig. 5(c) While the respective ripple voltages across C_2 are 1.27 V, 0.7 V and 0.2 V corresponding to the modulation index of 1, 0.8 and 0.6.

Eventually, 200 Ω + 150 mH at 0.97 lagging PF is considered as the load Z_3 for the inverter, and i_o lags v_o by 13.34° as observed in Fig. 5(d). It is also identified that the respective ripple voltages in V_{c1} are 0.76 V, 0.46 V, 0.29V, and 0.06 V for the m_a of 1, 0.8, 0.6 and 0.3 While the ripple

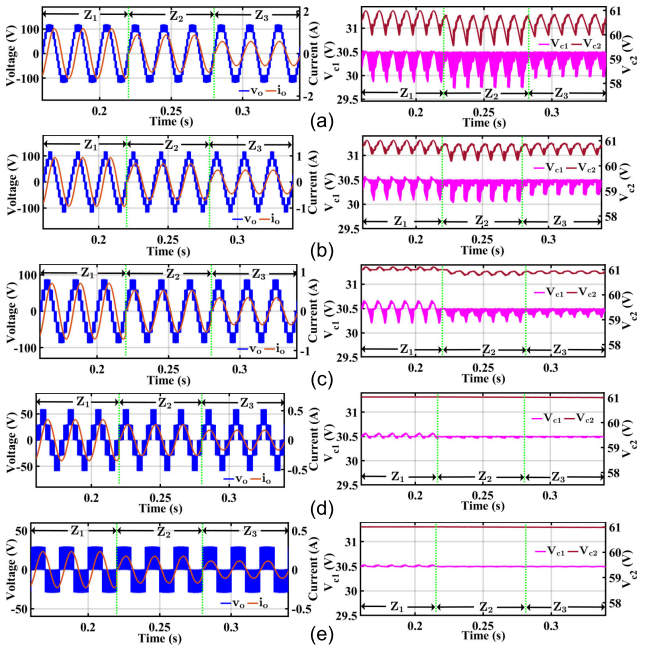

FIGURE 6. Output voltage, output current, and capacitors voltage waveforms for the step change in load at (a) $m_a = 1$, (b) $m_a = 0.8$, (c) $m_a = 0.6$, (d) $m_a = 0.3$, and (e) $m_a = 0.2$.

TABLE 3. Losses in the semiconductor devices.

Losses↓\ Device→	D_1	D_2	S_1	S_2	S_3	S_4	S_5	S_6	S_7	S_8	S_9
Conduction loss (W)	0.46	0.12	0.33	0.37	0.038	0.036	0.035	0.09	0.0326	0.035	0.376
Switching loss (W)	11.625e-12	3.487e-12	0.095	0.12	0.0138	0.0025	7.3e-4	0.023	2.62e-3	7.36e-4	0

voltage of C_2 are 1.27 V, 0.68 V, and 0.2 V at the same step change in modulation index till $m_a = 0.3$ which can be seen in Fig. 5(d).

The dynamic response of the proposed inverter for the step change in the load at the modulation index of 1, 0.8, 0.6, 0.3 and 0.2 are depicted in Fig. 6 (a), (b), (c), (d) and (e) respectively. For each modulation index, the inverter is operated under three loads of $Z_1 = 50\ \Omega + 275$ mH, $Z_2 = 120\ \Omega + 185$ mH and $Z_3 = 200\ \Omega + 150$ mH for the time duration of 0.16 s – 0.22 s, 0.22 s – 0.28 s and 0.28 s – 0.34 s respectively. The output voltage v_o varies with the modulation index but remain the same for all loading conditions.

As the load changes from Z_1 to Z_2 and Z_2 to Z_3 the magnitude of i_o's peak decreases from 1.22 A to 0.91 A and 0.91 A to 0.59 A respectively at $m_a = 1$ which can be observed in Fig. 6(a). In addition, the load PF also increased as the phase difference between v_o and i_o decreased from 60° to 25.84° when the load changed from Z_1 to Z_2 and 25.84° to 13.34° when load changed from Z_2 to Z_3. The ripple voltages of C_1 are 0.66 V, 0.76 V, and 0.53 V while 1.02 V, 1.27 V, and 0.88 V across C_2 for the load Z_1, Z_2 and Z_3 respectively.

The load current i_o also varied with the output voltage v_o depending on the modulation index for the same load. It is also noticed from Fig. 6 that the value ΔV_{c1} and ΔV_{c2} depend on the magnitude of the current and nature of the load.

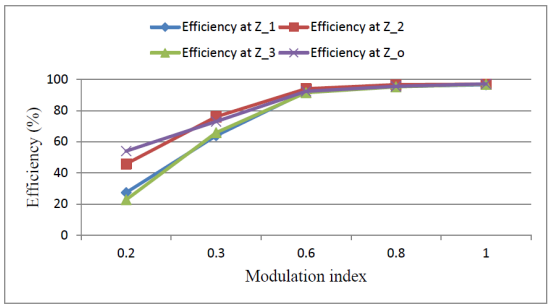

FIGURE 7. Efficiency plots under all the loading conditions.

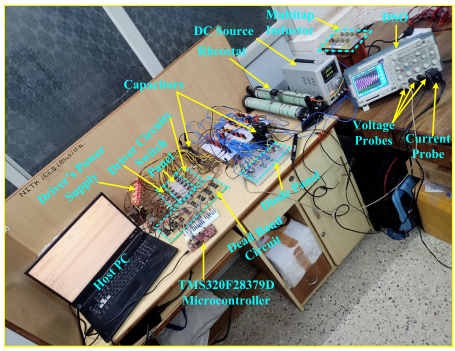

FIGURE 8. Experimental prototype setup of the proposed nine-level inverter.

The losses can be evaluated using the formulae given in section III or can be found in the PLECS simulation. The losses that occurred in each semiconductor device have been obtained by modeling switches and diodes in PLEXIM software, and the associated losses have been listed in Table 3 for UPF load at $m_a = 1$ and 31 V of supply. In which S_1 and S_2 have the highest switching loss among all the switches while S_9 has the highest conduction losses. However, S_9 has zero switching loss as it goes through the switching action at the moment of v_o's polarity reversal only, and at the same time, the switching action occurs while the body diode of the switch is already conducting. Fig. 7 shows the efficiency curves of the inverter for each loading condition, and it indicates that efficiency is deteriorating as the modulation index decreases for a fixed load.

B. EXPERIMENTAL RESULT AND ITS ANALYSIS

The performances of the proposed topology have been further verified through the hardware prototype and discussed in this subsection of the paper. Table 4 sums up the components and specifications used for the experimental setup. The hardware prototype setup indicating the respective components is shown in Fig. 8.

Microcontroller TMS320F28379D is employed to generate the required switching pulses based on the discussed logic strategy and processes through the dead-band circuit to avoid short through. Thereafter, the pulses were fed to each TLP250 optocoupler-based driver circuit associated with

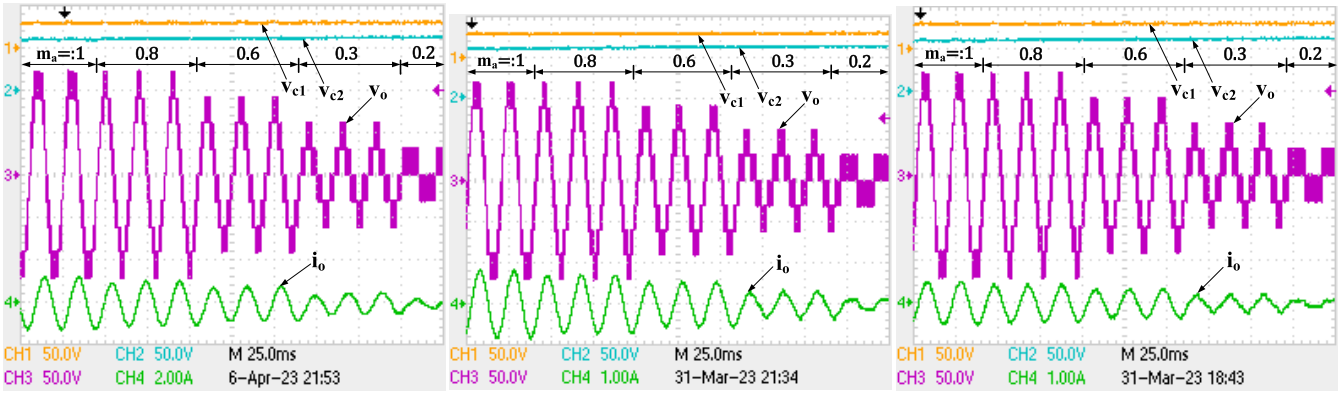

FIGURE 9. Output Voltage, load current and capacitors' voltage waveforms with the step change in m_a under the loading condition of (a) $Z_1 = 50\ \Omega + 275$ mH at 0.5 lagging PF, (b) $Z_2 = 120\ \Omega + 185$ mH at 0.9 lagging PF, and (c) $Z_3 = 200\ \Omega + 150$ mH at 0.97 lagging PF.

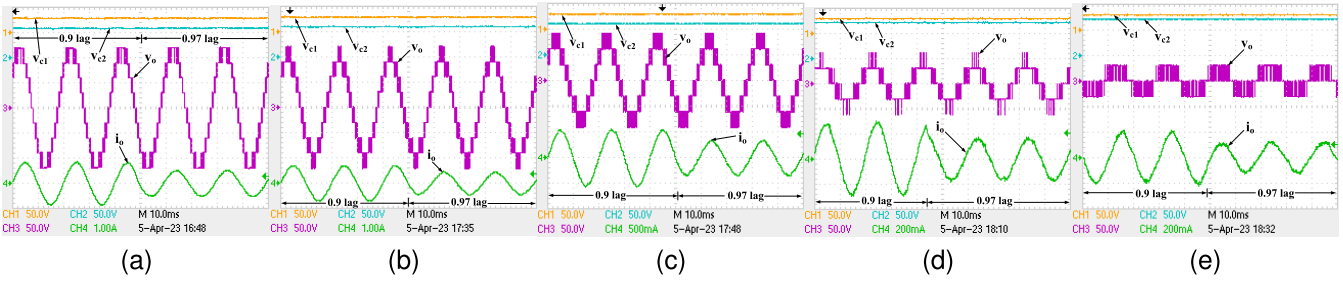

FIGURE 10. Dynamic response of the proposed inverter with change in load from 120 Ω + 185 mH at 0.9 lagging PF to 200 Ω + 150 mH at 0.97 lagging PF. At (a) $m_a = 1$, (b) $m_a = 0.8$, (c) $m_a = 0.6$, (d) $m_a = 0.3$, and (e) $m_a = 0.2$.

TABLE 4. Devices and their specifications experimental setup.

Device	Part No.	Specifications
Switch	MOSFET IRF 460	500 V, 21 A
Diode	Fast Recovery diode MUR1560	600 V, 20 A
Capacitor (C_1)	ALCON PG-6DI	3300 μF, 250 V
Capacitor (C_2)	ALCON PG-6SR 026	3300 μF, 400 V
Load Resister (R)	RHEOSTAT	200 Ω, 5 A
Load Inductor (L)	Multitap inductor	(0-5-15-30-50-100-200-300) mH, 8 A, 50 Hz
DSO	Tektronix TPS 2024B	4-Channel, 200 Mz
Current Probe	Tektronix TCP2020	20A_{RMS}, 0–50 MHz

individual MOSFETs. The DC power supply to the driver is realized using a multi-winding transformer cum rectifier circuit. MOSFETs IRF460 and fast recovery power diodes MUR1560 are used as the power electronic components. The same parameters have been considered for both under experimental conditions and MATLAB simulation.

The prototype of the inverter is operated under varied modulation index as well as loads to validate its dynamic performance and the responses are shown in Fig. 9 to 12. The wave forms of v_o, i_o, V_{c1} and V_{c2} for the step change in m_a from 1 to 0.8, 0.6, 0.3 and 0.2 is captured and depicted in Fig. 9. The experimental waveforms for varied modulation index under three different loads $Z_1 = 50\ \Omega + 275$ mH at 0.5 lagging PF, $Z_2 = 120\ \Omega + 185$ mH at 0.9 lagging PF, and $Z_3 = 200\ \Omega + 150$ mH at 0.97 lagging PF are shown in Fig. 9(a), (b) and (c) respectively. It is observed from Fig. 9 that the output voltage has nine levels at modulation index 1 and 0.8 with the peak amplitude of ±122 V while at the modulation index 0.6, 0.3, and 0.2 the output voltage has seven levels, five levels, and three levels, and corresponding peak amplitudes are ±91.5 V, ±61.5 V, and ±30.5 V respectively.

For Z_1 load, the respective i_o's peak amplitudes are ±1.22 A, ±1.22 A, ±0.915 A, ±0.615 A, and ±0.305 A at the modulation index of 1, 0.8, 0.6, 0.3 and 0.2. In addition, i_o lags v_o by 60°. Similarly, i_o's peak decreases as the modulation index decreases for the other two loads Z_1 and Z_2 and lags v_o by 24° and 14° respectively. The capacitors' voltage profiles are stable throughout the variation in the modulation indexes for all the loads (Z_1, Z_2, Z_3), which indicates that the capacitors' voltages are self-balancing.

The experimental waveforms under the step load change are shown in Fig. 10 to 12. At first, the load has been changed from 120 Ω + 185 mH at 0.9 lagging PF to 200 Ω + 150 mH at 0.97 lagging PF at the modulation index of 1, 0.8, 0.6, 0.3 and 0.2 which can be recognized in Fig. 10(a), (b), (c), (d) and (e) respectively. It also shows that the capacitors' voltages are getting self-balanced for all modulation indices and even during the load changes. The output voltage waveforms of the inverter remain the same for varied loading conditions under different modulation indices. However, the output current's waveforms and its

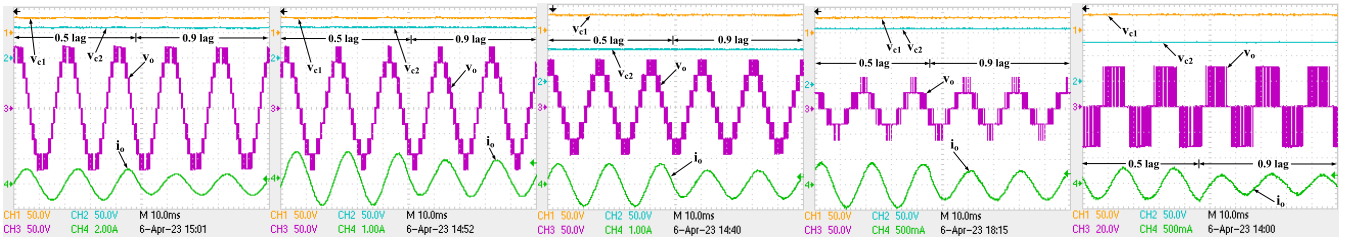

FIGURE 11. Dynamic response of the proposed inverter with change in load from 50 Ω + 275 mH at 0.5 lagging PF to 120 Ω + 185 mH at 0.9 lagging PF. At (a) $m_a = 1$, (b) $m_a = 0.8$, (c) $m_a = 0.6$, (d) $m_a = 0.3$, and (e) $m_a = 0.2$.

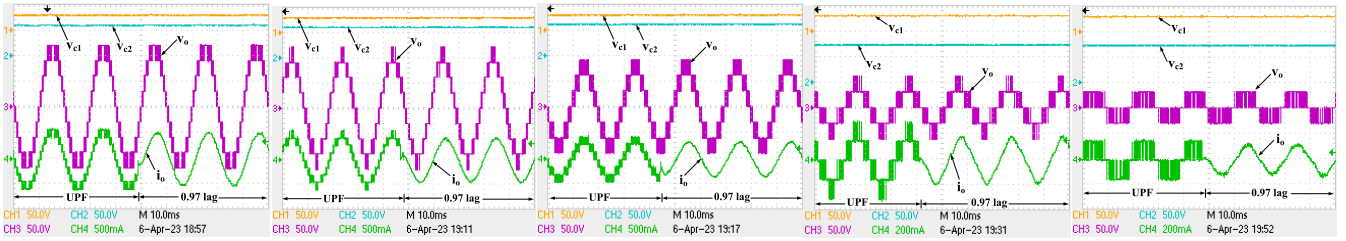

FIGURE 12. The response of the inverter with a step change in load from 200 Ω at UPF to Z_3 = 200 Ω + 150 mH at 0.97. At (a) $m_a = 1$, (b) $m_a = 0.8$, (c) $m_a = 0.6$, (d) $m_a = 0.3$, and (e) $m_a = 0.2$.

peak amplitude change with the loading condition changes. Moreover, the response of the inverter for varied loading from 50 Ω + 275 mH to 120 Ω + 185 mH is shown in Fig. 11 to validate the inverter's performance under a wider range of PF. The respective Fig. 11(a), (b), (c), (d) and (e) show the experimental results of stable capacitors' voltage, output voltage, and load current when the load changes from 0.5 lagging PF to 0.9 lagging PF at the modulation index of 1, 0.8, 0.6, 0.3 and 0.2.

The dynamic response of the proposed nine-level inverter under step change in load from the purely resistive type of 200 Ω to a resistive-inductive type of 200 Ω + 150 mH at 0.97 PF while keeping the modulation index fixed at 1, 0.8, 0.6, 0.3 and 0.2 is depicted in Fig. 12(a), (b), (c), (d) and (e) respectively. The shown spectrum confirms the stable operation of the inverter even under sudden changes in the type of loading from UPF to 0.97 PF.

Eventually, the capacitors' voltage profile has been maintained within the desirable limit ($\Delta V_c \leq 5\%$) under all these loading conditions, which indicates the self-balancing of the capacitors' voltage. In addition, it shows that the inverter can operate for resistive as well as inductive loads and for load changes at particular values of the modulation index and vice versa. At modulation index 1, the output voltage's amplitude acquired 122 V, quadrupling the input voltage of 31 V and can be observed in Fig. 12(a). Hence, it validates the aforementioned advantages and characteristics of the proposed inverter.

For a more in-depth examination of the dynamic operation of the proposed inverter, Fig. 13 illustrates the impact of step changes in the load, modulation index, and input voltage

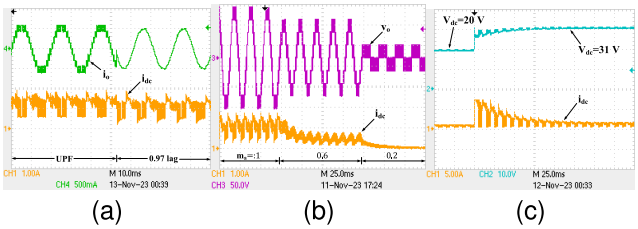

FIGURE 13. Experimental waveform of input current during a step change in (a) load, (b) modulation index, and (c) source voltage.

on the inverter's input current. Fig. 13(a) shows the output current and input current during step change is load from 200 Ω to 200 Ω +150 mH at unit modulation index. It can be observed from Fig. 13(b) that the out voltage and input current decreases with a decrease in the modulation index. The inverter's input current increases in Fig. 13(c) with the increase in the input voltage from 20 V to 31 V at a constant load. Most importantly, the input current of the proposed inverter is continuous under all circumstances, which means that it has better DC utilization and can be used in solar photovoltaic applications.

Fig. 14(a) shows the maximum charging current for the capacitors is approximately ten times the load current at the starting time. Therefore, some of the switches must understand the same maximum current. In a steady state condition, Fig. 14(b)-(e) illustrates the current stress on the switches, confirming that the maximum current stress is around 2.5 times the load current for S_1, D_1, S_2, S_9 and twice for S_6, D_2. Additionally, for S_3, S_4, S_5, S_7, S_8, the current

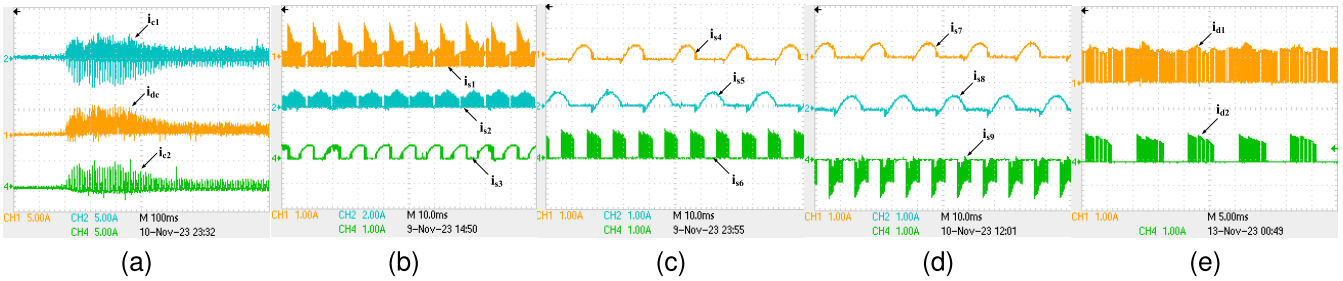

FIGURE 14. Experimental waveforms under the load of Z_3 and unity modulation index. (a) Inrush current of the proposed MLI (i_{dc}) and SCs (i_{c1} & i_{c2}). (b) Steady-state current through S_1, S_2, S_3, (c) S_4, S_5, S_6, (d) S_7, S_8, S_9 and (e) D_1, D_2.

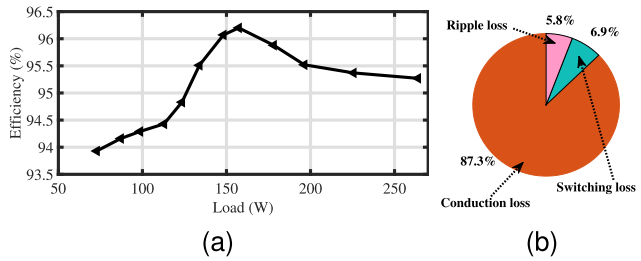

FIGURE 15. (a) Measured efficiency. (b) Distribution of losses under the load of 157.3 W.

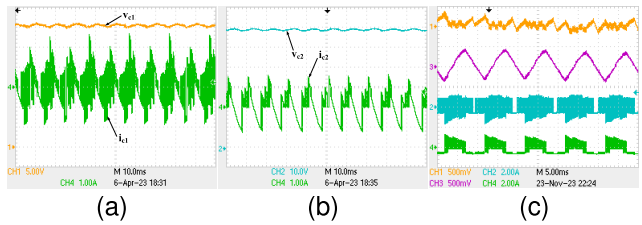

FIGURE 16. (a) Capacitor C_1's voltage (V_{c1}) and current (i_{c1}) at Z_1 (b) Capacitor C_2's voltage (V_{c2})and current (i_{c1}) at Z_1 and (c) Capacitors' ripple voltage and current at resistive load Z_0.

stress equals the load current. The current stress is equally important as voltage stress for the design consideration and selection of components for the inverter.

The efficiency of the proposed inverter prototype is examined across different loads, and the outcomes are presented in Fig. 15. It is evident from the figure that the proposed topology exhibits a notable operating efficiency, with a peak efficiency of 96.2% achieved at 157.3 watts. The three major components of the inverter losses are conduction loss, switching loss, and ripple loss. The devices' total conduction and switching losses at 157.3 W are measured as 5.41 W and 0.43 W, respectively. The ripple loss occurred due to two switched capacitors and was measured as 0.36 W.

Fig. 16 shows the capacitors' voltage and currents through it at unity modulation index with 50 Ω + 275 mH at 0.5 lagging PF loading conditions, which is considered here as the worst operating condition for the capacitors among all other discussed conditions. In this case, C_1 is getting a little extra charge at $\pm V_{dc}$ voltage level by the inductive part of the load. Because of the load's highly inductive nature, the load current flows in the same direction (direction at the previous voltage level) for some moment. Therefore, at V_{dc} voltage level, the load current is flowing in the same direction as it was at zero voltage level, and it occurred through the path S_4's body diode, S_9, C_1, S_2 and S_8's body diode. In Fig. 16(a), it can be identified that the capacitor C_1's current can reach a maximum value that is approximately 2.1 times the load current. Fig. 16(b) depicts C_2's peak current, which is 1.4 times the load current, and the voltage across it is around 60.5 V. To conduct a thorough analysis of the ripple in the capacitor voltages V_{c1} and V_{c2}, Fig. 16(c) presents the experimental waveforms depicting the ripple voltage and current for both capacitors at resistive load Z_0 and unity modulation index. It can be observed from the waveforms that the capacitor voltage is stable, and voltage ripple is maintained below 5%. Therefore, the capacitors' peak currents are well within the limit, even at higher loads and poor PF. Hence, the proposed nine-level quadruple boost MLI possesses self-balancing capacitors' voltage under a wide range of load PF at various modulation indexes.

VI. CONCLUSION

A novel quadruple boost reduced component nine-level inverter with continuous input current is proposed in this paper. The preeminence of the proposed inverter over the standard nine-level switched-capacitor inverters has been discussed through comparative analysis. The multi-carrier PDPWM method is implemented to generate the desired switching pulses for the proposed nine-level inverter, and responses are analyzed in the MATLAB/Simulink platform, which is further validated by experimental prototype hardware results. The proposed inverter operates satisfactorily under modulation index (m_a) ranging from 1 to 0.2 as well as load of unity power factor (UPF) to 0.5 lagging power factor. The stable dynamic response observed in the proposed inverter affirms the self-voltage balancing characteristics of the capacitors utilized. This performance is sustained across an output power range of 37 W to 264 W, with a measured maximum efficiency of 96.2%. These findings underscore the reliability and efficiency of the proposed inverter, establishing it as a promising advancement in power electronics.

ACKNOWLEDGMENT

(Devanand Kumar, Ravi Raushan, and Suprava Chakraborty contributed equally to this work.)

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