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TOPICAL REVIEW

FinFET to GAA MBCFET: A Review and Insights

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ABSTRACT This review article presents a journey from Fin-shaped field effect transistor (FinFET) to gate-all-around multi-bridge channel field effect transistor (GAA MBCFET) technology, unraveling the evolution of semiconductor architectures. This article provides a concise yet insightful overview of the development of FinFET, exploring modified architectures, current trends, and associated constraints. The growing importance of other semiconductor materials instead of Si in FinFET or other technologies has been studied in detail. The article explores an emerging technology called 'GAA MBCFET', highlighting its advantages over FinFET. It also delves into the notable drawbacks and complex fabrication challenges associated with the upcoming GAA MBCFET technology.

INDEX TERMS Gate-all-around (GAA), multi-bridge channel (MBC), silicon on insulator (SOI).

I. INTRODUCTION

The electronics industry heavily relies on semiconductor devices. Semiconductor devices such as diodes, transistors, integrated circuits, etc. are ubiquitous components in almost every electronic circuit that we encounter in our daily lives. One of the most crucial components is the Metal-Oxide-Semiconductor Field-Effect Transistor (MOSFET), which has dominated the semiconductor industry for over four decades. Indeed, the semiconductor industry has made remarkable improvements in response to the escalating demands for miniaturization, higher operational speeds, reduced power consumption, and cost-effectiveness. These advancements have been achieved through innovative changes in device structures and materials, driving the industry's continuous progress. The multi-gate nature of FinFET suppresses the short channel effect and reduces the OFF-state leakage current that is faced by planar MOSFET. For more than one decade, FinFET technology has ruled the semiconductor industry due to its robustness towards low power consumption and high-efficiency properties. In recent times, transistors have reached dimensions in the few nanometer (<3nm) range, but further scaling has posed challenges, particularly in FinFETs, where gate controllability over the channel decreases. To address these issues, researchers are actively working to develop novel semiconductor structures that can be scaled below 5nm, aiming to overcome the limitations in a new era of advanced electronics.

This review starts with the history of semiconductor devices. The technology roadmap and transistor evolution have been discussed in detail. The emerging semiconductor device with their expertise has been discussed elaborately. Notably, the focal point is the leading semiconductor device FinFET where its evolution, operational principles, advantages, advancements, and applications are extensively discussed. Additionally, the paper addresses the ongoing challenges faced by FinFET technology, providing valuable insights into potential solutions and areas for improvement.

II. HISTORY OF SEMICONDUCTOR DEVICE

The first seed of the electronics industry, called the vacuum tube, launched in 1904 [1]. The vacuum tube controls the flow of electrons in the vacuum. However, in the Second World War, the demand for vacuum tubes increased. It was noted that the reliability of the device has diminished, owing to the growth in power consumption, manufacturing expenses, and overall size. At the end of the 1940s, the electronic industry invented the two most essential semiconductor devices, Point-Contact Germanium Transistor and Bipolar Junction Transistor (BJT). In 1947, the Point contact transistor was built by a team of William Shockley, John Bardeen, and Walter Brattain [2] shown in Fig.1.

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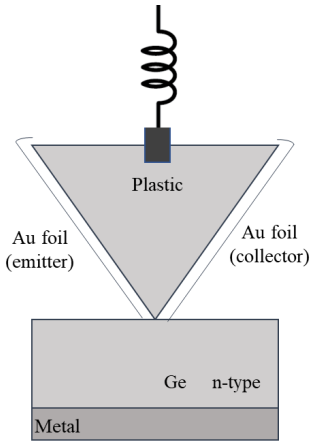

FIGURE 1. First point contact transistor.

In 1948, BJT was invented by William Shockley. Point contact transistors and BJTs are more power-efficient and reliable than vacuum tubes [3]. In 1958, Jack Kilby developed the first integrated circuit (IC.), where several transistors are joined or fabricated in one silicon substrate by wire bonding [4]. On the other hand, [5] Leo Esaki studied and noticed that a narrow junction would introduce tunneling. In 1957, Leo Esaki first invented a Germanium-based tunneling diode. On the other hand, he invented silicon-based in 1958. After developing the transistors, Shockley and

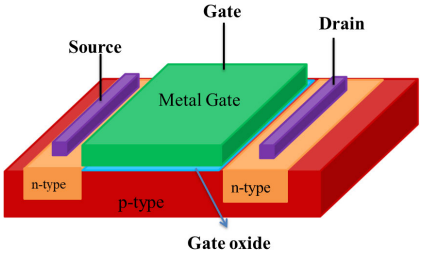

FIGURE 2. The planar MOSFET semiconductor device.

Brattain focused on designing field-effect devices. In bipolar transistors, various unwanted problems have been noticed. The researchers did not correctly clear the semiconductor surface in bipolar transistors. In 1956, M.M Atalla presented the issues regarding surface, and Silicon dioxide can be considered a solution for semiconductor surfaces [6]. During this period, he designed the Insulated-Gate Field Effect Transistor (IGFET), which is now called MOSFET [7]. Later in 1962, F.P. Heiman and S.R Hofstein modified the IGFET structure [8]. In 1963, Steven Hofstein and Fredic Heiman published [9] their work on silicon MOSFET, which was acknowledged by the semiconductor industry.

MOSFET has been the driving engine of the digital World. The planar MOSFET device is shown in Fig.2. This was the most famous invention of the 20th century due to its successful incorporation into IC. MOSFET device improves the packing density while maintaining the low fabrication cost. These devices also improved the operating frequencies with better speed. The MOSFET device has ruled above 40 years in the semiconductor industry due to its robustness. We need to integrate more transistors on an IC to get more efficiency from the MOSFET. As a result, the device provides more drain current with low power consumption. These all advantages can be obtained by diminishing the device dimensions, and the process is called 'scaling'. The term 'scaling' is significant, with billions of transistors integrated into IC, increasing the device's capabilities with a minimum cost. The main advantage of transistor scaling is that it reduces the manufacturing cost and enhances the speed of the device. Multiple numbers of tasks can be processed simultaneously due to the scaling property. Without any extraordinary miniaturization methods, scaling of device dimensions is not possible to meet the demands of the semiconductor industry.

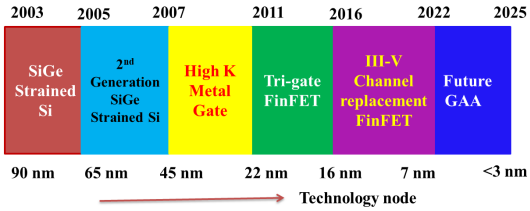

FIGURE 3. Technology roadmap for semiconductor transistor.

To increase the chip density, various vital parameters such as drain/source region, oxide thickness, channel length, and gate length are scaled down, impacting the device's performance. The controlling capability of the channel has been reduced due to the over-scaling of the device dimensions, especially the reduction of source, drain, channel length, and oxide thickness. The over-scaling gives rise to unwanted side effects known as non-ideal effects or short-channel effects (SCEs).

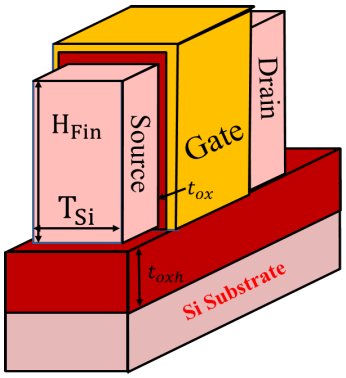

FIGURE 4. Schematic diagram of conventional FinFET.

Several undesirable consequences in MOSFET include subthreshold slope (SS) degradation, drain-induced barrier lowering (DIBL), threshold voltage (V_{th}) variation, hot

carrier injection, mobility degradation, velocity saturation, and more. As the industry advances towards smaller dimensions, MOSFETs encounter significant challenges from these effects. To overcome the limitation that MOSFET has been facing, various alternative structures are introduced by the researcher in the semiconductor industry that have been discussed in detail in the following part.

III. TECHNOLOGY ROAD-MAP AND TRANSISTOR EVOLUTION: PLANAR FET TO 3D FETS

Alternative structures are implemented through the application of various engineering techniques, involving variations in material, work-function, gate length, and spacer materials. The new 2020 edition of ITRS (international technology roadmap for semiconductors) presents the scenario of emerging devices considered replacements of MOSFET, which is regarded as the best solution for the semiconductor industry. All these devices have shown a significant improvement, which would benefit the future complementary metal-oxide-semiconductor (CMOS) industry. Here, we will delve into the intricate details of all the latest and ongoing semiconductor devices. The Technology roadmap is shown in Fig.3 and the challenges of the different transistors at the technology node are shown in table 1.

Continuous gate-length scaling requires a new modified semiconductor device that can improve the device performance whereas conventional Si MOSFET was not able do improve in the performance with excess scaling. To enhance the performance with scaling of gate length for a 90 nm node and beyond, a strained Si and SiGe channel was required. The strained Si and SiGe channel enlarges the carrier mobility. On the other hand, over-gate oxide thickness introduces a tunneling issue. to overcome these issues, an alternative dielectric with a higher dielectric constant was required. Hafnium dioxide (HfO_2) is the most promising one to replace SiO_2 for the future generation due to its large band offsets, higher frequency response, and better thermodynamic stability contact with Si [10].

Furthermore, triple gate-based Fin-shaped FET (FinFET) has been introduced to enhance the gate controllability over the channel and optimize the leakage issue. The schematic diagram of conventional FinFET is shown in Fig. 4. FinFETs offered significant improvements in performance and power efficiency compared to previous planar transistor architectures. The Fin-like structure of FinFETs allows better control of current flow, reducing leakage and improving switching speed. For the last decade, FinFET technology has been widely applied across various domains, specifically in mobile devices. The detailed study of FinFET is discussed in the following part.

A. ADVANTAGES OF SOI OVER BULK MOS

Silicon-on-insulator (SOI) offers several advantages over traditional bulk MOS (metal-oxide-semiconductor) structures. SOI devices have a thin layer of silicon considered an active layer which is placed on top of an insulating layer composed of silicon dioxide. This insulating layer decreases the capacitance effect of source and drain regions, resulting in faster switching speeds and lower power consumption compared to bulk MOS devices. Lower capacitance also means that SOI devices generate less heat, making them more energy-efficient. The insulating layer in SOI helps to minimize the leakage current of the transistor when the transistor is in the off state. The SOI structure allows for lower operating voltage levels without compromising performance. This feature reduces power consumption and extends battery life in portable devices. SOI structure can be integrated into existing CMOS fabrication processes with relatively minor modifications, making it easier for semiconductor manufacturers to adopt this technology. SOI technology allows for the integration of both digital and analog circuitry on the same chip with reduced interference between them. This is particularly advantageous for system-on-chip (SoC) designs where digital and analog functions coexist.

B. ADVANTAGES OF DUAL GATE OVER SINGLE GATE

In 1967, Farrah and Steinberg introduced the concept of a dual-gate thin-film transistor [11], while in 1980, Toshihiro Sekigawa pioneered the double-gate MOSFET by demonstrating that sandwiching an SOI device between two connected gate electrodes could significantly alleviate the limitations of SCE [12]. Dual-gate MOS transistors offer many advantages, but they also come with increased complexity in terms of design and fabrication. Dual-gate structures offer several advantages over single-gate, primarily due to their enhanced control over the channel. Dual-gate transistors mitigate these effects by better controlling the channel, reducing leakage currents, and maintaining better electrostatic integrity, which is essential for scaling technology to smaller nodes.

C. EMERGENCE OF VARIOUS SEMICONDUCTOR DEVICES OVER MOSFET

The semiconductor industry is highly dynamic and continually evolving. As new materials, technologies, and application requirements emerge, researchers and engineers will continue to explore and develop various semiconductor devices to meet the ever-growing demands of the electronics industry. Certain applications, such as high-frequency communication, power electronics, and quantum computing, require semiconductor devices tailored to their specific needs. Different devices may offer advantages in these specialized areas. A few emerging semiconductor devices have been discussed in the following part.

A tunnel field-effect transistor (TFET) is [13] and [14] based on quantum mechanics with band-to-band tunneling mechanism. TFET is a gated p-i-n structure, that works on very low gate voltages in reverse bias conditions. TFET can obtain a subthreshold swing value of less than 60mV/dec at room temperature which reduces the power consumption. However, TFET has some shortcomings such as low current,

TABLE 1. Challenges at different technology node.

Node	Best Device	Issue	Solution
<0.1um	Bulk MOSFET	Short channel effect, low drive current	•Strained SiGe •Metal Gate •High K dielectric
0.1um-32nm	SOI MOSFET	Power, leakage current	•Ultra thin body SOI
32nm - 10nm	FinFET	SCE are prominent	•Multi-gate material •Multi-channel •Stacked oxide
<5nm	GAA	Power, Area and Cost	•Multi-bridge channel

delayed output saturation, and the uncontrollable p-i-n forward current, etc. [15] that limit the application in circuits. Dual-gate transistors allow you to independently adjust the threshold voltage of the device by applying different voltages to the front and back gates. This tunability is valuable for optimizing device characteristics for specific circuit requirements.

Carbon Nanotube Field Effect Transistor (CNTFET) [16], [17] is another type of transistor where a single or array of carbon nanotube is used as a channel instead of silicon and it shows superior performance at low gate voltage compared to other semiconductor devices. CNT FET can be scaled to the sub 10nm regime, showing better electron and hole transport properties. Due to the ultrathin dimensionality of CNT FET, the device provides a superb energy gap of 0.6eV to 0.8eV with a minimum short channel effect. CNT FETs mainly operate as Schottky barrier transistors for both n and p modes of transport. Although CNT FET possesses numerous advantages over traditional silicon and other semiconductor materials, their widespread adoption has been hindered by the technology's high production cost [18].

Nanowire Field Effect Transistor (NW FET) has the potential to replace the conventional MOSFET where the channel is made of nanowire [19], [20].The dimension of this nanowire is considered to be 0.5nm. Various materials such as silicon, germanium, composed III-V materials, and II-IV materials are used for the channel. The nanowire FET structure exhibits quantum confinement behavior due to the ultrathin diameter of the nanowire that helps to optimize the short channel effect as much as possible. The potential of nanowire MOSFETs extends beyond future CMOS scaling at advanced technology nodes. Nanowire FETs hold great promise in the field of biomedicine. They can be utilized for real-time monitoring of biological processes within cells, tissues, or organs, enabling advancements in medical diagnostics and personalized medicine. However, researchers need to address challenges related to scalability, reliability, and cost-effectiveness to fully utilize the potential of nanowire FETs in practical devices and systems.

Two-dimensional (2D) materials-based graphene FET (G-FET) [21], [22] is also considered to be a promising candidate for the advanced electronics industry. Graphene as a channel material is accounted for instead of Si in the G-FET configuration. The electrostatic control capability is more in grapheme FET compared to CNT FET. The mobility of charge in 2D materials is very high, and this is very useful for radio frequency applications (RF). Mainly, G-FET can be used as highly sensitive sensors for detecting various gases, chemicals, and biomolecules. The primary hurdle in utilizing G-FET as a semiconductor device lies in its inherent 'zero bandgap' property. This absence of a bandgap makes it challenging to achieve a significant on/off current ratio, leading to difficulties in achieving low power consumption and precise control of the transistor's behavior [23].

The negative gate capacitance (NC) FET has also shown a lot of potential to become an emerging device in the semiconductor industry [24]. The ferroelectric materials are used as dielectric materials instead of the standard insulator in negative gate capacitance FET. HfO_2 is the most commonly used dielectric material doped with Si, Zr, or Al. The ferroelectric capacitor property of NC FET helps to amplify the gate voltage. The NC FET devices can achieve the sub-threshold swing of 60mV/dec owing to low voltage operation like the TFET structure. This semiconductor device is a strong candidate to replace the conventional FET and is mainly used for high-frequency circuits and memory applications.

IV. FINFET: THE WELL-KNOWN 3D TECHNOLOGY

A. EVOLUTION OF FINFET

To optimize the SCEs issue, two different structures were introduced: the first one is a 'fully DEpleted Lean-channel TrAnsistor (DELTA)' and the second is a double gate SOI structure'. In 1989, Hisamato et al. designed and fabricated [25] DELTA structure, which was considered the first FinFET-like architecture. Two significant points were focused on minimizing the short-channel effect. The effective device length should be larger than the depletion width when vertical MOSFET is considered. In the second method, the device thickness should be smaller than the depletion layer where thin-film technology has been used.

In 1992, Hong-Yan et al. [26] proposed a double gate (DG) SOI Si MOSFET structure, and in 1997, Choi et al. [27] fabricated a 30nm ultra-thin-body (UTB) SOI MOSFET device to mitigate the problem faced by the conventional MOSFETs. In 1996, the DARPA (The Defense Advanced Research Projects Agency) launched a program to save Moore's Law for a new device technology of 25nm. In 1998, Hisamato et al. proposed and fabricated [28] a 'folded channel transistor' considered a new variant structure of DG SOI MOSFET. In 1999, Huang et al. [29] fabricated a p-channel-based DG MOSFET structure to mitigate the short channel attributes. They fabricated the device where a gate length and oxide thickness value are considered to be 45nm and 2.5nm. The fabricated device enlarges the performance if the gate length is down to 18nm. Finally, in 1999, Dr. Chenming Hu, a distinguished electrical engineer

and professor in the field of semiconductor devices and technology, discovered FinFET technology. Dr. Chenming Hu proposed two important structures after hearing the DARPA call. One structure was called fully depleted (FD) SOI technology. The other one was 3D FinFET technology where the channel was surrounded by three sides of a gate. In 2000, DARPA and Semiconductor Research Corporation (SRC) showed interest in FinFET technology due to more significant advantages over planar MOSFETs. In 2001, N.Lindert et al. fabricated [30] quasi planar FinFET device to suppress the DIBL effect where Fin width is considered an optimum value than the gate length (2/3 of gate length). In 2002, Yeo et al. introduced and fabricated [31] a spacer lithography-based structure where SiGe Heterostructure is a channel. The introduction of a spacer provides a uniform Fin width. Yu et al. fabricated [32] a double gate-based FinFET device where a gate length and Fin width value are assumed to be 10nm and 12nm. It is noticed that the device has a greater driving current with minimum short channel effects. In 2003, Doyle et al. [33] fabricated fully-depleted (FD) tri-gate (TG) transistors. FD TG transistor fabricated on SOI substrate where gate length is considered 60nm.

B. ADVANCEMENT OF FINFET ARCHITECTURES

In this segment, the next phase of the evolution of FinFET has been discussed. To improve the performance, various innovative structures of FinFET are proposed. The proposed FinFET devices are discussed in brief, along with a fundamental analysis of those structures. To maintain an organized discussion, the proposed architectures are discussed in a paragraph.

In 2005, Vishal et al. designed a double gate (DG) [34] FinFET considering the gate-source/drain (G-S/D) underlap region. The underlap region provides extra source/drain extension length without source/drain paunch-through. The overall effective gate length optimizes the resistances of the source and drain region which helps SCEs. In 2007, Tamara et al. studied [35] and proposed a triple gate FinFET device to observe the gate-to-channel tunneling current and compared the performance of gate leakage current with a quasi planar device where Fin width and gate electrodes are the varying attributes. The study has explored the significance of doped and undoped channels, as well as the importance of gate stacks. It is accounted that a triple gate FinFET device with a narrow Fin width reduces the gate tunneling current compared to the quasi-planar device based on a long Fin width. This decrease applies to both doped and up-doped channels. The HfO_2 gate oxide material is more prominent than SiON for getting less tunneling current from the channel to the gate region.

In 2007, Monoj et al. investigated [36] the impact of high-k dielectric materials in FinFET to observe the device performance. It is noticed that a device with high dielectric materials degrades the short channel parameters. The lesser value of Fin width with high-k dielectric materials improves the short channel parameters performance. Mirko et al. in 2009, proposed [37] a solution to suppress the cornet effect in triple-gate bulk FinFETs. By increasing body doping at the corner site of the FinFET device can optimize the parasitic effect. The suppression of the corner effect helps to mitigate the SCE's performance. Chew et al. in [38] 2014, proposed a High K/Metal Gate (HKMG) FinFET architecture to observe the electrostatic behaviour due to variation of silicon Fin width. It is observed that narrow Fin width decreases gate capacitance value owing to substrate resistance.

In 2015, Pradhan et al. introduced a symmetric high-k spacer hybrid FinFET structure as a means to enhance performance [39]. This hybrid FinFET incorporates an ultra-thin body (UTB) and spacer material with high-k dielectric, built on SOI technology. The proposed device demonstrates superior drain current performance compared to conventional FinFETs and effectively mitigates short-channel effects. Biswas et al. [40] proposed a junction-less accumulation mode (JAM) bulk FinFETs to explore the significance of different spacer materials. The importance of spacer length has been also studied. Simulation results reveal that spacer materials with high-k dielectric offer better performance in the case of analog and RF parameters, and optimizing spacer length enhances various aspects of short-channel effects performance.

Bourcott et al. in 2017, [41] 8nm n-FinFET structure to observe the importance of Fin numbers. 3C-SiC is considered as the channel material whereas Al_2O_3 is assumed as a dielectric material for the gate. It is observed that an increased number of Fin enhances the driving current that improves the transconductance performance. On the other hand, the lower value of Fin thickness reduces the sub-threshold swing, DIBL, leakage current, etc.

Rajesh et al. in 2018 proposed [42] a GaAs-based SOI FinFET device to implement the impact of dielectric material to observe the electrical performance. A comparative analysis between Si conventional and GaAs FinFET devices has been studied. They also proposed a digital inverter to check the delay of the signal. It is observed that GaAs FinFET has improved the drain current performance with minimum SS, DIBL, and leakage current due to its higher mobility properties. However, the average delay of the digital inverter has increased for high k materials.

In 2018, Gaspard [43] studied a bulk FinFET architecture to extract the equivalent oxide thickness (EOT) from accumulation capacitance measurement. An association between surface potential and semiconductor charge is developed to enhance the subband energies above the conduction/valence band. Somjot et al. in 2019 approached [44] Artificial Neural Network (ANN) and Genetic Algorithm (GA) procedure to minimize the power consumption of the architecture of 14nm dual-gate material dual gate dielectric material heterojunction (DGMDGDMHetro) SOI FinFET. They conducted a comparative analysis between ANN-GA and TCAD simulated data and observed that 1.4% error in performance as compared to

simulated data. So, the ANN-GA algorithm can be used in the proposed architecture for optimizing device parameters. Furthermore, it is observed that the suggested device holds promise for applications requiring of consuming of less power and high switching capabilities.

The experimental investigation of subthreshold leakage current in triple-gate FinFETs has been carried out, considering a drain voltage (V_{dd}) of 1 V, focusing on the relationship between Fin width, gate length, and leakage current behavior where gate length and the channel width is the variant parameter [45]. They also studied the impact of sidewall gate and top-gate interface trap charge density. It is noticed that the decreased value of Fin width due to more trap charges present at sidewall gates enhances the leakage current more. In narrow FinFET devices have negligible SCEs when Fin width is considered 25nm.

Aditya et al. [46] examined the diverse short channel parameters in fully depleted (FD) underdoped symmetric SOI FinFETs under both semi-classical and quantum confinement conditions. The findings underscore that optimizing the performance of SCE parameters is more effective when considering the semi-classical case rather than quantum confinements. Hussam et al.in 2019 [47] studied the self-heating effect (SHE) in static random access memory (SRAM) using 14nm FinFET technology. Furthermore, the impact of SHE on negative capacitance (NC) FINFET has been studied. It is observed that the proposed device with SHE, is more compatible than conventional FinFET and it operates at low voltages.

Anju et al. in 2019, [48] Implemented a FinFET architecture with a wavy design on a SOI substrate, incorporating an ultra-thin layer. Wavy FinFET emerges as a novel hybrid device that has improved current driving capability and provides high density While avoiding any compromise on the device's spatial efficiency. Various optimization methods such as gate length, work function, channel length, and spacer materials have been varied to optimize the leakage current and lower threshold value issue. It is demonstrated that the proposed device with a lesser channel length, has reduced the leakage current by 44%. The lower gate work function has reduced the leakage current 35.48%.

Boukott et al. [49] presents the influence of gate length, source/drain concentration, and gate work function on the performance of 3-dimensional tapered 8nm-FinFETs by using the Silvaco TCAD tool. It is concluded that a lesser value of gate length (6nm) enhances leakage current more which affects the transistor efficiency. However, the enhanced value of the work function increases the ON current and response time.

In 2020, Om Prakash et al. proposed a 14 nm NC FinFET and studied the influence of SHE [50]. BSIM-CMG model (Berkeley short-channel IGFET model – common multi-gate) is used to study the SHE from the device to the circuit level. It has been noted that the ferroelectric layer of NC FinFETs remains comparatively cooler than the channel region when subjected to the effects of SHE.

Vinay et al. in 2021, has shown a comparative analysis between GAA FET and bulk Si-FinFET device, considering gate length of 5nm [51]. The comparative analysis stated that in the GAA FET structure, the gate material surrounds the entire channel, providing better control over the flow of electrons compared to FinFETs where the gate covers only three sides of the channel. This results in enhanced electrostatic control and reduced leakage currents. On the other hand, FinFET devices with 5nm nodes show adequate results of SS, DIBL, etc while the large-scale fabrication of GAA FETs would pose substantial challenges. Bhavya et al. 2021 [52] proposed a junction-less accumulation mode gate stack gate all around (JAM-GS-GAA) FinFET to optimize the Fin aspect ratio (AR). It is demonstrated that a lesser value AR helps to optimize the linearity and harmonic distortion and improves the RF/analog performance. It is also noticed that the ON/OFF ratio has improved by 152.37% and reduced the SS by 6.5% owing to its GAA concepts.

Dong-woo et al. in 2021 [53] discussed the influence of dielectric material with various geometric structures in FinFET devices. Buried dielectric thickness is varied to improve power efficiency during electrothermal annealing (ETA). It is noticed that an optimum value of gate length and channel width increases the temperature during ETA as the self-heating effect increases.

C. ANALYTICAL MODELING IN FINFET GEOMETRICS

This section discusses the analytical model of FinFETs available in the literature. Various models such as the drain current model, surface potential model, and short channel effect models have been proposed to date.

Balwinder et al. [54] develops a compact model for drain current and threshold voltage quantum mechanical (QM) in FinFET. This compact model's results are being compared with classical and experimental data. This model helped to predict the FinFET characteristics.

Alexander et al. proposed a model of FinFET device for electrostatic potential. The electrostatic potential model determines the V_{th} and SS performance. The proposed model has solved 3D Poisson's equation.

Rajesh et al. [55] proposed a lightly doped double material gate (DMG) FinFET device and developed a 3D analytical model of electrostatic potential to determine the minimum surface potential, V_{th} and SS shown in Fig.5. It is observed that the proposed model can be used to optimize the DIBL effect and hot carrier effect.

Ritzenthaler et al. [56] fabricated a methodical model of sub-threshold slope characteristics for the Pi-gate multiple-gate FET transistor by considering 3D Laplace's equation. The two critical attributes, SS and DIBL, are measured and compared with the experimental data. The proposed model also determines the scalability of the device.

Romain et al. [57] demonstrated a model for the sub-threshold current of the Pi-gate FET structure. 3D Laplace's

equation develops the model. The sub-threshold current and DIBL are measured and validated with TCAD simulation software. Guangxi et al. [58] demonstrated the analytical model for channel potential, V_{th} and SS of the FinFET device. The surface potential and sub-threshold current model for an underlap dual-material dual gate (DMDG) FinFET are demonstrated by Narendar et al. [59]. This two-dimensional analytical model has been derived by solving Poisson's equation and compared with single material dual gate (SMDG) FinFET. The model results concluded that the increasing value of underlap length decreases the sub-threshold current due to greater gate controllability in DMDG FinFET over SMDG FinFET structure.

Saha et al. in the year 2018 [60], designed a compact 2D model of SS, V_{th} and surface potential for triple material gate (TMG) FinFET device shown in Fig. 6. The proposed model considered 2D Poisson's equation to implement the device characteristics, and the proposed model was validated against TCAD simulation software. Furthermore, the effect of work function is studied in the proposed model.

Jhang et al. fabricated an analytical model of ferroelectric capacitors for NC-FinFET by applying the Preisach model. It is understood from fabricated results that the proposed analytical model exhibits improved SS value for short-channel devices than long-channel devices. A theoretical model for a cylindrical GAA FinFET device is proposed by Rajashree et al. [61]. This theoretical model is solved by two-dimensional Poisson's equation using the superposition principle, and the validity of this model is examined by TCAD simulation software. The model presents surface potential, drain current, V_{th}, and SS performance. It is reported that fabricated results have improved the performance and fabricated results show calibrated with simulation results.

A 3D mathematical model of SOI multigate GAA FinFET, TG FinFET, and DG FinFETs is presented by Vadthiya et al. [62]. The resolution of the analytical model involves applying the superposition method to Poisson's equation for each FinFET, along with the consideration of appropriate boundary conditions. It is understood from these models that GAA FinFET has improved electrostatic control and helps in maintaining better transistor behavior even at smaller device dimensions as compared to other structures.

Abhishek et al. [63] proposed a rectangular gate-all-around (RE-GAA) FinFET, and the proposed model, derived using Poisson's equation and boundary conditions, encompasses the electrostatic potential, SS, DIBL, on current, and off current. The simulated results demonstrate a high level of accuracy in the proposed model.

Shalu et al. [64] designed a 2D mathematical model of channel potential profile and the V_{th} of double gate junction-less (DG-JL) FinFET structure by considering the 2D Poisson's equation. The proposed model includes the influence of the spacer on the electrostatic potential characteristics in the Gaussian channel. The validity of the proposed model is checked by TCAD simulation software.

The surface potential model of the symmetrical and unsymmetrical DG FinFET solves 2D Poisson's equation, which helps achieve the surface potential and V_{th} for the TG FinFET device. This surface potential model is proposed by Suparna et al. [65]. It is seen that high-k HfO_2 dielectric material maintains the same potential value compared to SiO_2 dielectric material.

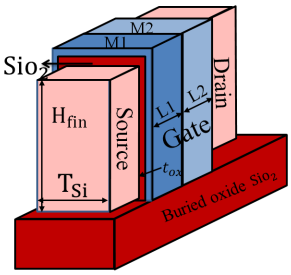

FIGURE 5. Schematic diagram of DMG FinFET.

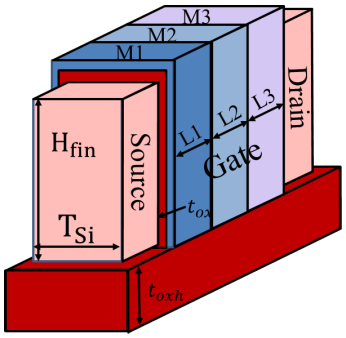

FIGURE 6. Schematic diagram of TMG FinFET.

V. NON-IDEAL EFFECTS ON FINFET

This section primarily explores the importance of temperature, interface trap charges, and diverse noise factors of FinFET devices. The operating temperature of the device has changed with the variation of device dimensions. Temperature, [52] both high and low, can significantly influence impact device performance in terms of efficiency.

C.W. Chang et al. have discussed the SHE and joule heating effects of increasing temperature in the back end interconnect of FinFET device. More heat is produced due to the SHE, which impacts the reliability of the device. They have designed metal sensors of various metal layers in the FinFET device. They have found that increasing the temperature SHE can mitigate the reliability concerns of back-end interconnects of FinFET.

Longxiang et al. [66] have examined the self-heating effect in nano-scale Ge p-channel FinFETs with Si substrate. The self-heating effect is a serious issue that reduces the drain current performance and enhances the leakage issue. The SHE can be minimized by increasing the Fin pitch and decreasing the Fin height. Rajib et al. [67] have proposed

hybrid FinFET and the impact of self–heating effect on the performance of hybrid FinFET is studied. The influence of channel length, Fin width, Fin pitch, etc. is discussed. They have concluded that the SHE increases the gate capacitance. The proposed device reduces the SHE by increasing Fin pitch and increased Fins.

Rinku et al. [68] have studied the significance of temperature in FinFET to observe the SCEs parameter performances. The importance of gate length and dielectric materials is also studied. It is accounted from the simulation results that the FinFET device with high-K dielectric materials, has optimized the SCEs attributes performance for a reduction of gate length value.

Paper [69] has demonstrated a FinFET device where the temperature is the variant parameter and InAs material is considered as channel material. Their study mainly focuses on the switching ratio performance. It is reported that the increased value of temperature reduces the switching ratio of FinFET devices, which degrades performance. They have also observed that InAs material is more immune to temperature stability, and Si material is more suitable for temperature sensitivity.

Ho Le Minh Toan et al. [70] have proposed quadruple gate FinFET and demonstrated various temperature variation performances. It is reported that a device with a low temperature has shown an improvement in SS and DIBL. A device with a high temperature has degraded the RF performance as gate capacitance and transconductance performance increases with high temperature.

Rajesh et al. [71] has observed the RF/analog and linearity parameters performance of DMG FinFET at varied temperatures. It is obtained that the SS value enlarges with temperature whereas the threshold voltage shows the opposite characteristics with temperature. A superior linearity characteristic can be observed as temperature increases.

Nikhil et al. has [72] discussed the DC and RF parameters performance of single material gate (SMG) FinFET. The importance of hybrid spacer raised source and drain extension, and silicide interfaces have been analyzed with temperature variation. They have found that devices with hybrid spacers have lesser static power loss for all temperature variations.

Emona et al. [73] have presented a comparative study between junction-less (JL) and conventional FinFET to observe the analog, linearity, and harmonic distortion performance. It is found that JL FinFET is more immune than conventional FinFET and has provided less harmonic distortion and superior analog performance. Stress engineering is a fundamental technique for improvising CMOS technology's device characteristics. The uniaxial stress effects on mobility and drain current improvement of FinFET are reported by Masumi et al. [74]. They showed that compressive stress can minimize leakage current, whereas mobility can be enhanced by longitudinal stress.

Guo et al. [75] presents an experimental work on the impact of mechanical stress on the fully depleted bulk FinFET. Peo et al. [76] has discussed the stress-induced local new effect (LNE) due to various CT layout designs in 14nm FinFET devices to observe the device performance.

Sojog et al. [77] have studied the band-gap and stress engineering on the performances of the FinFET device to optimize the leakage and OFF current. Paper [78]has checked the reliability issue and self-heating effect (SHE) of 14nm bulk FinFET.

Vincent et al. investigates [79] the stress effect in n FinFET with gate-first and gate-last stacks. It is reported that the tensile stressed Contact-Etch Stop layers (t-CESL) technique on nFinFET structure with gate-last schemes is more effective in improving mobility performance. They also showed that mobility is improved with Fin pitch, where more Fins are used. Short channels nFinFET device with CESL stress technique improves the mobility performance due to the substantial boost of stress compared to planar FET structure.

Geert et al. [80]reported comparing stress on bulk FinFET and planar nFETs by introducing gate-first and gate-last schemes. They reported that the gate-first scheme reduces the efficiency of tensile Contact Etch-Stop Layers (CESL) of bulk FinFET compared to planar nFETs where gate-last schemes increase the efficiency for both bulk FinFET and nFETs.

Sinha et al. [81] proposed a Ge FinFET where SiGe stressor material is added into the source and drain region. The compressive and tensile stress generated owing to SiGe material has been investigated whereas SiGe material length and volumes are varied. It is noted that a stressor length of 15nm created compressive stress which improves the p-channel FinFET performance in terms of drain current.

Pratap et al. [82] developed a junctionless cylindrical surrounding-gate (JL CSG) MOSFET with two configurations: gate material engineered (GME) and single-material gate (SMG), examine their reliability performance in the presence of interface trap charge (ITC) and temperature variation. Furthermore, the various RF, analog, and linearity attributes are studied with temperature variation. The results concluded that GME JL CSG MOSFET has improved the performance specifically for linearity attributes and this configuration is more immune against ITC compared to SMG JL CSG MOSFET configuration.

Bansal and Kaur [83] proposed a Ge-based NC FinFET to observe the influence of fixed trap charges on the voltage transfer characteristics (VTC) performance and compared the performance with conventional Ge FinFET device. It is observed that the NC FINFET device with positive trap charges (PTC) has enhanced the VTC performance whereas the presence of negative trap charges (NTC) demeans the VTC performance.

Paper [84] investigated the impact of interface trap charge on the performance of FinFET devices with different Fin shapes, where variations were made to the Fin or channel shape. Conversely, a random telegraph noise (RTN) is induced due to a single interface trap charge. It is

TABLE 2. Comparative analysis of subthreshold swing (SS) for various semiconductor technologies.

Sl No	References	Device name	SS value , mV/dec
1	Das *et al.* [86]	Multi-Fin FinFET	85
2	Vasanthan*et al.* [87]	Junctionless FinFET	64
3	Espineira*et al.* [88]	GAA FET	71
4	Das *et al.* [61]	GAA FET	110
5	Nagy *et al.* [89]	GAA Nanowire (NW)	68
6	Chabra *et al.* [90]	SOI FinFET	74
7	Sreenivasulu *et al.* [91]	Tri-gate junction-less (TG JL) gate FinFET	68.1
8	Rinku *et al.* [92]	GaAs M-FinFET	72
9	Mitra *et al.* [93]	SOI TFET	62

observed that the amplitude of RTN is lower in the case of trapezoidal Fin than in rectangular Fin shape FinFET device. Suman et al. [85] examine the influence of interface trap charges specifically positive and negative trap charges in GAA MOSFET device. They also studied the impact of high-k dielectric material on the device's performance. It is revealed from the simulation study that GAA MOSFET is affected by the presence of interface trap charges whereas high-K dielectric material $ZrTiO_4$ minimizes the degradation caused by interface trap charges and improves the driving current and analog attributes performance.

Ranjan and Singh [94] have performed a simulation study on interface trap density and interface trap charges in the GAA FinFET device. In the nano-scaled regime, the tunneling current is observed through the Oxide-Silicon interface. AlO_3 and HfO_2 are considered dielectric materials, which minimizes the tunneling issue due to trap charges. It is reported that AlO_3 and HfO_2 are preferable to SiO_2, improving the drain current.

Privat et al. [95] presents an experimental work to investigate the influence of ionizing dose on 14nm bulk FinFETs. The presence of interface trap charges was studied and showed that a device with interface trap charges increases the leakage current. Ho Pee Lo et al. [96] investigates the interface trap impact on the NC FinFET device. It is reported that the NC FinFET device is less sensitive to the trap charges than the baseline FinFET. Talmat et al. [97] has performed low noise frequency versus temperature on the n-channel triple gate FinFET to assess the gate oxide interface's quality and indemnify silicon traps that affect the device performance. The spontaneous fluctuation of the signal is called noise [98] in current or voltage outputs which are the very important factor that limits the quality of device outputs [99]. A systematic study of noise characteristics of GaAs-based FET is carried out by Harman et al.. The noise generated by saturated and unsaturated carriers is calculated.

In 1994. Devide et al. designed a single-stage differential low-noise amplifier and compared the performances between planar bulk and SOI FinFET. It is observed that planar technology exhibits lower power consumption than FinFET, which is very useful for ultra-wideband (UWB) applications. Lim et al. [100] studied random telegraph signal (RTS) with flicker noise (1/f) for GAA p-type Si-FinFETs. They showed that the proposed device had higher RTS amplitudes than conventional MOSFETs due to the scaling property. The systematic study of DC and LF noise behavior in FinFET is discussed by Bennamane et al. [80]. It is found that the variation temperature deteriorates the low field mobility of the device as the gate length is scaled.

The fluctuation of Fin width in low standby power (LSTP) 32nm FinFETs have been demonstrated by Baravelli et al. [101]. The variability of threshold voltage (Vth) and drain current has been extracted through the Monte Carlo statistical approach and sensitivity analysis. It is understood from this work that the performance of drain current depends on the Fin width, and the Monte Carlo approach provides more accurate results of drain current and threshold voltage than sensitivity analysis.

Kushwaha et al. [102] proposed a model for flicker noise in FinFET for various gate length and oxide thickness configurations. It is reported that the proposed model has improved the BSIM CMG compact model for FinFET. A detailed investigation of flicker noise (1/f) in the existence and nonexistence of interface traps in GAA Nanowire MOSFET structure has been investigated by Anandan et al. [103]. The various interface traps for Gaussian, Uniform, and Exponential distribution are also studied. The concluding point from this work is that the increased value of electron density increases the concentration of interface traps, increasing the flicker noise. A uniformly distributed trap enhances the 1/f noise compared to Gaussian and Exponential traps.

A mathematical model for channel thermal noise in FinFET is proposed by Mukherjee and Maiti [104]. Various high-frequency noise attributes such as minimum noise figure, equivalent noise resistance, and optimum source admittance are reported. Mahor and Pattanaik [105] proposed an independent gate (IG) FinFET-based wide fan-in dynamic OR gate to reduce the low noise immunity. It is reported that the proposed design helps to optimize the OFF current by using the back gate technique.

Senthilkumer et al. [106] proposed a design of an operational amplifier using a FinFET device to reduce electromagnetic interference (EMI). The proposed structure added a low-pass filter to remove noise signals. It is concluded from this study that this operation amplifier can minimize almost 75 offset voltage than conventional FinFET devices, and power consumption is also less than the CMOS counterpart.

VI. ALTERNATIVE CHANNEL MATERIALS OVER SILICON FOR PERFORMANCE ESCALATION

Researchers have been exploring alternative materials that have high mobility, wide bandgap, better thermal conductivity, and high density, providing better performance in

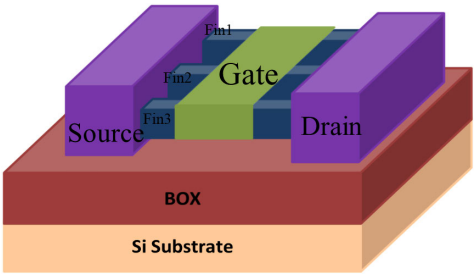

FIGURE 7. Schematic diagram of M-FinFET.

high-power and high-temperature applications. Germanium (Ge) and various III-V materials have the potential to be replacements in future CMOS technology. Germanium (Ge) has garnered significant attention as a potential channel material due to its higher mobility compared to Silicon. Additionally, Ge has a lower energy bandgap, which further enhances carrier current density. One of the key advantages of using Ge as a channel material is its compatibility with existing Silicon process technology. This means that Ge-based CMOS devices can be seamlessly integrated into current manufacturing processes without requiring major change. Some compound materials, like GaN, GaAs, InGaAs, etc. offer improved electron mobility, which results in reduced power consumption and improved efficiency in various applications, including power amplifiers and high-frequency devices. A comparative analysis between SiGe JL-FinFET and Si JL-FinFET has been conducted by Xinlong et al. [107] where doping concentration is varied from 1×10^{19} to 5×10^{19}. It is concluded that SiGe JL-FinFET has improved the hole and electron mobility by 28% and 9%, respectively. the SiGe-based device exhibited significant gains, including a 38% increase in saturation current, a 26%, boost in transconductance, a 45% improvement in intrinsic gain, and a 27% reduction in intrinsic delay when compared to the Si-based device.

Vandana et al. [108] in 2023, has shown a comparison among high-k SOI GaN FinFETs, Bulk GaN FinFETs, and Si FinFETs to observe the performance of DC, analog/RF, and linearity attributes. It is observed that SOI GaN FinFET has enhanced the ON current by 24 times and also achieves an optimal SS value of 66 mV/dec which is 35.9% less than Si FinFET.

Aneesh et al. [109] demonstrated the single-event transients (SET) current model in InGaAs FinFET. This SET model has been derived from 3-D electrostatic potential equations and the results are matched with TCAD simulation results.

Buqing et al. [110] in 2022, has integrated strained Ge channel with Si-based FinFETs to improve the aspect-ratio (AR). A selective epitaxial growth process for Ge material was executed on a patterned substrate using reduced-pressure chemical vapor deposition (CVD). They examined the samples using various techniques like SEM, TEM, EDS, HRXRD, and HRRLMs to study the structure topography,

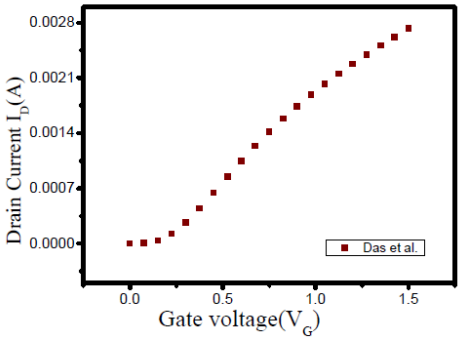

FIGURE 8. Schematic diagram of M-FinFET [93].

defect propagation, and strain distribution in the grown Ge material and observed significant progress in the selective epitaxy of pure Ge on the channels of FinFETs.

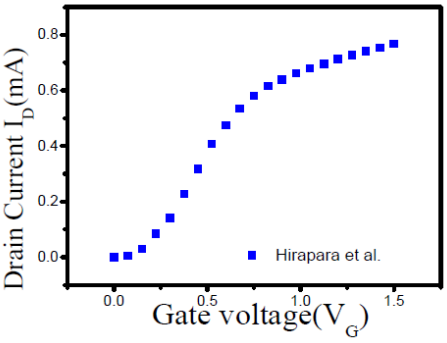

FIGURE 9. Schematic diagram of M-FinFET [149].

Rinku et al. has introduced a GaAs-based M-FinFET device whereas a multiple number of channels are placed in between the source and drain shown in Fig.7. The stress effect on RF/analog performance has been examined. The introduction stress has enhanced the drain current I_{ON} by 159.2%. The V-I characteristic of GaAs based M-FinFET is shown in Fig. 8. It is also noted that the M-FinFET device demonstrates significant enhancements in various analog attributes, including transconductance (G_m), drain conductance (G_d), transconductance gain factor (TGF), intrinsic gain (A_v), and early voltage (V_{EA}), which increase by 251.6%, 231.1%, 46.75%, 20.1%, and 35.2%, respectively, with the introduction of stress effects. Hirapara et al. investigated a multi-Fin FinFET (M-FinFET) to examine its DC and RF/analog performance, as well as the significance of the gate material's work function. We conducted simulations and extracted the V-I characteristics of the M-FinFET using available data, as illustrated in Fig.9. The SS and V_{th} performances for various semiconductor technologies are shown in Fig. 10.

VII. FABRICATION TECHNIQUE OF FINFET

Yu et al. demonstrated the design, manufacturing, performance, and integration challenges encountered in the context

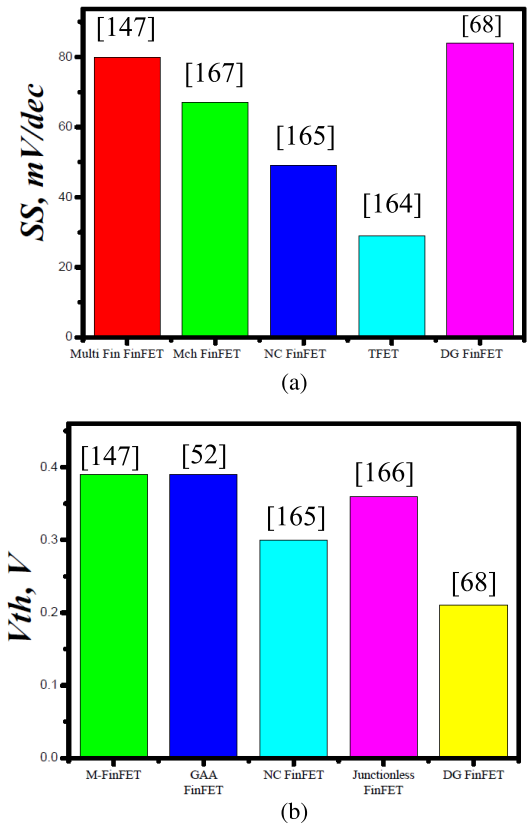

FIGURE 10. (a) SS (b) V_{th} performance of various existing FET devices.

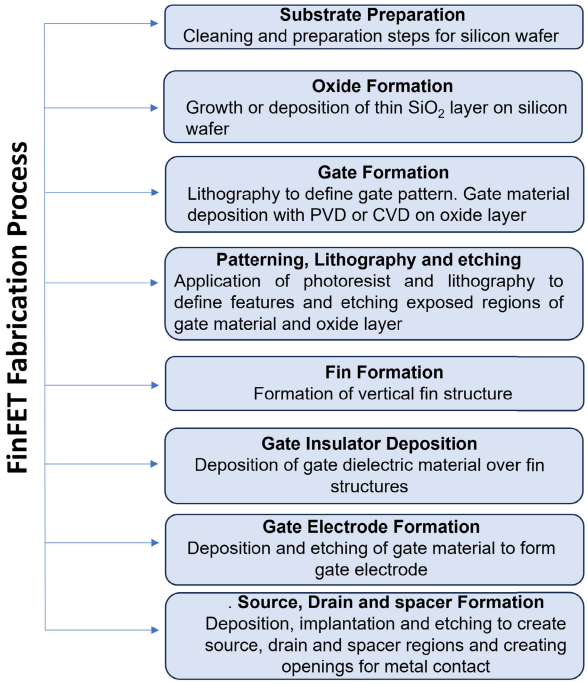

FIGURE 11. Flowchart for the FinFET fabrication process.

of double-gate FinFET in their study. This comprehensive investigation specifically delved into scenarios where the physical gate length underwent a considerable reduction to 10 nm, accompanied by a proportional decrease in the fin width to 12 nm [32]. FinFETs were constructed on SOI wafers employing a customized planar CMOS process. The gate electrodes were dual-doped poly-Si gates, doping achieved through ion implantation and subsequent activation with rapid thermal annealing (RTA). Optical lithography with wavelengths of 193nm and 248nm facilitated the patterning of the Si fin and gate, respectively. Using a pattern reduction technique enabled the attainment of sub-10nm dimensions for both fin width and gate length. The gate insulator comprised a nitrided oxide with a physical thickness of 17 Å. The process features low-temperature source/drain annealing, NiSi, and Cu metallization. The construction of CMOS FinFET inverters, assembled from multiple-fin transistors, was also executed. The fabrication of FinFET, in general involves several key steps in the semiconductor manufacturing process. The fabrication flowchart of FinFET device is shown in Fig. 11

VIII. DEVICE CIRCUIT INTERACTION

FinFETs have gained significant importance in both analog and digital circuit design within the semiconductor industry. FinFET optimizes the SS, V_{th} variation, leakage current, and other various significant SCE characteristics. The driving capability of the device is also improved with a modified FinFET structure which makes FinFET suitable for low-power applications. FinFET can work at lower supply voltage which reduces the dynamic and static power consumption, making them ideal for energy-efficient digital circuits. Additionally, it has lesser variation in threshold voltage, which is an advantage for making analog circuits.

A. DIGITAL CIRCUIT INTERACTION

FinFET devices have emerged as a promising alternative, offering superior gate control and performance compared to traditional CMOS designs in a nano-scaled regime. FinFET technology boasts numerous advantages, including superior optimization capabilities for SCE and greater scalability compared to CMOS technology [111]. FinFET-based SRAM and DRAM memory cells consume less power which increases the battery lifetime.

Rajeev et al. [112] examine 6T SRAM cells utilizing 18nm FinFET technology. analyzed the 18nm FinFET technology-based 6T SRAM cells to optimize the leakage current and compared it with standard conventional MOSFET. The examination primarily focused on power consumption and leakage concerns in FinFET and compared it with the conventional MOSFET configuration. It is accounted that the FinFET technology demonstrates exceptional optimization with a mere power consumption of 16.8μW and an impressively swift delay of 0.4nS, while the MOSFET exhibits significant drawbacks, consuming a substantial 14.2mW and experiencing a delay of 4.3nS. Soumya et al.

implemented [113] various energy recovery logic gates such as 2N2P, 2N-2N2P, PFAL, and DCPAL by using 32nm FinFET technology. A comparative analysis is made between FinFET and standard CMOS devices. It is observed that FinFET-based logic circuits reduced the power consumption by 12%, leakage power 10%, and switching power 11.4% compared to CMOS devices. Soo et al. studied [114] the AC and DC stress for the reliability of 22nm FinFET with the high-k dielectric and metal-gate structure.

Liu et al. [115] proposed Tri Independent Gate (TIG) FinFET in 2017 for 6T SRAM cells and discussed the read stability, speed, write margin, leakage power consumption, and delay in read and write. These electrical characteristics are being compared with conventional SRAM FinFET devices. The results showed that the proposed structure helps to reduce the read-write conflict. Shilpa et al. [116] designed an ST13T SRAM cell based on FinFET technology. The FinFET structure used the power gating technique to develop the ST13T SRAM cell and found that the FinFET-based ST13T SRAM cell offers 12.84 less delays, consumes less power, and improves the speed of the device. Sina et al. [117] designed 8T SRAM cells using FinFET technology by considering the back gate as an independent gate. This work concludes that the proposed work improves the static power, the read SNM, and the write static noise margin. The FinFET-based 8T SRAM cell also provides low leakage with high. Min et al. in 2020 designed a capacitor-less IT dynamic random access memory (DRAM) cell using FinFET technology where Poly-Si material is used for manufacturing the device. The IT DRAM with Poly-Si material was developed in the presence and absence of vertical and horizontal GB. Shalu et al. designed [118] 6T SRAM cells using FinFET technology. The non-uniform Gaussian doping effect has been demonstrated on the output characteristics of JL FinFET. It is reported that Gaussian doped JL FinFET 6T SRAM cell has improved the read/write access time. Waqas et al. [119] has investigated FinFET 6T-SRAM cell to observe the noise margins, read operation, and write operation as these performance measurement parameters are very significant in digital circuit design. They varied the V_{th}, and drain bias, and scaled the device dimensions to get an optimized value of power, area, and performance. Consequently, each cell is categorized as high-density (HD), high-performance (HP), or high-current (HC) to meet specific design objectives. It is observed that HD cell configurations offer less power consumption during read and write operation as compared to other configurations. However,the HC cell configuration demonstrated an efficient write access time of 9.17 ps than HD cell. Joshi et al. demonstrated [120] the FinFET-based SRAM cells with the help of compact simulation models to minimize the delays. Using mixed-mode Taurus simulations, Guo et al. [121] analyzed 6-T and 4-T FinFET-based SRAM cells for cache memory applications with high density and low power consumption at very low voltage. Brad et al. [122] investigated the significance of Fin shape and designed ultra-low power nFinFETs to minimize the leakage current, SS, and V_{th}. Wu et al. [123] designed 16nm FinFET CMOS technology-based high-density (HD) SRAM for mobile applications. This 16nm FinFET CMOS technology increases the speed gain and reduces power consumption. Using extreme ultra-violet (EUV) lithography, Song et al. proposed [124] 7nm FinFET SRAM technology to achieve low power and density at extremely low voltages. An IG-FinFET-based chained new reconfigurable SRAM array for in-memory computing and a non-volatile RRAM array has been proposed by Nemati et al. 50% and 20% improvements in the write energy consumption and CWLM have been achieved compared to the 8T SRAM cell with this architecture [125] Resistive Random-Access Memory (RRAM) is a non-volatile memory device that has less power dissipation compared to SRAM. RRAM cells are more compact, allowing for higher-density memory arrays, which can be advantageous in applications where space is limited. It is reported that a hybrid RRAM/FinFET technology memory cell with 3T1R array architecture has reduced the delay and power consumption [126]. Hsieh et al. proposed a bipolar 14 nm node FinFET RRAM architecture and improved the ON/OFF window along with good endurance and retention performance. FinFET RRAM also reduces standby and active powers [127]. Magnetoresistive random-access memory (MRAM) is a non-volatile memory that stores data in magnetic domains. MRAM [128] is mainly a combination of SRAM and DRAM that offers fast read and write speeds. The integration of MRAM into a FinFET technology [129] offers 10-year retention capability and $>10^6$ write endurance. However, RRAM and MRAM technology is still evolving, and its manufacturing process may not be as mature or widely available as SRAM.

B. ANALOG CIRCUIT INTERACTION

The 3D architecture of FinFET has to get attraction from researchers due to its easy fabrication technique and impressive electrostatic control capabilities. FinFETs can be employed in precision analog applications where low offset voltage, low noise, and high linearity are crucial. Their reduced leakage current and improved SCEs can enhance analog/RF attributes performance. Analog parameters like transconductance (G_m), drain conductance (G_d), transconductance gain factor (TGF) or device efficiency, and intrinsic gain (A_v) are very crucial attributes. The extension of source/drain region [130]and high-k dielectric spacers in the underlap section enhances analog performance under strong inversion biasing conditions.

On the other hand, superior linearity performance is indicated by minimal intermodulation and harmonic distortion at the device's outputs. To assess linearity, various figure-of-merits (FOMs) such as higher-order voltage intercept point (VIP) and current intercept point (IIP), harmonic distortion such as intermodulation distortion (IMD), higher distortion (HD) and the 1 dB compression point are employed. Enhanced linearity and reduced distortion are

achieved when VIP, IIP, and the 1 dB compression point exhibit high values, while IMD and HD are minimized. The higher-order derivative of G_m serves as a key indicator of overall linearity parameter performance. However, FinFET has limited application in analog circuits as compared to traditional MOSFETs. Mohapatra et al. in 2015, studied the significant process parameters of FinFET such as Fin Height (H_{Fin}) and Fin width (W_{Fin}) to design the RF/analog circuit. Another critical parameter, the aspect ratio (AR = W*Fin* / H*Fin*), was also examined, offering valuable insights for the design of FinFET analog circuits. The research highlighted that taller fins are necessary to enhance current drivability, whereas narrower fins contribute to greater immunity against Short-Channel Effects (SCEs).

Jagar et al. in 2018, demonstrated a comparative analysis between 14nm FinFET and 28nm planar FET to analyze the RF and analog parameters performances. It shows that higher value f_t (414/180 GHz)and f_{max} (180/140Ghz) has been noticed for N/P FinFET as compared 28nm planar FET devices. A thin channel body of FinFET optimizes the SCE in terms of DIBL and improves the self-gain (G_m/G_{ds}) and 1/f noise behavior. Jeong proposed [131] 14nm FinFET technology for low-power mobile RF applications. It is observed that 14nm RF FinFET provides higher intrinsic gain and improved quality factor with low DC power dissipation. Lee et al. [132] developed FinFET technology-based Intel 22FFL process technology for RF and mmWave applications. It is noticed that 22FFL boosts f_t and f_{max} by 300GHz and 450GHz respectively, solidifying its position as a superior choice for advanced wireless technologies. Rinku et al. in 2021, proposed a multi-channel FinFET (M_{ch}-FinFET) to examine the temperature variation effect for the RF/analog, linearity, and harmonic distortion characteristics. It is observed that at lower temperatures (300k), the M_{ch}-FinFET improved performance in RF/analog parameters, including G_m, G_d, A_v, TGF and cut-off frequency (F_t). Conversely, as temperature increases, both gate capacitance (C_{gg}) and intrinsic time delay (τ) experience an increase. Additionally, elevated temperatures lead to improved linearity parameters performance which is particularly advantageous for low-power applications. Devenderpal et al. in 2020 [133], studied a detailed analysis of three channel structures: tri-layer stack channel (TLSC), double-layer stack channel (DLSC), and single-layer channel (SLSC) of junction-less tri-gate FinFET to analyze the RF/analog performance. SiGe material is considered for the channel in the proposed device. It is noticed that the TLSC of the proposed FinFET exhibits higher I_{ON} and V_t compared to the other structures. Furthermore, TLSC emerges as a preferred choice for analog applications due to its superior g_m, gain, cut-off frequency, and maximum oscillation frequency. The peak gm of TLSC is 11.9% higher than that of SLC and 29.3% higher than DLSC. Rajeewa et al. [134] 2023, conducted a study focusing on the analog/RF and linearity performance attributes of metal-ferroelectric-insulator-semiconductor (MFIS) based negative capacitance (NC) FinFETs, employing high-threshold voltage (HVT) techniques. This HVT technique has been demonstrated by increasing channel doping (N_{ch}HVT), drain-side underlap modulation (L_{dsu}-HVT), and increasing the channel length (L_g-HVT). They revealed that L_g-HVT technique of NC FinFET offers a minimum value of leakage current with an optimum value of DIBL compared to the other two techniques. It is also noticed that L_{dsu}-HVT led to a remarkable enhancement of f_T, gain-bandwidth product (GBP), and transconductance-frequency product (TFP), increasing by approximately 33.9%, 58.1%, and 50.3%, respectively.

C. APPLICATION OF FINFET IN FUZZY LOGIC SYSTEMS AND NEURAL COMPUTING

The use of FinFET technology into fuzzy logic systems signifies a remarkable progression in the computational intelligence domain. Compared to conventional planar MOSFETs, FinFETs provide better electrical characteristics, including better scalability, lower leakage current, and greater performance [135]. This is due to their unique three-dimensional structure. By utilising these benefits, FinFET applications in fuzzy logic systems show potential for improving processing speed, maximising power efficiency, and facilitating the more precise and accurate realisation of complicated fuzzy logic algorithms. [136] Moreover, the resilience and dependability of fuzzy logic systems are enhanced by the intrinsic variability mitigation capabilities of FinFETs, especially in settings with harsh external impacts or variable operating circumstances.

The hardware proposed by Behbahani et al. had used 28 FinFETs for grayscale image edge detection. The suggested fuzzy hardware showed 81% and 71% reductions in power and energy usage at the circuit level when compared to earlier fuzzy hardware created with the same technology manufacturing node. The suggested hardware is resistant to significant process fluctuations and has a maximum inaccuracy of 5.25%. [137]

FinFETs' capacity to reduce variability adds to the stability and dependability of neural computing systems, allowing for more precise and consistent model predictions in practical applications. By using features like increased switching speed, lower leakage current, and improved scalability, FinFETs can significantly speed up neural network training and inference procedures when used in neural computing systems.

Seo et al. proposed a highly scalable synapse device for neuromorphic applications based on a junction less (JL) ferroelectric (FE) FinFET. Experimental evidence was shown for the synaptic behaviours of the JL metal-ferroelectric-insulator-silicon (MFIS) FinFET. The MFIS synaptic device was used to experimentally confirm synaptic behaviour in the HfZrOx (HZO) based synaptic device after the ferroelectric properties of the HZO film were confirmed using an MFM capacitor. For neuromorphic applications, the pattern

recognition accuracy for handwritten digits was confirmed to be about 80%. [138]

Graphene-based devices can significantly enhance neuromorphic computing and improve applications utilising neuromorphic architecture because of their better mechanical, electrical, and thermal characteristics. Walters et al. described the development of neuromorphic synapses and neurons using graphene-based memristive devices. They have shown that while graphene is often used as an electrode in neuromorphic synapses because of its high conductivity, however it can be used in other neuromorphic settings because of its important neuromorphically relevant properties, including size, endurance, retention, and R_{off} /R_{on} ratio. [23]Jooq et al. have designed leaky integrate and fire (LIF) neuron and spike-timing-dependent plasticity (STDP) circuits using the cutting edge low-power 7nm FinFET technology. The suggested STDP circuit achieves a 68% improvement in total average power consumption and a 43% reduction in energy dissipation in comparison to earlier works, in addition to a 60% space savings. In comparison to its equivalents, the suggested LIF neuron circuit exhibits a 34% area saving, 46% power saving, and 40% energy saving. [139]

IX. LIMITATIONS AND CHALLENGES OF FINFET TECHNOLOGY

As we know, the transition from 22nm to 16nm provoked the semiconductor industry to shift from MOSFET to FinFET technology. However, the ongoing reduction in device dimensions (beyond 3nm) within FinFET technology has exposed it to a range of reliability challenges, including issues like SHEs, negative bias temperature instability (NTBI), positive bias temperature instability (PTBI), and stress-induced leakage current (SILC). These reliability challenges have now become a critical impediment in the processes of modeling, designing, and manufacturing advanced technological devices due to their rigorous nature process requirements [140]. As FinFETs are 3D structures, Ultra Violet (EUV) lithography is required to process the fabrication. However, the current unavailability of this lithography technique necessitates the use of an additional mask for double patterning.

X. GATE ALL AROUND MULTI-BRIDGE CHANNEL FIELD EFFECT TRANSISTOR (GAA MBCFET)

GAA MBC-FET is the ultimate solution that has more than one channel utilized, and each channel is surrounded by gates on all sides that make it a 'GAA' structure shown in Fig.13. The GAA structure (a) Vertical and horizontal view (b) & (c) is shown in Fig. 12. This innovative design significantly enhances gate control capacity over the channels, and it is an efficient solution to mitigate leakage current and advance FinFET technology. The key advantage of MBC-FET lies in its ability to provide better electrostatic control and improved current flow characteristics compared to conventional FinFETs. Due to multiple channels, MBC-FET offers

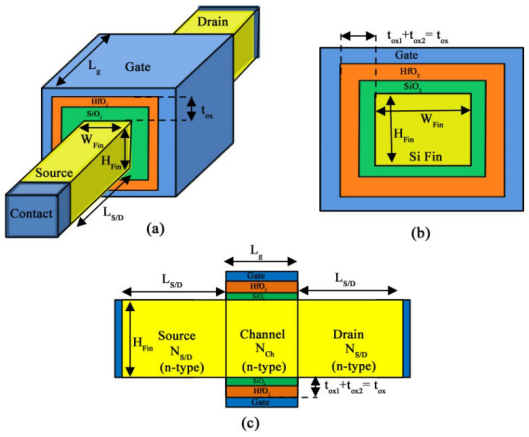

FIGURE 12. Schematic diagram of GAA structure along (a) Vertical and horizontal view (b) & (c).

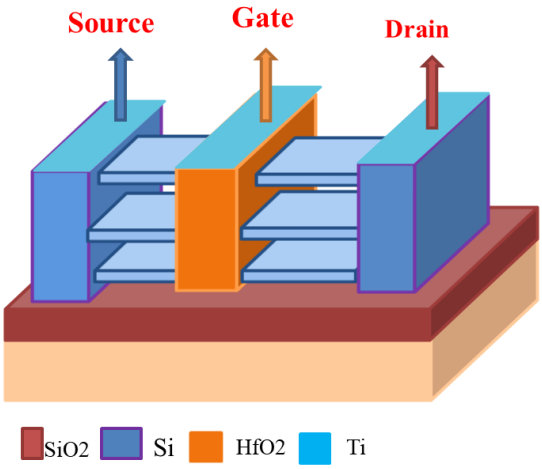

FIGURE 13. Schematic diagram of GAA MBCFET.

increased effective channel width, reducing the resistance and enabling higher current drive capabilities. This leads to improved device performance, such as faster switching speed and lower power consumption. These new structures can maintain the same device footprint without requiring additional space for speed improvement compared to existing FinFET technology. A significant amount of research has been directed towards improving the performance of MBC-FET devices by optimizing their limitations.

Ahmed et al. in 2020 [141] conducted a comparative analysis among existing FinFET, nanowire FET, and proposed MBCFET devices. The study focused on threshold voltage, SS, and ON/OFF ratio as performance metrics. The results concluded that the proposed MBCFET device exhibits a greater switching ratio and optimizes OFF current compared to the existing FinFET and nanowire FET devices. Hitesh et al. in 2022 [142] fabricated a 3-level MBCFET utilizing MoS_2 as the channel material and incorporating both dual-gated and gate-all-around concepts. The device has shown excellent results, including a high saturation current of

174.9 μA, an ideal SS of 63 mV/dec, and a switching ratio exceeding 10^8. Yadav et al. in 2022 [143] studied the effect of work-function (WF) variation on the DC/RF performance of GAA MBCFET. It is noticed from the results that varying the gate WF from 4.4 eV to 4.8 eV greatly reduces the OFF-current (I_{OFF}) by 99%, of the device. However, an increase in gate WF also leads to V_{th} roll-off, a decrease in ON-current by 76%. Bae et al. in 2018 [144] implemented and fabricated the MBCFET through the adaptation of over 90% of FinFET processes. The proposed fabricated device enhances design flexibility with SS of 65mV/dec and higher ON current. The researcher also fabricated a 6T SRAM macro using the MBCFET to test the feasibility and the performance of the 6T SRAM was found to be comparable to that of FinFET SRAM with a similar size. Joung et al. in 2019 [145] proposed a modified version of the MBCFET device by adding a core insulator layer in the channels. This modification was aimed at enhancing the gate controllability over the channels. The performance of the ring oscillator (RO) and SRAM was tested with the proposed structure, and it was found that the performance of both circuits was improved. Affandi et al. in 2022 [146] studied a junctionless (JL) MBC-FET with strained SiGe material concerning the performance of threshold voltage, ON current, and potential distribution along with the channel. The results concluded that JL MBC-FET with higher Ge mole strain led to an increase in the ON-current. However, more research in this direction is required.

XI. FINFETS VS GAA MBCFETS

Here we are going to discuss the advantage of GAA MBCFET over FinFET technology.

A. FOOTPRINT AREA AND SPEED

In FinFET, we can add more Fins that make Multi-Fin FinFET (M-FinFET) configurations [147]. Researchers have devised M-FinFET architectures wherein multiple ''fins'' or channels are positioned in parallel between the source and drain. This addition of fins serves to enhance the device's speed by enabling a higher number of charge carriers to traverse from source to drain simultaneously. The primary distinction between M-FinFET and MBCFET lies in their spatial requirements. M-FinFET demands extra area for each added Fin, whereas GAA MBCFET allows the inclusion of more channels without necessitating additional space. This property of GAA MBCFET contributes to an elevated device speed when compared to M-FinFET.

B. INTERNAL STRUCTURE

In both semiconductor devices, a three-dimensional architecture is employed. In FinFETs, the gate encloses the channel on three sides, while in GAA MBCFETs, the gate surrounds it. This ''gate all around'' concept grants the capability to dynamically alter the channel width, which is a functionality absent in traditional FinFET designs.

C. PRODUCTION

The fabrication of both FinFETs and GAA MBCFETs can be achieved using identical process tools and manufacturing procedures. This eliminates the necessity for additional external tools to manufacture GAA MBCFET technology. As a result, the implementation of this new technology can be seamlessly integrated without incurring extra costs.

D. LOW LEAKAGE CURRENTS, OPERATIONAL VOLTAGE, AND DYNAMIC POWER

As the gate in FinFETs surrounds solely three sides of the channel, it leads to one side being without gate control. Conversely, in the context of GAA MBCFET, all sides of the channel are enveloped by gates, substantially enhancing the electrostatic gate control capacity and consequently reducing issues related to leakage. When comparing FinFET and GAA MBCFET technologies, the semiconductor industry will shift from FinFET technology to GAA MBCFET technology very soon.

Using FinFET and GAAFET technology in power management methods has led to a change in the optimization of energy efficiency in electronic systems [148], [149]. Dynamic voltage and frequency scaling (DVFS) is made possible by the unique three-dimensional structure of FinFETs and their improved gate control capabilities [150], [151]. This allows for effective power allocation that is adapted to workload needs. Additionally, FinFET is especially well-suited for low-power applications because of its built-in leakage power reduction techniques [152], [153]. The gate-all-around design of GAAFETs provides unmatched scalability and gate control, opening the way to voltage scaling and adaptive body biassing. Power management systems can realize previously unheard-of levels of energy efficiency by utilizing the special qualities of FinFET and GAAFET, meeting the urgent requirement for high-performance, environmentally friendly electronics in a variety of applications. Power management systems can realize previously unheard-of levels of energy efficiency by utilizing the special qualities of FinFET and GAAFET, meeting the urgent requirement for high-performance, environmentally friendly electronics in a variety of applications.

XII. PRACTICAL CHALLENGES OF GAA MBCFET FABRICATION TECHNOLOGY

GAAFETs involve a more complex fabrication process compared to traditional FinFETs [154]. The manufacturing process needs to be refined and optimized to ensure high yields and cost-effectiveness. GAAFETs typically use nanowires and nanosheets as the channel material [155]. Achieving uniform and precise nanowire formation is crucial for device performance. Controlling the diameter, length, and placement of these nanowires with high precision is a challenge [156]. The choice of materials for the various layers in GAAFETs must be compatible with the fabrication

process [157]. Ensuring that the materials used are stable, have good electrical properties, and can be integrated seamlessly is a significant challenge. The processes for etching and deposition in GAAFET fabrication need to be highly precise [158]. Any variations in these processes can lead to defects and impact transistor performance. The gate dielectric is a critical component in transistor performance [159]. Achieving a high-quality gate dielectric with low leakage and high capacitance is challenging. Insulator materials need to be carefully chosen to ensure the desired properties. The formation of low-resistance contacts is crucial for efficient electron flow in GAAFETs [154]. Minimizing contact resistance while ensuring reliability poses challenges in the fabrication process. As GAAFETs are introduced, integrating them with existing semiconductor technologies and ensuring compatibility with established processes can be a challenge. This is particularly important for large-scale manufacturing and industry adoption. As the semiconductor industry moves towards smaller nodes, scaling GAAFET technology becomes challenging. Issues such as quantum effects and increased sensitivity to manufacturing variations can become more pronounced at smaller scales [160].

A. CHANNEL FORMATION

GAAFETs typically use silicon as the channel material. The equipment required for channel formation includes:

- Deposition Tools: Chemical vapor deposition (CVD) or atomic layer deposition (ALD) systems are commonly used for depositing thin films of semiconductor materials to form channel.
- Etching Tools: Reactive ion etching (RIE) or other advanced etching techniques are employed to define and shape the nanowires

B. GATE FORMATION

The gate in GAAFETs surrounds the channel from all sides. The equipment used for gate formation includes:

- Lithography Tools: Photolithography or advanced lithography techniques are used to define the gate pattern on the substrate.
- Deposition Tools: Physical vapor deposition (PVD) or chemical vapor deposition (CVD) systems are used to deposit the gate material conformally around the nanowire.

C. GATE DIELECTRIC FORMATION

The gate dielectric is a critical insulating layer between the gate and the channel material. Equipment for gate dielectric formation includes:

- Deposition Tools: ALD or PVD systems for depositing high-quality dielectric materials with precise thickness.
- Annealing Tools: Thermal annealing processes are often used to enhance the properties of the gate dielectric.

D. SOURCE AND DRAIN FORMATION

The source and drain regions are where the current flows into and out of the channel. Equipment for source and drain formation includes:

- Implantation Tools: Ion implantation systems are used to introduce dopants into the substrate to create the source and drain regions.
- Annealing Tools: Rapid thermal annealing or other annealing processes are employed to activate dopants and repair any damage caused during implantation.

E. CONTACTS AND INTERCONNECTS

Metal contacts and interconnects are crucial for connecting the transistor to the broader circuit. Equipment for contact and interconnect formation includes:

- Deposition Tools: PVD or CVD systems for depositing metal layers for contacts and interconnects.
- Lithography Tools: Photolithography for defining patterns for metal contacts and interconnects.

Continued advancements in lithography techniques are essential for achieving smaller feature sizes in GAAFET fabrication. Techniques such as extreme ultraviolet (EUV) lithography are increasingly being explored to overcome the challenges associated with traditional optical lithography [161]. Etching plays a critical role in defining the structures in GAAFETs. Advanced etching techniques, such as cryogenic and plasma-based etching, are important for achieving high precision in shaping nanowires and other features.

The fabrication process of GAAFET initiates with the creation of alternating layers of silicon and silicon-germanium (SiGe), which are patterned into pillars. While establishing the Si/SiGe heterostructure and patterning pillars closely align with conventional fin fabrication, subsequent steps are uniquely tailored for nanosheet transistors [162]. A critical innovation involved introducing an indentation in the SiGe layers to accommodate an inner spacer between the source/drain regions, defining the gate width. Following the placement of inner spacers, a channel release etch selectively removes the SiGe. Subsequently, atomic layer deposition (ALD) is employed to deposit the gate dielectric and metal into the spaces between silicon nanosheets. The germanium content in the SiGe layers is minimized to mitigate lattice distortion and defects. However, optimizing the germanium content presents a challenge, as higher germanium concentrations enhance etch selectivity but risk erosion of silicon layers during critical fabrication steps. This study presents a novel approach to address the challenges associated with the vapor phase HCl etch process, which conventionally results in a half-moon meniscus shape along the etch front. The research conducted at IBM Research and TEL Technology Center demonstrates a remarkable 150:1 selectivity for $Si_{0.75}Ge_{0.25}$ relative to silicon, featuring a rectangular etch front. This advancement significantly enhances dimensional control, leading to superior device

TABLE 3. Comparative analysis of electrical performance for various semiconductor technologies.

Reference	Device Structure	Channel material	Device dimensions	Device parameters performance
Das *et al.* [68]	Double Gate (DG) FinFET	Silicon	L_g=25nm V_D=0.525V, T_{ox}=2nm,	I_{ON}= 0.0012 mA, SS=84mV/dec DIBl= 88 mV/V, V_{th}=0.21V
Ghosh *et al.* [164]	Ferro electric L-patterned gate TFET	Silicon	L_{ch}=40nm V_D=0.525V, T_{ox}=2nm,	I_{ON}= 0.00045 mA, SS=29mV/dec, Switching ratio 5.8x1011,
Saha *et al.* [165]	NC FinFET	Silicon	L_g=30nm, T_{ox}=1nm, V_{DS}= 0.5 V,	I_{ON}=0.001mA, SS=49.1mV/dec, V_{th}=∼0.3V,
Chhabra *et al.* [166]	GaAS junctionless FinFET	GaAs	L_g=20nm, T_{ox}=2nm, V_{DS}= 0.1 V,	I_{ON}=0.04mA, switching ratio=1.2x10^{16} V_{th}= 0.36V,
Das *et al.* [167]	Ge Mch-FinFET	Ge	L_g =7nm T_{ox}=1nm and V_D =0.5V, T=300K	I_{ON} =10.92mA, SS=67.1mV/dec, G_{mpeak} =14.48mS, $I_{ON}/_{OFF}$ =9.4x10^{14}
Myoungsu *et al.* [168]	SOI U-shaped FinFET	Silicon	L_g =16nm,V_D =0.7V, EOT=1.05,	I_{ON}=0.1mA G_{mpeak} =0.65mS,TGF=40^{-1}
Saha *et al.* [147]	Multi Fin FinFET (M-FinFET)	Silicon	L_g =30nm T_{ox}=1.5nm,V_D =0.5V,	=4.5eV, SS=79.92mV/dec, V_{th}=0.39V, I_{ON} =0.01mA
Jo *et al.* [169]	GAA MBCFET	$In_{.53}Ga_{.47}As$ nano sheets,	Lg =130nm, Wns=300nm, Tns=15nm	G_{mmax}=5.7 mS/m, I_{ON} = 2.2 mA/m, V_{DS} =0.8V
Kumar *et al.* [52]	GAA FinFET	Silicon	L_g =7nm, T_{ox}=1nm, V_D =0.5V, T=300K,	I_{ON} =0.19mA, SS=105mV/dec, V_{th}=0.39V, switching ratio=1.2x10^4, G_{mpeak} = 0.037mS, TGF= 45^{-1}

yield and reduced variability for both n-type and p-type transistors.

F. STRAIN ENGINEERING

GAAFETs often employ strain engineering to enhance carrier mobility, which adds an additional layer of complexity [163]. The fabrication process must carefully introduce strain into the nanowires without compromising the structural integrity of the device. The optimization of carrier mobility in highly scaled planar transistors relies heavily on strain engineering. While this technique has proven effective in two-dimensional structures, its application becomes notably more intricate in three-dimensional devices due to their complex geometry. In the context of nanosheet transistors, the introduction of strain is inevitable owing to the lattice mismatch between silicon and SiGe. However, the impact of this strain remains uncertain, and whether it will yield positive or negative effects is yet to be conclusively determined.

TABLE 4. Comparative analysis of electrical performance for various semiconductor technologies at Lg 5-8nm.

References	Device Structure and Materials used	Parameters
Kumar *et al.* [52]	GS GAA FinFET (Si as channel, TiN as gate material, HfO_2+SiO_2 as dielectric constant)	L_g=7nm, T_{ox}=1nm, V_D=0.5, T=300K, I_{ON}=0.019mA, G_{mpeak}=0.037mS, SS=105mV/dec, TGF=$45V^{-1}$, switching ratio=1.2x10^4
Das *et al.* [167]	Mch-FinFET (HfO_2: dielectric constant and Ge as a channel)	L_g =7nm T_{ox}=1nm and V_D =0.5V, T=300K, I_{ON} =10.92mA,SS=67.1mV/dec, G_{mpeak} =14.48mS, $I_{ON}/_{OFF}$ =9.4x10^14
Narendar *et al.* [170]	HS hybrid FinFET (HfO_2+Si_3N_4 as High-K and low-K spacer)	L_g=5nm,T_{ox}=1nm, V_D=0.7V I_{ON}=0.006mA, SS=64.8mV/dec, TGF=$40V^{-1}$, G_{mpeak}=0.015mS,
Kumar *et al.* [90]	GaN SOI FinFET structure (ZrO_2: dielectric constant and GaN as channel)	L_g=8nm, T_{ox}=1nm V_D=0.1V,I_{ON}=0.9mA, TGF=$135V^{-1}$ G_{mpeak}=0.9mS, switching ratio=5x10^9, V_{th}=0.6065V
Das *et al.* [171]	GAA FET (Si as channel)	L_g =8nm, EOT=0.57nm, I_{ON} =14um, SS=110mV/dec, DIBL=150mV, I_{OFF} =10nA

XIII. PRESENT INDUSTRY SCENARIO OF GAA MBCFET TECHNOLOGY

Samsung is the first semiconductor foundry that revealed the first chip based on this groundbreaking manufacturing methodology in the summer of 2022, called GAA MBCFET, and planning to shift from FinFET to GAA MBCFET technology very soon. Additionally, Samsung is on track to introduce its second-generation 3nm chips in 2023. In parallel, TSMC is aiming to develop 2nm GAA chips by approximately 2026. Similarly, Intel is also set to launch 2nm GAA chips around 2024. However, both TSMC and Intel are still manufacturing chips using FinFET technology. The comparative analysis of electrical performance for various semiconductor technologies as tabulated in table 3. The comparative analysis of various FET technologies, whose gate lengths is considered from 5 to 8 nm are tabulated in table 4

XIV. CONCLUSION

This review article offers an insightful look into the ongoing topic 'FinFET' technologies by providing a comprehensive overview of the progress in modified architecture, existing trends, and associated constraints. The importance of other semiconductor materials instead of Silicon has been highlighted in a thorough discussion. The article conducts a thorough examination of the emerging 'GAA MBCFET' technology, addressing both its prominent drawbacks and the challenges encountered during fabrication in a detailed discussion. Additionally, recent advancements in GAA MBCFET development are prominently featured.

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