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RESEARCH ARTICLE

Investigations on $In_{0.12}Al_{0.88}N/AlN/Al_xGa_{1-x}N/In_{0.12}Al_{0.88}N$ MOS-HFETs With Symmetrically-Graded Wide-Gap Channel and Drain Field-Plate Design

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ABSTRACT Novel $In_{0.12}Al_{0.88}N/AlN/Al_xGa_{1-x}N/In_{0.12}Al_{0.88}N$ metal-oxide-semiconductor heterostructure field-effect transistors (MOS-HFETs) grown on a SiC substrate with a drain field-plate (DFP) were investigated. A symmetrically-graded $Al_xGa_{1-x}N$ ($x = 0.32 \rightarrow 0.1 \rightarrow 0.32$) wide-gap channel with an $In_{0.12}Al_{0.88}N$ back-barrier was devised to enhance the carrier confinement, channel conductivity, and breakdown characteristics. The MOS-gate structure, employing high-k Al_2O_3 gate dielectric and surface passivation deposited by the non-vacuum ultrasonic spray pyrolysis deposition (USPD) technique, has resulted in enhanced gate modulation and decreased gate leakage current. A control MOS-HFET (sample A) with an equivalent $Al_{0.21}Ga_{0.79}N$ channel and DFP was fabricated in comparison with the present design without/with DFP (samples B1/B2). The present sample B2 (A) has demonstrated a superior maximum drain-source current density ($I_{DS,max}$) of 937.4 (838.8) mA/mm, maximum extrinsic transconductance ($g_{m,max}$) of 89.6 (80.6) mS/mm, on/off-current ratio (I_{on}/I_{off}) of 1.8×10^8 (1.3×10^8), two-terminal off-state gate-drain breakdown voltage (BV_{GD}) of −530 (−490) V, three-terminal on-state drain-source breakdown voltage (BV_{DS}) of 520 (465) V at 300 K, and the corresponding Baliga's figure-of-merit (BFOM) of 79.5 (39.3) MW/cm^2. The present design is promising for high-voltage power-switching circuit applications.

INDEX TERMS Symmetrically-graded channel, wide-gap AlGaN channel, InAlN back-barrier, MOS-HFET, Al_2O_3, ultrasonic spray pyrolysis deposition, drain field-plate.

I. INTRODUCTION

GaN-based heterostructure field-effect transistors (HFETs) have been extensively studied for radio frequency (RF) power amplifier (PA), low noise amplifier (LNA), and high frequency switching applications [1], [2], [3], [4], [5], [6], [7] due to the advantageous properties of high electron mobility, high threshold electric field, and wide bandgap of GaN. Recently, with the growing demands for high-voltage operation in vehicle electronics [8] and renewable energy [9], AlGaN with higher Johnson's figure-of-merit (JFOM) [10] and Baliga's figure-of-merit (BFOM) [11] has been used as the channel recipe for metal-oxide-semiconductor HFETs (MOS-HFETs) [12], [13], [14], [15], [16]. As compared to GaN channel devices, the wide-gap AlGaN channel devices have demonstrated improved high-voltage power switching performance. Various AlGaN-channel MOS-HFETs have been studied in our previous works, including:

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(1) increased carrier density with intentionally doped AlGaN channel [12], [13], [14], (2) reduced contact resistance with optimum recess depth within source/drain regions [12], (3) enhanced carrier confinement by using step-graded channel design [13], (4) improved surface properties by using an in-situ SiN passivation layer [13], (5) reduced gate leakage current and suppressed surface scattering effect with oxide passivation [12], [13], [14], [15], [16], and (6) improved carrier transport and enhanced spontaneous polarization by devising lattice-matched InAlGaN barrier/buffer layers [16]. This work presents, for the first time, $In_{0.12}Al_{0.88}N/AlN/Al_xGa_{1-x}N/In_{0.12}Al_{0.88}N$ MOS-HFETs with integrated designs of a symmetrically-graded wide-gap $Al_xGa_{1-x}N$ ($x = 0.32 \rightarrow 0.1 \rightarrow 0.32$) channel to improve the channel conductivity, an in-situ Si-doped n-GaN capper ($Si = 3 \times 10^{18}$ cm^{-3}) to effectively reduce the contact resistance, an $In_{0.12}Al_{0.88}N$ back-barrier to suppress the substrate leakage, an MOS-gate structure [17], [18] to reduce gate leakage current and improve gate modulation capability, and a drain field-plate (DFP) structure [19], [20], [21] to improve the breakdown voltage. A reference MOS-HFET with an equivalent $Al_{0.21}Ga_{0.79}N$ channel compound was fabricated in comparison.

II. MATERIAL GROWTH AND DEVICE FABRICATION

Figs. 1(a)-(c) show the device schematic structures of (a) the control $In_{0.12}Al_{0.88}N/AlN/Al_{0.21}Ga_{0.79}N/In_{0.12}Al_{0.88}N$ MOS-HFET with DFP structure (sample A) and (b)/(c) the present $In_{0.12}Al_{0.88}N/AlN/Al_xGa_{1-x}N$ ($x = 0.32 \rightarrow 0.1 \rightarrow 0.32$)/ $In_{0.12}Al_{0.88}N$ MOS-HFET without/with DFP structure (samples B1/B2), respectively. The epitaxial structures were grown on a SiC substrate by using a low-pressure metal-organic chemical vapor deposition (LP-MOCVD) system. Samples B1 and B2 have the same epitaxial layer structures, as shown in Figs 1(b)-1(c). Upon the SiC substrate, the layer structure includes a C-doped high resistivity (HR) GaN buffer, an intrinsic 10-nm $In_{0.12}Al_{0.88}N$ back-barrier, an intrinsic 20-nm symmetrically-graded $Al_xGa_{1-x}N$ ($x = 0.32 \rightarrow 0.1 \rightarrow 0.32$) channel, an intrinsic 1-nm AlN interlayer, an intrinsic 10-nm $In_{0.12}Al_{0.88}N$ barrier, and a 2-nm Si-doped ($\sim 3 \times 10^{18}$ cm^{-3}) GaN capper. As shown in Fig. 1(a), the control sample A has the same layer structures as samples B1/B2, except for replacing the $Al_xGa_{1-x}N$ channel with a 20-nm $Al_{0.21}Ga_{0.79}N$ channel. The Al-ratio of 0.21 was equivalent to the average Al-ratio of the symmetrically-graded $Al_xGa_{1-x}N$ ($x = 0.32 \rightarrow 0.1 \rightarrow 0.32$) channel. All samples were fabricated at the same time by using conventional photolithography and lift-off processing [22]. For the device fabrication of sample B2, mesa etching was first performed to provide device isolation by using an inductively coupled-plasma reactive ion etcher (ICP-RIE). The etching gas was BCl_3 at a flow rate of 40 sccm with the ICP/RF power settings of 110/110 W, respectively. The chamber pressure was maintained at 1 Pa. After photolithography, the 2-nm n-GaN capper between the source and drain regions was etched away to prevent parallel conduction.

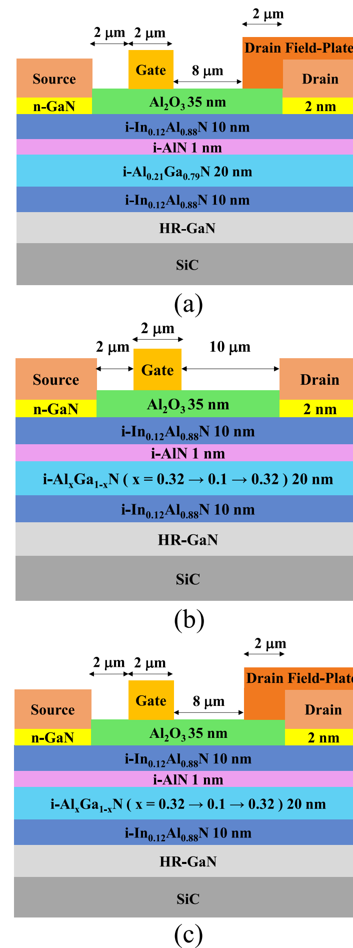

FIGURE 1. Device schematic structures of (a) the control MOS-HFET (sample A) and (b)-(c) the present symmetrically-graded channel MOS-HFET design without/with DFP (samples B1/B2).

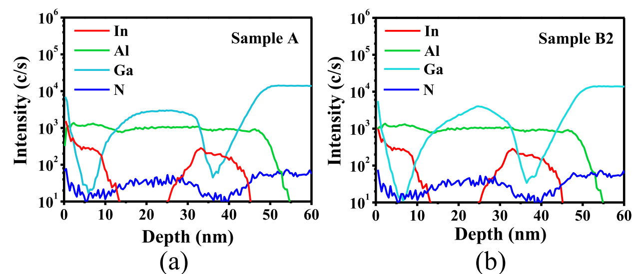

FIGURE 2. The SIMS profiles of the epitaxial structures for samples (a) A and (b) B2.

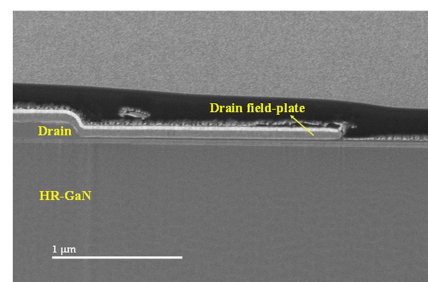

FIGURE 3. The SEM photo of the DFP structure of sample B2.

The mixed etching gases were BCl_3/Cl_2 at flow rates of 10/5 sccm with the ICP/RF power settings of 110/12 W. Metal stacks of Ti (20 nm)/Al (100 nm)/Ni (20 nm)/Au (80 nm) were evaporated as the source/drain electrodes. The sample was subsequently annealed for 30 seconds at 900°C to form the ohmic contacts by using an ULVAC MILA-5000 rapid thermal annealing system (RTA). Then, a 35-nm thick Al_2O_3 layer was deposited by using the ultrasonic spray pyrolysis deposition (USPD) technique to serve as both surface passivation and gate dielectric at the same time. Finally, Ni (100 nm)/Au (75 nm) metal stacks were evaporated after photolithography to simultaneously form both the gate and DFP structures, as shown in Fig. 1(c). The same device fabrication procedures were applied to samples A and B1, except that sample B1 was fabricated without DFP. As shown in Figs. 1(a)-(c), all samples has the same gate length (L_G) of 2 μm and gate-to-source spacing (L_{GS}) of 2 μm. The DFP length (L_{DFP}) of samples A and B2 was 2 μm with gate-to-drain spacing (L_{GD}) of 8 μm, whereas the L_{GD} was 10 μm for sample B1 without DFP. Figs. 2(a)-(b) illustrate the secondary ion-mass spectrometry (SIMS) profiles for the epitaxial structure of samples A and B2 without device fabrication. It is noted that the corresponding reduction of Al-intensity was not observed with the increased Ga-profile within the $Al_xGa_{1-x}N$ graded channel in sample B2. It was mainly due to the matrix effect [23]. The primary ion source for characterizing the Al-profile was Cs^+ 5 keV. The Cs^+ ion intensity normalized by sputter rates would increase with decreasing AlN mole fraction x in $Al_xGa_{1-x}N$. The characterized SIMS profiles have verified the heterostructural designs of the studied samples. Fig. 3 shows the scanning electron microscopy (SEM) photo of the DFP structure for sample B2. The L_{DFP} length was also verified to be 2 μm as devised.

III. EXPERIMENTAL RESULTS AND DISCUSSION

The epitaxial structures for both samples B1 and B2 are the same. Hall measurement was performed on samples A and B2 at room temperature under a magnetic field of 5000 G. The electron mobility (μ_n) and two-dimensional electron gas (2DEG) concentrations (n_{2DEG}) were determined to be 478 (282) cm^2/V-sec and 2.7 (3.5) $\times$ 10^{13} cm^{-2} for sample B2 (A). Similar n_{2DEG} concentrations were obtained since both devices had the same averaged Al-composition in the AlGaN channel. Fig. 4 shows the calculated band diagrams for samples A and B1/B2 by using SILVACO simulation tool. According to the Fermi level (E_F) position, the electrons were effectively confined within the devised channel structure for all three samples. Besides, the channel electrons of sample B2 was confined near the central region (x = 0.1) of the devised graded-channel. Since lower Al ratio of $Al_xGa_{1-x}N$ has exhibited higher μ_n, the measured μ_n in sample B2 was higher than sample A. Consequently, higher μ_n-n_{2DEG} product of 1.29 $\times$ 10^{16} $(V\text{-sec})^{-1}$ in sample B2 was obtained than 0.99 $\times$ 10^{16} $(V\text{-sec})^{-1}$ in sample A. The improved channel conductivity is beneficial to enhance current densities and reduce contact resistance for sample B2. Fig. 5 shows the measured C-V characteristics at 1 MHz for the fabricated Schottky-diode and MOS-diode by using the same epitaxial

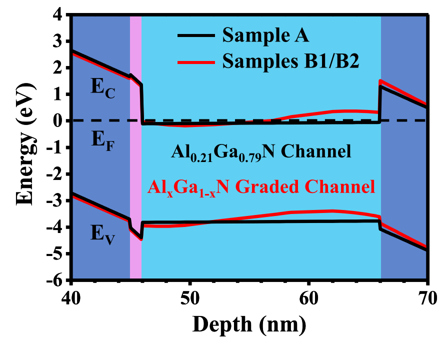

FIGURE 4. The calculated band diagrams for samples A and B1/B2 by using SILVACO.

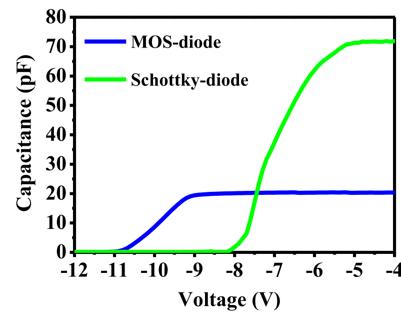

FIGURE 5. The measured C-V characteristics for Schottky-diode and MOS-diode at 1 MHz.

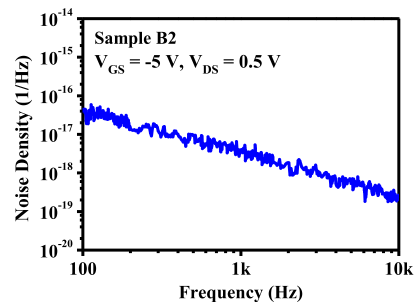

FIGURE 6. Low-frequency 1/f noise spectra of sample B2 at 300 K.

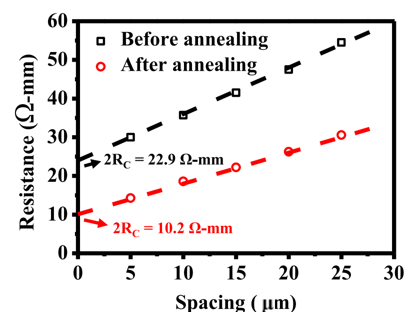

FIGURE 7. TLM characterization for the source/drain ohmic contact before/after annealing.

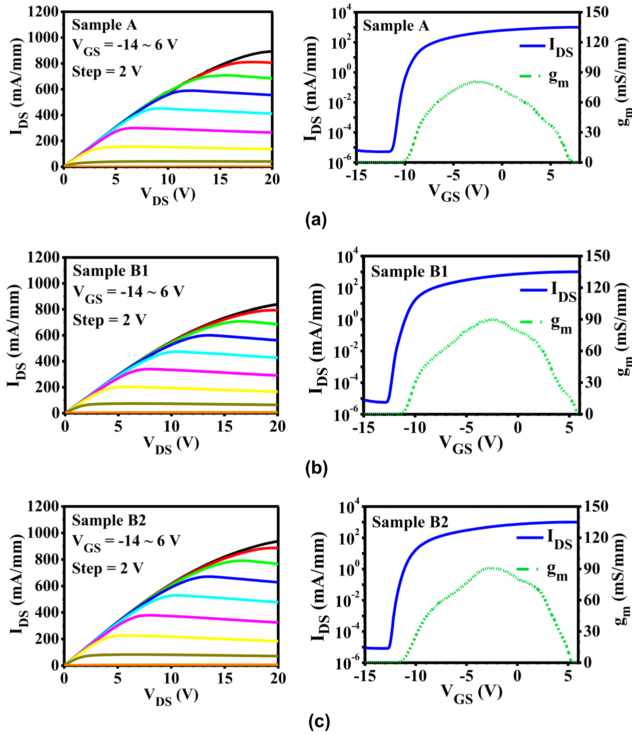

FIGURE 8. Common-source I_{DS}-V_{DS} characteristics (left) and the transfer I_{DS}/g_m-V_{GS} characteristics (right) at V_{DS} = 20 V of samples (a) A, (b) B1, and (c) B2 at 300 K, respectively.

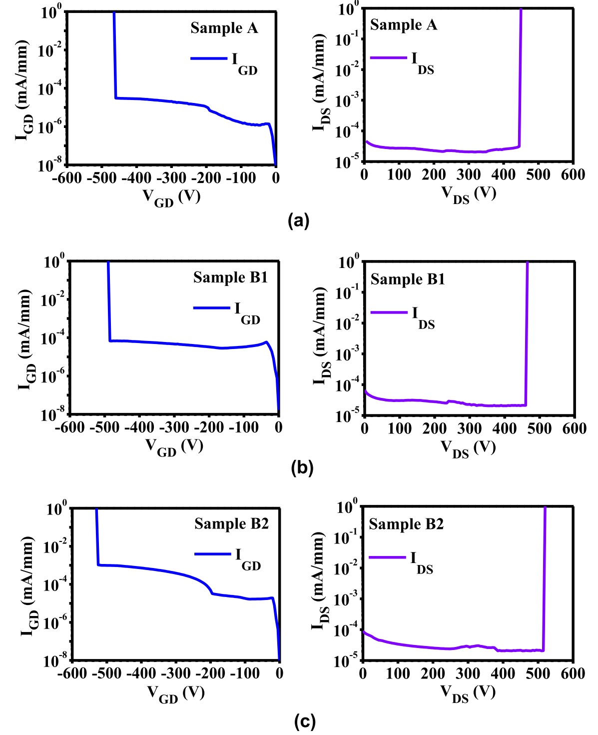

FIGURE 9. BV_{GD} (left) and BV_{DS} (right) characteristics of samples (a) A, (b) B1, and (c) B2 biased at $V_{GS} = -15$ V and 300 K, respectively.

structure of sample B2. The diode area (A) was 11781 μm^2, and the oxide thickness (d_{ox}) of the USPD-grown Al_2O_3 was 35 nm. The MOS-diode capacitance (C_{MOS}) is equivalent to the series connection of the depletion capacitance (C_{dep}) and the oxide capacitance (C_{ox}), as shown below.

$$\frac{1}{C_{MOS}} = \frac{1}{C_{ox}} + \frac{1}{C_{dep}} \quad (1)$$

C_{MOS} and C_{dep} measured from the MOS-diode and Schottky-diode, respectively, were 20.3 pF and 71.8 pF. C_{ox} was calculated to be 28.3 pF. The dielectric constant (k) of the Al_2O_3 was characterized to be 9.5.

Fig. 6 shows the *1/f* noise spectra of sample B2 measured by using an Agilent 35670A amplifier and a BTA 9812B spectrum analyzer within the frequency range of 100 Hz ∼10 kHz. The device was biased in the linear region with $V_{GS} = -5$ V and $V_{DS} = 0.5$ V. The Hooge coefficients (α_H) at $f = 100$ Hz was extracted [24] to be 3.2×10^{-6} with the corresponding noise density of 3.9×10^{-17} Hz^{-1}. The present sample B2 has shown lower α_H than other works [25], [26], indicating that the reduced surface electron trapping and improved interfacial quality was obtained by the surface passivation of the USPD-grown Al_2O_3. The crystalline quality of the USPD-grown Al_2O_3 and the trapping-related gate leakage mechanisms of the fabricated MOS-gate have been studied in our previous work [27]. In addition, the transfer length method (TLM) [28] was performed for sample B2, as shown in Fig. 7, to characterize the source/drain ohmic contact property before/after annealing. The pad spacing was 5 μm and the measured separation was varied from 5 μm to 25 μm. The contact resistance (R_C) and the corresponding specific contact resistivity (ρ_c) before/after annealing were determined to be 11.5/5.1 Ω-mm and $4.3 \times 10^{-5}/1.3 \times 10^{-5}$ Ω-cm^2, respectively. R_C was effectively reduced after annealing. Lower R_C than other works [12], [15] was due to the devised n-GaN capper and performing RTA. It is advantageous to reduce the on-resistance (R_{on}) for power-switching applications.

Figs. 8(a)-(c) show the common-source current-voltage (I_{DS}-V_{DS}) characteristics and the corresponding transfer characteristics (I_{DS}/g_m-V_{GS}) for samples A, B1, and B2 at 300 K, respectively. The devices were measured by using a KEITHLEY 4200 analyzer with the V_{GS} biased from −14 V to 6 V at 2 V/step. Good pinch-off property was observed for all three devices. It was attributed to (1) the reduced gate leakage current by using the MOS-gate design with surface passivation and (2) the suppressed substrate leakage current by the devised wide-gap $In_{0.12}Al_{0.88}N$ back-barrier. The maximum I_{DS} density ($I_{DS,max}$) at $V_{DS} = 20$ V and the maximum extrinsic transconductance ($g_{m,max}$) for samples B1/B2 (A) were found to be 992.6/937.4 (838.8) mA/mm and 90.8/89.6 (80.6) mS/mm, respectively. The corresponding R_{on} characterized at $V_{DS} = 1$ V and the specific on-resistance ($R_{on,sp}$) were to be 11.1/13.8 (19.4) Ω-mm and 3.2 / 3.4 (5.5) mΩ/cm^2. Enhanced $I_{DS,max}$ characteristics

and reduced R_{on} in samples B1/B2 were contributed by the improved channel conductivity and carrier confinement capability by the symmetrically-graded $Al_xGa_{1-x}N$ design. These are consistent with the Hall measurement and TLM results. Higher I_{DS} densities have also resulted in better $g_{m,max}$. The present samples B1/B2 have shown superior $g_{m,max}$ to other widegap-channel devices with $g_{m,max} = 80.5$ mS/mm [29] and $g_{m,max} = 11.8$ mS/mm [30]. Besides, the threshold voltage (V_{th}) was determined by the extrapolated intercept of the $(I_{DS})^{1/2}$ curve to the V_{GS}-axis. The V_{th} values were extracted to be 10.9 V and of −11.1 (−11.0) V for samples A and B2 (B1). As discussed before, the Hall data showed that the studied devices had the comparable 2DEG concentrations, since the equivalent Al-ratio of the AlGaN channel was devised to be the same of 0.21. Similar V_{th} values were observed in studied samples. Besides, the gate-voltage swing (GVS) and on/off-current ratios (I_{on}/I_{off}) for samples B1/B2 (A) were characterized to be 4.8/4.9 (4.3) V and $1.8 \times 10^8/1.8 \times 10^8 (1.3 \times 10^8)$, respectively. GVS was defined as the available V_{GS} range where the g_m values were within 90% of $g_{m,max}$. Good gate insulation, gate modulation capability, and effective surface passivation were obtained by the MOS-gate design by using the USPD-grown high-k and wide-gap Al_2O_3. The leakage current was further reduced by the wide-gap $In_{0.12}Al_{0.88}N$ back-barrier. The present samples B1/B2 have exhibited improved GVS linearity and I_{on}/I_{off} ratio with respect to sample A due to the increased I_{DS} densities and reduced leakage current.

Figs. 9(a)-(c) show the measured two-terminal off-state gate-drain breakdown voltage (BV_{GD}) and three-terminal on-state drain-source breakdown voltage (BV_{DS}) characteristics at 300 K for samples A, B1, and B2, respectively. BV_{GD} was characterized with the floated source terminal, whereas BV_{DS} was measured at $V_{GS} = -15$ V with the depleted channel for all devices. The BV_{GD} (BV_{DS}) was determined to be the V_{GD} (V_{DS}) bias where the I_{GD} (I_{DS}) magnitude was equal to 1 mA/mm. BV_{GD} and BV_{DS} for samples B1/B2 (A) were found to be −490/−530 (−490) V and 470/520 (465) V, respectively. All devices have shown good breakdown characteristics. It was mainly attributed to (1) reduced thermionic emission phenomenon by the wide-gap Al_2O_3 of the MOS-gate, (2) reduced surface leakage by the USPD-grown Al_2O_3 passivation, (3) increased threshold electric field by the wide-gap AlGaN channel, and (4) reduced buffer leakage current by the wide-gap $In_{0.12}Al_{0.88}N$ back-barrier. Besides, sample B2 has demonstrated about 11 (12) % improvement in BV_{DS} as compared to sample B1 (A). It was mainly contributed by the DFP design, since the electric field distribution within the gate-drain region was effectively alleviated. Besides, higher Al-ratio of the symmetrically-graded $Al_xGa_{1-x}N$ channel near the channel/barrier interface has resulted in higher threshold electric field, which was further advantageous to the BV_{DS} performance.

TABLE 1. Device characteristics of the studied samples.

Sample	A	B1	B2
$I_{DS,\ max}$ (mA/mm)	838.8	992.6	937.4
$g_{m,\ max}$ (mS/mm)	80.6	90.8	89.6
V_{th} (V)	-10.9	-11.0	-11.1
GVS (V)	4.3	4.8	4.9
I_{on}/I_{off}	1.3×10^8	1.8×10^8	1.8×10^8
R_{on} (Ω-mm)	19.4	11.1	13.8
$R_{on,\ sp}$ (mΩ/cm²)	5.5	3.2	3.4
BV_{GD} (V)	-490	-490	-530
BV_{DS} (V)	465	470	520
BFOM (MW/cm²)	39.3	69.0	79.5

The BFOM, defined as $BV_{DS}^2/R_{on,sp}$., is an important criterion for power-switching applications. The present sample B2 has demonstrated superior BFOM of 79.5 MW/cm^2 as compared to 39.3 (69.0) MW/cm^2 of sample A (B1). Significant improvement of 102 (15) % has been achieved. The achieved BFOM performance is also superior to other AlGaN-channel devices, including 27.8 MW/cm^2 [30], 45.9 MW/cm^2 [31], 49.0 MW/cm^2 [32], and 74.2 MW/cm^2 [33]. Table 1 has summarized the device characteristics of the studied samples.

IV. CONCLUSION

$In_{0.12}Al_{0.88}N/AlN/Al_xGa_{1-x}N/In_{0.12}Al_{0.88}N$ MOS-HFETs on a SiC substrate with symmetrically-graded wide-gap $Al_xGa_{1-x}N$ ($x = 0.32 \rightarrow 0.1 \rightarrow 0.32$) channel, wide-gap $In_{0.12}Al_{0.88}N$ back-barrier, and DFP were reported for the first time. Low R_{on} was obtained owing to reduced contact resistance by using the n-GaN capper. Decreased gate leakage, enhanced gate modulation capability, and good surface passivation were obtained by the MOS-gate design by using the USPD technique. Enhanced I_{DS} densities with high BV_{GD}/BV_{DS} performance were also achieved. Consequently, the present sample MOS-HFET with DFP has demonstrated improved $I_{DS,max}$ of 937.4 mA/mm, $g_{m,max}$ of 89.6 mS/mm, I_{on}/I_{off} of 1.8×10^8, BV_{GD} of −530 V, BV_{DS} of 520 V, and BFOM of 79.5 MW/cm^2. It is promisingly useful for high-voltage power-switching applications.

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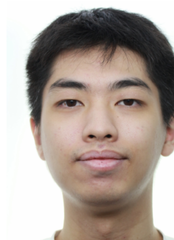

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