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RESEARCH ARTICLE

Analysis of Power-Supply-Rejection Enhancement Techniques for Low-Dropout Regulators

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ABSTRACT This article presents a comprehensive analysis of power-supply-rejection (PSR) enhancement techniques in low-dropout regulators (LDOs) for efficient power management within system-on-chips (SoCs). The PSR is a critical performance metric for LDOs, as it ensures the suppression of power supply ripple and provides stable output voltages. Various PSR enhancement techniques aimed at enhancing PSR characteristics have been proposed, and this study endeavors to offer insights by analyzing these techniques. PSR enhancement techniques can be broadly categorized into two main categories: supply ripple insensitivity/bandwidth improvement and feedforward supply ripple cancellation (FFRC). Supply ripple insensitivity techniques involve the use of a cascading LDO to pre-regulate the supply ripple in the main LDO loop, and bandwidth improvement techniques focus on improving the ripple suppression bandwidth of the LDO. FFRC techniques aim to mitigate the supply ripple by injecting supply ripple through a feedforward path. In addition to analyzing PSR enhancement techniques, this article discusses recent research trends through a performance comparison. Furthermore, it provides valuable insights into the design and optimization of LDOs for PSR enhancement.

INDEX TERMS Low-dropout regulator (LDO), power management unit (PMU), power-supply-rejection (PSR), PSR enhancement, feedforward supply ripple cancellation (FFRC).

I. INTRODUCTION

In the domain of system-on-chips (SoCs) and chiplet architectures, each analog and digital block is designed to operate within a specific voltage range to ensure proper functionality and performance. However, during actual circuit operation, the power supply voltage is highly susceptible to fluctuations caused by external switching noise and internal current variations. To address this issue, power management units (PMUs) have emerged as important components of modern SoCs, aiming to mitigate the impact of external noise and ensure the stability of the power supply [1], [2].

The PMU is composed of two key components: switching regulators and low-dropout regulators (LDOs), as shown in Fig. 1. Although switching regulators offer excellent power conversion efficiency, they inherently generate switching ripple that can compromise the stability of the supply voltage [3], [4]. To overcome this challenge, LDOs are integrated in series with the switching regulator within the PMU, enabling them to provide a ripple-suppressed and stable power supply.

LDOs can address the specific needs of noise-sensitive blocks, such as analog, digital, and RF circuits, which require a reliable and stable voltage source. These blocks are highly susceptible to disturbances caused by power supply ripple, which can adversely affect their performance and overall system integrity. By utilizing LDOs with superior power-supply-rejection (PSR) capabilities, the PMU ensures a clean and stable power supply to satisfy the stringent requirements of these noise-sensitive blocks.

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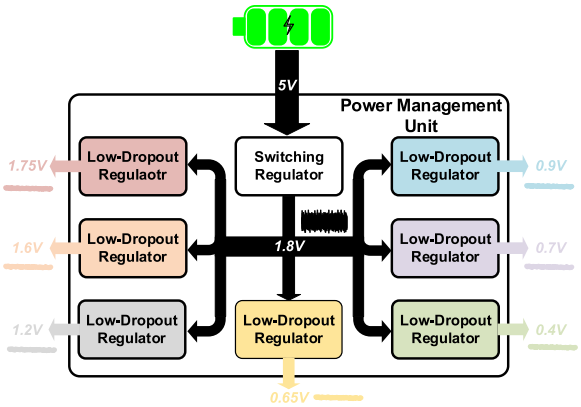

FIGURE 1. Block diagram of power management unit.

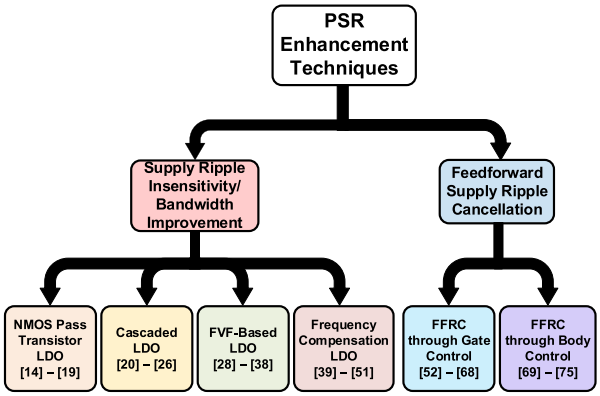

FIGURE 2. PSR enhancement techniques for LDOs.

In recent years, significant advancements have been made to enhance the PSR characteristics of LDOs. PSR enhancement techniques have been proposed to improve the ability of LDOs to reject power supply ripple and deliver a stable output voltage. As shown in Fig. 2, PSR enhancement techniques can be divided into two main categories: 1) supply ripple insensitivity/bandwidth improvement, and 2) feedforward supply ripple cancellation (FFRC). Supply ripple insensitivity/bandwidth improvement focuses on enhancing the supply ripple insensitivity/bandwidth of the LDO to achieve higher PSR performance. These techniques enable an LDO to effectively reject the power supply ripple and maintain stable output voltages. NMOS pass transistor LDO and FVF-based LDO structures can provide wide loop bandwidth and improve PSR performance. The cascaded LDO structure enhances PSR performance by employing an additional LDO in a cascading configuration to pre-regulate the supply ripple. FFRC techniques aim to cancel the power supply ripple by utilizing a feedforward path, thereby achieving a cleaner and more stable power supply. Various FFRC techniques, such as gate control and body control, have been proposed to effectively mitigate the supply ripple and enhance the PSR of LDOs.

This paper presents a comprehensive analysis of the PSR enhancement techniques recently employed in LDOs. It offers insights into LDO design for PSR enhancement by conducting a small-signal model analysis of PSR enhancement techniques. Additionally, it compares the advantages and limitations of each architecture and examines state-of-the-art works, thereby summarizing recent research trends in PSR enhancement techniques.

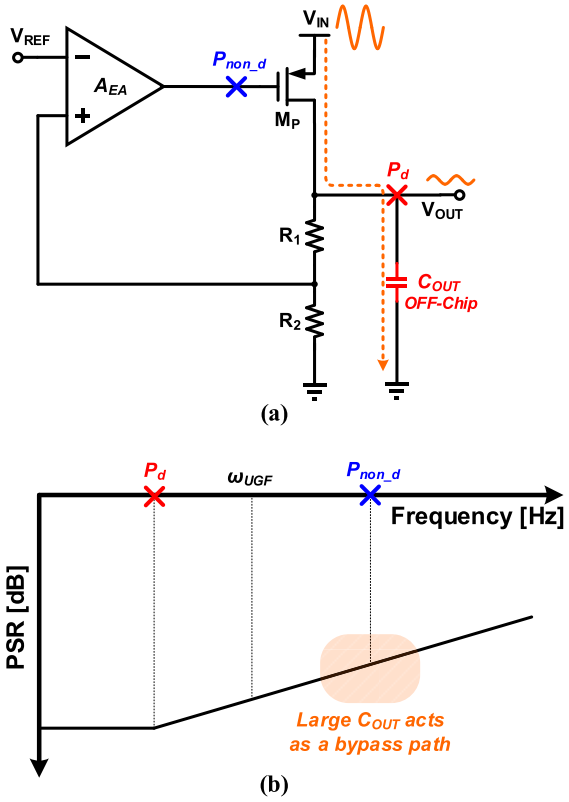

FIGURE 3. (a) Basic LDO structure with external dominant pole configuration and (b) corresponding PSR characteristic.

The remainder of this paper is organized as follows: Section II provides a basic analysis of the PSR characteristics in an LDO. Section III describes PSR enhancement techniques incorporating supply ripple insensitivity/bandwidth improvement. Section IV explores FFRC techniques applied to LDOs, such as ripple cancellation through gate control and ripple cancellation through body control, and evaluates their effectiveness in mitigating ripple and improving PSR. Section V presents a comprehensive comparison of the state-of-the-art studies focusing on PSR enhancement. This analysis examines their advantages, limitations, and performance metrics. Section VI summarizes the key findings of this study.

II. BASIC ANALYSIS OF POWER SUPPLY REJECTION IN LDOs

In general, LDOs can be broadly categorized into two distinct types: those with an external dominant pole and those with

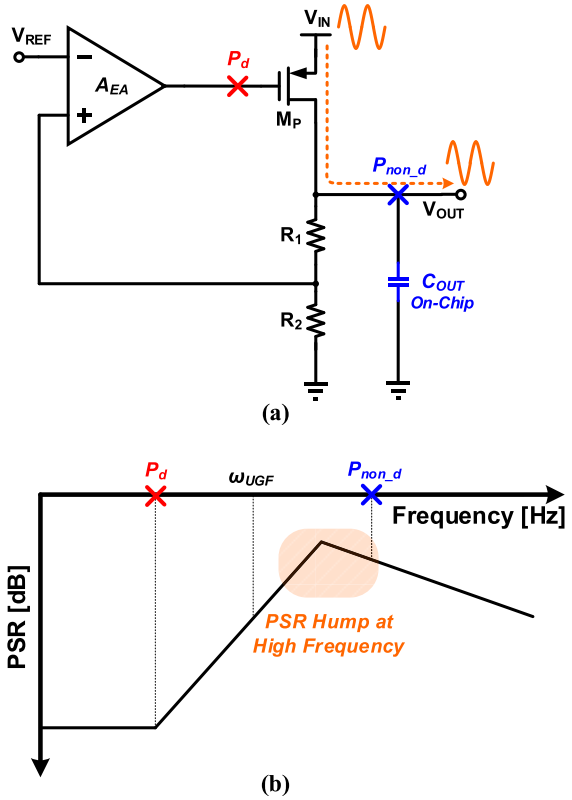

FIGURE 4. (a) Basic LDO structure with internal dominant pole configuration and (b) corresponding PSR characteristic.

an internal dominant pole, each with different characteristics in terms of PSR dynamics. Fig. 3(a) illustrates an LDO with an external dominant pole configuration, where a large output capacitor (C_{OUT}) ranging from several micro-farads to nano-farads is located externally, and the dominant pole is associated with C_{OUT} [9]. Fig. 3(b) indicates that the LDO exhibits higher PSR at frequencies above its unity gain frequency (ω_{UGF}) [9]. This can be attributed to the large C_{OUT}, which creates a bypass path at high frequencies. This bypass path allows the supply ripple to flow through and attenuate as it reaches the ground [11]. By attenuating the supply ripple away from the LDO output voltage, the large C_{OUT} effectively mitigates its impact and enhances PSR performance. The presence of a dominant pole associated with C_{OUT} in an LDO configuration introduces stability concerns, particularly when the load current increases. As the dominant pole moves towards the second pole, instability can occur. To ensure stable regulation, a sufficiently large C_{OUT} is necessary. The size of C_{OUT} plays a critical role in stabilizing the LDO's feedback loop and maintaining a suitable phase margin. However, an excessively large C_{OUT} can limit the bandwidth. By utilizing an appropriately sized C_{OUT}, an LDO can compensate for load current variations and prevent the dominant pole from approaching the second pole too closely, thereby avoiding the degradation of the phase margin and ensuring stability.

Fig. 4(a) shows the configuration of an LDO with an internal dominant pole, where C_{OUT} is integrated within the chip at the scale of hundreds of pico-farads. In recent years, there has been a growing trend in the use of capacitor-less LDO designs, in which capacitors are fully integrated within the chip, in response to the demand for cost reduction. Fig. 4(b) shows the presence of a PSR hump at a high frequency near ω_{UGF}, indicating the existence of a worst PSR zone near ω_{UGF} [13]. The PSR hump arises because of the reduction in the loop gain beyond ω_{UGF}, leading to a diminished capability to maintain the output voltage. To mitigate PSR humps at high frequencies, it is necessary to shift the dominant pole; however, this approach often introduces stability issues. Furthermore, under light-load conditions, the dominant pole approaches the second pole, resulting in poor stability.

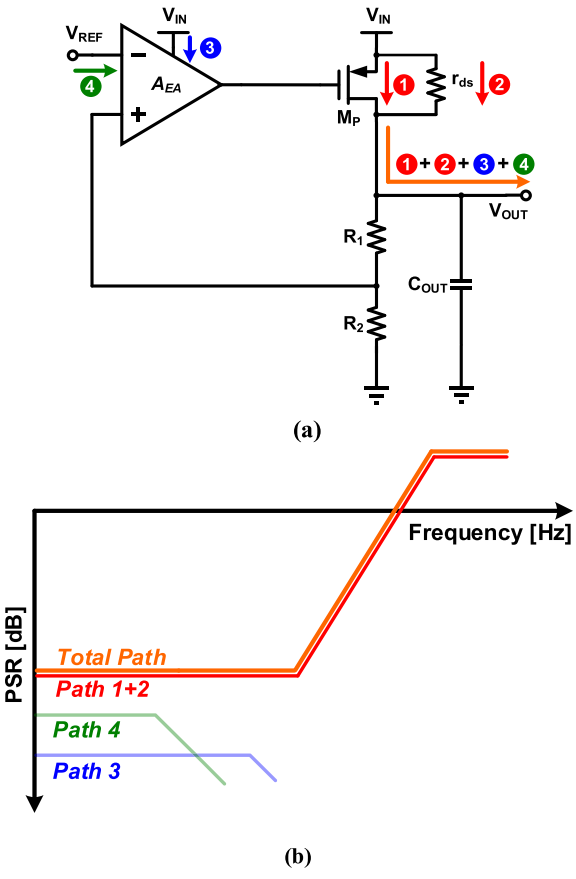

FIGURE 5. (a) Power supply ripple injection paths in output-capacitor-less LDO and (b) corresponding PSR characteristic [6].

Fig. 5(a) shows the supply ripple injection paths in the output-capacitor-less LDO structure. These paths are significant because they determine how the power supply ripple can influence the output voltage and the overall ripple rejection capability of the LDO. Thus, understanding and analyzing these paths is paramount for improving the PSR performance of LDOs.

Fig. 5(b) depicts the PSR characteristic corresponding to the power supply ripple path in the output-capacitor-less

LDO. Path 1 is formed through the pass transistor (g_{mp}), and path 2 is the result of the finite drain-source resistance of the pass transistor (r_{ds}). Finally, paths 3 and 4 result from the finite power-supply-rejection-ratio (PSRR) of the error amplifier and bandgap reference, respectively.

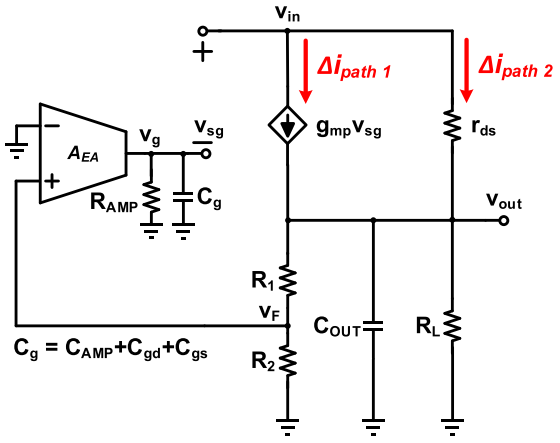

FIGURE 6. Small-signal model of output-capacitor-less LDO.

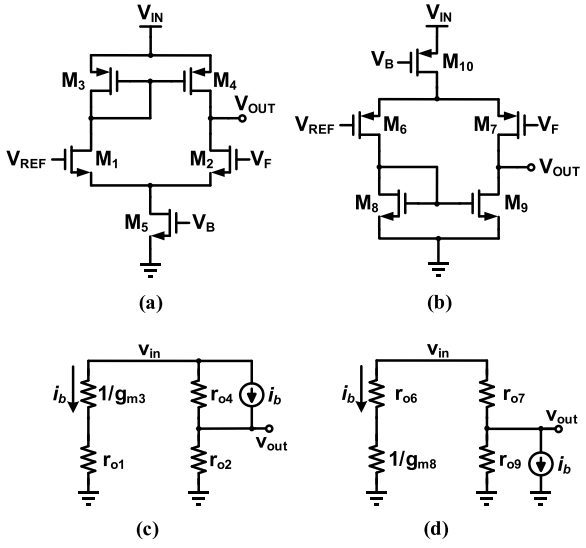

FIGURE 7. Schematics of (a) N-type input error amplifier and (b) P-type input error amplifier. (c) Small-signal model of n-type input error amplifier. (d) Small-signal model of p-type input error amplifier [8].

Fig. 6 presents a small-signal model of the output-capacitor-less LDO. The input ripple voltage, denoted by v_{in}, signifies the fluctuating or noisy components of the incoming power supply. In contrast, the output ripple voltage, referred to as v_{out}, represents the variation or ripple observed in the regulated output voltage of the LDO. Paths 1 and 2 are strongly affected by the characteristics of the pass transistor, particularly g_{mp} and r_{ds}. Variation in these parameters directly impacts the LDO's supply ripple rejection performance. The transfer functions in paths 1 and 2 from v_{in} to v_{out} can be derived as [55]

$$v_g = A_{EA}v_F + \frac{sC_{gs}}{s\left(C_{AMP}+C_{gs}+C_{gd}\right)}v_{in} \tag{1}$$

$$v_F = \frac{R_2}{R_1+R_2}v_{out} \tag{2}$$

$$\Delta i_{Path1} = g_{mp}\left(v_{in}-v_g\right)$$

$$\Delta i_{Path2} = g_{ds}\left(v_{in}-v_{out}\right) \tag{3}$$

$$\frac{v_{out}}{v_{in}}(s)\Big|_{path1,2} = A_{DC}\frac{(1+s/\omega_{z1})}{(1+s/\omega_{p1})(1+s/\omega_{p2})} \tag{4}$$

$$A_{DC\_Basic} = \frac{\mathbf{1}+g_{mp}r_{ds}}{\mathbf{1}+\frac{g_{mp}r_{ds}A_{EA}R_2+r_{ds}}{R_1+R_2}+\frac{r_{ds}}{R_L}} \tag{5}$$

$$\omega_{p1} = \frac{\mathbf{1}}{R_{AMP}(C_{AMP}+C_{gd}+C_{gs})} \tag{6}$$

$$\omega_{p2} = \frac{g_{ds}+\frac{1}{R_1+R_2}+\frac{1}{R_L}+\frac{g_{mp}A_{EA}R_2}{R_1+R_2}}{C_{OUT}} \tag{7}$$

$$\omega_{z1} = \frac{g_{mp}+g_{ds}}{R_{AMP}\{(g_{mp}+g_{ds})(C_{AMP}+C_{gd}+C_{gs})-C_{gs}\}} \tag{8}$$

where ω_{p1}, ω_{p2}, and ω_{z1} are the dominant pole, second pole, and dominant zero, respectively. C_{OUT} represents the output-capacitor. A_{EA} and R_L are the gain of the error amplifier and the load resistor, respectively. R_1 and R_2 are resistors that forming a divider in the feedback path. R_{AMP} determines the output resistance of the error amplifier. C_{AMP} is the output capacitance of the error amplifier. (4) provides a comprehensive representation of the combined influence of paths 1 and 2 on the PSR performance of the LDO. This highlights the significant impact of the parameters of g_{mp} and r_{ds} on the ability of the LDO to reject the supply ripple. In the low-frequency range, the PSR characteristics of paths 1 and 2 are highly dependent on A_{EA} and the resistive divider formed by R_1 and R_2. However, as the supply ripple frequency increases, the PSR becomes dependent on g_{mp} and the output equivalent resistance by r_{ds}, as well as R_L.

Path 3 in Fig. 5(a) depends on the input type of the error amplifier. Fig. 7 depicts the error amplifiers and corresponding small-signal models based on the input type.

The PSR characteristics of paths 3 and 4 can be derived in the same manner as the deviation in [8].

$$i_b = \frac{v_{in}}{\left(\frac{1}{g_{m2}}+r_{o1}\right)} \tag{9}$$

$$A_{PSRR\_N} = \frac{v_{out}}{v_{in}} = \frac{\frac{1}{r_{o2}}+\frac{1}{\frac{1}{g_{m2}}+r_{01}}}{\frac{1}{r_{o2}}+\frac{1}{r_{01}}} \approx 1\left(\frac{1}{g_{m2}} \ll r_{01}\right) \tag{10}$$

$$A_{PSRR\_P} = \frac{v_{out}}{v_{in}} = \frac{\frac{1}{r_{o1}}-\frac{1}{\frac{1}{g_{m2}}+r_{01}}}{\frac{1}{r_{o2}}+\frac{1}{r_{01}}} \approx 0\left(\frac{1}{g_{m2}} \ll r_{01}\right) \tag{11}$$

where i_b, A_{PSRR_N}, and A_{PSRR_P} are the small-signal current, PSRR of the n-type input error amplifier, and PSRR of the

TABLE 1. Pros and cons of LDO architectures with supply ripple insensitivity and bandwidth improvements.

	NMOS LDO	Cascaded LDO	FVF-Based LDO
Pros	Wide loop bandwidth Area efficiency of pass gate	Improved PSR at low-frequency range	Low output impedance Fast transient response
Cons	Need a voltage boosting circuit for pass gate voltage	Large dropout voltage	Limited Load Current Range

p-type input error amplifier, respectively. (9) represents the small-signal current relationship. (10) and (11) provide the transfer functions of the error amplifier based on the input type. The n-type input error amplifier passes the supply ripple directly to the output, leading to a lower error amplifier PSRR. In contrast, the p-type input error amplifier can exhibit a better error amplifier PSRR, as it cancels out the supply ripple. When considering the overall transfer function of the LDO, the n-type error amplifier can outperform the p-type error amplifier.

$$v_{out}\,(s=\mathbf{0})|_{path3,4}=\frac{g_{mp}r_{ds}\left\{A_{EA}v_{ref}-A_{PSRR}v_{in}\right\}}{1++\frac{r_{ds}}{R_1+R_2}+\frac{g_{mp}r_{ds}A_{EA}R_2}{(R_1+R_2)}+\frac{r_{ds}}{R_L}} \tag{12}$$

where v_{ref} represents the supply ripple component through the bandgap reference and A_{PSRR} denotes the PSRR of the error amplifier. This can be attributed to (12), where the term involving A_{PSRR} cancels out the supply ripple caused by path 3. As a result, the n-type error amplifier can provide superior PSR performance compared to that of the p-type error amplifier in the LDO. In path 4, a bandgap reference is typically combined with an RC filter to filter out ripple [12]. Therefore, the reduction in PSR caused by path 4 does not dominantly influence the overall PSR characteristics of the LDO.

In summary, the effect of supply ripple injection paths on PSR performance in the LDO can be observed. The overall PSR performance is affected by various supply ripple injection paths; specifically, paths 1 and 2 have a primary impact on the PSR of the LDO across all frequency ranges.

III. PSR ENHANCEMENT TECHNIQUES USING SUPPLY RIPPLE INSENSITIVITY/BANDWIDTH IMPROVEMENT

As explored in Section II, the PSR performance of an LDO is highly dependent on its loop gain and bandwidth. The high loop gain provides accurate regulation and suppression of the power supply ripple being injected into the output node. The wide loop bandwidth means that the LDO can handle high-frequency power supply ripple, extending the PSR bandwidth. However, high loop gain and wide bandwidth may result in unstable operation, causing stability issues.

One popular approach to address this stability issue is using a frequency-compensation technique. One example is the introduction of a left-half-plane (LHP) zero within the feedback loop of the LDO [39], [40], [41], [42], [43], [44], [45], [46], [47], [48], [49], [50], [51]. The LHP zero can counteract the effects of the poles in the system, effectively cancelling them out. This technique, known as pole-zero cancellation, is a form of frequency compensation that can help improve system stability. By widening the bandwidth, the LDO can provide improved PSR at high frequencies. Fig. 8 shows an LDO employing the reverse-nested Miller compensation technique [41]. This approach generates an LHP zero using a current buffer and an inverting current buffer. By creating this LHP zero, pole-zero cancellation is executed, which allows the LDO to provide a wide bandwidth. To further enhance performance, [42] applied the Q-reduction technique to the LDO design, resulting in a bandwidth exceeding 100 MHz. Moreover, [39], [43], [44], [45], [46], and [48] proposed sensing load current changes and adaptively shifting the position of the zero.

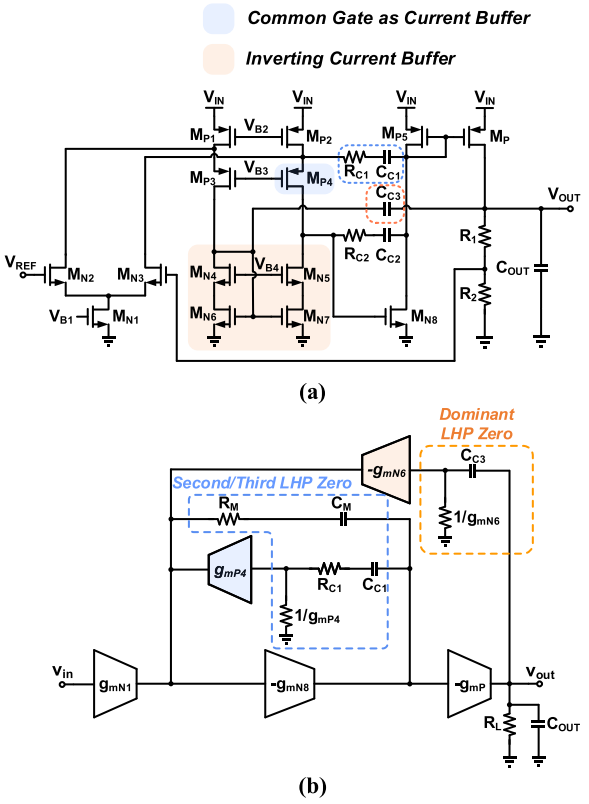

FIGURE 8. (a) Frequency compensation LDO. (b) Small-signal model of frequency compensation LDO [41].

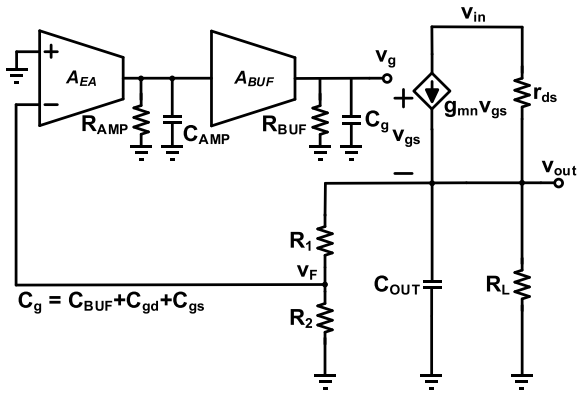

FIGURE 9. Small-signal model of NMOS LDO.

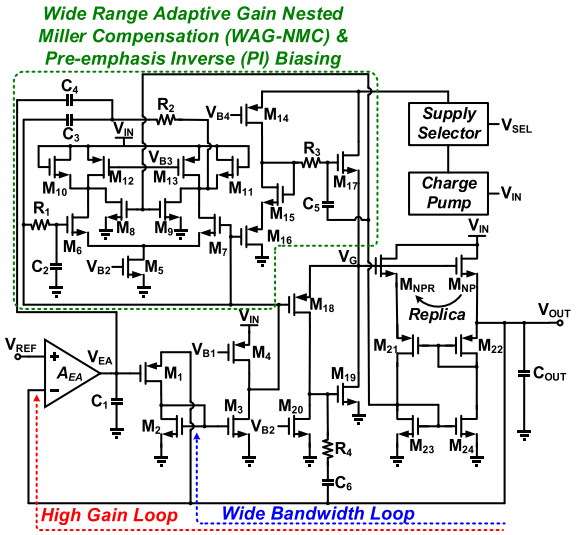

FIGURE 10. Example implementation of NMOS LDO [16].

In addition to frequency compensation, several techniques have been proposed to ensure stable operation and high PSR [14], [15], [16], [17], [18], [19], [20], [21], [22], [23], [24], [25], [26], [27], [28], [29], [30], [31], [32], [33], [34], [35], [36], [37], [38], [39], [40], [41], [42], [43], [44], [45], [46], [47], [48], [49], [50], [51]. NMOS pass transistor LDO [14], [15], [16], [17], [18], [19] and flipped voltage follower based LDO [28], [29], [30], [31], [32], [33], [34], [35], [36], [37], [38] have also been adopted to enhance bandwidth without impacting stability. Additionally, cascaded LDO [20], [21], [22], [23], [24], [25], [26] delivers a stable operating voltage to the main LDO loop by regulating the supply ripple at the cascade stage, thereby providing a high PSR. The pros and cons of the above-mentioned LDO architectures are summarized in Table 1. In this section, these design techniques are investigated further.

A. NMOS PASS TRANSISTOR LDO

To achieve a high PSR at high frequencies, a wide-bandwidth NMOS LDO has been proposed [14], [15], [16], [17], [18], [19]. NMOS LDOs are constructed with an NMOS pass transistor, thus forming a source follower stage that offers a low output impedance. Compared to PMOS LDO designs within the same load current range, NMOS pass transistors can exhibit better mobility in many CMOS processes, rendering them more area-efficient and providing higher transconductance. Owing to the combination of low output impedance and reduced gate parasitic capacitance, NMOS LDOs can achieve loop bandwidths wider than those of PMOS LDOs.

Fig. 9 shows the small-signal model of an NMOS LDO. The output load impedance of the NMOS LDO is calculated as follows:

$$Z_{OUT} = \left(\frac{1}{sC_{OUT}} \| \frac{1}{g_{mn}} \| R_L\right) \tag{13}$$

where Z_{OUT} denotes the output impedance of the NMOS LDO, g_{mn} is the transconductance of the NMOS pass transistor, and R_L is the load resistance. As is evident in (13), the total output impedance cannot be larger than $1/g_{mn}$ owing to the output impedance of the source follower stage. The overall transfer function of the NMOS LDO from v_{in} to v_{out} can be determined as follows:

$$\frac{v_{out}}{v_{in}}(s) = A_{DC}\frac{(1+s/\omega_{z1})}{(1+s/\omega_{p1})(1+s/\omega_{p2})(1+s/\omega_{p3})} \tag{14}$$

$$A_{DC} = \frac{g_{mn}r_{ds}}{1+\frac{g_{mn}r_{ds}A_{EA}+r_{ds}}{R_1+R_2}+\frac{r_{ds}}{R_L}+g_{mn}} \tag{15}$$

$$\omega_{p1} = \frac{1}{R_{BUF}(C_{BUF}+C_{gd}+C_{gs})} \tag{16}$$

$$\omega_{p2} = \frac{1}{R_{AMP}C_{AMP}} \tag{17}$$

$$\omega_{p3} \approx \frac{1}{(\frac{1}{g_{mn}} \| R_L \| r_{ds})C_{OUT}} \tag{18}$$

$$\omega_{z1} = \frac{g_{ds}}{R_{BUF}\{g_{ds}(C_{BUF}+C_{gd}+C_{gs})+g_{mn}C_{gs}\}} \tag{19}$$

where R_{BUF} and C_{BUF} denote the output resistance and output capacitance, respectively, in the buffer stage. Owing to the low parasitic capacitance, when compared to PMOS LDO designs within the same load current range, and typically having R_{BUF} as $1/g_{m\_BUF}$(which is significantly smaller than R_{AMP}), the dominant pole of the NMOS LDO exists at a frequency higher than that of the PMOS LDO. Consequently, the NMOS LDO offers a wider bandwidth than the PMOS LDO. Fig. 10 illustrates an example implementation of an NMOS LDO. This specific design utilizes a combination of low output impedance and a super source follower buffer to provide a wide bandwidth. However, to address the shifting of poles due to load current conditions, a wide range adaptive gain nested Miller compensation (WAG-NMC) is incorporated, effectively resolving the stability issues. Additionally, a dual-feedback loop is employed to offer high gain and wide bandwidth. However, NMOS LDOs have a specific

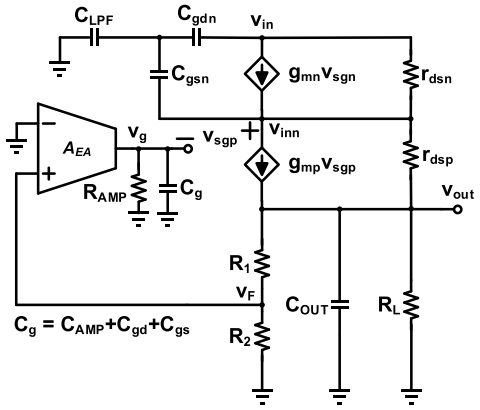

FIGURE 11. Small-signal model of cascaded LDO [23].

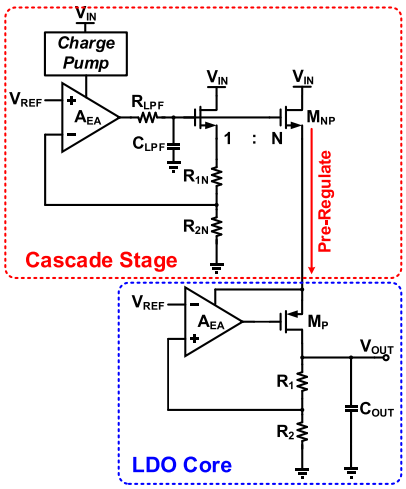

FIGURE 12. Example implementation of cascaded LDO [20].

operational requirement: the gate-source voltage (V_{gs}) must be greater than the threshold voltage (V_{th}) for the transistor to turn on. To achieve the required gate voltage for an NMOS pass transistor, a gate-boosting circuit such as a voltage doubler or charge pump, is required [14], [16], [18], [19]. These additional circuits are responsible for boosting the gate voltage above the threshold voltage. However, the inclusion of such circuitry comes at the cost of increased current consumption and additional area.

B. CASCADED LDO

Cascaded LDO ensures a stable operating voltage to the main LDO loop by regulating the supply ripple occurring at the cascade stage, thereby effectively improving the PSR performance. Fig. 11 shows the small-signal model of an LDO with a cascaded configuration. The NMOS LDO in the cascaded stage pre-regulates the supply ripple to deliver a stable voltage to the main LDO and enhance its PSR performance. The PSR transfer function of the cascaded LDO is calculated as follows [23]:

$$\frac{v_{out}}{v_{in}}(s) = \frac{v_{inn}}{v_{in}} \times \frac{v_{out}}{v_{inn}} = \frac{v_{inn}}{v_{in}} \times \frac{v_{out}}{v_{in}}(s)\Big|_{path1,2}$$

$$\frac{v_{out}}{v_{in}}(s) \approx \frac{sC_{gdn} + \frac{s(C_{gdn}+C_{gsn}+C_{LPF})}{(sC_{gsn}+g_{mn})r_{dsn}}}{s\left(C_{LPF}+C_{gdn}\right) + \frac{s(C_{gdn}+C_{gsn}+C_{LPF})}{(sC_{gsn}+g_{mn})r_{dsn}}} \times \frac{v_{out}}{v_{in}}(s)\Big|_{path1,2} \tag{20}$$

$$\frac{v_{out}}{v_{in}}(s)\Big|_{S=0} \approx \frac{C_{gdn}g_{mn}r_{dsn} + \left(C_{gdn}+C_{gsn}+C_{LPF}\right)}{g_{mn}r_{dsn}\left(C_{LPF}+C_{gdn}\right) + C_{gdn} + C_{gsn} + C_{LPF}} \times A_{DC\_Basic} \tag{21}$$

where g_{mn} and C_{gdn}, C_{gsn}, r_{dsn} are the transconductance, gate-drain parasitic capacitance, gate-source parasitic capacitance, and drain-source resistance of the NMOS pass transistor in the cascade stage, respectively. C_{LPF} denotes the capacitor of the low-pass filter. $v_{out}/v_{in}(s)|_{path1,2}$ presents the transfer function of a basic output-capacitor-less LDO, represented by (4). A_{DC_Basic} refers to the low-frequency PSR of a basic output-capacitor-less LDO, as observed in (5). Compared to the transfer function of the PMOS LDO represented by (5), the pre-regulation of the NMOS LDO through low-pass filtering in the cascade stage leads to an overall reduction in the term of the transfer function, as observed in (21). This suggests that the cascade configuration effectively improves the system characteristics.

Fig. 12 shows an example of a cascaded LDO structure. This cascade configuration effectively reduces the impact of supply ripple on the output of the main LDO loop [20], [21], [22], [23], [24], [25], [26]. However, it is essential to consider the trade-off associated with a cascaded design, specifically the increase in dropout voltage, which leads to lower power conversion efficiency [7]. A large dropout voltage can cause larger power dissipation within the LDO, leading to reduced overall power conversion efficiency.

C. FLIPPED VOLTAGE FOLLOWER-BASED LDO

The flipped voltage follower (FVF)-based LDO introduces the FVF as an output stage configuration [28], [29], [30], [31], [32], [33], [34], [35], [36], [37], [38]. This architecture leverages a shunt feedback mechanism to achieve low output impedance [27]. Notably, the lower gate parasitic capacitance further enhances the LDO's loop bandwidth. The extended bandwidth facilitates high PSR performance, particularly at high frequencies. In contrast to a PMOS LDO with a common gate amplifier output stage, an FVF-based LDO features an output stage configured as a buffer stage. This results in a lower loop gain in the low-frequency region. The approximate output impedance of an FVF-based LDO can be derived

TABLE 2. Pros and cons of LDO architectures with FFRC.

	VM-Gate Ripple Injection	CM-Gate Ripple Injection	Body Ripple Injection
Pros	Easy to adjust ripple injection gain	Implementation simplicity	High PSR improvement at high-frequency range
Cons	Need additional voltage summing amplifier	Prone to PVT variation	Susceptibility to forward bias

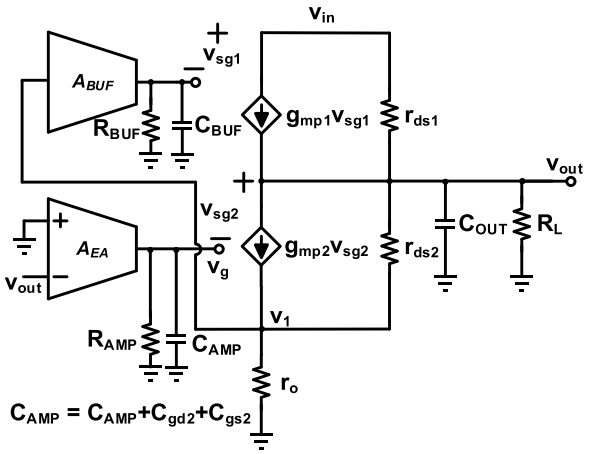

FIGURE 13. Small-signal model of flipped voltage follower-based LDO.

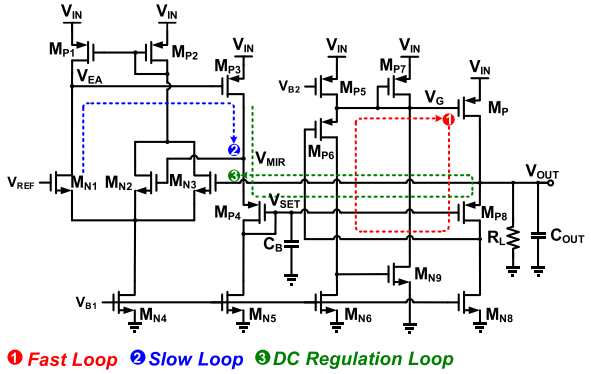

FIGURE 14. Example implementation of flipped voltage follower-based LDO [28].

as follows [27]:

$$Z_{OUT} = \left(\frac{1}{sC_{OUT}} \| \frac{1}{g_{m1}g_{m2}r_{ds2}} \| \frac{1}{R_L}\right) \approx \frac{1}{g_{m1}g_{m2}r_{ds2}} \tag{22}$$

Fig. 13 shows the small-signal model of the FVF-based LDO. Significantly, the incorporation of the FVF output stage can be approximated as $1/g_{m1}g_{m2}r_{ds2}$. This value is exceptionally small, resulting in a remarkably low output impedance for the FVF-based LDO. In conclusion, the output impedance of the FVF-based LDO can be represented as (22). The PSR transfer function of the FVF-based LDO can be derived as follows:

$$\frac{v_{out}}{v_{in}}(s) = A_{DC}\frac{(1+s/\omega_{z1})}{(1+s/\omega_{p1})(1+s/\omega_{p2})(1+s/\omega_{p3})} \tag{23}$$

$$A_{DC} \approx \frac{1+g_{m1}r_{ds1}}{1+g_{m1}r_{ds1}+\frac{r_{ds1}}{R_L}+g_{m1}g_{m2}r_{ds2}r_{ds1}\,(1+A_{EA})} \tag{24}$$

$$\omega_{p1} \approx \frac{1}{(\frac{1}{g_{m1}g_{m2}r_{ds2}} \| R_L)C_{OUT}} \tag{25}$$

$$\omega_{p2} = \frac{1}{R_{AMP}(C_{AMP}+C_{gd2}+C_{gs2})} \tag{26}$$

$$\omega_{p3} = \frac{1}{R_{BUF}(C_{BUF}+C_{gd1}+C_{gs2})} \tag{27}$$

$$\omega_{z1} = \frac{g_{m1}+g_{ds1}}{R_{BUF}\{(g_{m1}+g_{ds1})(C_{gd1}+C_{BUF})+g_{ds1}C_{gs1}\}} \tag{28}$$

This reduced output impedance contributes enhanced PSR performance. Compared to the PMOS LDO design, (25) exhibits a high frequency owing to its significantly low output impedance. Consequently, the FVF-based LDO design offers a wide bandwidth, providing a high PSR at high frequencies. Additionally, (26) and (27) exist in the range of several GHz because of their very small parasitic capacitances. An FVF-based LDO is shown in Fig. 14. The architecture of this LDO consists of an error amplifier with an FVF output stage, providing efficient voltage regulation capability. Moreover, it contains three distinct loops. The fast loop aids in maintaining the output voltage during rapid load current fluctuations. On the other hand, the slow loop and DC regulation loop enhance DC voltage performance, such as load regulation and line regulation. Consequently, this design demonstrates high performance over a wide bandwidth, offering a fast-transient response and high PSR at high frequencies. However, owing to its low output impedance, it provides a low loop gain in DC, resulting in a reduced PSR at low frequencies.

IV. PSR ENHANCEMENT THROUGH FEEDFORWARD SUPPLY RIPPLE CANCELLATION

Recently, to effectively address the issue associated with the PSR hump observed at high frequencies, FFRC was presented in [52], [53], [54], [55], [56], [57], [58], [59], [60], [61], [62], [63], [64], [65], [66], [67], [68], [69], [70], [71], [72], [73], [74], and [75]. The FFRC technique is a

promising approach for overcoming PSR limitations without compromising the stability of the system. The basic principle of FFRC is to mitigate the supply ripple through feedforward injection of the ripple into a pass transistor. Depending on the feedforward path, FFRC can be categorized into two groups: ripple injection into the gate node of the pass transistor, and ripple injection into the body node of the pass transistor. Table 2 summarizes the pros and cons of FFRC techniques.

A. RIPPLE CANCELLATION WITH GATE RIPPLE INJECTION

FFRC with gate ripple injection mitigates the PSR hump at high frequencies by manipulating the gate voltage of the pass transistor. This adjustment aims to make the supply ripple transfer gain in (4) zero, thereby leading to a significant reduction in the PSR hump at high frequencies. Depending on the implementations that combine the feedforward ripple path and LDO feedback path, there are two possible realizations: voltage-mode and current-mode ripple injections.

1) VOLTAGE-MODE GATE RIPPLE INJECTION

The voltage-mode gate ripple injection has been proposed in previous studies to efficiently eliminate the supply ripple [52], [53], [54], [55], [56], [57], [58], [59], [60], [61]. This configuration sums the voltages from the feedforward ripple injection path and LDO feedback control path. Fig. 15 shows the small-signal model of the voltage-mode gate ripple injection. $H_{FF\_VM}(s)$ denotes the transfer function of the feedforward injection path, and its output voltage v_{FF} can be derived as [55]

$$v_{FF} = -H_{FF\_VM}(s)v_{in} \tag{29}$$

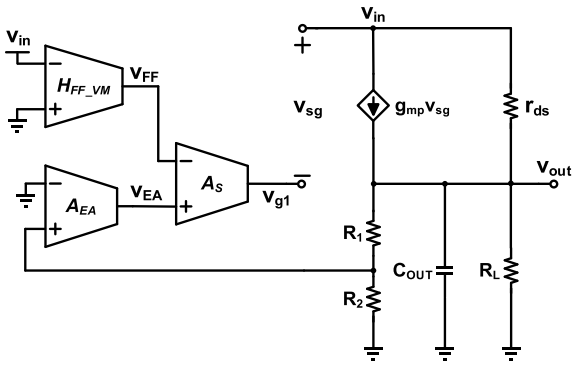

FIGURE 15. Small-signal model of FFRC with voltage-mode gate ripple injection.

The injection voltage of v_{g1} can be calculated as follows:

$$v_{g1} = A_s\left(A_{EA}\frac{R_2}{R_1+R_2}v_{out} + H_{FF\_VM}(s)v_{in}\right) \tag{30}$$

where A_s and A_{EA} are the injection and error amplifier gains, respectively. The PSR transfer function of the LDO from v_{in}

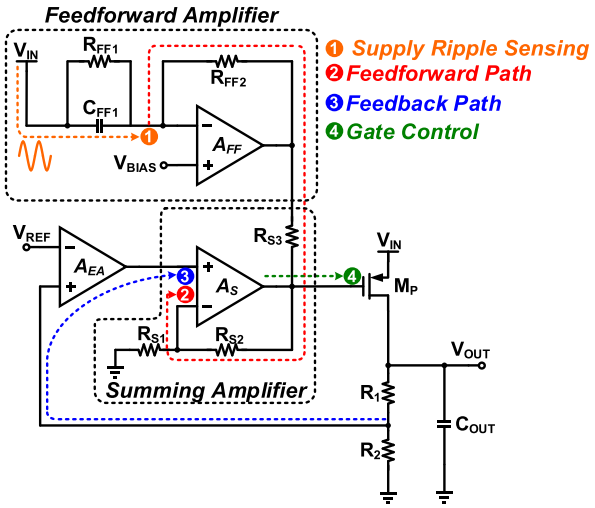

FIGURE 16. Example implementation of FFRC with voltage-mode gate ripple injection [55].

to v_{out} can then be derived as follows [55]:

$$\frac{v_{out}}{v_{in}}(s) = \frac{\frac{\{1+g_{mp}r_{ds}(1-H_{FF\_VM}(s)A_s)\}}{\left(1+\frac{s}{\omega_s}\right)}}{1+sC_{OUT}r_{ds}+\frac{r_{ds}}{R_1+R_2}+\frac{g_{mp}r_{ds}A_{EA}A_SR_2}{(R_1+R_2)(1+\frac{s}{\omega_s})(1+\frac{s}{\omega_{ea}})}+\frac{r_{ds}}{R_L}} \tag{31}$$

where ω_s is the dominant pole of the summing amplifier. From the perspective of the small-signal model, (31) should approach zero to achieve optimal PSR performance. As a result, the optimal $H_{FF\_VM}(s)$ can be calculated as follows:

$$H_{FF\_VM}(s) = \left(\frac{1+\frac{s}{\omega_s}}{A_s}\right)\left(\frac{g_{mp}+g_{ds}}{g_{mp}}\right) \tag{32}$$

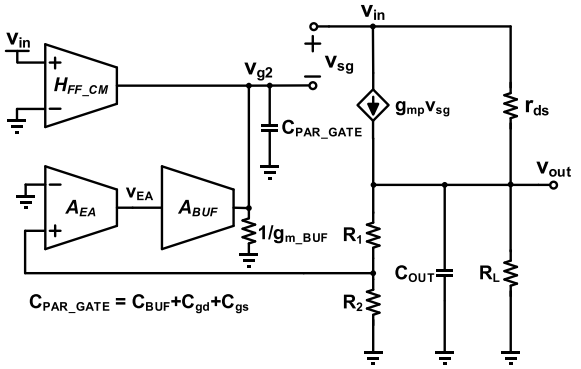

FIGURE 17. Small-signal model of FFRC with current-mode gate ripple injection.

The optimal value of $H_{FF\_VM}(s)$ can vary depending on the load current variation, which affects g_{mp} and g_{ds}. By adjusting $H_{FF\_VM}(s)$ based on the load current variation, the LDO can achieve optimal ripple cancellation. Hence, the LDO

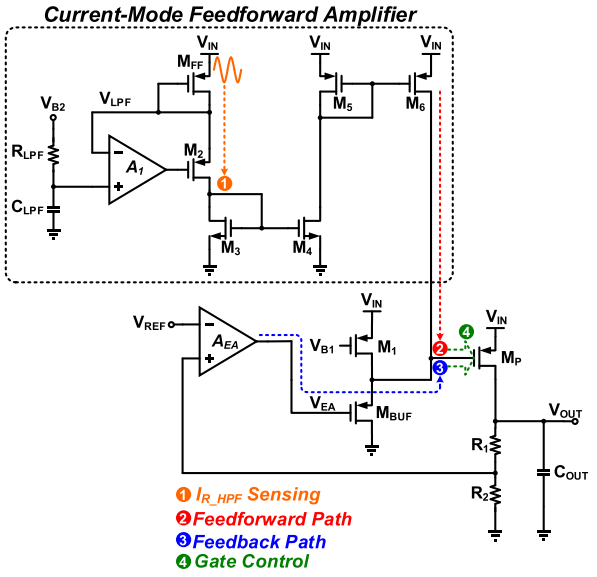

FIGURE 18. Example implementation of FFRC with current-mode gate ripple injection [65].

designs in [52], [54], and [56] incorporated an adaptive adjustment of the $H_{FF\_VM}(s)$ value. A correlator-based gain control was employed to control the gain of the feedforward amplifier [52]. To programmatically adjust g_{mp}, load current tracking technique was utilized in [54]. In [56], a replica pass transistor cell of was utilized to sense the load current and adjust the feedforward gain.

Fig. 16 shows an example implementation of FFRC with voltage-mode gate ripple injection. The feedforward path in the LDO senses the supply ripple voltage and injects the ripple voltage into the feedback path that maintains a constant LDO output. To realize voltage summation at the gate node of the pass transistor, an additional summing amplifier [54], [55], [56], [57], [58], [59] and coupling capacitor [52], [53], [61] were employed in the LDO. By properly adjusting the summation coefficients between the feedforward and feedback paths, the LDO can achieve optimal ripple cancellation without compromising loop gain or bandwidth, in contrast to conventional approaches.

2) CURRENT-MODE GATE RIPPLE INJECTION

FFRC with current-mode gate ripple injection [62], [63], [64], [65], [66], [67], [68] combines the current signals of the FFRC path and the feedback voltage regulation path. Current summation eliminates the need for an additional summing amplifier or capacitor in the voltage-mode implementation. Fig. 17 shows the small-signal model of an LDO with the current-mode gate ripple injection structure. Similar to the analysis in [65], the high-frequency ripple current of the current-mode feedforward amplifier i_{R_HPF} can be derived as follows [65]:

$$Z_{Gate} = \frac{1}{g_{m\_BUF}} \| \frac{1}{sC_{PAR\_GATE}} \approx \frac{1}{g_{m\_BUF}} \tag{33}$$

$$i_{R\_HPF} = g_{m\_FF}\left(v_{in} - v_{in\_LPF}\right) = g_{m\_FF} v_{in\_HPF} \tag{34}$$

where g_{m_BUF} determines the transconductance of the buffer stage and C_{PAR_GATE} presents the gate parasitic capacitance of the pass transistor. Z_{Gate} denotes the gate impedance of the pass transistor. Owing to the low output impedance of the buffer, this term can be approximated as $1/g_{m\_BUF}$. g_{m_FF} is the transconductance of the current-mode feedforward amplifier and v_{in_LPF} denotes the low-frequency v_{in} ripple. v_{in_HPF} corresponds to the high-frequency v_{in} ripple. The feedforward voltage signal can be calculated as follows [65]:

$$v_{FF} = i_{R\_HPF} Z_{Gate} \approx \frac{i_{R\_HPF}}{g_{m\_BUF}} \approx \frac{g_{m\_FF}}{g_{m\_BUF}} v_{in} \tag{35}$$

where v_{FF} denotes the feedforward voltage signal. The transfer function of $H_{FF\_CM}(s)$ can be calculated as follows [65]:

$$H_{FF\_CM}(s) = \frac{g_{m\_FF} Z_{Gate}}{\left(1 + \frac{s}{\omega_{ff}}\right)} = \frac{g_{m\_FF}\left(\frac{1}{g_{m\_BUF}} \| \frac{1}{sC_{PAR\_GATE}}\right)}{\left(1 + \frac{s}{\omega_{ff}}\right)}$$

$$H_{FF\_CM}(s) \approx \frac{g_{m\_FF}}{g_{m\_BUF}} \tag{36}$$

$$v_{g2} = A_{BUF} A_{EA} \frac{R_2}{R_1 + R_2} v_{out} + v_{FF}$$

$$v_{g2} \approx A_{EA} \frac{R_2}{R_1 + R_2} v_{out} + H_{FF\_CM}(s) v_{in} \tag{37}$$

where ω_{ff} represents the dominant pole of the feedforward amplifier. Because ω_{ff} is located at a very high frequency, the denominator can be approximated as unity. The transfer function from v_{in} to v_{out} can be derived as follows [65]:

$$\frac{v_{out}}{v_{in}}(s) = \frac{\left\{1 + g_{mp} r_{ds}\left(1 - H_{FF\_CM}(s)\right)\right\}}{1 + sC_{OUT} r_{ds} + \frac{r_{ds}}{R_1 + R_2} + \frac{g_{mp} r_{ds} A_{EA} R_2}{(R_1 + R_2)(1 + \frac{s}{\omega_{ea}})} + \frac{r_{ds}}{R_L}} \tag{38}$$

To achieve high PSR performance in an LDO, the numerator term in (38) must be zero. Hence, the term involving $H_{FF\_CM}(s)$ must be set to unity. The buffer is typically implemented as a source follower, which provides a low output impedance. This characteristic allows the buffer to have a dominant influence on the gate impedance of the pass transistor compared to the gate parasitic capacitor. Consequently, (37) can be approximated as follows [65]:

$$H_{FF\_CM}(s) = \frac{g_{m\_FF}}{g_{m\_BUF}} = \frac{g_{mp} + g_{ds}}{g_{mp}} \tag{39}$$

From (36) and (38), we obtain (39). The optimal gain of the feedforward amplifier is determined using the ratio of g_{m_FF} and g_{m_BUF}.

The variation in load conditions causes this ratio to change, limiting the ability to achieve a high PSR across a wide load range. In previous studies [62], [64], [66], [68], various approaches were proposed to adjust the gain of the feedforward amplifier to improve the PSR performance of the LDO. In [62], an adaptive current source was employed to regulate the gain of a pass transistor. References [64] focused

on approximating the feedforward amplifier gain using the value of the pass transistor's parasitic capacitor at a high frequency. Additionally, [64] presented the use of a replica cell to track the replica gate-drain capacitance (C_{gdr}) of a pass transistor, enabling adaptive adjustment of the feedforward amplifier gain based on variations in C_{gd}. In [66], the feedforward amplifier gain was designed to operate in two modes: high- and low-load conditions. In [68], a novel approach was proposed to dynamically adjust the feedforward amplifier gain by utilizing a replica pass transistor cell to track its g_{mp} and g_{ds}.

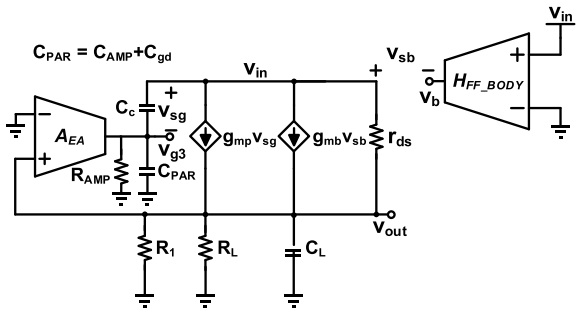

FIGURE 19. Small-signal model of FFRC with body ripple injection [69].

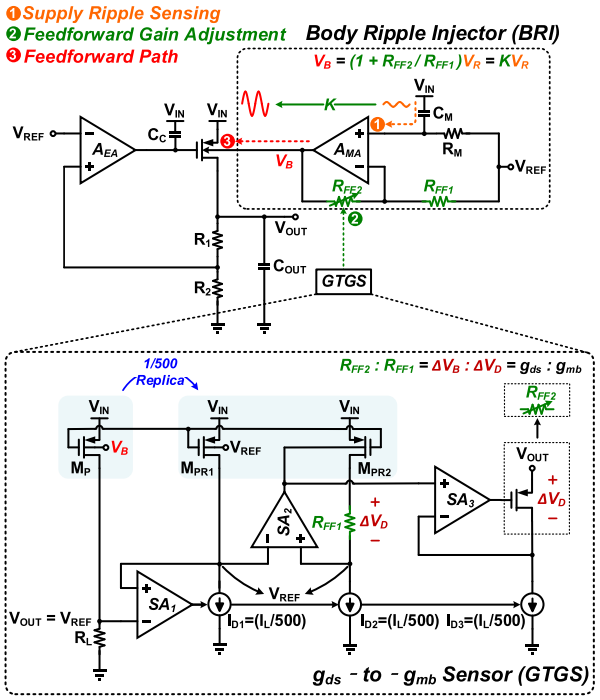

FIGURE 20. Example implementation of FFRC with body ripple injection using adaptive supply ripple cancellation [69].

Fig. 18 illustrates an example implementation of FFRC with current-mode gate ripple injection. This approach utilizes a low-pass filter to sense the high-frequency supply ripple and M_{FF} to generate the high-frequency supply ripple current. The generated high-frequency ripple current is employed to establish the feedforward path through a current mirror. Additionally, the ripple current produced in the feedback path is combined at the gate node of the pass transistor, enabling ripple cancellation. This design achieved a remarkable PSR performance of over -68 dB at 2 MHz.

B. RIPPLE CANCELLATION WITH BODY RIPPLE INJECTION

FFRC with body ripple injection utilizes the body voltage of the pass transistor to control the FFRC path, thereby providing high PSR performance [69], [70], [71], [72], [73], [74], [75]. The body ripple injection approach is based on the body effect of the pass transistor, as follows:

$$|V_{th}| = |V_{th0}| + \gamma \left(\sqrt{2\emptyset_F + V_{SB}} - \sqrt{2\,|\emptyset_F|} \right) \tag{40}$$

where V_{SB} is the source-body voltage, V_{th} is the threshold voltage, V_{th0} is the zero bias ($V_{SB} = 0$) threshold voltage, γ is the body effect coefficient, and $\emptyset_F$ is the Fermi potential. During the control of the body voltage based on (40), it is important to set an appropriate V_{SB}, as a large V_{SB} can cause the source-body diode to turn on, resulting in significant current leakage. Therefore, careful consideration must be given to properly configure V_{SB} to prevent undesired current leakage. This technique leverages the smaller parasitic capacitance of the body compared to the gate, as well as the smaller body transconductance (g_{mb}) compared to g_{mp} [69]. These factors enable the implementation of a high DC gain and wide bandwidth feedforward amplifier, making it superior to FFRC with gate ripple injection [73]. Furthermore, because the feedforward ripple signal is directly injected into the body node, additional summing amplifiers or capacitors are unnecessary, in contrast to the gate ripple injection method.

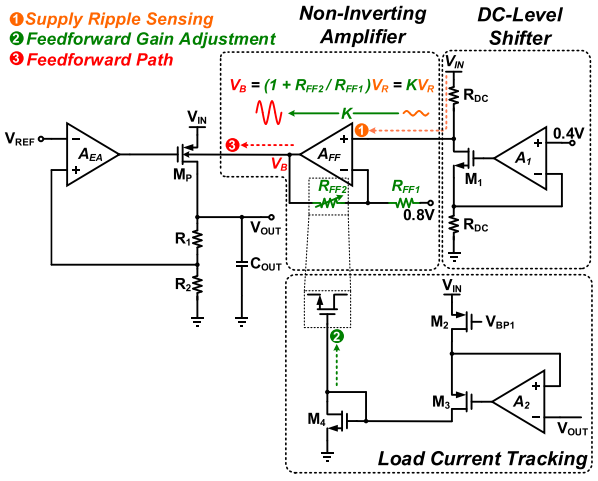

FIGURE 21. Example implementation of FFRC with body ripple injection using bulk-driven feedforward circuit [70].

Fig. 19 shows the small-signal model of FFRC with body ripple injection. The gate node voltage v_{g3} and body node voltage v_b of the pass transistor can be derived as follows [69]:

$$v_{g3} = \frac{sC_c}{s(C_c + C_{gd} + C_{AMP}) + \frac{1}{R_{AMP}}} v_{in} + A_{EA} v_{out}$$

TABLE 3. Comparison of state-of-the-art performance using supply ripple insensitivity/bandwidth improvement.

Design	[16]	[17]	[18]	[20]	[21]	[23]	[32]	[33]	[34]	[39]	[40]	[42]
Topology	NMOS LDO			Cascaded LDO			FVF-Based LDO			Frequency Compensation LDO		
Process [nm]	180	130	250	350	350	350	65	28	65	65	180	130
Active Area [mm^2]	0.185	0.0345	0.108	0.066	N/A	0.084	0.01	0.0086	0.053	0.0021	0.0035	0.008
V_{DD} [V]	1.2	2.0	1.5-3.3	1.6	3.3	1.8	1.05-1.2	0.9	1.2	1.0-1.4	0.5-1.8	1.0-1.4
V_{OUT} [V]	1.0	1.2-1.8	1.0-3.0	1.2	2.8	1.2	0.9	0.85	1.0	0.8-1.2	0.47	0.8
V_{DO} [V]	0.2	0.2	0.24	0.4	0.5	0.6	0.15	0.05	0.2	0.2	0.03-1.33	0.2-0.6
C_{OUT} [F]	100p	1.0μ	1.0μ-47μ	100p	10p	0-100p	0-100p	30p	300p	0-25p	0	0-25p
I_{LOAD} [mA]	0.1-300	0-1000	0-150	0-10	0-50	0-12	0.1-20	0-20	0.005-20	0-25	0-2*/ 0-200**	0.12-25
I_Q [μA]	80-87	35-1000	1.24-100	19.4-70	36.1-37.7	43.9	65	33	27-82	1.6-24.2	22.2*/ 35.7**	112
Line Regulation [mV/V]	N/A	0.23	N/A	0.25	23.4	0.28	N/A	17.5	N/A	0.7	0.34**	2.25
Load Regulation [mV/mA]	0.01	0.0006	25	0.32	0.31	0.68	N/A	0.26	0.015	0.28	9.5**	0.173
ΔI_{LOAD} [mA]	299	1000	150	10	N/A	12	19.9	20	19.9	25	2*/ 200**	24.88
ΔV_{OUT} [mV] @Undershoot	59	11	135	410	N/A	105	35	176	59	36	87*/ 152**	284
T_{Edge} [ns]	100	100	10	60	N/A	500	5	0.1	0.8	100	100	0.3
Edge Time Ratio K	1000	1000	100	600	-	5000	50	1	8	1000	1000	3
$T_{Settling}$ [ns]	480	8000*	900	1200	N/A	N/A	160	220	30*	1200	862	50
PSR (Frequency) [dB] @ I_{LOAD} [mA]	-42* (100k) -22* (1M) -15* (10M) @ 100	-51 (100k) -50 (1M) -30* (10M) @500	-10* (100k) -35* (1M) -36* (10M) @150	-40* (100k) -25* (1M) -22* (10M) @10	-45 (100k) -37* (1M) -20* (10M) @N/A	-60* (100k) -41* (1M) -40* (10M) @12	-45* (100k) -23 (1M) -5.2 (10M) @20	-30* (100k) -24 (1M) -14* (10M) @20	-58* (100k) -42 (1M) -25 (10M) @20	-44 (100k) -26 (1M) -11 (10M) @25	-37*/ -45** (100k) -20**/ -28*** (1M) 0**/ -2** (10M) @0	-65* (100k) -57 (1M) -22 (10M) @25
Peak Current Efficiency [%]	99.97	99.9	99.93	99.3**	99.92**	99.63**	99.97	99.83**	99.59**	99.9	98.9***/ 99.9***	99.55
FoM_1 [mV]	13.97	11	9	1722	-	1920	5.72	0.29	1.94	34.85	27.13	3.84
FoM_2 [ps]	11.05	25.3	10.67	472.4	-	-	36.8	22.9	0.98	58.23	6.13	0.31

*Estimation from graph point. **Calculated using I_Q. *$V_{DD} = 0.5V$. **$V_{DD} = 1.8V$

$$FoM_1 = K\frac{\Delta V_{OUT} \cdot I_Q}{\Delta I_{LOAD}}, K = \frac{T_{Edge}\ used\ in\ the\ measurement}{the\ smallest\ T_{Edge}\ among\ the\ designs\ for\ comparison}$$

$$FoM_2 = \frac{T_{Settling} \cdot I_Q}{PSR \cdot I_{LOAD,MAX}}, (@\ PSR\ at\ 1MHz\ [V/V])$$

TABLE 4. Comparison of state-of-the-art performance using FFRC.

Design	[55]	[56]	[57]	[62]	[64]	[65]	[66]	[67]	[69]	[70]	[73]	[75]
Topology of FFRC	Voltage-mode Gate-Injection			Current-mode Gate-Injection					Body-Injection			
Process [nm]	130	65	180	90	180	180 BCD	130	65	65	130	130	180
Active Area [mm^2]	0.049	0.048	0.037	0.015	0.14	0.12	0.018	0.036	0.087	0.0046	0.00245	0.075
V_{DD} [V]	1.15-1.8	1.2	1.8-2.5	1.15	1.8-2.6	5.0	1.15-1.4	1.15-1.3	1.2	1.2-1.5	1.2	0.7-1.1
V_{OUT} [V]	1.0	1.0	1.6-2.3	1.0	1.6	1.5-4.5	1.0	1.0	1.0	1.0	1.0	0.6
V_{DO} [V]	0.15-0.8	0.2	0.2	0.15	0.2-1	0.178	0.15-0.4	0.15-0.3	0.2	0.2-0.5	0.2	0.1-0.5
C_{OUT} [F]	2.0μ	4.7μ	1.0μ	1.0μ	28p	2.2μ	20p	4.0μ-4.7μ	120p – 540p	0-400p	N/A	0-300p
I_{LOAD} [mA]	0-25	0.1-100	0.1-200	0-140	0-50	0.1-250	0.05-50	0.0001-25	0.1-25	0-50	1-5	0.01-30
I_Q [μA]	50	40	0.9-160	33-145	55	5.6-35.6	35.4-37.32	150-350	8-297.5	42	99.04	0.22-660
Line Regulation [mV/V]	26	8.75	4.86	N/A	N/A	10.2	8.1	1	3.8	0.3	N/A	0.82
Load Regulation [mV/mA]	0.048	0.01	0.055	0.043	0.14	0.112	0.056	0.04	0.042	0.01	50	0.35
ΔI_{LOAD} [mA]	25	99.9	199.9	140	50	249.9	49.95	24.9999	24	50	1.5	24
ΔV_{OUT} [mV] (Undershoot)	10	4.0	78	70	75	36.36	54	12	55/225	140	120*	215
T_{Edge} [ns]	10	1000	100	N/A	100	250	200	20	400/100	100	200	100
Edge Time Ratio K	100	10000	1000	-	1000	2500	2000	200	4000/1000	1000	2000	1000
$T_{Settling}$ [ns]	N/A	3000	N/A	N/A	6000	9900	400	700	1500/1300	300	160	N/A
PSR (Frequency) [dB] @ I_{LOAD} [mA]	-60 (100k) -67 (1M) -56 (10M) @25	-89 (100k) -70 (1M) -62 (10M) @100	-52* (100k) -41 (1M) -52* (10M) @200	-53 (100k) -62 (1M) -56 (10M) @140	-60* (100k) -70 (1M) -37 (10M) @50	-75* (100k) -70 (1M) -62* (10M) @250	-41* (100k) -40 (1M) -20* (10M) @50	-55* (100k) -61 (1M) -47 (10M) @1	-55* (100k) -52 (1M) -37 (10M) @25	-90 (100k) -64 (1M) -18* (10M) @50	-75* (100k) -57 (1M) -41 (10M) @1	-57 (100k) -41 (1M) -22* (10M) @30
Peak Current Efficiency [%]	99.8**	99.96**	99.9	99.9	99.89**	99.99**	99.92**	99.4	98.82**	99.91	98.05**	97.8
FoM_1 [mV]	2	16.02	62.43	-	82.5	12.95	80.69	33.6	2789	117.6	15846	59125
FoM_2 [ps]	-	0.38	-	-	2.09	0.45	3.0	8.73	38.86	0.16	4.48	-

*Estimation from graph point. **Calculated by I_Q at Maximum I_{LOAD}.

$$FoM_1 = K\frac{\Delta V_{OUT} \cdot I_Q}{\Delta I_{LOAD}}, K = \frac{T_{Edge}\ used\ in\ the\ measurement}{the\ smallest\ T_{Edge}\ among\ the\ designs\ for\ comparison}$$

$$FoM_2 = \frac{T_{Settling} \cdot I_Q}{PSR \cdot I_{LOAD,MAX}}, (@\ PSR\ at\ 1MHz\ [V/V])$$

TABLE 5. Summary of PSR formulas for supply ripple insensitivity/bandwidth improvement techniques.

Topology	PSR Formula
Basic LDO	$\frac{v_{out}}{v_{in}}(s)\Big\|_{path1,2} = A_{DC\_Baisc}\frac{(1+s/\omega_{z1})}{(1+s/\omega_{p1})(1+s/\omega_{p2})}$ $\boldsymbol{A_{DC\_Basic} = \frac{1+g_{mp}r_{ds}}{1+\frac{g_{mp}r_{ds}A_{EA}R_2+r_{ds}}{R_1+R_2}+\frac{r_{ds}}{R_L}}}$
NMOS LDO	$\boldsymbol{\frac{v_{out}}{v_{in}}(s) = A_{DC}\frac{(1+s/\omega_{z1})}{(1+s/\omega_{p1})(1+s/\omega_{p2})(1+s/\omega_{p3})}}$ $A_{DC} = \frac{g_{mn}r_{ds}}{1+\frac{g_{mn}r_{ds}A_{EA}+r_{ds}}{R_1+R_2}+\frac{r_{ds}}{R_L}+g_{mn}}$
Cascaded LDO	$\frac{v_{out}}{v_{in}}(s) = \frac{v_{inn}}{v_{in}}\times\frac{v_{out}}{v_{inn}} = \frac{v_{inn}}{v_{in}}\times\frac{v_{out}}{v_{in}}(s)\Big\|_{path1,2}$ $\approx \frac{sC_{gdn}+\frac{s(C_{gdn}+C_{gsn}+C_{LPF})}{(sC_{gsn}+g_{mn})r_{dsn}}}{s(C_{LPF}+C_{gdn})+\frac{s(C_{gdn}+C_{gsn}+C_{LPF})}{(sC_{gsn}+g_{mn})r_{dsn}}}\times\frac{v_{out}}{v_{in}}(s)\Big\|_{path1,2}$ $A_{DC} \approx \frac{C_{gdn}g_{mn}r_{dsn}+(C_{gdn}+C_{gsn}+C_{LPF})}{g_{mn}r_{dsn}(C_{LPF}+C_{gdn})+C_{gdn}+C_{gsn}+C_{LPF}}\times A_{DC\_Basic}$
FVF-Based LDO	$\boldsymbol{\frac{v_{out}}{v_{in}}(s) = A_{DC}\frac{(1+s/\omega_{z1})}{(1+s/\omega_{p1})(1+s/\omega_{p2})(1+s/\omega_{p3})}}$ $A_{DC} \approx \frac{1+g_{m1}r_{ds1}}{1+g_{m1}r_{ds1}+\frac{r_{ds1}}{R_L}+g_{m1}g_{m2}r_{ds2}r_{ds1}(1+A_{EA})}$

$$v_{g3} \approx v_{in} + A_{EA}v_{out} \tag{41}$$

$$v_b = A_{FF\_BODY}v_{in} \tag{42}$$

where C_c determines the coupling capacitance between v_{in} and v_{g3}. When C_c is greater than C_{gd}, the first term of v_{g3} is approximated as v_{in}. A_{FF_BODY} represents the transfer function of the feedforward amplifier that performs body ripple injection. The PSR transfer function of the LDO can be derived as follows [69]:

$$\frac{v_{out}}{v_{in}}(s) = \frac{1+g_{mb}r_{ds}(1-A_{FF\_BODY})}{1+sC_{OUT}r_{ds}+\frac{r_{ds}}{R_1}+\frac{g_{mp}A_{EA}r_{ds}}{\left(1+\frac{s}{\omega_{ea}}\right)}+\frac{r_{ds}}{R_L}} \tag{43}$$

(43) provides the transfer function that accounts for g_{mb} and g_{mp} from v_{in} to v_{out} in the LDO. To achieve optimal PSR performance, it is desirable to set the numerator in (46) to zero. Hence, the optimal transfer function of the feedforward amplifier can be calculated as follows [69]:

$$A_{FF\_BODY} = \frac{g_{mb}+g_{ds}}{g_{mb}} \tag{44}$$

(44) indicates that feedforward gain is essential for achieving a high PSR.

Fig. 20 shows the schematic of FFRC with body ripple injection using adaptive supply ripple cancellation. This circuit includes two key components: $g_{ds}-$ to $-g_{mb}$ (GTGS) and a body ripple injector (BRI). The GTGS is responsible for adaptive control of the feedforward amplifier gain,

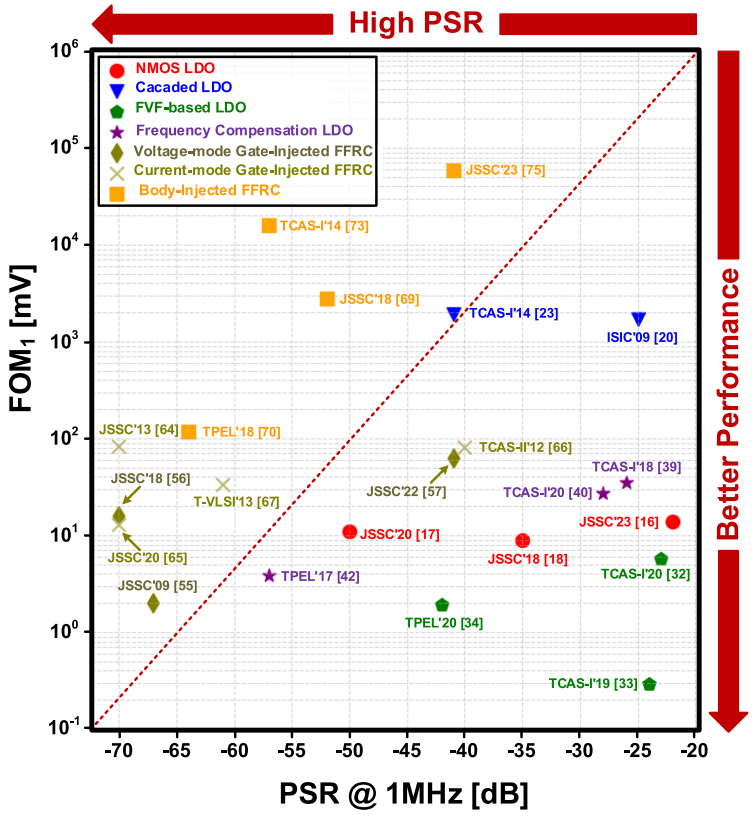

FIGURE 22. Comparison of LDO FOM1 versus PSR at 1 MHz.

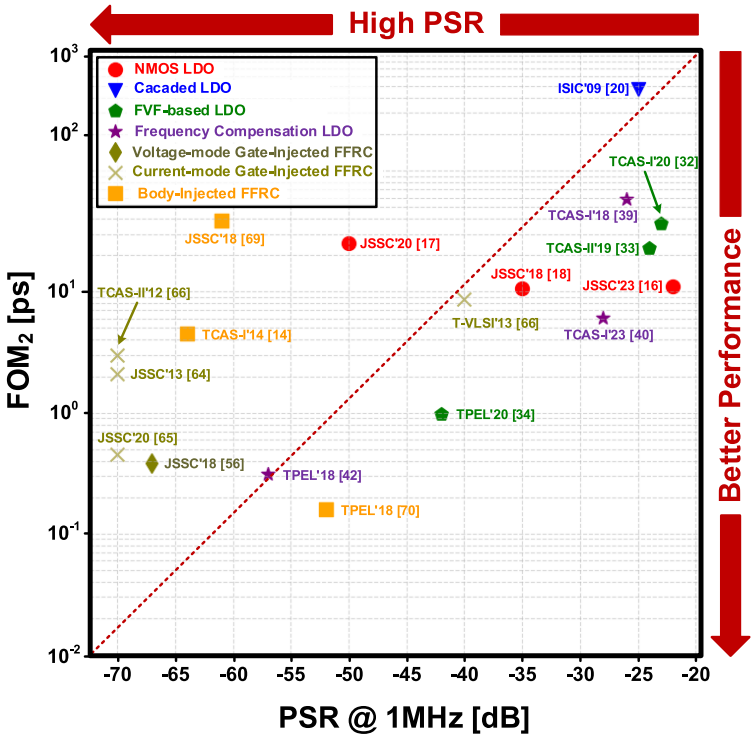

FIGURE 23. Comparison of LDO FOM2 versus PSR at 1 MHz.

whereas the BRI injects the optimal value into the body to effectively cancel out the supply ripple. The GTGS includes a pass transistor replica cell and a sensing amplifier that tracks changes in the load current, allowing for the adjustment of

TABLE 6. Summary of PSR formulas for FFRC techniques.

Topology	PSR Formula	Optimal Feedforward Gain
VM Gate-Injected FFRC	$\frac{v_{out}}{v_{in}}(s) = \frac{\frac{\{1+g_{mp}r_{ds}(1-H_{FF\_VM}(s)A_s)\}}{\left(1+\frac{s}{\omega_s}\right)}}{1+sC_{OUT}r_{ds}+\frac{r_{ds}}{R_1+R_2}+\frac{g_{mp}r_{ds}A_{EA}A_SR_2}{(R_1+R_2)(1+\frac{s}{\omega_s})(1+\frac{s}{\omega_{ea}})}+\frac{r_{ds}}{R_L}}$	$\boldsymbol{H_{FF\_VM}(s) = \left(\frac{1+\frac{s}{\omega_s}}{A_s}\right)\left(\frac{g_{mp}+g_{ds}}{g_{mp}}\right)}$
CM Gate-Injected FFRC	$\frac{v_{out}}{v_{in}}(s) = \frac{\left\{1+g_{mp}r_{ds}\left(1-H_{FF\_CM}(s)\right)\right\}}{1+sC_{OUT}r_{ds}+\frac{r_{ds}}{R_1+R_2}+\frac{g_{mp}r_{ds}A_{EA}R_2}{(R_1+R_2)(1+\frac{s}{\omega_{ea}})}+\frac{r_{ds}}{R_L}}$	$H_{FF\_CM}(s) = \frac{g_{m\_FF}}{g_{m\_BUF}} = \frac{g_{mp}+g_{ds}}{g_{mp}}$
Body-Injected FFRC	$\frac{v_{out}}{v_{in}}(s) = \frac{1+g_{mb}r_{ds}(1-A_{FF\_BODY})}{1+sC_{OUT}r_{ds}+\frac{r_{ds}}{R_1}+\frac{g_{mp}A_{EA}r_{ds}}{\left(1+\frac{s}{\omega_{ea}}\right)}+\frac{r_{ds}}{R_L}}$	$A_{FF\_BODY} = \frac{g_{mb}+g_{ds}}{g_{mb}}$

TABLE 7. Topology classification based on application requirements.

Application Requirements	Topology
Heavy Load Current (> 100 mA)	NMOS LDO [16]-[18], Frequency Compensation [40], VM -Gate-Injected FFRC [55],[56], CM-Gate-Injected FFRC [65]
Fast Transient Response (< 50 ns)	FVF-Based LDO [34], Frequency Compensation LDO [42]
Low-Voltage Operation (< 1.0 V)	FVF-Based LDO [33], Frequency Compensation LDO [40], Body-Injected FFRC [75]
High PSR at Low-Frequency Range (> -60 dB @10 kHz)	Cascaded LDO [21],[23], FVF-Based LDO [34], Frequency Compensation LDO [40] VM -Gate-Injected FFRC [55]-[57], CM-Gate-Injected FFRC [64]-[67] Body-Injected FFRC[70],[73]
High PSR at High-Frequency Range (> -40dB @1 MHz)	NMOS LDO [17], Cascaded LDO [23], Frequency Compensation LDO [34] FVF-Based LDO [42], Gate-Injected FFRC [55]-[57] CM-Gate-Injected FFRC [62], [64]-[67], Body-Injected FFRC [69],[70],[73],[75]

the feedforward amplifier gain. This design attained impressive PSR performance, consistently exceeding -36 dB across frequencies ranging from 10 kHz to 1 GHz.

Fig. 21 illustrates the implementation of FFRC with body control using a bulk-driven feedforward circuit. The circuit comprises components such as a DC-level shift, non-inverting amplifier, and load current tracking circuit. The DC-level shift performs level shifting from the supply voltage to the body bias voltage, ensuring that the source-body diode does not turn on, and serves the purpose of sensing the supply ripple. The non-inverting amplifier injects V_B into the body. The load current tracking circuit, consisting of an NMOS diode-connected transistor, is designed to adaptively adjust the gain of the feedforward amplifier based on changes in the load current. This design demonstrated remarkable results, with values of -90 and -64 dB at frequencies of 100 kHz and 1 MHz, respectively.

V. COMPARISON OF STATE-OF-THE-ART WORKS

This section discusses state-of-the-art studies related to the topologies mentioned in Sections III and IV. To compare the performances of the state-of-the-art LDOs, we evaluated

them using two different figures of merits (FOMs).

$$FoM_1 = K\frac{\Delta V_{OUT}\cdot I_Q}{\Delta I_{LOAD}} \tag{45}$$

(45) was defined to benchmark the transient response performance of the LDOs with respect to changes in the load current [76]. This metric encompasses various parameters, including the edge time ratio K, undershoot voltage during load transient ΔV_{OUT}, quiescent current I_Q, and load current step ΔI_{LOAD}.

$$FoM_2 = \frac{T_{Settling}\cdot I_Q}{PSR\cdot I_{LOAD,MAX}} \tag{46}$$

(46) was introduced to evaluate the PSR performance of the LDOs [70]. FoM_2 includes the settling time $T_{Settling}$, I_Q, PSR at 1 MHz, and $I_{LOAD,MAX}$. Using this metric for performance comparison, we efficiently assessed the PSR performance of various LDOs. $T_{Settling}$ refers to the duration it takes for an LDO's output voltage to stabilize. Particularly, when rapid load current variation occurs, a short settling time is crucial as it enhances the stability and performance of the system. Additionally, PSR is a crucial metric that indicates how effectively an LDO can mitigate variations and noise in the supply. High PSR performance ensures the delivery of clean power to each sub-block in SoCs. Therefore, $T_{Settling}$ and PSR are considered key parameters in LDO design [77].

Table 3 summarizes state-of-the-art studies using supply ripple insensitivity/bandwidth improvement techniques. As indicated in the table, the NMOS pass transistor LDO exhibits a wide bandwidth and high PSR owing to its low output impedance, especially at higher frequencies. In [17], it achieves a PSR performance of -50 dB at 1 MHz and -30 dB at 10 MHz. Additionally, it attains an FoM_1 value of 11 mV and an FoM_2 value of 25.3 ps. Similarly, the FVF-based LDO offers a wide bandwidth owing to its low output impedance. In [34], -42 dB of PSR performance at 1 MHz and -25 dB at 10 MHz were reported. The FoM_1 for this LDO is 1.94 mV, and the LDO achieves an impressively low FoM_2 value of 0.98 ps. In contrast, in [23], the cascaded LDO utilizes a cascade stage to pre-regulate the supply ripple, thereby enhancing the PSR. It achieves PSR performance of -41 dB at 1 MHz; the FoM_1 measures 1920 mV. The frequency compensation LDO achieves a wide bandwidth by cancelling the pole at a high frequency to zero. In [42], the LDO attains a PSR of -57 dB at 1 MHz and -22 dB at 10 MHz, achieving an FoM_1 of 3.84 mV and an FoM_2 of 0.31 ps. Table 4 summarizes state-of-the-art studies that utilized FFRC techniques. FFRC with gate ripple injection in [56] enhanced the PSR by utilizing a feedforward path to control the gate of the pass transistor, thereby cancelling the supply ripple. This study achieved PSR performance of -70 dB at 1 MHz and -62 dB at 10 MHz. This study also achieved an FoM_1 of 16.02 mV and an FoM_2 of 0.38 ps. In contrast, FFRC with body ripple injection in [70] utilized a feedforward path to control the body of the pass transistor by adjusting its V_{th} to cancel the supply ripple. This study achieved PSR performance of -64 dB at 1 MHz and -18 dB at 10 MHz. The measured FoM_1 and FoM_2 are 117.6 mV and 0.16 ps, respectively. Fig. 22 shows a comparison of these state-of-the-art studies in terms of FoM_1 versus PSR at 1 MHz. Notably, [33] and [34] exhibit FoM_1 values of 0.29 mV and 1.94 mV, respectively, while their PSR values at 1 MHz are -24 dB and -42 dB, respectively, highlighting their superior performance. Fig. 23 also presents a comparison of FoM_2 versus PSR at 1 MHz for the state-of-the-art studies. References [56] and [70] demonstrate the highest performance, with FoM_2 values of 0.38 ps and 0.16 ps, respectively. Their PSR values at 1MHz achieve -70 dB and -64 dB, respectively. Table 5 and 6 summarize the PSR formulas for supply ripple insensitivity/bandwidth improvement techniques and FFRC techniques, respectively. For LDO design, classify topologies based on various application conditions in Table 7.

VI. CONCLUSION

This paper presents a comprehensive analysis of PSR enhancement techniques for LDOs to facilitate efficient power management within SoCs. Analyses of PSR enhancement techniques are categorized into two groups: supply ripple insensitivity/bandwidth improvement, and FFRC techniques. Supply ripple insensitivity involves configuring the LDO in a cascade to pre-regulate the supply ripple, thereby providing a stable operating voltage to the main LDO loop and enhancing the PSR. Bandwidth improvement approaches such as NMOS pass transistor LDOs and FVF-based LDOs configure the output stage as a buffer to reduce the output impedance, thereby providing a wide bandwidth. FFRC techniques establish a feedforward injection path to control the supply ripple injected into the pass transistor through gate or body adjustments, thereby effectively cancelling the ripple and enhancing the PSR. This article provides the transfer functions, poles, and zeros for each structure through small-signal analysis. Additionally, recent research trends are discussed by comparing the advantages and limitations of each architecture. Finally, this study offers valuable insights into the design and optimization of LDOs for PSR enhancement.

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