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RESEARCH ARTICLE

Vertical Surrounding Gate Transistor for High Density and Low Voltage Operation in DRAM

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ABSTRACT In this article, a honeycomb vertical surrounding gate access transistor array scheme is proposed to further decrease the DRAM cell area with aggressively shrink bit line (BL) pitch and word line (WL) pitch adopting the ZigZag BL and WL air gap. To verify the process feasibility, process flow emulation is optimized by virtual fabrication with SEMulator3D®. Moreover, the ZigZag BL feasibility in lithography process is evaluated by optical proximity correction (OPC) simulation. In addition, the parasitic capacitance of BL and WL decrease 22.8% and 76.8%, respectively, as compared to reference paper. And the electrical properties of the proposed device are simulated by three-dimensional technology computer aided design (3D TCAD). The GIDL effect is prohibited through prolonging the drain extension and reducing its doping concentration. Finally, the surrounding gate transistor can achieve high on-state current (>30 μA) at V_g = 1.5 V and off-state current below 0.1 fA at $V_d = -0.2$ V. These results are beneficial for the direction of pathfinding for increasing the density and decreasing the energy consumption of DRAM.

INDEX TERMS Vertical surrounding gate transistor (VSGT), dynamic random-access memory (DRAM), parasitic capacitance, optical proximity correction (OPC), area scaling, power saving.

I. INTRODUCTION

The access transistor in dynamic random-access memory (DRAM) cell is the switch between bit-line data path and the capacitor [1]. The basic electrical requirement of the access transistor is high I_{on}/I_{off} ratio, which lead to long retention time and high write speed [2]. As the cell area shrinks from $8F^2$ to $4F^2$, the access transistor structure of 1T1C DRAM need to overcome short channel effect during the technology scaling down progress. Thus, the access transistor structure transforms from planar asymmetric junction structure and saddle-fin structure to vertical channel structure [2], [3]. The vertical channel transistor (VCT) can release the channel length in the vertical direction [4], which become the most suitable candidate for $4F^2$ architecture [5].

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Several researchers have been studied the VCT for DRAM access transistor, among them the vertical surrounding gate transistor offers better gate control, lower current leakage and immunity for Row Hammer effect [6], [7]. The existing VCT array scheme adopt the non-closely aligned square arrangement [8]. This arrangement will face huge challenge in process and device performance when the word-line (WL) pitch and BL pitch keep decreasing. Meanwhile, it is also difficult for orthogonal VCTs to form storage node pads for connecting honeycomb capacitors. Therefore, other access transistor arrangement is desirable for close-packed array. Besides, the power consumption of DRAM is a key point in modern computer system. Reducing the supply voltage become the main solution. For access transistor, the low operating voltage is desirable [9]. To decrease the operation voltage, decreasing the BL contact resistance is essential. However, the buried BL with low contact resistance is

difficult to form through implanting and etching process. For non-vertical surrounding gate transistor, researcher optimized the epitaxial source/drain growth process to reduce the contact resistance [10], [11]. Nevertheless, epitaxial BL has higher resistance than metal BL. Innovative method to form low resistance BL is necessary for low operation voltage of DRAM.

Herein, a novel vertical surrounding gate transistor arranged in honeycomb array for further scaling down $4F^2$ DRAM architecture is proposed. First, the integration process is explored and the process scheme is optimized, including the ZigZag BL and WL air gap. Among them, the horizontal and vertical pitch of ZigZag BL are investigated by optical proximity correction (OPC). Afterwards, the capacitance of WL and BL are extracted. Then the device optimization and simulation are conducted, which indicate the novel vertical surrounding gate transistor can operate at low voltage.

II. PROCESS INTEGRATION

To further reduce the cell area, a novel vertical surrounding gate array transistor process integration scheme was proposed. The process flow emulation was built by SEMulator3D® virtual fabrication platform.

As shown in Figure 1, the honeycombs Si drain pillar were recess etched by 300 nm to corelate the isolation process in core and peripheral regions. The oblique and orthogonal self-aligned double patterning (SADP) was used to generate patterns of the polysilicon. Then using polysilicon as hard mask to etch SiO_2. Afterwards, SiO_2 acted as a shelter from Si multi-etch. Removing the SiO_2 and depositing the polysilicon before thermal oxidation to cure the etch damage.

Figure 2 shows the scheme of BL formation process. The high dose arsenic was implanted to Si pillar for ohmic contact. Then depositing oxide and etching hole to fill Si_3N_4 as the hard mask. Following which, the SAQP process was adopted to form ZigZag trench. Finally, $TiSi_x$ salicidation and W CMP process were carried out.

To control the gate length precisely, the gate length was defined using oxide deposition thickness, instead of the lithography or etch [12]. The detailed flow was depicted in Figure 3, where sandwich structure (oxide/ nitride/ oxide/ nitride/ oxide) with aligned etched holes provides the low-temperature epitaxy location. The selective epitaxial growth should be proceeded under 600°C to protect BL salicidation [13]. Next, in-situ doping is performed while growing the polysilicon at temperature below 450°C. At such low temperature, the arsenic doping concentration could reach 1×10^{21} cm^{-3}.

Using polysilicon as hard mask of oxide, the upper oxide layer was etched back. Then, Si_3N_4 was deposited on the pillar. Afterwards, Si_3N_4 was etched back straightly to expose the middle oxide layer. Deposit oxide and CMP to acquire smooth surface. Define the WL gap by lithography and etch. Following that, the polysilicon was deposited as sacrifice layer. And the oxide was removed by wet etch. All the above process are shown in Figure 4. Then, the high-k metal gate

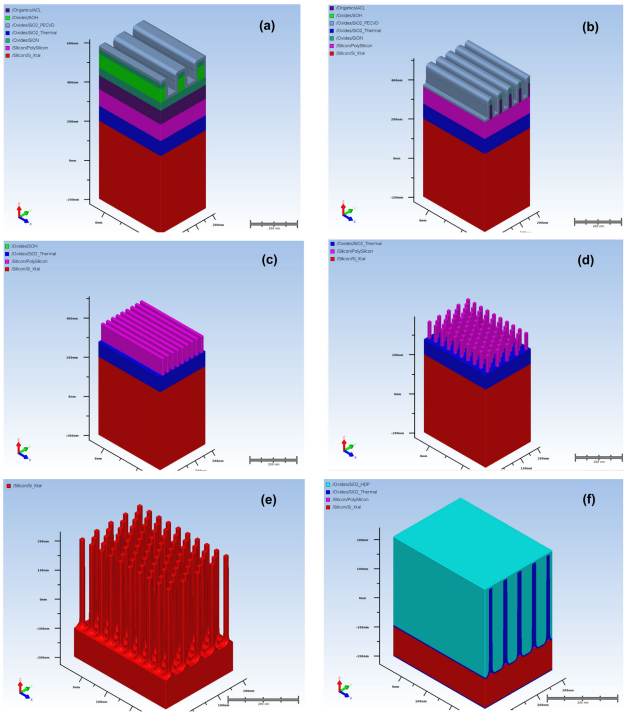

FIGURE 1. The drain pillar formation process scheme. (a) The 1st SADP process. (b) The 2st SADP process. (c) The horizontal polysilicon hard mask patten. (d) The polysilicon pillar hard mask patten. (e) Si pillar after multi-etch. (f) Oxidation and isolation.

layers were deposited by ALD. Fill in the W and etch back to form the WL. Deposit the oxide and expose the silicon surface. After removing the polysilicon and exposed high-k material, fill in the Si_3N_4 and etch back. Finally deposit the oxide and remove Si_3N_4 by wet etch. The air-gap WL was formed as Figure 5 depicts.

As Figure 6 shown, the oxide and high-k material were etched back to expose the highly-doped polysilicon layer, and then oxide was deposited and SNC contact holes were generalized. Eventually, $TiSi_x$ silicide and W contact were formed. Figure 7(a) shows the final SGT array structure. Figure 7(b) (c) display the cross-sections of the device.

The BL capacitance (CAP) is an important factor for the sensing margin of BL sense amplifier (SA). And the WL capacitance is related to the access transistor loading. The air gap was adopted to reduce WL coupling issue and alleviate the signal delay. And the firstly formed BL and finally formed Si transistor will decrease BL2SUB CAP. The BL and WL CAP were extracted and listed in TABLE 1.

III. ZigZag BL OPC EVALUATION

The ZigZag BL can be fabricated by SAQP process [15]. The width and pitch of BL mandrel are preset at 65 nm and 132 nm, respectively. The vertical pitch of BL mandrel is predetermined as 57.2 nm, as Figure 8 shows. Using the Inverse Lithography Technology (ILT), no matter how the mask shape changes in horizontal post OPC, the contour is straight. It is speculated that the pitch between the two

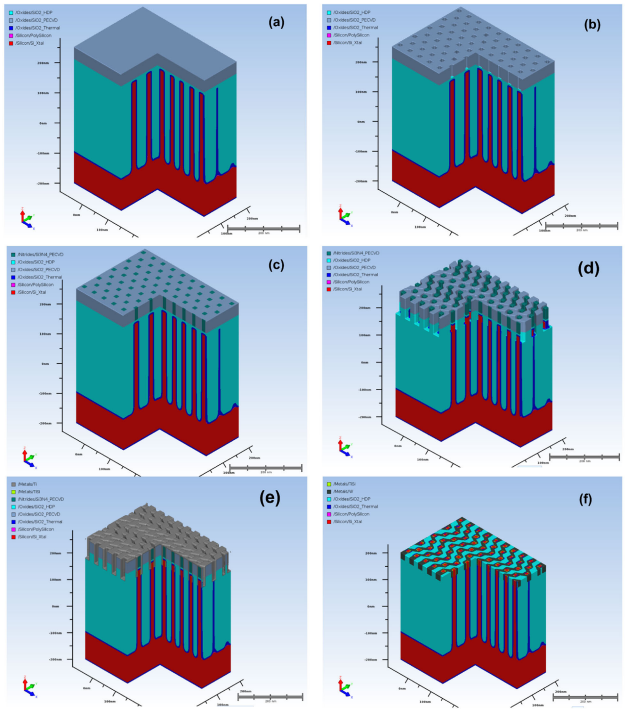

FIGURE 2. The ZigZag BL formation process scheme. (a) Implantation and oxide deposition. (b) Hole open align to the Si pillar. (c) SiN_X filling as hard mask. (d) ZigZag trench formation by SAQP. (e) $TiSi_X$ salidation. (f) Ti removal and CMP to expose the Si surface.

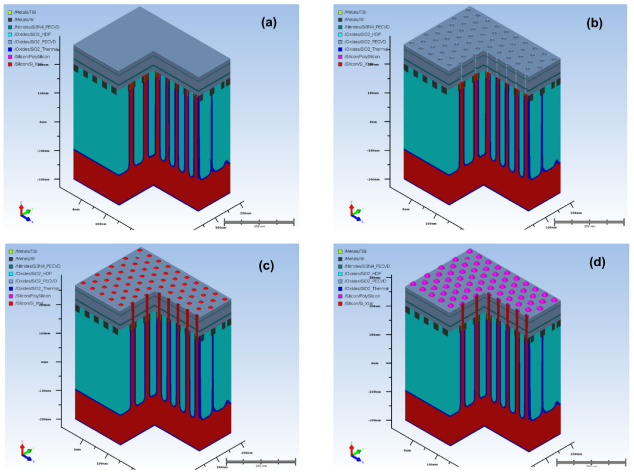

FIGURE 3. The channel formation process scheme. (a) The oxide/nitride/oxide/nitride/oxide structure deposition. (b) The aligned hole open. (c) Low temperature selective Si epitaxial growth. (d) Highly doped polysilicon epitaxial growth.

inflection points (57.2 nm) is too small and exceeded the resolution limit.

To achieve the ZigZag BL, the BL vertical pitch is doubled. The virtual lithography simulation scene is set as immersion scanner. The light source wavelength is 193 nm, and the numerical aperture (NA) is 1.35. Figure 9 (b) is the optimized light source. We simulated the BL mandrel width at 45 nm and 65 nm, the results are shown in Figure 9 (c) and (d), respectively. When the exposure latitude (EL) set at 5% and

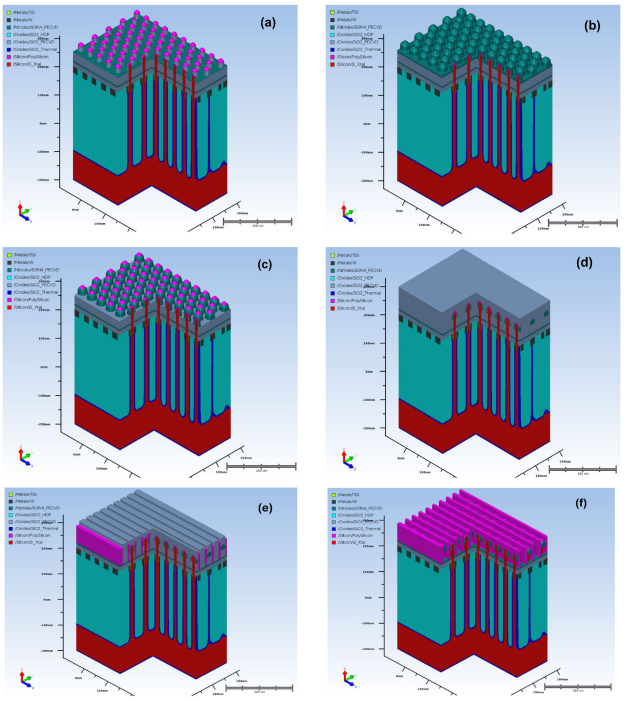

FIGURE 4. The WL formation process scheme. (a) Straight etch the oxide layer. (b) SiN_X deposition. (c) Anisotropic etching the SiN_X. (d) Depositing the oxide and CMP. (e) WL definition. (f) oxide removal.

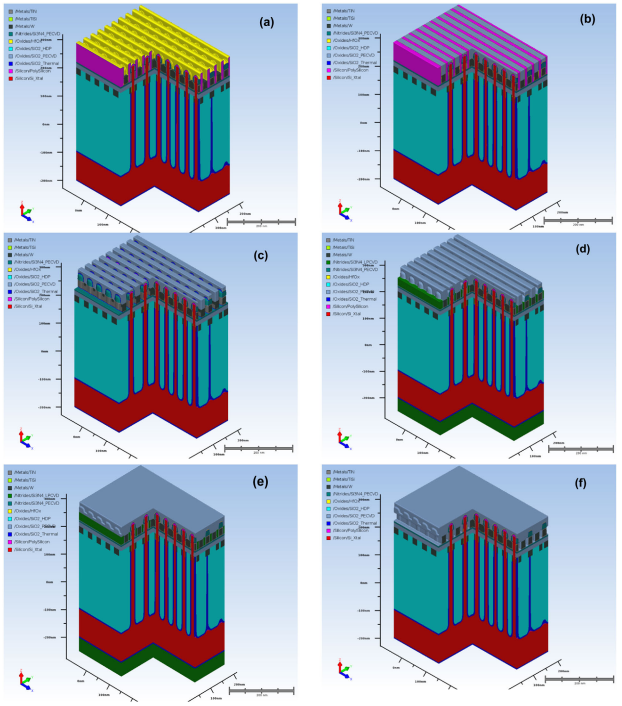

FIGURE 5. The WL air gap formation process scheme. (a) High k metal gate formation. (b) Filling oxide and CMP to expose polysilicon. (c) Polysilicon removal. (d) SiN_X deposition and etch back. (e) Oxide deposition and CMP. (f) SiN_X removal.

the critical dimension at +/- 5%, the depth of focus (DOF) of Figure 9 (c) and (d) are 80 nm and 196 nm, respectively.

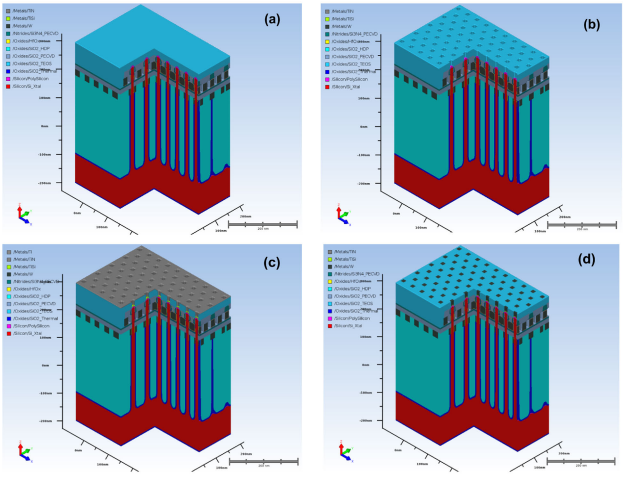

FIGURE 6. The storge node contact formation. (a) Oxide deposition and CMP. (b) Contact hole open. (c) $TiSi_X$ salidation. (d) W deposition.

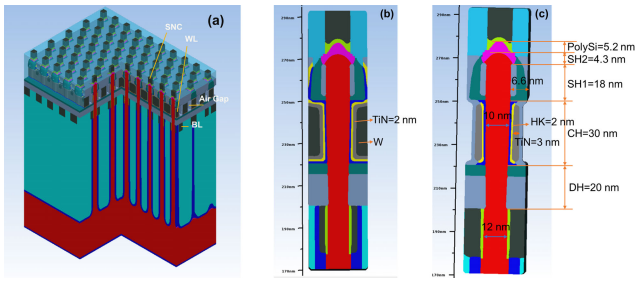

FIGURE 7. (a) The final SGT array structure. (b) The cross-section view along the WL. (c) The cross-section views perpendicular the WL.

TABLE 1. The extracted WL and BL capacitance.

Design Items	Units	SGT [This paper]	VCT [14]
CBL2Sub	aF/cell	0.4	1.5
CBL2BL	aF/cell	7.53	8.8
CBL2WL	aF/cell	1.95	2.5
CBL2SN	aF/cell	1.5×10^{-6}	NA
CWL2WL	aF/cell	2.20	20.3
CWL2BL	aF/cell	1.95	3.6
CWL2SN	aF/cell	1.84	1.9
RBL	Ω/cell	8.6	NA
RWL	Ω/cell	47	NA

The process window OPC is accessible in lithography process [16].

As described in Figure 2(d), the Zigzag pattern could be realized by SAQP process. The first mandrel width is defined

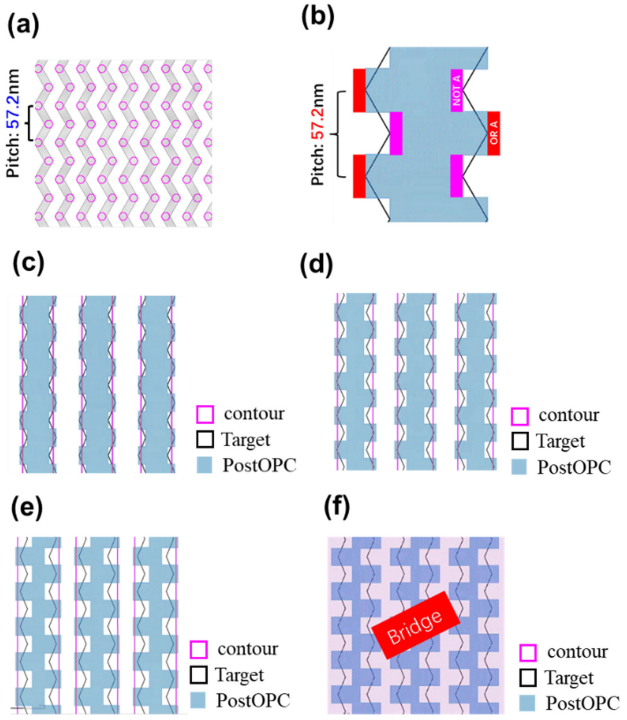

FIGURE 8. The wave distance split in horizontal. (a) the original ZigZag BL scheme. (b) The OPC cell patten (c) The additional horizontal protrusion (A) assumed 0 nm. (d) The A assumed 5 nm. (e) The A assumed 10 nm. (f) The A assumed 15 nm.

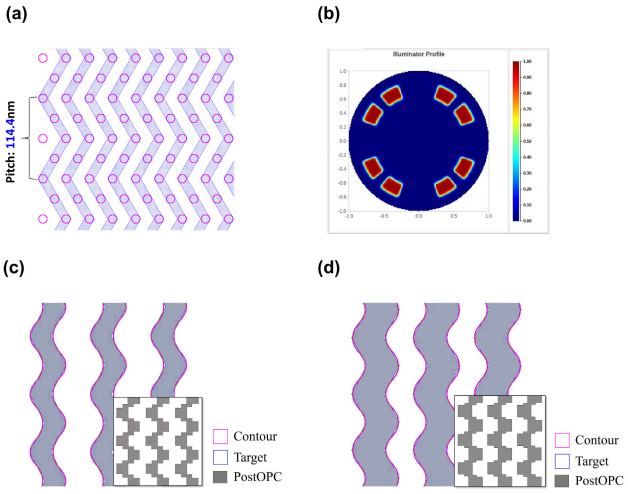

FIGURE 9. (a) The optimized ZigZag BL with double vertical pitch. (b) The source illuminator profile (TE mode). (c) The mandrel width is 45 nm. (d) The mandrel width is 65 nm.

as 45 nm, and its vertical pitch is defined as 114.4 nm. The first mandrel was generated by etch process, and then mandrel 2 was deposited on the surface of mandrel 1. The straight etch was implemented on the mandrel 2, which generate the first sidewalls. The mandrel 1 was removed and the lateral mandrel 2 pitch was reduced by half. The second sidewalls were created by deposition and etching. Then the second sidewall act as hard mask and the Si pillar side region were exposed to generate BL contact.

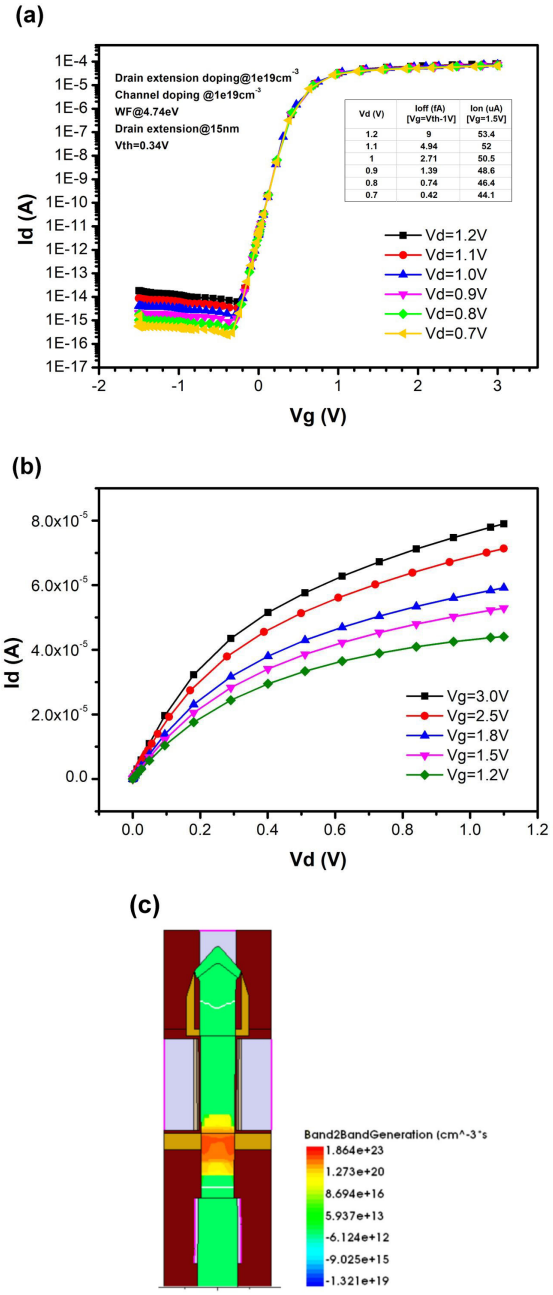

FIGURE 10. (a) The transfer characteristics of the SGT. (b) The output characteristics of the SGT. (c) Band2band generation rate of the SGT.

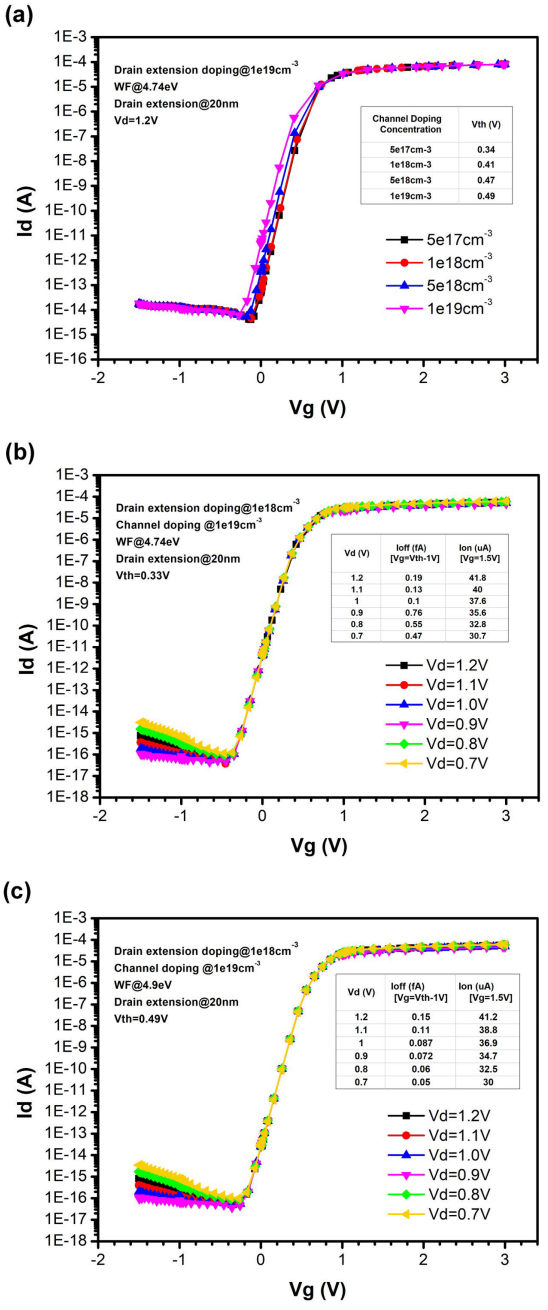

FIGURE 11. (a) The transfer characteristic with different channel doping. (b) The transfer characteristic with WF at 4.74eV. (c) The transfer characteristic with WF at 4.9 eV.

IV. DEVICE EVALUATION AND OPTIMIZATION

Since the formation scheme of SGT transistor enables higher doping concentration implantation in BL and feasible in process, this would drop the BL resistance dramatically, leading the low voltage with appropriate operation current. And then, the transistor can operate at low voltage with appropriate operation current. The junctionless SGT transistor gained constant doping at 1×10^{19} cm^{-3} by in-situ doping during epitaxy process and the gate metal WF at 4.74 eV. The bandgap narrowing and Fermi-Dirac model are activated for heavy doped regions in TCAD simulation. And the Philips Unified and Lombardi are also included in the mobility model. The Auger, Shockley-Read-Hall and nonlocal band–to-band tunneling are invoked in recombination model.

The SGT's transfer characteristic and output characteristic are shown in Figure 10. The I_{on} at 1.5 V in gate voltage is 10 times larger than other researcher's simulation value [14]. Nevertheless, the off-state current is 27 times larger than that. For the junctionless transistor, the gate induced drain leakage (GIDL) is the main reason for high off-state current, especially the lateral band-to-band tunneling [17], [18], [19].

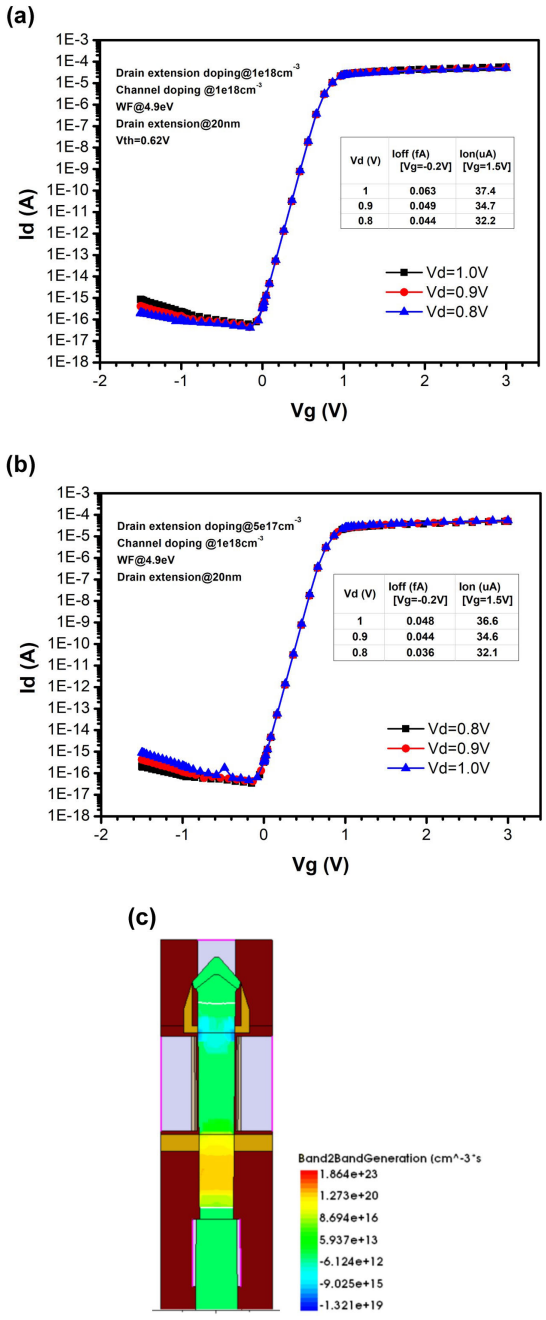

FIGURE 12. (a) The transfer characteristic with drain extension doping at $1 \times 10^{18}\text{cm}^{-3}$. (b) The transfer characteristic with drain extension doping at $5 \times 10^{17}\text{cm}^{-3}$. (c) Band2band generation rate of the SGT of (b).

In Figure 10 (a), the BTBT-induced parasitic BJT is trigged in junctionless transistor, which make the off-state current less dependent on the gate voltage [20]. Figure10 (c) shows the band-to-band generation rate is very high in the junction between channel and drain. The narrow depletion region may cause such GIDL effect. Thus, decreasing the doping concentration and prolonging the length of drain extension region will prohibit the band-to-band tunneling. Figure 11 demonstrates the GIDL effect was alleviated and I_{off} was reduced to below 0.1 fA with relatively high I_{on}.

The threshold voltage (V_{th}) of access transistor in DRAM should be larger than logic devices for lower off-state current. In junctionless transistors, decreasing the channel doping concentration and increasing the gate metal work function (WF) are benefit for channel volume depletion, which lead to the increase in V_{th} [21]. Figure11(a) shows the V_{th} increased from 0.34 V to 0.49 V as the channel doping decreased to $5 \times 10^{17}\text{cm}^{-3}$. Figure11(b) show the higher WF will increase the V_{th} from 0.33 V to 0.49 V. Since the V_{th} is as low as 0.4 V, the gate bias condition of the access transistor is defined as -0.2 V to increase noise immunity. After device optimization, the SGT achieved higher I_{on} (32.1 μA) at 1.5 V gated bias, and lower I_{off} (0.036 fA) at -0.2 V gate bias, as Figure 12 shows. In practice, the off-state current can be tested by array to avoid the limitations of electrical test equipment. After device tunning, the GIDL effect is alleviated, depicted in Figure 12 (c).

V. CONCLUSION

A novel SGT array transistor was proposed in honeycomb arrangement, with the benchmark against the 1α DRAM technology node. The process flow emulation shows it can overcome the pitch scaling limits and offer low voltage operation performance at $4F^2$ cell area. the BL formation and the followed transistor fabrication decrease the BL contact resistance greatly. The electrical results of SGT transistor show excellent SS (73 mV/dec), on-state current (32.1 μA), and off-state current (0.036 fA). The ZigZag BL can reduce the cell area without increasing the BL capacitance. Compared with the square arrangement [8], the honeycomb SGT array density has doubled. The WL air gap decrease the WL2WL coupling. The results of this simulation are input into a silicon evaluation to determine the feasibility of developing low-temperature epitaxial equipment and process. All these above merits make such SGT potential for scaling-up and low power consumption.

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