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RESEARCH ARTICLE

Voltage Injection Based MPDPC Technique for Individual Phase Loss Reduction in Active Front-End Rectifier

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ABSTRACT Active front-end (AFE) rectifiers are a well-known solution in industries due to bidirectional power flow, sinusoidal line currents, and dc-link voltage adjustment. Typically, in three-phase AFE rectifiers, the power is distributed evenly among the phase legs, aiming for a natural balancing of aging over time. However, uneven thermal stress caused by different switching frequencies or design of cooling system and prior replacement of failure power switches might create an unavoidable aging mismatch between phase legs of AFE rectifier. In this article, a per-phase model predictive direct power control with offset voltage injection is proposed. The proposed method notably reduces power loss of the weakest phase to improve the lifespan of circuit and reduce maintenance costs. The power components of the AFE rectifier are regulated utilizing predicted rectifier voltages, which are changed by adding proper zero-sequence signal to decrease losses in the most aging leg. The minimum power loss of the weakest leg involves avoiding changing the corresponding switching state for two-thirds of the source period. Simulations and experiments are conducted to validate the developed technique.

INDEX TERMS AFE rectifier, direct power control, switching loss reduction, lifespan.

I. INTRODUCTION

Over an extended period, diode rectifiers have been the primary choice for ac-to-dc conversion due to their durability and straightforward implementation. Nevertheless, the intrinsic disadvantages of diode rectifiers, such as a deteriorating power factor as the firing angle increases, elevated harmonic components in the line currents, and the restriction to unidirectional power flow, have restricted their use in advanced control systems requiring high performance. The AFE rectifier, as depicted in Fig. 1, features benefits of high current waveform quality, high power factor, and bidirectional power flow compared to the diode rectifier [1], [2], [3]. Due to its low harmonic distortion of input currents, high power factor, and stable dc-link voltage, the AFE rectifier has been widely adopted in a variety of applications where high system performances are required, including uninterrupted power supply, photovoltaic and wind turbines, electric vehicles, and stationary applications [2], [3], [4], [5]. The control strategy for this AFE rectifier must demonstrate strong stability and efficiency in order to mitigate issues related to poor power quality with high total harmonic distortion (THD) and a low power factor. Consequently, to enhance the effectiveness and capabilities of this AFE rectifier, multiple research attempts have been undertaken. The conventional control approaches rely on voltage-oriented control (VOC) [6], virtual-flux-oriented control [7], and direct power control (DPC) strategies [8], all of which make use of proportional–integral (PI) controllers. In addition to using PWM modulation, the model predictive control (MPC)

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algorithm has gained appeal as a control method for AFE rectifiers when compared to conventional approaches, thanks to its straightforward and intuitive concept, without the need for PWM blocks. [9], [10]. Furthermore, configuring the MPC algorithm with constraints and addressing nonlinearity is a straightforward process, making it feasible for practical implementation. In MPC approaches, the control schemes for the VOC of an AFE rectifier, employing predictive control for current regulation, are outlined in [11], [12]. In the meantime, when taking into account the theory of instantaneous power, it becomes feasible to predict and regulate the input active power and reactive power behavior of the AFE rectifier. This approach is known as MPDPC [13], [14].

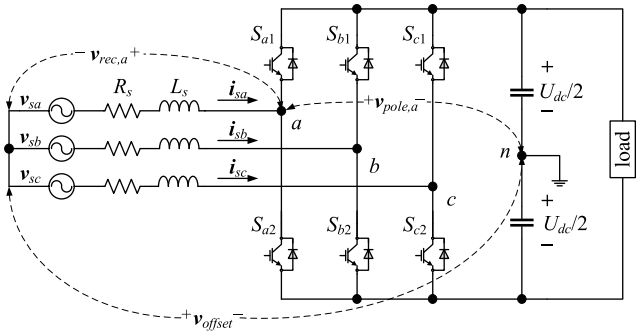

FIGURE 1. Topology of the AFE rectifier.

Ensuring the dependability of power converters has emerged as a critical concern, given its critical role in power system design. The foundation of system reliability relies on the consistent and dependable performance of the AFE rectifier [15], [16]. Nonetheless, under specific circumstances such as high voltage, extensive capacity, and high-power density requirements, fully controlled high-power switching components are employed. These switching devices are susceptible to experiencing a shortened operational lifespan or potential damage due to transient voltage or current surges during the switching process. The cumulative effect of this wear and tear can ultimately result in the failure of these switching devices. It is evident that the dependability of these switching devices is closely related to the overall reliability of the power system. If a single power switch malfunctions, the AFE rectifier will cease to function. As a result, the most aging state decides the lifespan of AFE converter. This implies that enhancing the lifespan of the switching devices contributes to an augmentation of the reliability of both the AFE rectifier and the power system [17]. The discrepancies with different aging conditions in phase legs can arise from unequal thermal stress, as shown in Fig. 2(a). An imbalanced aging among phase legs are resulted from the unbalanced thermal stress in the switches. Replacement of a new switch leads to more serious condition in disparity of aging condition, as depicted in Fig. 2(b).

The unbalanced aging situations in phase legs have not been until now addressed despite various aspects of research for the AFE rectifiers. However, enhancing the operational lifespan by minimizing switching losses has been a

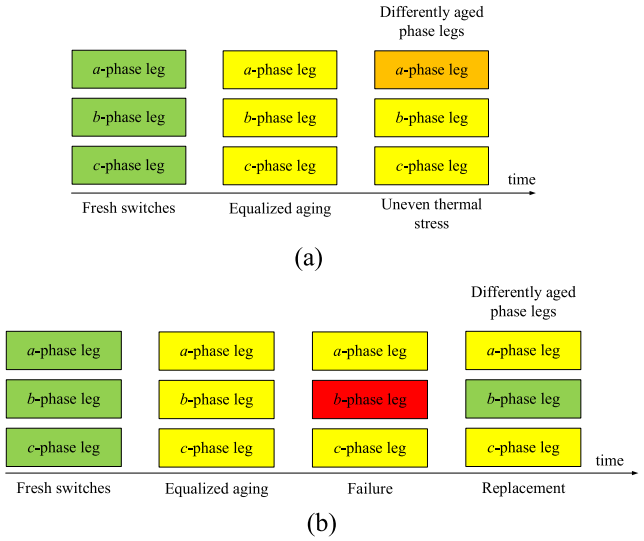

FIGURE 2. Stress and aging evolution between phase legs in AFE with (a) unbalanced heating stress, (b) supplant due to failure.

significant area of research for AFE rectifiers, especially since they are more commonly used in medium- to high-power systems. The discontinuous PWMs (DPWMs) have been known as an effective technique to decrease switching losses by injecting zero sequence voltages in the VOC method by making the switches of each phase not operate within only one-third of the fundamental cycle [18], [19]. Other approach to increase the efficiency of AFE rectifier using MPDPC using vector preselection and future offset voltage injection are introduced in [20] and [21], respectively. Another solution using altering DPWM for loss reduction for specific AFE leg was introduced in the platform of the PWM operation [22].

The contribution of this article is to enhance the lifespan of the weakest leg within AFE by applying a per-phase MPDPC by utilizing zero-sequence signal properly in each phase. Contrary to the conventional MPDPC method and prior MPC strategies aiming to reduce switching loss, the objective of developed algorithm is to achieve the minimum switching loss in the most aged leg of AFE converter, yielding better lifespan in the leg and correspondingly working time of overall converter. The developed technique adds a proper predicted offset voltage to the rectifier voltages, enabling the realization of minimum switching loss in the most aged phase. As a result, the weakest leg have significant reduction in switching loss by using the control of the predicted active and reactive power, which are produced by adding predicted offset voltage to rectifier voltage. This results in the reduction of thermal stress in the weakest leg, leading to an improved lifespan of the leg and overall AFE rectifier. Moreover, the developed scheme does not deteriorate the converter performance.

Regarding the proposed approach, it necessitates identifying the most aged leg. Diagnostic techniques involve utilizing an aging indicator to ascertain the power switch aging. The process of identifying aging indicators in these devices involves conducting accelerated aging tests while checking

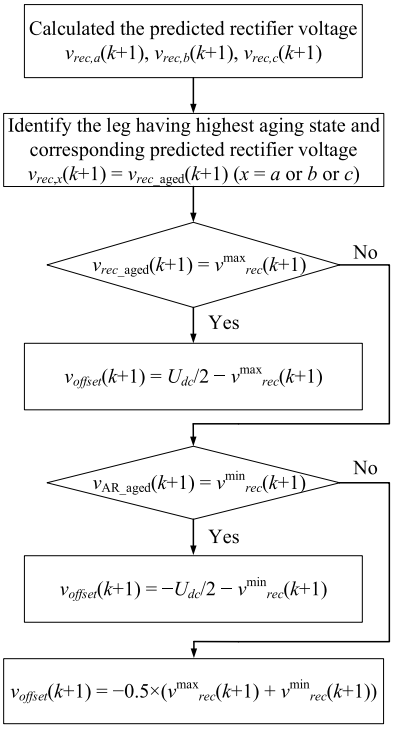

FIGURE 3. Flowchart of predicted offset voltage generation.

specific values. Through those experiments, it becomes possible to analyze the impacts of failure mechanisms and identify indicators of aging. Various electrical indicators of aging for switches were explored and suggested in existing articles, including on-state voltage in the collector-emitter terminal, $V_{ce,on}$ [23], [24], and threshold voltage V_{th} [25], [26], and temperature [27], [28], [29]. However, monitoring techniques is out of this research topic and is not addressed. Furthermore, as highlighted in prior research [30], [31], the performance of the rectifiers linked to a non-strong grid can be impacted by the phase-locked loop system. This system might fail to accurately calculate the grid angle especially for transient periods, potentially leading to system instability. However, the rectifiers using the proposed method based on power adjustment with a weak grid can operate correctly, maintaining the appropriate phase gap between source current and voltage, based on the developed technique. Nonetheless, in scenarios where significant harmonic distortion exists in the input voltage, the input current may struggle to maintain a precise sinusoidal waveform. Therefore, further enhancements are required for the proposed approach to perform effectively under both ideal and fragile grid conditions. Both simulation and experiment are conducted to show the accuracy and efficacy of the developed per-phase MPDPC with offset voltage injection for the AFE rectifier.

II. DEVELOPED PER-PHASE MPDPC TECHNIQUE

A. PREDICTIVE MODEL OF THE AFE RECTIFIER AND CONVENTIONAL MPDPC APPROACH

As shown in Fig. 1, the circuit of three-phase AFE rectifier is composed of six power switches with antiparallel diodes,

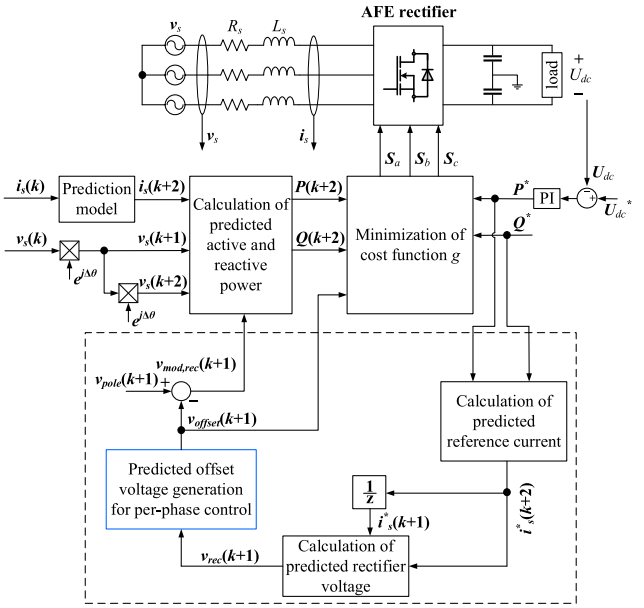

FIGURE 4. Block diagram of developed per-phase MPDPC approach.

TABLE 1. AFE rectifier parameters in simulation.

Parameter	Value
Supply voltage (V_{peak})	80
Source resistor value (Ω)	0.1
Source inductor value (mH)	15
Output capacitor value (μF)	1100
Output resistor value (Ω)	100
Sampling step (μs)	50
Dc voltage (V)	220

where S_{x1} and $S_{x2}(x = a, b, c)$ represent the switches in upper and lower parts of phase leg, respectively. The AFE rectifier is connected to the three-phase supply through input line inductance L_s and resistance R_s. To prevent short circuit problems, the two switches in each leg must operate complementarily. The gating signal $S_x(x = a, b, c)$ determines the AFE switching states is

$$S_x = \begin{cases} 1, & S_{x1} \text{ is ON, } S_{x1} \text{ is OFF} \\ 0, & S_{x1} \text{ is OFF, } S_{x1} \text{ is ON} \end{cases} \quad (1)$$

Therefore, the switching function vector $\overrightarrow{S}$ of the converter is

$$\overrightarrow{S} = \frac{2}{3}\left(S_a + S_b e^{j\left(\frac{2\pi}{3}\right)} + S_b e^{j\left(\frac{4\pi}{3}\right)}\right) \quad (2)$$

The AFE rectifier voltage v_{rec} is expressed with the voltage U_{dc} and the switching vector as

$$\overrightarrow{v_{rec}} = \overrightarrow{S} \times U_{dc} \quad (3)$$

There are eight voltage vectors obtained from the signal S_a, S_b, and S_c. These possible voltage vectors can change input power dynamic, which leads to the MPDPC approach. Kirchoff's voltage law is employed at the input of the AFE

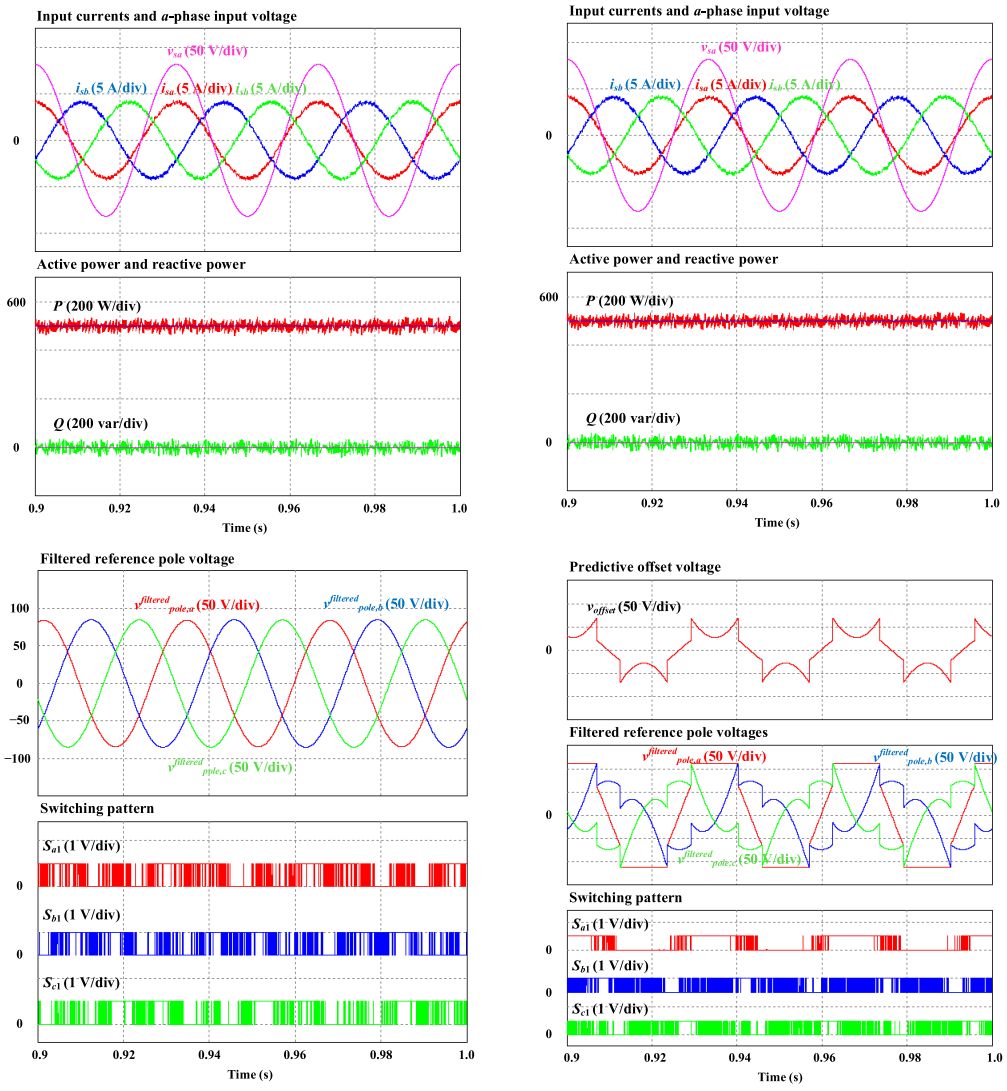

FIGURE 5. Simulation results from (a) conventional method, (b)developed per-phase technique.

converter, where the input current vector $\overrightarrow{i_s}$, and the AFE rectifier voltage $\overrightarrow{v}_{rec}$ is related as

$$L_s \frac{d\overrightarrow{i_s}}{dt} = \overrightarrow{v_s} - \overrightarrow{v_{rec}} - R_s \overrightarrow{i_s} \tag{4}$$

where $\overrightarrow{v_s}$ is the source voltage vector. The values of currents and voltages in the next sampling instant $(k+1)^{\text{th}}$ are predicted from the measured quantities at the $(k)^{\text{th}}$ sampling step by utilizing a discrete-time model. The derivative of system model, dx/dt, obtained using Euler approximation, is represented as

$$\frac{dx}{dt} \approx \frac{x\,(k+1) - x\,(k)}{T_{sp}} \tag{5}$$

Using one step advance of the above approximation, the equation of the predicted input currents and voltages for the next $(k+2)^{\text{th}}$ sampling instant of the AFE is

$$\overrightarrow{i_s}\,(k+2) = \left(1 - \frac{R_s T_{sp}}{L_s}\right) \overrightarrow{i_s}\,(k+1) + \frac{T_{sp}}{L_s}\left[\overrightarrow{v_s}\,(k+1) - \overrightarrow{v_{rec}}(k+1)\right] \tag{6}$$

The source voltage vector $\overrightarrow{v_s}$ at $(k+1)^{\text{th}}$ sampling instant can be obtained by multiplying $\overrightarrow{v_s}\,(k+1)$ to $e^{j\Delta\theta}$ where $\Delta\theta = \omega T_{sp}$ indicates the variation of source voltage vector angle in each sampling instant. The predicted power components can be obtained using the predicted input currents and predicted source voltage vectors is

$$\begin{bmatrix} P(k+2) \\ Q(k+2) \end{bmatrix} = \begin{bmatrix} v_{s\alpha}\,(k+2) & v_{s\beta}\,(k+2) \\ v_{s\beta}\,(k+2) & -v_{s\alpha}\,(k+2) \end{bmatrix} \begin{bmatrix} i_{s\alpha}\,(k+2) \\ i_{s\beta}\,(k+2) \end{bmatrix} \tag{7}$$

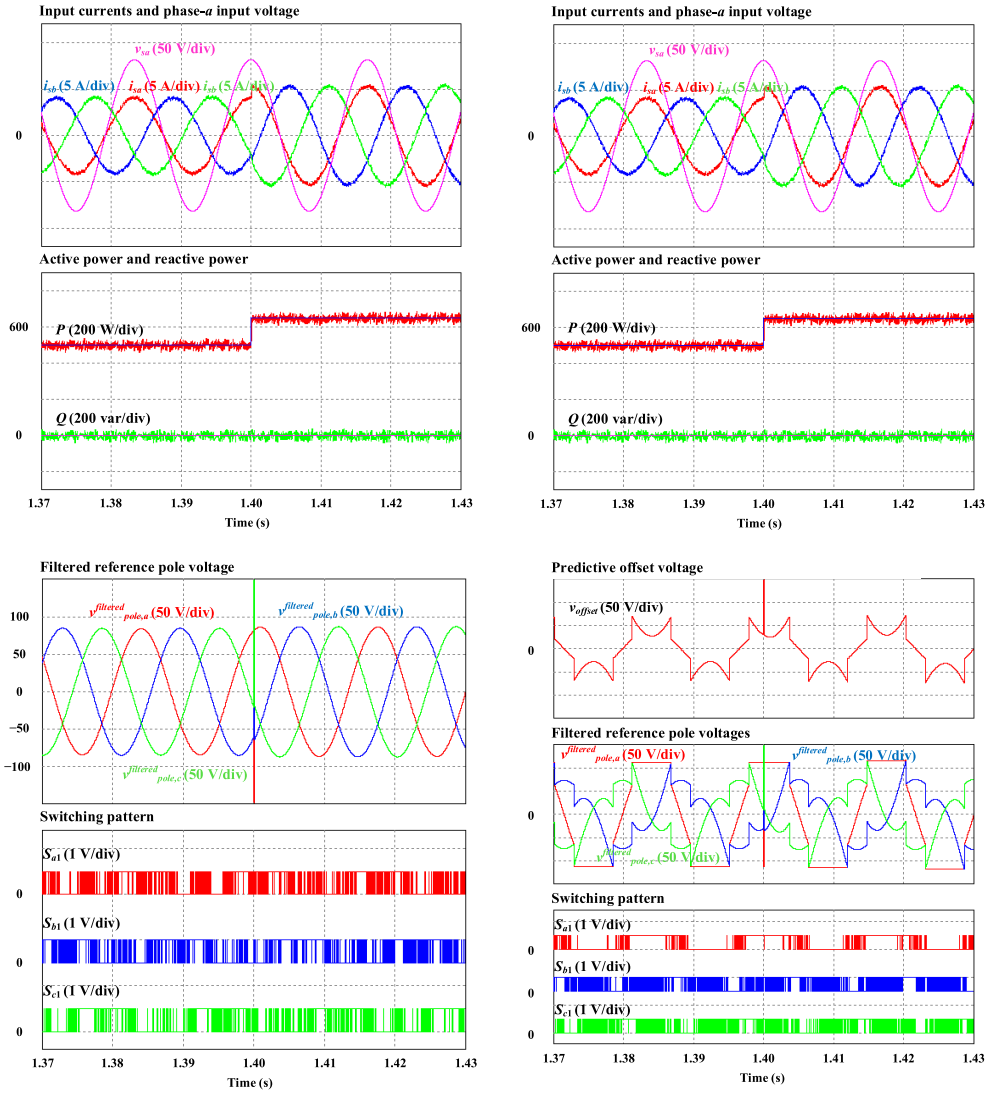

FIGURE 6. Transient-state waveforms when increasing reference active power P^* from 500 W to 750 W from (a) conventional method, (b) developed per-phase technique.

where $v_{sy}(k+2)$ and $i_{sy}(k+2)(y = \alpha, \beta)$ are $\alpha\beta$ components of predicted source voltages and predicted input currents at $(k+2)^{\text{th}}$ step.

Eliminating errors between predicted values of discrete variables and corresponding references is the primary goal of MPC approach. Then, the MPDPC method considers the cost of every switching state in terms of power components and pick the best one leading to the least power ripple, which can be quantified as

$$g = \left|P^*(k+2) - P(k+2)\right| + \left|Q^*(k+2) - Q(k+2)\right| \tag{8}$$

where $P^*(k+2)$ and $Q^*(k+2)$ represent reference power components.

B. PRINCIPLE OF DEVELOPED PER-PHASE MPDPC METHOD

There might exists an aging mismatch between phase legs of AFE rectifier caused by unequal thermal stress resulted from processes of maintenance and the production process. As a result, unbalance in the lifespan in legs might happen. If a single power switch malfunctions, the AFE rectifier will cease to function, thus, it is important to obtain improved lifespan of the weakest leg.

To reduce loss in the weakest converter phase, the predicted rectifier voltage will be changed by injecting a predicted offset voltage. The predicted offset voltage is produced in such a manner that the particular phase rectifier voltage with predicted offset voltage injection connects the leg having highest aging state to the positive or negative dc bus bar to generate clamping regions. During the clamping region, the

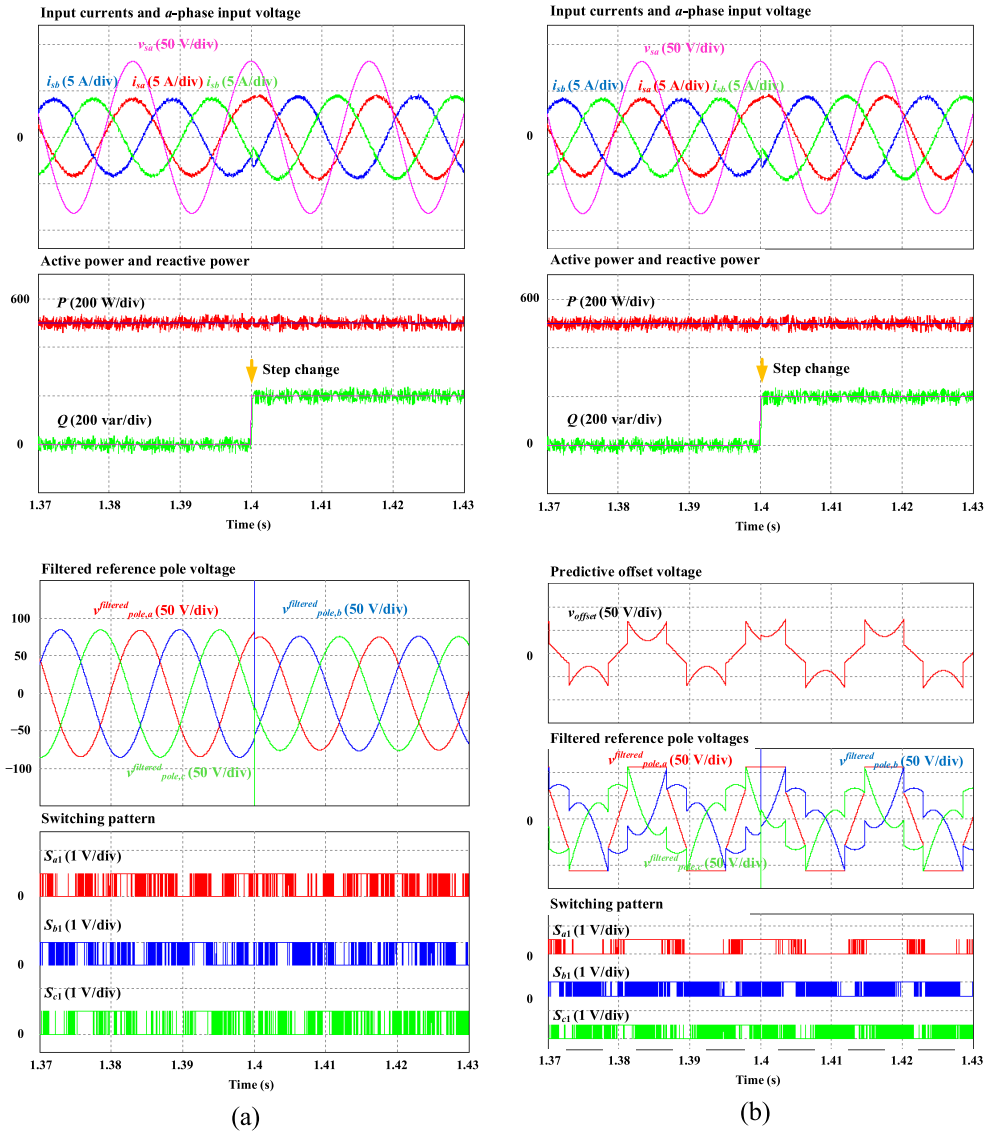

FIGURE 7. Transient-state waveforms when increasing reference active power Q^* from 0 to 200 var from (a) conventional method (b) developed technique.

weakest leg stops switching, yielding the reduction of thermal stress as well as switching loss and an increase of corresponding lifespan. To determine the predicted offset voltage, first, the rectifier voltage can be yielded by rearranging (6) as follows:

$$\begin{aligned}&\overrightarrow{v_{rec}}\,(k+1)\\&=\overrightarrow{v_s}\,(k+1)\\&\quad+\frac{L_s}{T_{sp}}\left\{\left(1-\frac{R_sT_{sp}}{L_s}\right)\overrightarrow{\imath_s}\,(k+1)-\overrightarrow{\imath_s}\,(k+2)\right\}\end{aligned}\tag{9}$$

By adding offset voltage to rectifier voltage, the pole voltage vector $\overrightarrow{v_{pole}}$, depicted in Fig. 1, can be expressed as follows:

$$\overrightarrow{v_{pole}}\,(k+1)=\overrightarrow{v_{rec}}\,(k+1)+v_{offset}\,(k+1)\tag{10}$$

From (8), the calculation of predicted rectifier voltage requires input current vector at sampling instants $(k+1)^{\text{th}}$ and $(k+2)^{\text{th}}$. Although the actual input currents can be used, they may cause a sampling delay and contain ripples, which affect the calculated result of rectifier voltage. Thus, the predicted reference current will be utilized to obtain the predicted converter voltage. The predicted reference currents in $\alpha\beta$-coordinate can be achieved as

$$\begin{aligned}i^*_{s\alpha}\,(k+2)&=\left(\frac{v_{s\alpha}(k+2)}{V^2_{peak}}\right)\\&\quad\times\left(P^*\,(k+2)+Q^*\,(k+2)\,\frac{v_{s\beta}(k+2)}{v_{s\alpha}(k+2)}\right)\\i^*_{s\beta}\,(k+2)&=\left(\frac{v_{s\beta}(k+2)}{V^2_{peak}}\right)\end{aligned}\tag{11}$$

$$\times \left(P^*(k+2) + Q^*(k+2) \frac{v_{s\alpha}(k+2)}{v_{s\beta}(k+2)} \right) \quad (12)$$

where, V_{peak} implies the voltage amplitude. The predicted reference input currents in *abc*-coordinate can be yielded by using $\alpha\beta - abc$ transformation. Fig. 3 illustrates the predicted rectifier voltages in *abc*-coordinate after substituting predicted reference input current in *abc*-coordinate to (8). In this article, *a*-phase is considered the weakest leg. Determining non-switching region in *a*-phase relies on the instantaneous magnitude of phase rectifier voltages. The predicted converter voltages are ordered based on their instantaneous amplitude as

$$v_{rec}^{\max}(k+1) = \max\left[v_{rec,a}(k+1), v_{rec,b}(k+1), v_{rec,c}(k+1)\right] \quad (13)$$

$$v_{rec}^{\text{mid}}(k+1) = mid\left[v_{rec,a}(k+1), v_{rec,b}(k+1), v_{rec,c}(k+1)\right] \quad (14)$$

$$v_{rec}^{\min}(k+1) = \min\left[v_{rec,a}(k+1), v_{rec,b}(k+1), v_{rec,c}(k+1)\right] \quad (15)$$

The non-switching intervals of *a*-phase imply the periods with $v_{rec,a}^*(k+1) = v_{rec}^{\max}(k+1)$ and $v_{rec,a}^*(k+1) = v_{rec}^{\min}(k+1)$. Meanwhile, in cases that the amplitude of the *a*-phase predicted converter voltage becomes $v_{rec,a}^*(k+1) = v_{rec}^{\text{mid}}(k+1)$, the corresponding phase leg should continuously change its switching state for the linear operation of the AFE rectifier. This is due to clamping a prohibitive phase that might lead to over-modulated operation in AFE rectifier, and thus, the controllability of input current is deteriorated [19]. The non-switching areas in upper and the lower dc-side of *a*-phase correspond to one-third fundamental period. It yields overall non-switching period in the weakest phase is 240° in one entire period, which results in a significant reduction of switching loss due to the switches of the weakest leg being maintained during clamping region. Based on the determination of clamping regions, the predicted offset voltage calculation for lowering switching loss in *a*-phase will be employed as follows:

$$v_{offset}(k+1) = \begin{cases} \frac{U_{dc}}{2} - v_{rec}^{\max}(k+1) & \text{if } v_{rec}^{\max}(k+1) = v_{rec,a} \\ -\frac{U_{dc}}{2} - v_{rec}^{\min}(k+1) & \text{if } v_{rec}^{\min}(k+1) = v_{rec,a} \\ -\frac{v_{rec}^{\max}(k+1) + v_{rec}^{\min}(k+1)}{2} & \text{if } v_{rec}^{\text{mid}}(k+1) = v_{rec,a} \end{cases} \quad (16)$$

The predicted offset voltage $v_{offset}(k+1)$ is produced in such a manner that the power switches of the weakest leg keep the present state during clamping regions, which corresponds to $v_{rec}^{\max}(k+1)$ or $v_{rec}^{\min}(k+1)$. Fig. 3 depicts the flowchart for the generation of predicted offset voltage.

After generating the predicted offset voltage, the modified rectifier voltage will be calculated from (10) as follows:

$$\overrightarrow{v_{rec}^{mod}}(k+1) = \overrightarrow{v_{pole}}(k+1) - v_{offset}(k+1) \quad (17)$$

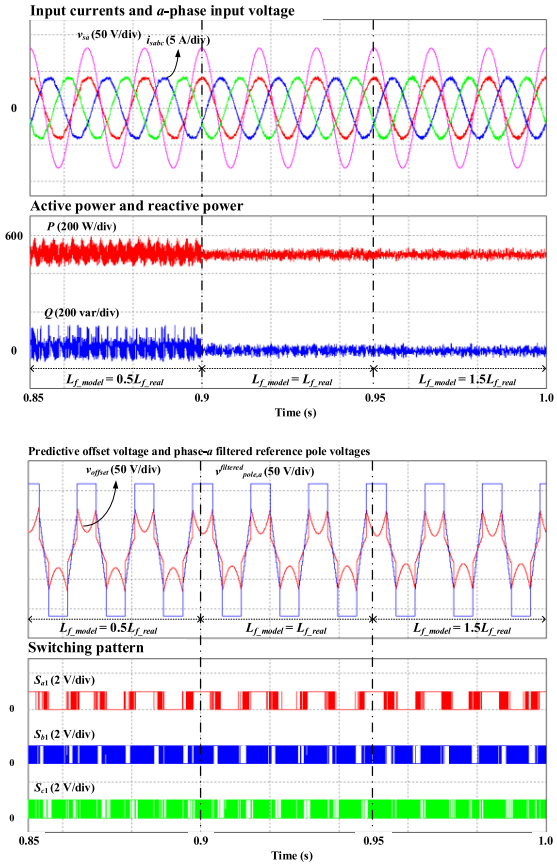

FIGURE 8. Waveforms under parameter mismatch obtained by proposed method in simulation environment.

TABLE 2. AFE rectifier parameters in experiment.

Parameter	Value
Supply voltage (V_{peak})	80
Source resistor value (Ω)	0.1
Source inductor value (mH)	15
Output capacitor value (μF)	1100
Out resistor value (Ω)	100
Sampling step (μs)	50
Dc voltage (V)	200

where the predicted pole voltage $\overrightarrow{v_{pole}}(k+1) = U_{dc}/2$ when the upper switch is ON and $\overrightarrow{v_{pole}}(k+1) = -U_{dc}/2$ when the upper switch is OFF. Along with eight possible switching state combinations, there will be eight cases of pole voltage value. The modified predicted input currents in the proposed per-phase MPDPC approach can now be calculated following modified rectifier voltage using (6) and (17) as follows:

$$\overrightarrow{i_s^{mod}}(k+2) = \left(1 - \frac{R_s T_{sp}}{L_s}\right) \overrightarrow{i_s}(k+1) + \frac{T_{sp}}{L_s}\left[\overrightarrow{v_s}(k+1) - \left(\overrightarrow{v_{pole}}(k+1) - v_{offset}(k+1)\right)\right] \quad (18)$$

By combining (7) and (18), the predicted active and reactive power in the proposed per-phase MPDPC approach will

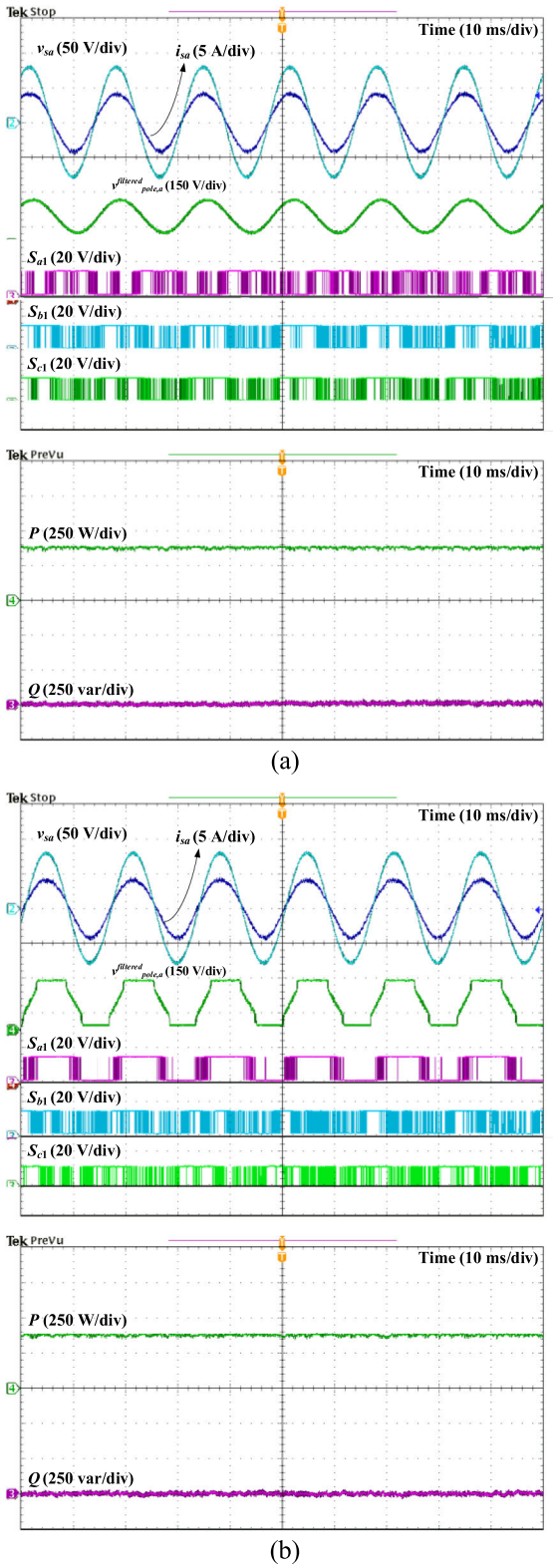

FIGURE 9. Waveforms from (a) conventional method, (b) developed per-phase technique.

be yielded. Hence, the cost function in (8) finalizes the best switching choice that results in the smallest error between the reference powers and predicted powers calculated by using

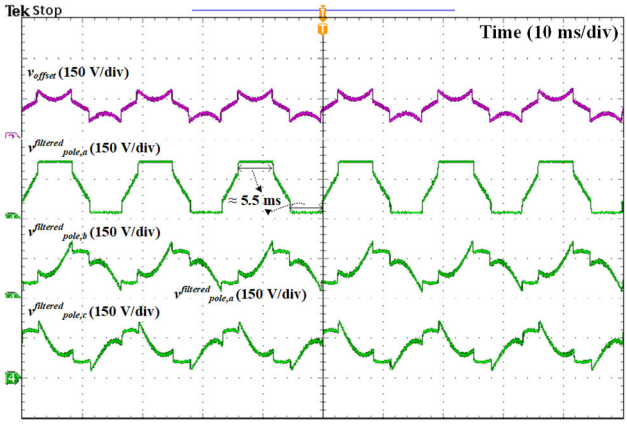

FIGURE 10. Steady-state waveforms of predicted offset voltage, filtered pole voltages from developed per-phase method.

modified rectifier voltages. The selection will be employed through eight possible cases of predicted power as in conventional MPDPC. However, the developed technique not only has the capability to directly regulate input power to match the reference powers but also manages to reduce losses in the weakest leg. Additionally, the selection of zero vector should not have an adverse effect on the clamping regions because using only the cost function in (8) cannot ensure proper selection of zero vector to avoid undesirable switching action during the clamping regions. Following [21], the zero vector selection should be employed by considering the polarity of predicted offset voltage. When the predicted offset voltages are positive, the zero-vector corresponding to turn ON all upper switches will be selected. Meanwhile, the zero-vector enabling to conduct all lower switches is selected when predicted offset voltages are negative. Fig. 4 is the block diagram of the developed method with the offset voltage injection. Similar to the conventional MPDPC scheme, the reference active power is generated by regulating the output dc-link voltage through a PI controller. Meanwhile, the reference reactive power is generally set as zero for the unity power factor. The offset voltage is introduced to generate modified rectifier voltages to minimize switching loss and corresponding thermal stress in the weakest leg. Furthermore, it is noteworthy that the developed method does not need extra components to be executed properly. Thanks to this proposed MPDPC strategy, the AFE rectifiers with the weakest leg function with minimal switching losses under all operating conditions, whether they are steady-state or transient state.

III. SIMULATION VERIFICATION

The developed method was tested with a circuit simulator PSIM. Performance of the developed approach was validated by comparing its simulation results with that of conventional MPDPC method. In the simulation of the proposed per-phase MPDPC method, *a*-phase is assumed to be the weakest leg. Variables used for the simulation are in Table 1.

Fig. 5 displays the simulated waveforms of the conventional and the developed methods, including *a*-phase supply

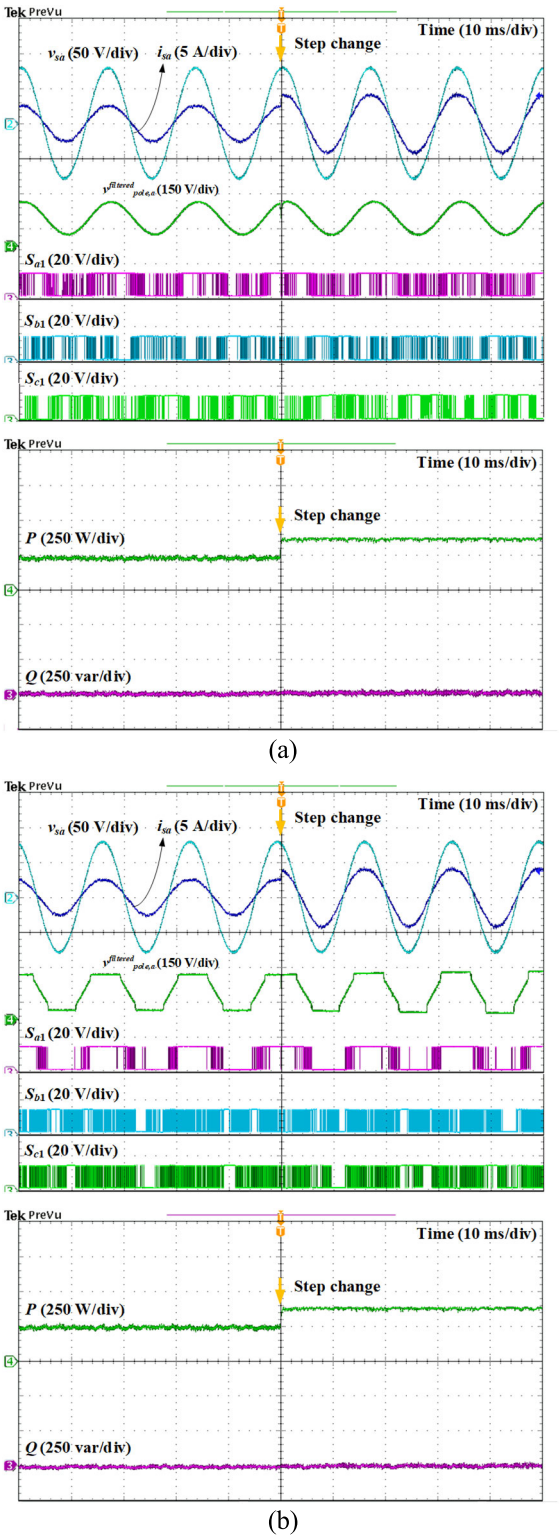

FIGURE 11. Transient-state waveforms when increasing reference active power P^* with 250W to 400W from (a) conventional method (b) developed per-phase technique.

voltage, supply currents, switch signals, and active and reactive powers. As can be seen in Fig. 5(a) and (b), the input currents acquired by two control schemes are balanced and correct in terms of phase. The input current and source voltage are in phase, indicating the achieved unity power factor. From Fig. 5(a) and (b), it can be seen that the actual power components follows their references at $P^* = 500$W and $Q^* = 0$var, respectively. The two control schemes display similar fluctuation in the two power components. Fig. 5(b) illustrates that the filtered pole voltages after adding offset voltage to rectifier voltage by proposed per-phase MPDPC are presented. Different from the filtered pole voltages acquired by proposed approach in Fig. 5(a), the offset voltage in conventional MPDPC is zero. Thus, the resulting pole voltages are sinusoidal. Meanwhile, the filtered pole voltage of a-phase has periods with the switches linked to either upper or lower dc bus bar without switching operations. This clamping region, accounting for one-third of one supply period, results in the total non-switching areas of 240^o for the weakest phase. It makes the weakest leg generate the minimum loss, yielding improved lifespan. The b-phase and c-phase filtered pole voltages obtained by the proposed scheme do not contain clamping region. This results in the normal switching patterns of b-phase and c-phase as in conventional MPDPC.

The transient responses are evaluated from Fig. 6, in which the P^* has a sudden step from 500W to 650W. Fig. 6 shows that the input current magnitudes of the two methods change correspondingly to the rise of active power. Additionally, there is no coupling in both active and reactive powers acquired by two control schemes. In Fig. 6(b), the switching pattern of a-phase has exact clamping regions of 120^o even during the transient-state thanks to the injection of predictive offset voltage.

Fig. 7 shows the simulation results in a case that Q^* changes from 0 to 200var, with $P^* = 500$W. It shows that the supply currents is out-of-phase with the supply voltage due to non-zero reactive power. Due to the rise of positive reactive power, the input current lags the input voltage. In Fig. 7(b), the switching pattern of a-phase has exact clamping regions of 120^o even during the transient-state thanks to the injection of predictive offset voltage.

The output performance and stability of power system might be degraded due to the parameter mismatch when employing MPC technique. Here, the accuracy of system parameters is crucial for the reliability of prediction model. Fig. 8 illustrates the AFE performance with mismatch of input inductor values from the developed approach. The first segment of waveform is a case that the input inductor value used in the controller modeling is 50% lower than the real inductor value ($L_{s,model} = 0.5L_{s,real}$); the middle segment is in a case that $L_{s,model} = L_{s,real}$; and the last segment is a case that $L_{s,model} = 1.5L_{s,real}$. As can be seen from Fig. 8, the proposed per-phase MPDPC technique properly regulates the supply currents. On the other hand, Fig. 8 indicates that the power components under $L_{s,model} = 0.5L_{s,real}$ possess notably greater ripples.

IV. EXPERIMENTAL VERIFICATION

To additionally confirm the merits of the of the developed technique, a practical configuration for the AFE was built.

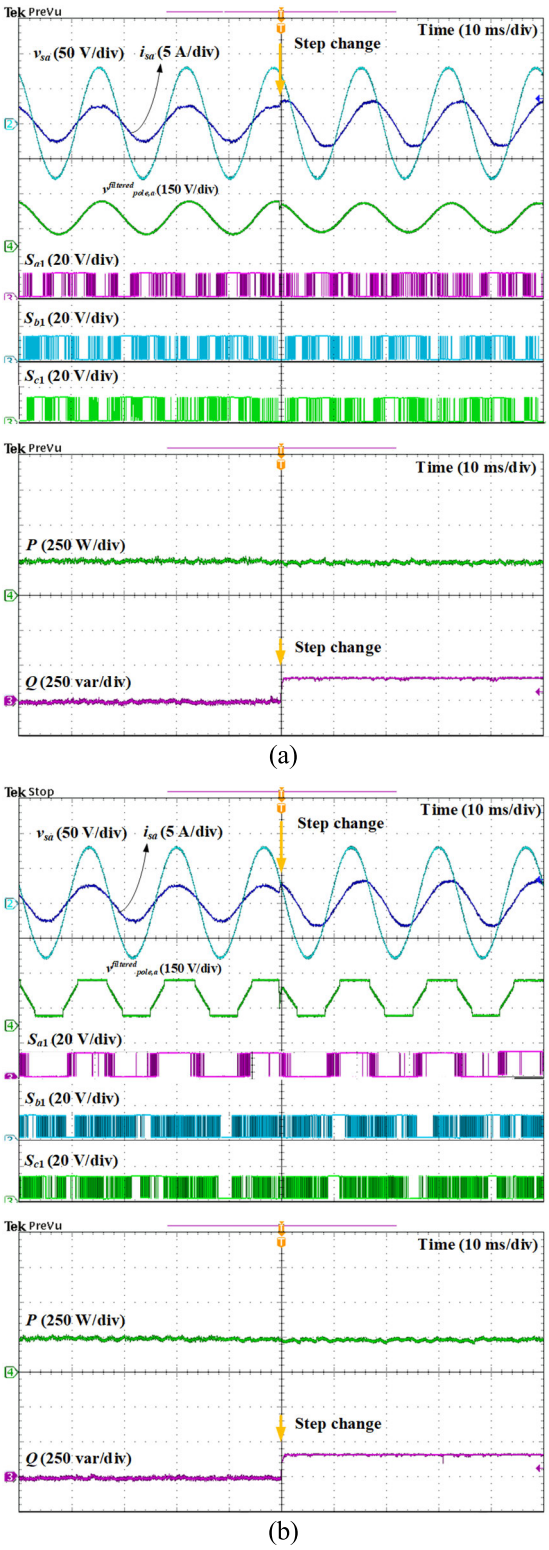

FIGURE 12. Transient-state waveforms when increasing reference active power Q^* from 0 to 200var from (a) conventional method (b)developed per-phase technique.

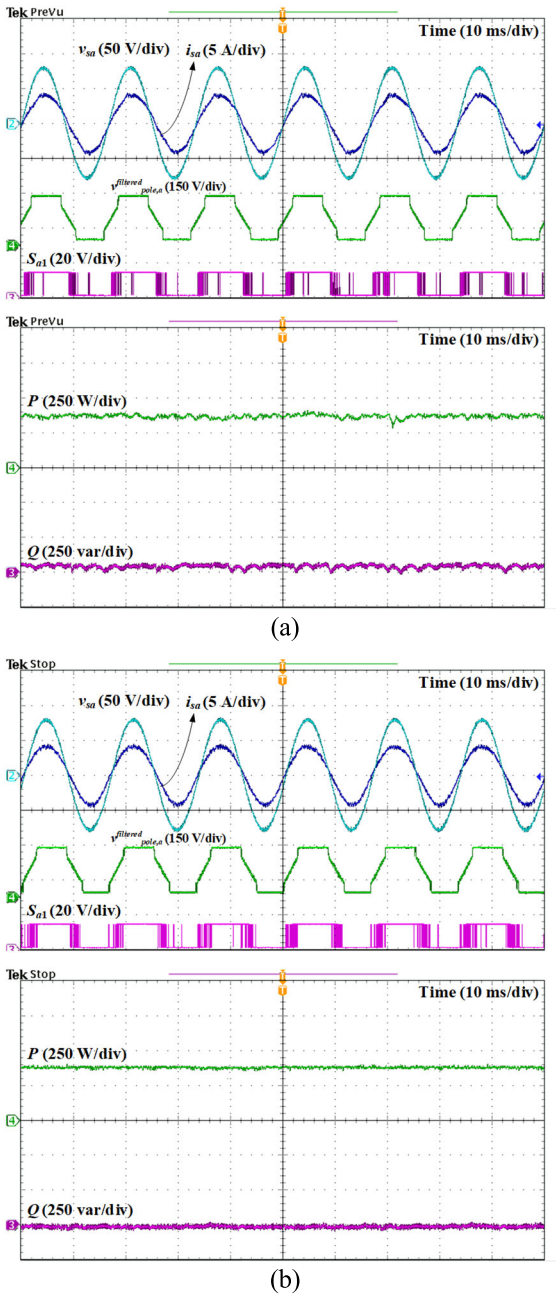

FIGURE 13. Waveforms under parameter mismatch obtained by proposed method in experimental environment.

The conventional and the developed techniques are executed using Texas Instrument TMS320F28335 Digital Signal Processor (DSP). The ac supply voltages are generated using CHROMA 61702. The parameters and conditions are listed in Table 2.

Fig. 9 displays the waveforms of the conventional and the developed method, including *a*-phase input voltage, *a*-phase supply currents, switch signals, and power components. As can be seen in Fig. 9(a) and (b), the input currents acquired by two control schemes are balanced and correct in terms of phase. The input current and source voltage are in phase, indicating the achieved unity power factor. From Fig. 9(a) and (b), the two power components follows the references with $P^* = 400$W and zero Q^*. The two

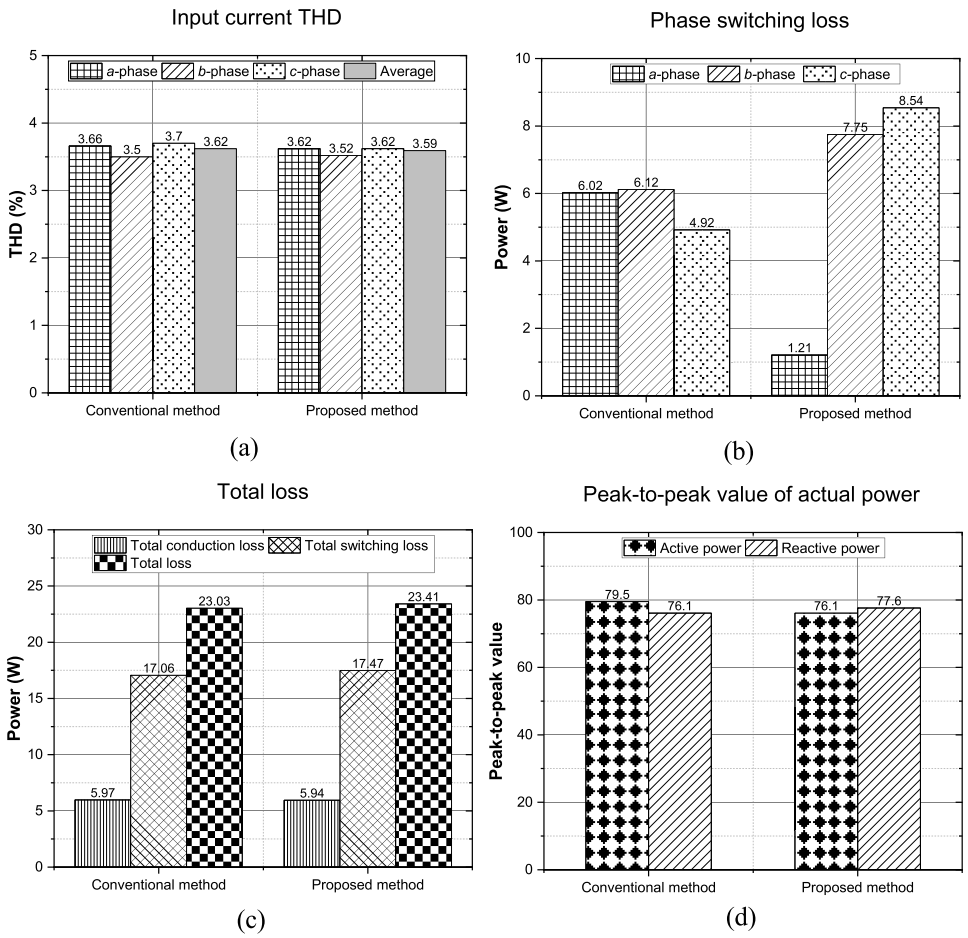

FIGURE 14. Comparison between conventional and developed techniques (a) source current THD, (b) switching loss, (c) entire loss, (d) ripples of power components.

control schemes display similar fluctuation in actual active and reactive power.

In Fig. 10, the waveform of offset voltage and filtered pole voltage obtained by the proposed approach is presented. The filtered pole voltage of a-phase has periods with the switches linked to either upper or lower dc bus bar. This clamping region, accounting for $^1/_3T_f = {}^1/_3 \times {}^1/_{60} \approx 5.55$ms, as shown in Fig. 10, results in the entire non-switching areas of 240^o for the weakest phase. The b-phase and c-phase filtered pole voltages obtained by the proposed scheme do not contain clamping region. This results in the normal switching patterns of b-phase and c-phase as in conventional MPDPC.

The transient response obtained from the two schemes is shown in Fig. 11, where P^* command from 250W to 400W. The two approaches have the same power tracking capability, as shown in Fig. 11, where the input current magnitude changes correspondingly to the rise of active power. Moreover, there is no coupling in both active and reactive powers acquired by the two algorithms.

Fig. 12 shows the experimental results with Q^* from 0 to 200var, whereas $P^* = 400$W. The two approaches have the same power tracking capabilities, as shown in Fig. 12. When the reactive power increases, the supply current is out-of-phase with the supply voltage. Due to the positive Q, the input current lags the input voltage. In Fig. 12(b), the switching pattern of a-phase has exact clamping regions of 120^o even during the transient-state thanks to the injection of predictive offset voltage.

Fig. 13 illustrates the experimental AFE performance with mismatch of input inductor values in the developed algorithm. Fig. 13(a) shows the experimental results with $L_{s,model} = 0.5L_{s,real}$, while Fig. 13(b) is a case of $L_{s,model} = 1.5L_{s,real}$. As can be seen from Fig. 13(a) and (b), although the developed technique accurately regulates the sinusoidal supply currents, the power elements under $L_{s,model} = 0.5L_{s,real}$ has higher ripples than that of $L_{s,model} = 1.5L_{s,real}$.

V. PERFORMANCE EVALUATION

The conventional and the developed techniques are comprehensively compared and evaluated as shown in Fig. 14(a) – (d) [32], [33]. Fig. 14(a) illustrates that the average and the a-phase input current THD by the developed method are marginally lesser than those attained using the conventional method. The developed per-phase MPDPC

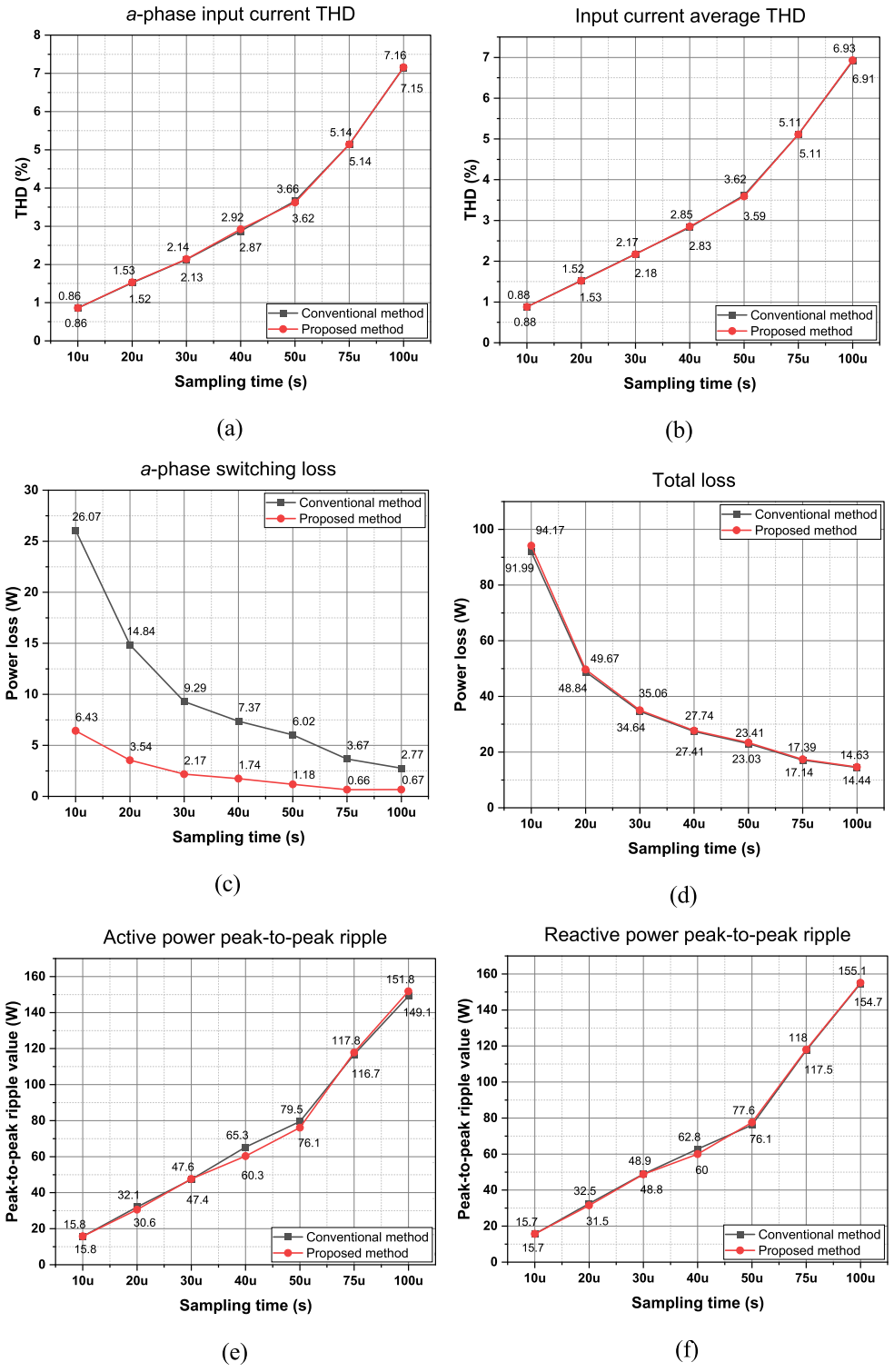

FIGURE 15. **Performance comparison between conventional and developed technique versus different sampling steps (a) *a*-phase current THD, (b) average THD, (c) *a*-phase switching loss, (d) total loss, (e) active power ripple, (f) reactive power ripple.**

technique greatly decreases the switching loss in *a*-phase by around 80%. Nonetheless, the switching losses in *b*-phase and *c*-phase increase over the conventional MPDPC method by approximately 26% and 74% respectively. The increasing loss from the two other legs represents a trade-off between maintaining low input current THD and minimizing power loss in the weakest leg. Additionally, the rise in loss in these phase legs will contribute to reducing the aging mismatch

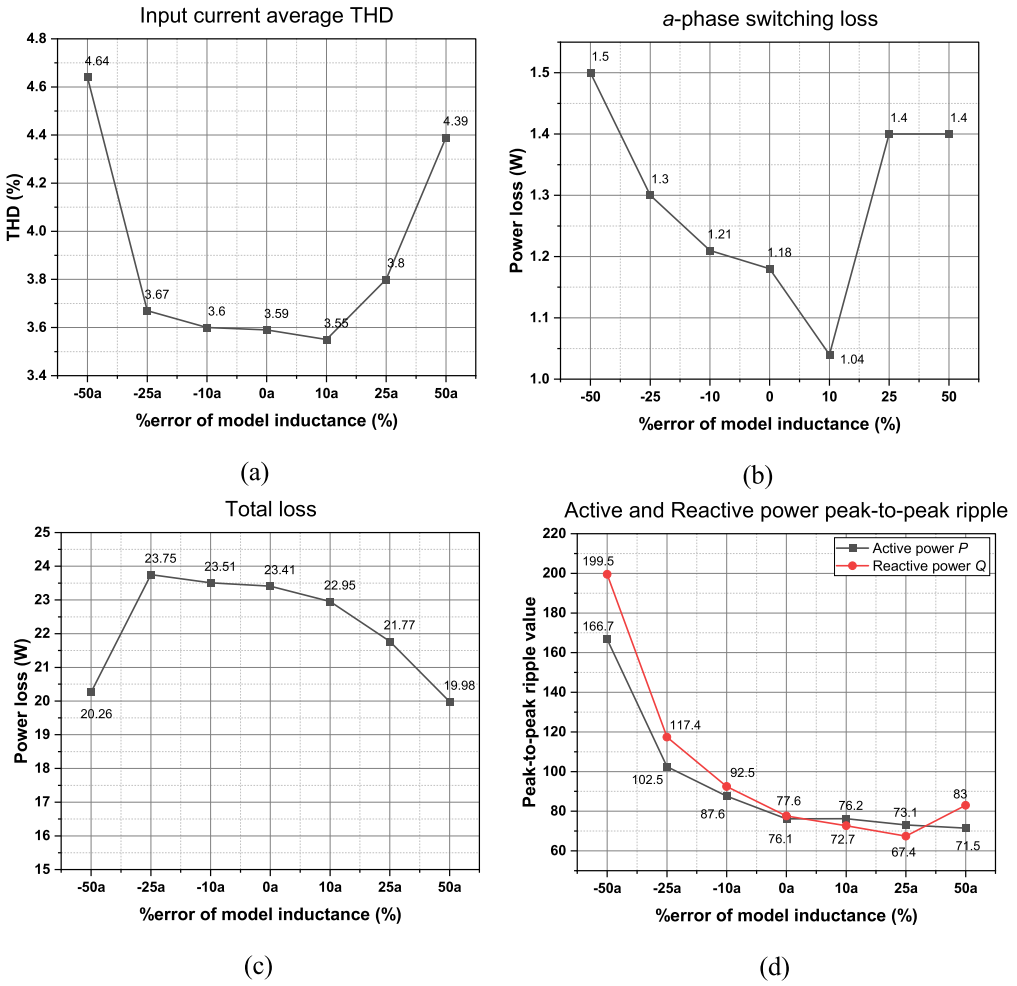

FIGURE 16. Performance of developed per-phase technique with mismatch of input inductor (a) average source current THD, (b) *a*-phase switching loss, (c) entire loss, (d) ripple of power components.

among the three-phase legs of the AFE rectifier. Comparison of the entire losses presented in Fig. 14(c) shows a negligible increase of proposed per-phase MPDPC scheme compared to the conventional approach. In Fig. 14(d), the active power ripple from the developed technique is reduced than that of the conventional method, whereas the reactive power from the developed technique has slightly higher ripples.

The comparative assessments are expanded with varying sampling steps in Fig. 15(a) – (f). It is well known that the reduced sampling time leads to improved control performance in the platform of the MPC. Fig. 15(a) and (b) depict the THD values from the *a*-phase current and total THD. An observable trend is the rise of THD as the sampling step increases, and the THD exhibit a similarity in the two techniques. The proposed control scheme decreases the *a*-phase switching loss by around 80% compared with the conventional method when sampling time varies, as shown in Fig. 15(d). In the meantime, the entire loss with various sampling times exhibits a similarity. The ripples of power components from Fig. 15(e) and (f) from the two algorithms show trivial differences.

Fig. 16(a) – (d) shows the results of the developed MPDPC method with mismatch of input inductor values. As depicted in Fig. 16(a), the average THD from the developed concept rises in a case that the model value of the input inductor is higher than the actual inductance and 50% lower case. The *a*-phase switching loss is lowest in a case that the model value is 10% higher than the actual inductance. On the other hand, the *a*-phase switching loss increases in a case that model value is lower or higher than the actual value. In Fig. 16(d), the power ripples notably rise in a case that the model inductor value is lower than the actual value, whereas they slightly reduce with higher model inductor value than the actual value.

VI. CONCLUSION

This paper addresses integrating an offset voltage injection technique in MPDPC method to control an AFE rectifier, aiming at reducing switching loss in the weakest leg to increase the lifespan of converters. The proposed method selects the appropriate offset voltage, which generates maximum clamping region of two-thirds of the fundamental period for the weakest leg. During the non-switching areas, the switches of

the only weakest leg does not work, leading to a significant reduction of loss and an increased lifespan of the corresponding AFE rectifier. The effectiveness of the developed per-phase MPDPC technique was found to enable significant decrease in losses of the weakest leg in comparison with the conventional MPDPC technique. Aside from the trade-off capacity of the developed per-phase MPDPC with offset voltage injection technique, the verification results validate a reduction of the switching losses for the particular most aged leg up to 80% and guarantee the input current performance as compared to the conventional MPDPC approach. The developed per-phase method performs well under steady-state and transient-state operation and different input power factor angles. Therefore, the proposed approach is applicable and valuable in practical power systems for improving lifespan and reducing maintenance costs. Regarding the unresolved issues of the proposed approach, the increasing loss in the two other legs represents a trade-off between maintaining low input current THD and minimizing power loss in the weakest leg. In the future, the proposed method should be improved to maintain low input current THD but not increase loss in the other legs or limit the amount of increment.

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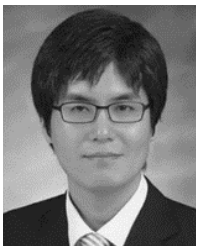

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