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RESEARCH ARTICLE

A 12-bit High-Speed Time-Interleaved Pipelined Asynchronous Successive-Approximation ADC in 22-nm FDSOI CMOS

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ABSTRACT A 12-bit time-interleaved (TI) analog-to-digital converter (ADC) with pipelined successive-approximation (SAR) channels is presented in this paper. The ADC consists of four TI channels, each incorporating a two-stage pipelined asynchronous SAR ADC. To facilitate clock distribution, a common bootstrapped sampler in front of the four channels is employed. The reset switch in the capacitive digital-to-analog converter (CDAC) of each channel is also bootstrapped to enhance the speed and linearity. A prototype ADC has been designed and implemented in a 22-nm FDSOI CMOS technology, with a core occupation area of 0.43 mm^2. Measurements show that the ADC achieves a signal-to-noise-and-distortion ratio of 50dB with a low-frequency input, and of 48.5 dB at Nyquist. The total power consumption is 37.5 mW; the core ADC consumes 19.3 mW from a 0.8V supply. With a 1.4 GS/s sampling rate and input at Nyquist, the ADC achieves a Walden's figure of merit of 114 fJ/conversion.

INDEX TERMS Analog-to-digital converter (ADC), CMOS, comparator, bootstrapped switch, dynamic amplifier (DA), asynchronous SAR, time-interleaved (TI), pipelined successive approximation (pipelined-SAR).

I. INTRODUCTION

The current trend in communication systems is geared toward achieving high-speed and energy-efficient solutions. This makes direct sampling receivers [1], [2] very attractive, at the same time placing stringent demands on the analog-to-digital converters (ADCs), which must allow high sampling rates –typically in the range of billions of samples per second (GS/s) – low power consumption, and mid-to-high resolutions. Flash ADCs [3], [4] stand out as the fastest converters among the various available architectures, making them the best choice for high-speed applications. However, they are not power and area-efficient when designed for high or medium-resolution applications. Delta-sigma ADCs, on the other hand, can deliver a high number of bits, but are primarily suitable for low-speed applications [5], [6]. Overall, successive approximation (SAR) ADCs emerge as strong contenders. They possess inherent digital-friendly characteristics and are known for their power-efficient operation while delivering resolutions ranging from moderate to high [7], [8], [9]. Nevertheless, SAR ADCs have a limitation regarding their operational frequencies, typically peaking in the range of a few hundred megahertz.

Time-interleaving (TI) and pipelining can enhance the speed of SAR ADCs [10], [11], [12], [13], [14]; this, however, comes at the expense of a higher design complexity and additional linearity issues [11], [15], [16], [17]. In this paper, we employ a 4-channel TI pipelined-SAR ADC and tackle the linearity challenge with digital error correction. The SAR parts of the ADC are operated asynchronously, with a locally generated high-speed clock for bit-level operations. Despite increasing the design complexity, this choice is attractive, as it results in an enhanced conversion speed and a reduced power consumption [18]. To further save power and reduce the noise contribution of the inter-stage amplifier, a dynamic amplifier (*DA*) is interposed between the two pipelined SAR stages of each TI channel (sub-ADC).

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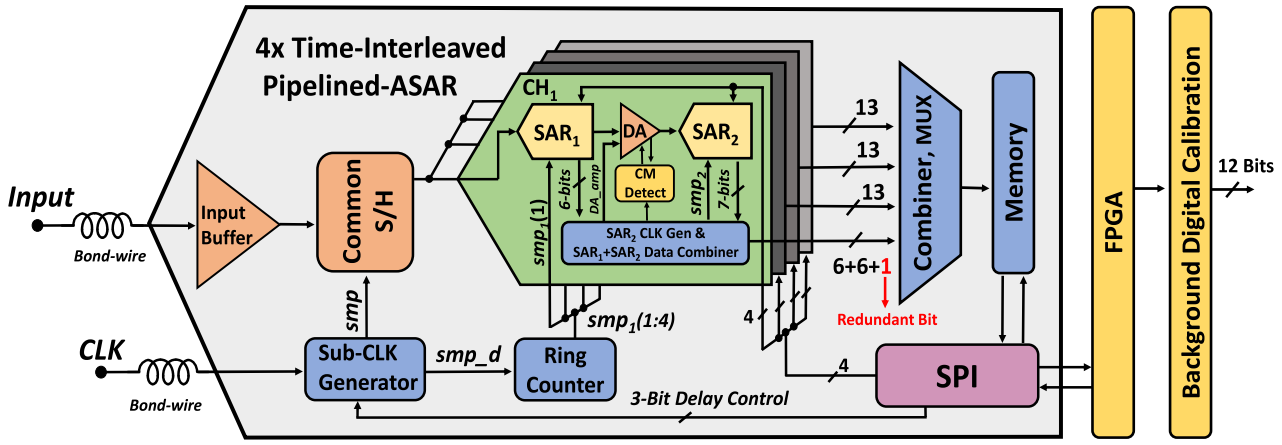

FIGURE 1. Simplified architecture of the designed ADC.

This paper builds upon the work disclosed in [19], elaborating on various design details, calibration methods, test setup, and measurement outcomes.

The remaining sections of this paper are structured as follows: section II introduces the proposed ADC and provides a comprehensive overview of its design specifics; section III deals with the test setup and showcases the measurement outcomes; finally, conclusions are drawn in section IV.

II. TI PIPELINED ASYNCHRONOUS SAR ADC

Fig. 1 shows the architecture of the designed ADC, where single-ended signals and blocks are depicted for simplicity, instead of the actual differential ones. The input signal enters the ADC through an on-chip input buffer, which plays a crucial role in isolating the sensitive ADC sampler from the large parasitic impedances introduced by bonding pads, bond wires, and the printed circuit board (PCB) housing the ADC die and all the components required for testing. The buffered signal is sampled by the common sample-and-hold circuit (S/H) and then distributed in sequence to each of the four channels. An external signal generator provides the clock signal *CLK* entering the *Sub-CLK Generator* and *Ring Counter* blocks, creating the sampling signals used in *Common S/H* and in the sub-ADCs. *Common S/H* is an NMOS switch bootstrapped as in [20], decreasing the switch on-resistance while keeping its value constant. This allows the S/H to handle a rail-to-rail input signal while maintaining high linearity.

As already mentioned, the ADC consists of four sub-ADCs operating concurrently in a TI fashion. Each sub-ADC features a two-stage (SAR_1 followed by SAR_2) pipelined ADC, where both SAR_1 and SAR_2 are asynchronous, with a resolution of six and seven bits, respectively. Additionally, each channel includes a *DA* to amplify the residue signal from SAR_1 and transfer it to SAR_2. Ancillary circuits are a common-mode detection circuit to control the on/off state of the *DA*, a digital block generating the sampling signal smp_2 for SAR_2, and digital circuitry to collect and combine the data from both SAR_1 and SAR_2. Subsequently, the data from all channels are collected, combined, and stored in an on-chip memory. The use of such a memory is crucial for testing the ADC, as it allows reading out the digital data off-line and at a suitably low rate, rather than run-time and at the full ADC rate. A serial peripheral interface (SPI) controls when the data is written to the memory and provides the control signals to the ADC for tuning the performance.

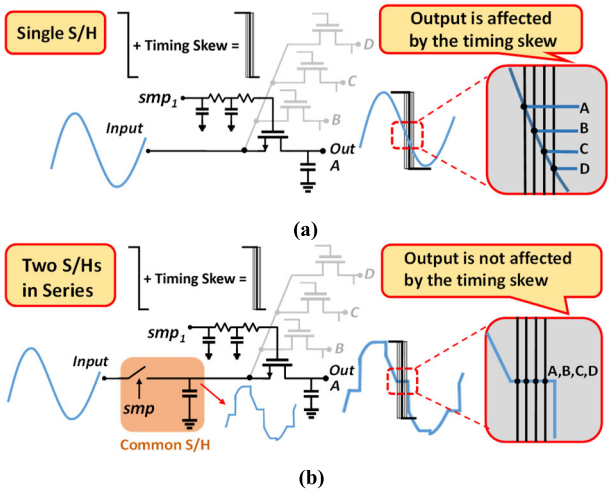

FIGURE 2. Distribution of smp_1 to the 4 channels without (a) and with (b) a *Common S/H*.

A. COMMON S/H AND SUB-S/H

The signal sampled by the common S/H is distributed to the individual channels via an additional S/H in front of each SAR_1 (shown later in Fig. 7). In the following, we will refer to this channel-specific sampler as the sub-S/H. The sub-S/H utilizes the same bootstrapping design as the common S/H, but with smaller device sizes due to its lower driving requirements.

The advantage of having common S/H and sub-S/H in series is shown in Fig. 2, where each S/H is modeled with a single NMOS switch and a hold capacitor for simplicity. Fig. 2 (a) shows the effect of clock skew on the sampled signal when the common S/H is removed: when the falling edges

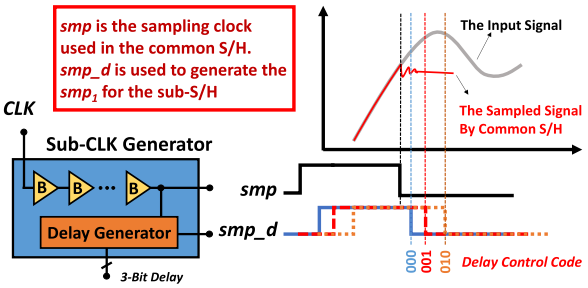

FIGURE 3. Tuning the sub-sampling instant over the *Common S/H*.

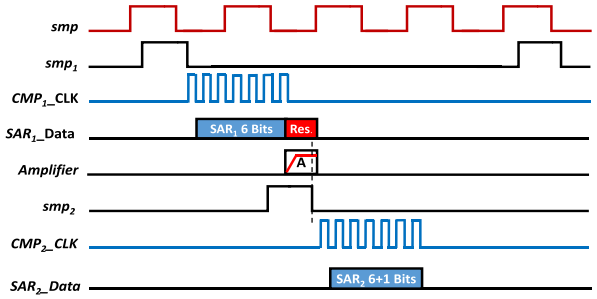

FIGURE 5. Timing diagram of the ADC.

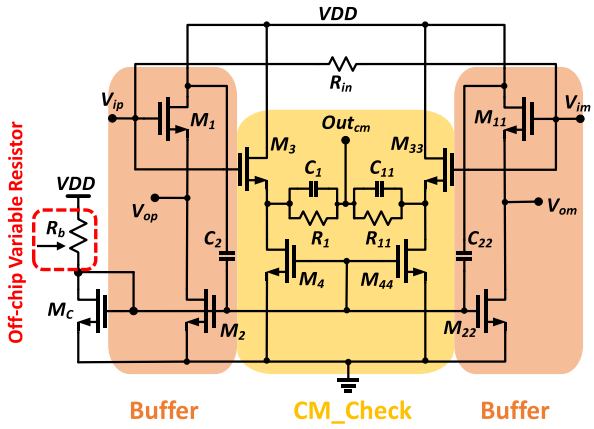

FIGURE 4. The input buffer.

of the clocks driving the sub-S/Hs are skewed, the sampled signals on the hold capacitors (*A, B, C, D* levels in Fig. 2(a)) are highly affected, especially for a high-frequency input. Although a good layout practice minimizes clock skew, it cannot be removed completely, because the different physical location of the four sub-ADCs, combined with unavoidable component mismatch, results in a different parasitic RC network from the clock source to each sub-ADC [21].

The use of common S/H greatly improves the clock skew issue, as shown in Figure 2 (b): the common S/H presents a stable DC level to the sub-S/Hs (at least, in a first-order approximation), with the consequence that the clock skew has a negligible impact on the samples delivered to the sub-ADCs: points *A, B, C*, and *D* consistently represent equal signal values. This highly facilitates the digital post-processing of the final data to eliminate the TI skew errors.

The generation of the sampling signals for the common S/H and the sub-S/Hs is shown in Fig. 3. The main clock *CLK*, which we assume is originally a sinusoidal signal, goes through a series of buffers inside the *Sub-CLK Generator* block, ultimately converting it into a square signal (*smp* in Fig. 1) to drive the common S/H. The *Sub-CLK Generator* block has a second purpose as well: it fine-tunes the timing relationship between *smp* and the delayed version *smp_d* of *smp*. Subsequently, *smp_d* is used in the *Ring Counter* block to produce the smp_1 clocks, which are driving the sub-S/Hs.

The possibility of adjusting the delay between *smp* and smp_1 is crucial for compensating any discrepancy between simulation models and fabricated chip, so that the transfer of the sampled data from the common S/H to the sub-S/Hs can be performed correctly. The *3-bit delay control* feature, which is accessible externally, allows for a fine tuning of the delay between *smp* and smp_1 in steps of 10 ps, from a minimum of 22 ps to a maximum of 95 ps. This is enough to counteract the impact of process-temperature-voltage (PVT) variations as well.

B. THE INPUT BUFFER

The input buffer, based on a pseudo-differential source follower (Fig. 4), ensures a signal-to-noise-and-distortion ratio (SNDR) of at least 65 dB according to post-layout simulations. The inner source-follower pair, whose transistors have smaller dimensions to consume less power, serves as a reference point for monitoring the common-mode voltage at the Out_{cm} node. This node is accessible off-chip, allowing measurement of the common-mode voltage in the buffer during testing. The current drawn by the buffer can be adjusted off-chip by varying resistor R_b to compensate for PVT variations and trading power with linearity. Decoupling capacitors C_2 and C_{22} are used to filter the noise on the gates of M_2 and M_{22}.

C. TIMING DIAGRAM

Fig. 5 illustrates the timing diagram of the ADC. As already mentioned, *smp_d* is generated from *smp*, then entering *Ring Counter* to generate the channel-specific smp_1 signals. Since there are 4 TI sub-ADCs, the rate of smp_1 is 1/4 that of *smp*.

When smp_1 goes low, the conversion process in SAR_1 begins. When all the bits in SAR_1 have been resolved, *DA* boosts the SAR_1 residue; once the *DA* amplification phase is over, smp_2 goes low, transferring the boosted residue to $CDAC_2$, at which the conversion in SAR_2 begins. At the same time, the bottom plates in the $CDAC_1$ capacitors are reset to a common voltage of 0.4V, to avoid a history-dependent charge-sharing between $CDAC_1$ and the common S/H when

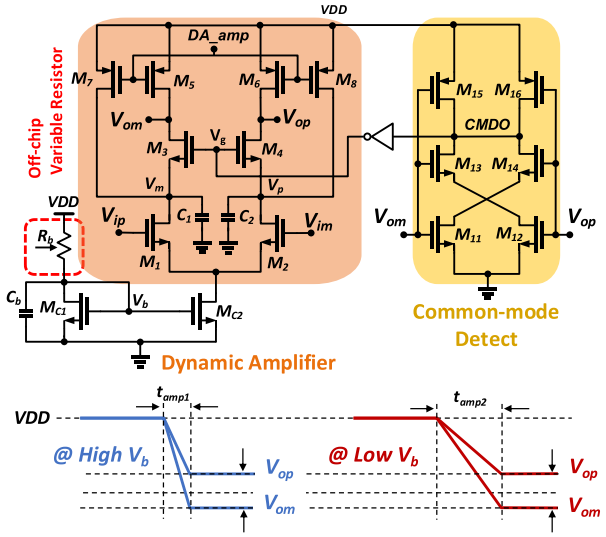

FIGURE 6. The dynamic amplifier and the common-mode detect.

the latter samples the next signal. The same operation is applied to $CDAC_2$ when SAR_2 has delivered its bits.

D. THE DYNAMIC AMPLIFIER

Fig. 6 displays the schematic of the *DA* and the common-mode detect (*CMD*) circuit. The cascode *DA* configuration is used to achieve higher gain. The gates of M_5 to M_8 are connected to an internally generated *DA_amp* control signal; when this goes low, M_5 to M_8 reset nodes V_{om}, V_{op}, V_m, and V_p to *VDD*, while M_3, M_4, M_{15}, and M_{16} are off. Consequently, *CMDO* is low, *Vg* is high, and the input transistors M_1 and M_2 are on, drawing current through M_7 and M_8. This helps increasing the speed and linearity of the *DA*, as changing the operating region of M_1 and M_2 from triode to saturation is time-consuming, affecting both the speed and linearity of the *DA*.

When *DA_amp* goes high, M_5 to M_8 turn off and M_1 and M_2 start discharging C_1 and C_2 to ground. M_3 and M_4 turn on when nodes V_m and V_p are discharged enough so the gate-source voltage of M_3 and M_4 exceeds that of their threshold. Nodes V_{om} and V_{op} start discharging from *VDD*, with a current limited by M_1 and M_2. When the common-mode level of V_{om} and V_{op} drops below a certain value, C*MDO* goes high, causing V_g to drop low. This turns off M_3 and M_4, and V_{om} and V_{op} will hold their value. By varying V_b, which controls the common-mode current through M_{C2}, speed can be traded with power consumption: the higher this current, the higher the discharging rate and the overall conversion speed with it ($t_{amp1} < t_{amp2}$).

E. THE SUB-ADC

Fig. 7 shows the simplified architecture of the asynchronous SAR-ADC for SAR_1 and SAR_2 where it can deliver a resolution of 6-bits and 7-bits (of which one bit is redundant), respectively. It is comprised of a differential *CDAC*,

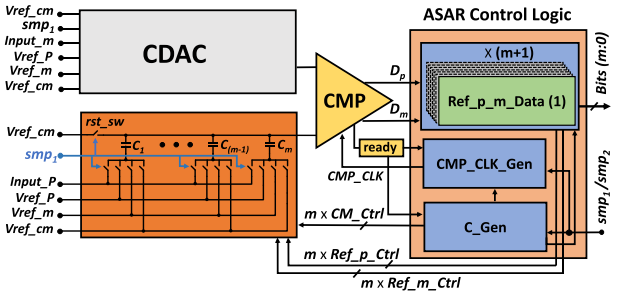

FIGURE 7. The sub-ADC.

a comparator, and a logic control unit. The *CDAC* uses the switching scheme introduced in [22], which guarantees a high energy efficiency.

Four switches connect the bottom plate of each capacitor in *CDAC* to one of the following four nodes: input signal, high reference voltage *Vref_p*, low reference voltage *Vref_m*, and common-reference voltage *Vref_cm*. The switches are sized in proportion to the capacitance they drive.

The *ASAR Control Logic* manages several crucial tasks: it stores the converted data, creates control signals for the *CDAC* switches, and generates the clock signal for the comparator. The corresponding blocks responsible for these actions are depicted in Fig. 7.

The conversion begins when the smp_1 goes low, disconnecting the top plates of the *CDAC* capacitors from *vref_cm* and sampling the *Input-m*(*Input_p*) onto the bottom plates of the *CDAC* capacitors through the sub-S/H switch. Subsequently, the bottom plate of all capacitors is connected to *Vref_cm*. The comparator clock *CMP_CLK* goes low, and the most significant bit (MSB) is converted. When the comparator has reached a decision, *ready* goes high and a new conversion cycle starts: the bottom plate of the (MSB-1) capacitance C_m is disconnected from *Vref_cm* and connected to either *Vref_m* or *Vref_p* according to whether MSB is high or low. Then a new *CMP_CLK* pulse is generated and the next bit is resolved; this process is repeated until the least significant bit (LSB) is resolved. It is critical to guarantee that the next *CMP_CLK* is generated after the bottom plate of the active capacitor has been connected to *Vref_m* or *Vref_p*; to enforce this, a feedback signal from *C_Gen* to *CMP_CLK_Gen* is employed. Moreover, the control signals to the *CDAC* switches should not overlap each other, in order to avoid a short circuit between the references. This is taken care of through an additional feedback from *C_Gen* to *Ref_p_m_Data*.

Finally, we remark that in SAR_1 the reset switch *rst_sw* is bootstrapped (as the sub-S/H switch), while the remaining switches are simple transmission gates. In SAR_2, on the contrary, all the switches are transmission gates, as the signal swing is lower there (additionally, the linearity requirement on SAR_2 is less stringent compared to SAR_1, due to the gain between the two stages [23]).

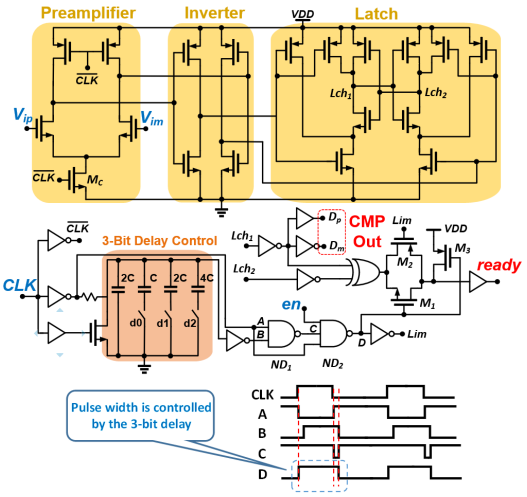

FIGURE 8. The comparator with the *ready* limiter.

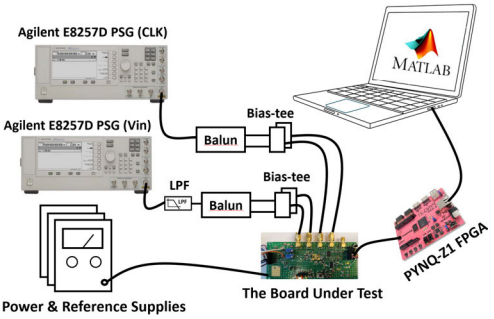

FIGURE 9. The measurement test bench of the prototype ADC.

F. THE COMPARATOR

Fig. 8 presents the schematic of the comparator, consisting of three stages: a preamplifier, an inverter, and a regenerative latch. A three-stage design offers advantages in terms of higher speed and reduced kickback noise when compared to single-stage and two-stage solutions [24], [25]. The preamplifier boosts the input voltage, lowering the decision time of the latch and reducing the input-referred offset; the inverter boosts the signal further, reducing the input-referred kickback noise of the latch; finally, the regenerative latch generates the digital decision levels. The latch output is buffered to increase its driving power before connecting it to the logic control.

The *ready* signal in Fig. 8 indicates the state of the comparison: when a decision has been taken, *ready* goes high and the next cycle can start. This works as follows: assuming the control signal *en* (which is set through the SPI) is low, the output of the 3-input NAND gate is high regardless of the voltages on A and C. Hence, the pass gate M_1-M_2 is on and M_3 is off, and *ready* is created by the XOR gate, which goes high when one latch output has reached digital high and the other digital low.

We can override this mechanism of *ready* generation by setting *en* high, which forces *ready* to go high when its generation takes too long; this is beneficial in case the comparator

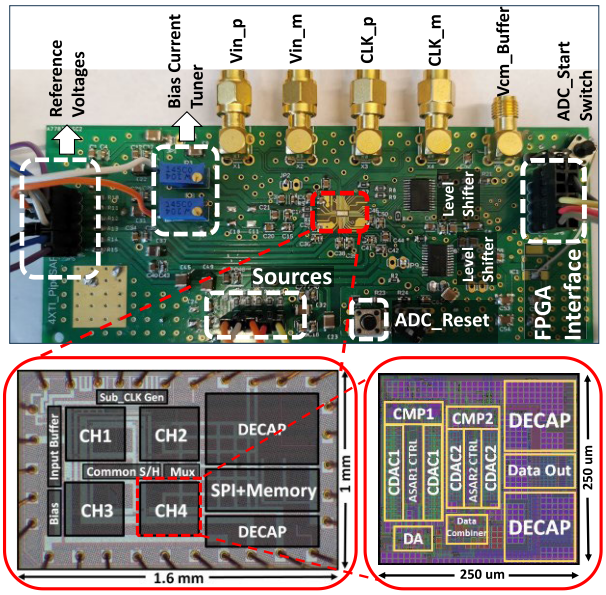

FIGURE 10. The PCB together with the bonded chip and the pipelined-SAR channel layout.

finds itself in a metastable state, as a consequence of a very small signal at its (differential) input. Specifically, when *en* is high, the output of ND_2 is determined by its two other inputs, A and C. With reference to the timing diagram in Fig. 8, when *CLK* goes high, A goes low and B goes high, where the delay between A and B can be tuned by turning on/off the *d0*-*d2* switches. This delay determines the overall pulse width at D. When *CLK* goes low, the comparator becomes active, working toward a decision while D is still high. When D finally goes low, M_1 and M_2 turn off and M_3 pulls *ready* high, irrespective of the XOR output (i.e., of whether the comparator has taken a decision or not). The maximum wait for *ready* is determined by the time C is low; approximately 90ps.

III. MEASUREMENT

A. THE TESTBENCH

Fig. 9 illustrates the test setup utilized for evaluating the designed chip. Two Agilent E8257D signal generators are employed to supply a single-ended input and a single-ended clock. The input signal is low-pass filtered to eliminate harmonic distortion components (several passive low-pass filters with different cut-off frequencies are used to take measurements across the ADC band). Both clock and input signals are subsequently transformed into differential signals using wideband baluns. External voltage supplies are also used to provide reference voltages, analog *VDD*, digital *VDD*, and dedicated supply for the input buffer. The data stored in the memory is accessed by a PYNQ-Z1 FPGA board, which is connected via an Ethernet cable to a PC where MATLAB is available. Communication with SPI is performed through the FPGA board, whereby all control signals for the fine-tuning of the ADC can be set. The collected data are post-processed

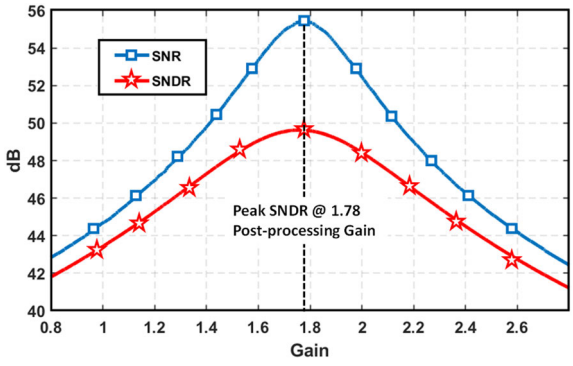

FIGURE 11. Measured SNR and SNDR with post-processing calibration of *DA* gain *DA_gain*.

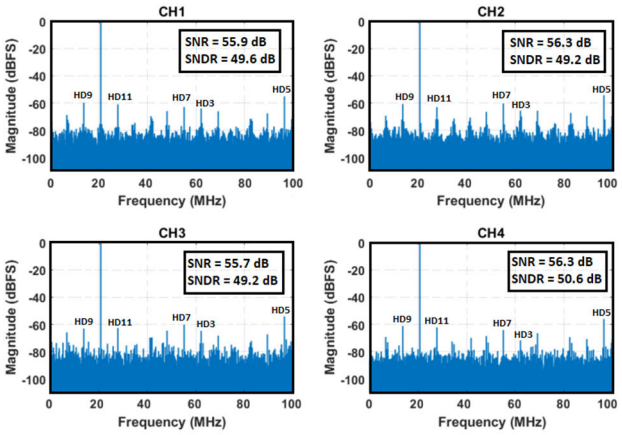

FIGURE 12. Measured spectrum of the four channels with post-processing gain of 1.78.

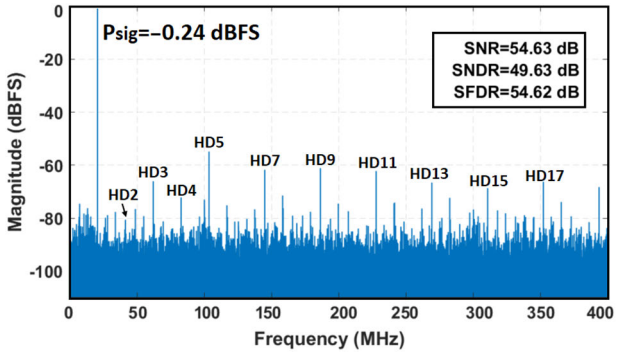

FIGURE 13. Measured spectrum of the prototype ADC with only gain calibration.

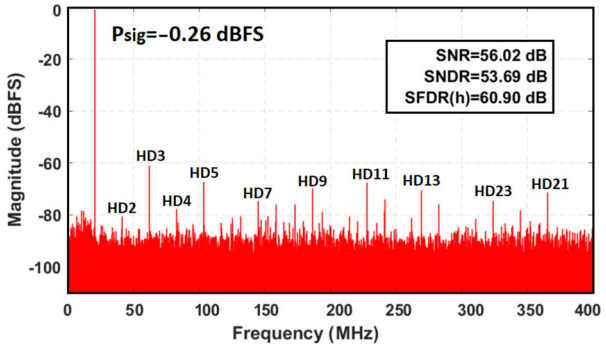

FIGURE 14. Measured spectrum of the ADC with bit-weights and gain calibration.

in MATLAB to calibrate the weight of all bits and to find the *DA* gain ensuring an optimal ADC performance. All MATLAB functions are amenable to on-chip implementation (albeit not without effort), which is of course vital for the relevance of the design.

B. THE PCB

Fig. 10 shows the PCB on which the chip was bonded, the bonded chip, and the layout of the channels. On the PCB, power source housings for analog and digital *VDD*, the input buffer *VDD*, and the SPI *VDD* are positioned at the bottom of the PCB while the references are located on the left side. The PCB also features the integration of zero-ohm resistors on the path of power sources, voltage references, and current references, enhancing the diagnostic capabilities during testing. Two level-shifters from Texas Instrument are also soldered on the PCB to level-shift the voltages from the FPGA board to those used by the ADC. Two variable resistors tune the current in the current mirrors biasing input buffer and *DA*. The common-mode voltage at the output of the input buffer is accessible via the *Vcm_Buffer* port, which allows monitoring the DC level of the input signal. Finally, large decoupling capacitors are used to clean all power supplies and voltage references.

C. THE CHIP

The ADC was implemented in a 22-nm FDSOI CMOS process. The total area occupied by the chip, including the pads, is 1.6 mm^2, of which 0.43 mm^2 is occupied by the ADC core. Each of the four sub-ADCs occupies 0.0625 mm^2, of which 40% is taken by routing and decoupling capacitors (DECAPs in Fig. 10). The location of the channels is chosen to ensure a balanced routing to the common S/H. Input buffer, analog blocks, and digital blocks use three dedicated voltage sources to avoid supply noise on sensitive (analog) nodes. Analog and digital sections are isolated from each other by deep-Nwell trenches underneath the digital cells and surrounding them with a guard ring. Multiple ground and supply pads are used to keep the resistance on the power distribution low. To prevent contamination of the input signal by the clock via magnetic coupling on the bond wires, a ground pad is placed between the signal pads and clock pads.

D. MEASUREMENT RESULTS

Analog and digital *VDD* pads are connected to voltage supplies of 0.8V; the supply of the input buffer is 1.2V. Initially, SAR_1 is configured with reference voltages of 0.6V, 0.4V, and 0.2V for $Vref_1\_p$, $Vref_1\_cm$, and $Vref_1\_m$, respectively. In contrast, SAR_2 has 0.43V, 0.4V, and 0.37V for $Vref_2\_p$,

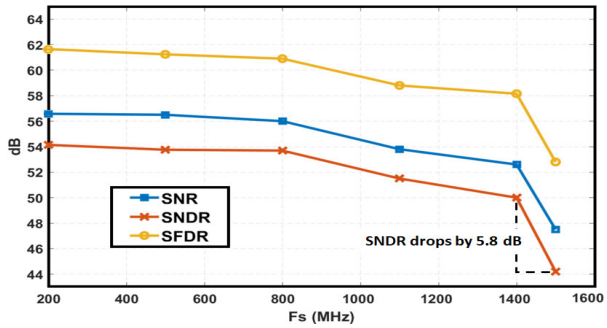

FIGURE 15. Measured performance of the ADC versus the sampling frequency, with low f_{in}.

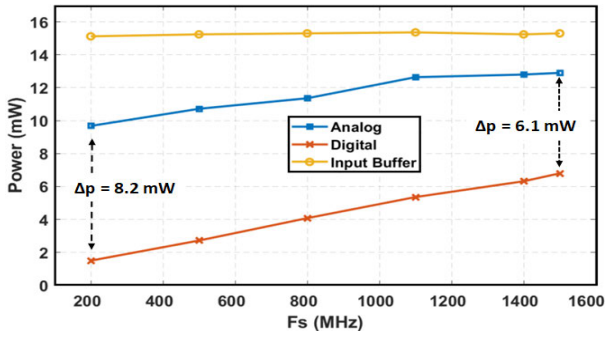

FIGURE 16. Measured power consumption vs f_s while f_{in} =20 MHz.

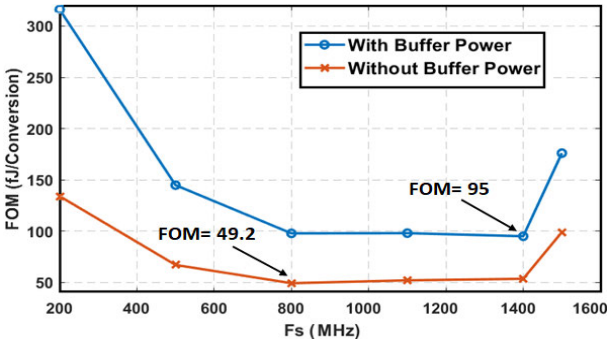

FIGURE 17. Measured Walden's FOM while f_{in} is 20 MHz.

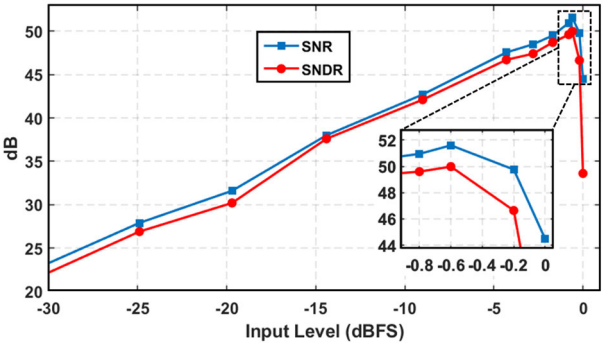

FIGURE 18. Measured dynamic range of the ADC.

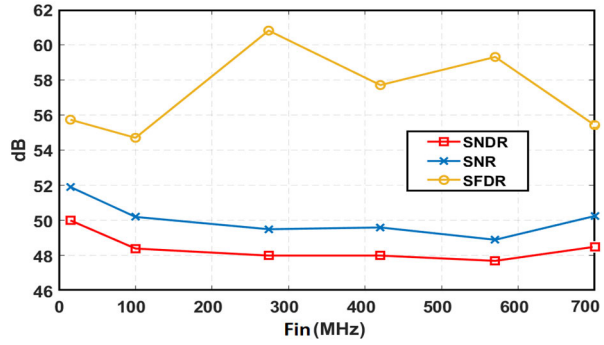

FIGURE 19. Measured performance of the ADC while f_s is fixed at 1.4GS/s.

$Vref_2\_cm$, and $Vref_2\_m$, respectively. During measurements, these voltage values are actively tuned and adjusted to achieve the best performance. The measured data is enhanced by two types of post-processing: interstage-gain tuning and bit-weight calibration.

Fig. 11 shows the measured SNDR and SNR of the ADC versus the inter-stage gain for a sampling frequency f_s of 800 MHz and an input frequency f_{in} of 20 MHz. To achieve a monotonous bit-weight distribution from SAR_1 to SAR_2, it is necessary that the DA gain DA_gain be such that the amplified SAR_1 residue SAR_1_Res fully covers the dynamic range of SAR_2 without exceeding it. Thus, the optimal condition linking the two quantities is

$$SAR_1\_Res \times DA\_gain = Vref2\_p - Vref2\_m \quad (1)$$

Due to parasitics and deviations from the simulated value of DA_gain, however, the above equation is not met in the measurements, even when DA_gain, is the highest possible. The difference between $Vref2\_p$ and $Vref2\_m$, is lowered until the best performance is achieved and SNDR is limited by thermal noise rather than the quantization noise. The rest of the required gain to satisfy (1) is provided by applying post-processing to the weight of the SAR_2 bits to recover a much higher linearity.

The output of each of the 4 sub-ADC channels is accessible and can be measured individually, as in Fig. 12, where four spectra are shown for the same values of f_s and f_{in} as before, where each channel operates at $f_s/4 = 200$ MHz. SNR and SNDR are reported for the optimal value of DA_gain (which, however, cannot be tuned individually in the four channels). In this example, channel 4 achieves the highest SNDR.

The second type of post-processing is tuning the bit-weights of the ADC relative to each other to reach the highest SNDR. Due to PVT variation and various parasitic capacitances, the actual capacitances in the CDAC deviate from their ideal binary-weighted values. To compensate for this, the calibration algorithm searches for a correcting gain to apply for each bit weight, resulting in an improved linearity and a lower noise floor. Figs. 13 and 14 show the ADC spectrum without and with bit-weight calibration, again with the same values of f_s and f_{in} as before. With bit-weight calibration, SNDR improves from 49.6 dB to 53.7 dB, while

TABLE 1. Performance summary and comparison.

	This Work	ESSCIRC 2017[10]	JSSCC 2019[11]	JSSCC 2017[12]	TCASI 2022[13]	TCASII 2022[14]
Architecture	TI-Pipe-SAR	TI-Pipe-SAR	TI-Pipe-SAR	TI-SAR	TI-Pipe-SAR	Pipelined-SAR
Technology	22 nm	28 nm	65 nm	40 nm	28 nm	40 nm
Interleaved channels	4	9	4	16	8	1
Resolution (bits)	12	12	12	8	13	10
Sampling Rate (GS/s)	1.4	1	1	2	2	1
Supply Voltage (V)	0.8/1.2	1.15/1.5	1.2/1.4/2.5	1.1	0.9/1.2//1.7/-0.8	1.2
SNDR @ Low f_{in} (dB)	50	56.1[1]	65.3	45[1]	64.86	46.8
SNDR @ Nyq. (dB)	48.5	56.1	56.2	39.4	60.36	41.37
Area (mm^2)	0.43	0.66	0.27	0.540	1.062[2]	0.06
Power (mW)	34.5[3]	89	31.5	54.2	252.6[2]	9.4
Walden FoM @ Nyq. (fJ/conv)	114	170	59.7	355	148.3	98.2

[1] Read from the plot.
[2] With estimated power and area of the digital calibration.
[3] Total power consumption excluding SPI and memory.

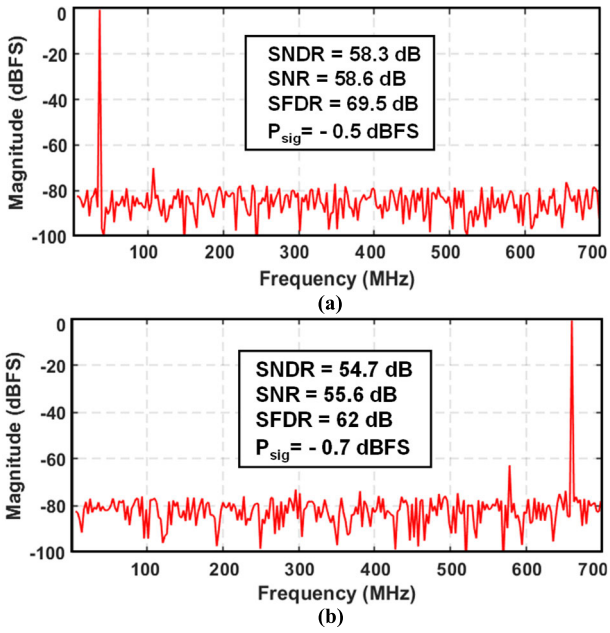

FIGURE 20. Post-layout simulation spectrum of the ADC with thermal noise and f_s of 1.4GS/s with f_{in} at (a) low frequency (b) Nyquist.

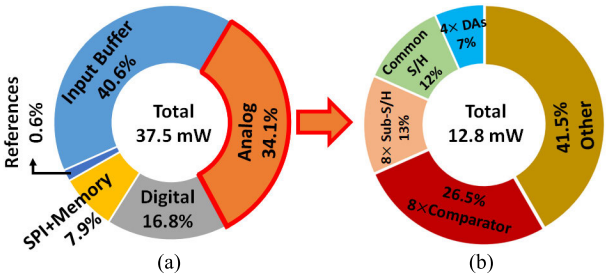

FIGURE 21. The power pie for (a) the whole ADC (measured) (b) the analog part (simulated).

the spurious-free dynamic range (SFDR) goes from 54.6 dB to 60.1 dB. In particular, we notice that the 5th distortion harmonic has been considerably reduced. We also remark that the calibration algorithm cannot address sources of distortion outside the ADC itself; thus, any distortion introduced by e.g. the input buffer is not affected.

To assess the bandwidth of the ADC, f_s is swept from 200 MHz up to 1.5 GHz, after which the SNDR quickly drops to below 20 dB. Fig. 15 shows SNR, SNDR, and SFDR when data is post-processed for the best *DA_gain* and bit-weights, with f_{in} = 20 MHz. The SNDR exhibits a gradual reduction as f_s increases to 1.4 GS/s, followed by an additional 5.8 dB drop with f_s = 1.5 GS/s.

The power consumption of the ADC is also measured vs f_s. Fig. 16 shows the power consumption of the input buffer, analog blocks, and digital blocks. Analog and digital blocks consume a higher amount of power when f_s increases. While this is expected for digital blocks, it is less so for analog ones. Nevertheless, this becomes clear when we consider that dynamic circuits such as bootstrapped switches and *DAs*, are powered by the analog supply. The power consumption of the input buffer, on the other hand, remains approximately constant, which is no surprise.

To further assess the ADC performance, the Walden figure of merit (FOM_W) [26] is calculated vs f_s with f_{in} kept at 20 MHz. FOM_W is shown in Fig. 17 with and without the power consumption of the input buffer; FOM_W decreases (i.e., improves) as the sampling rate increases. The FOM_W is at its best at 1.4 GS/s if the power consumption of the input buffer is considered. If it is excluded, the optimum FOM_W is instead achieved at 800 MS/s.

Fig. 18 shows the dynamic range (DR) of the ADC with f_s = 1.4 GS/s and f_{in} = 20 MHz, with the input amplitude swept from -30 dBFS to 0 dBFS. SNR and SNDR increase until the input level is -0.6 dBFS. Beyond this point, the ADC starts showing signs of clipping distortion, leading to a dramatic drop in SNDR.

Fig. 19 shows SNR, SNDR, and SFDR when f_{in} is swept from low frequencies up to the Nyquist limit, with f_s fixed at 1.4 GS/s. As already mentioned, different low-pass filters are used to clean input signals at different frequencies, and

adjustments are made to signal levels and reference voltages to optimize the SNDR; with $f_{in} = 20$ MHz, the ADC achieves an SNDR of 50.0 dB, which becomes of 48.5 dB at Nyquist.

To compare measurements with simulations, the post-layout simulated spectra for both low-frequency and Nyquist signals, with $f_s = 1.4$ GS/s and in the presence of thermal noise (which makes for very lengthy simulations) are shown in Fig. 20(a)-(b). It is clear that the deterioration from simulations to measurement is significant; on the other hand, several implementation non-idealities, such as the many wire bonds, may be suspected with reason to cause at least some of the performance drops.

The measured ADC power breakdown at $f_s = 1.4$ Gs/s is shown in Fig. 21(a), while Fig. 21(b) reports the simulated power consumption for the analog functions. From Fig. 21(a), it is clear that the input buffer consumes the highest amount of power, whereas the voltage references consume the lowest. Fig. 21(b), on the other hand, shows that the comparators are the most power-hungry analog blocks, the *DAs* lying on the opposite side of the scale. The common S/H is also rather power-hungry, as it drives a large capacitive load.

A comprehensive summary and performance comparison with state-of-the-art high-speed TI-SAR ADCs is presented in Table 1. Even with a high SNDR drop from simulation to measurement, the ADC shows a decent performance compared to the recently published works.

IV. CONCLUSION

A TI pipelined asynchronous SAR ADC has been designed and fabricated in a 22-nm FDSOI CMOS process. The main design choices have been discussed, together with details about the test bench and the calibration algorithms employed. With a sampling rate of 1.4 GS/s, the ADC achieves an SNDR (SNR) of 48.5 dB (50.0 dB) at Nyquist.

The ADC performance is in line with the state of the art for high-speed TI SAR ADCs.

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