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APPLIED RESEARCH

A New Method for Surprise Box Quantity Determination Based on Comparer

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ABSTRACT To address the limitation of traditional surprise boxes that only support single or fixed quantity customization, this paper proposed a new method: utilizing comparators to detect cascaded quantities for specific customization. This innovative approach aims to simplify the customization process of surprise boxes while avoiding the complexity of using micro-controllers for quantity determination. A dual comparator is employed to compare the results that are greater or smaller than the set quantity. Then the output of the dual comparator is connected to an AND gate circuit, triggering the hidden function of the central surprise box when the AND gate generates high levels. The system design involves setting the number of surprise boxes and connecting upper and lower limit comparators to the current surprise box connection signal. By selecting the size of the cascade resistor, the number of surprise boxes can be determined. This paper provides step-by-step instructions for calculating the cascade resistor. Furthermore, the proposed method's reliability in determining the number of surprise boxes is demonstrated by setting the number of secondary surprise boxes to seven and four, with the allowed resistance error 6.4% and 11%, respectively. The results indicate that a higher number of connected surprise boxes leads to a smaller range of cascaded resistors and higher accuracy requirements. Through these case studies, it has been verified that the design using dual comparators can achieve the desired quantity detection, and the detection circuit exhibits a high degree of redundancy in resistance value error, resulting in increased reliability of the detection results.

INDEX TERMS Comparer, quantity judgment, voltage comparison, series connection.

I. INTRODUCTION

Surprise box is a cultural product that only knows what is inside when opened, and its attraction lies in the uncertainty and randomness of its design. Traditional surprise boxes often focus on their appearance design, and there is no correlation between each surprise box. Each surprise box is collected separately, and a complete set of works can only be judged based on its appearance [1], [2].

With the continuous improvement of technology, higher requirements for the commemorative significance of traditional surprise boxes are required [3], [4]. The application of high-tech technology to surprise box will determine the new trend and prospects of surprise box development. The cultural demand for surprise boxes is no longer limited to the viewing of individual boxes. Due to the lack of electronic circuits, traditional surprise boxes cannot adapt to personal demand. The design of modular electronic surprise boxes can make up for the lack of personalized customization of surprise boxes, meet the personal and personalized needs of the public, and achieve the dual requirements of functionality and commemorative significance [5], [6].

Customized gifts for small or folk groups must have ornamental and commemorated significance [7]. Based on the principle of small and exquisite customized gifts, when designing surprise boxes, it is necessary to consider the different number of surprise box combinations and production cost requirements [8].

At present, determining the quantity of surprise box connections is usually done by hanging the device on the data bus or directly reading the high and low levels of whether the external device is online using a microcontroller [9]. The

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data bus makes the system complex and has manufacturing costs, while employing micro-controllers does not have personalized customization requirements. Therefore, the circuit design of the attached device is intricate [10], [11].

The simplified comparison circuit is designed to address the issue of quantity measurement [12]. The comparison counting method naturally has encryption properties, enhancing its security [13], [14]. A comparator is a circuit used to compare voltages and provide comparison results [15], [16]. Combining multiple comparators can be schemed for quantity determination and integrated to reduce power consumption [17], [18]. The idea of making judgments through comparison is also applied in image-based item recognition [19]. The quantity of items can be determined by connecting items in series and further designing a comparator circuit [20]. At the same time, there are other similar algorithms that utilize iterative optimization or fuzzy matching through controllers, which can provide inspiration [21], [22].

The existing methods for determining the quantity of surprise box connections involve either hanging the device on the data bus or using micro-controllers to read the high and low levels of the external device. However, these approaches have drawbacks such as complexity, high manufacturing costs, and lack of personalized customization. On the other hand, the simplified comparison circuit provides a solution to the quantity measurement issue. This method not only simplifies the circuit design but also enhances security through its inherent encryption properties. By combining multiple comparators, the power consumption can be reduced, making it a more efficient approach for quantity determination. The concept of comparison-based judgments is also applicable in other domains, such as image-based item recognition. By connecting items in series and designing a comparator circuit, the quantity of items can be accurately determined. These findings highlight the need for a novel approach that effectively addresses the gaps in the existing literature and provides a more efficient and secure solution for quantity determination in surprise box connections.

This article provides a method and structure based on operational amplifier design, which can reduce the overall complexity. The paper proposes a cascading method for the number of surprise boxes with personalized customization, which can reduce overall complexity and have a simple structure. It provides a cascading design method and supporting structural design based on two comparators.

II. QUANTITY DETERMINATION SYSTEM

A. MECHANICAL STRUCTURE DESIGN

The entire system is equipped with one center surprise box, and several sub-surprise boxes can be designed according to customized needs, with a quantity of N. Resistors of the same resistance are employed in the system, which brings two benefits. Firstly, different batches of surprise boxes are combined to support customization. Under the matched resistance, the internal circuit operates. Conversely, the internal circuit does not work with the mismatched resistance values. Secondly, it can reduce the complexity of production and assembly.

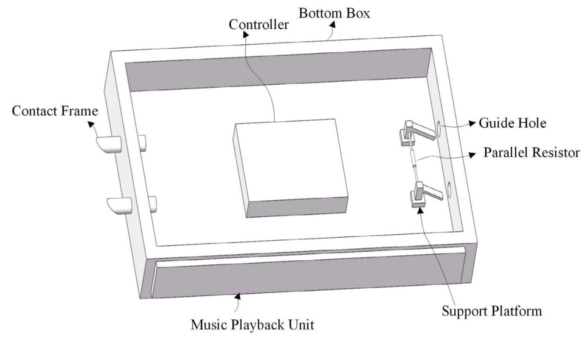

FIGURE 1. Mechanical structure diagram of surprise box.

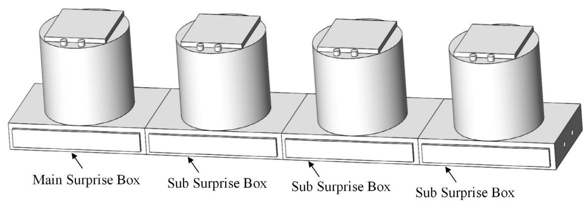

FIGURE 2. Surprise box cascading.

The center surprise box and the sub-surprise box are connected in a cascade manner, and the structural design jointly includes the bottom box, contact frame, support platform, guide hole, parallel resistor, and sub-components, as Figure 1 shows. The center surprise box is designed with a central controller, and the sub-surprise box is designed with a sub-controller. The running program of the two can be the same or different. However, the hidden function program of the sub-controller does not have triggering conditions. Therefore, its hidden function will not trigger. The sub-surprise box also has contact plates for cascading. There are two contact pieces and support platforms, both of which are symmetrically designed and fixed at the bottom of the bottom box. The two ends of the parallel resistor are fixedly connected to the symmetrically designed contact frame. The distance between the centers of the two contact pieces is equal to the distance between the centers of the two guide holes. The support platform material is non-conductive to avoid introducing additional resistance. At the same time, the outer side of the contact piece can be designed as an inclined plane, the prone mouth as an inverted trapezoid, the contact frame as a willing long strip, the shackle as a regular trapezoid, and the materials are all metal. Therefore, the contact piece can centertain good contact with the contact frame.

To distinguish the center surprise box from the sub-surprise box in appearance, the center surprise box removes the contact film, while only the sub-surprise box has the contact film. The effect of cascading four surprise boxes is shown in Figure 2.

The center and sub-controllers contain a power supply unit, buttons, a music playback unit, and an LED. The above modules are connected to the controller through wires. In addition, the center controller also includes a voltage comparison unit.

The voltage comparison unit detects the number of connected sub-surprise boxes. If the number of sub-surprise boxes exceeds the setting number, the hidden functions in the center surprise box will not be turned on. The method used is a lower limit comparator and an upper limit comparator to detect whether the number of connected sub-surprise boxes is greater than or less than the setting number N. The comparison results are sent to the AND gate circuit. Only the two comparators generate high levels. Then, the AND gate generates high levels, the hidden function of the center surprise box is triggered, such as lighting up the LED of the center surprise box.

After the sub-surprise box is connected, it causes a change in the judgment resistance inside the center surprise box, and the judgment resistance value varies depending on the number of connections. Different batches of resistors with significant differences in resistance values can be selected during manufacturing to determine whether they are the same group of surprise boxes based on internal resistance values. As the resistance is the primary factor in determining the number of surprise boxes and the key to distinguishing different groups of surprise boxes, the resistance value has become the focus in the surprise box design.

B. COMPARISON CIRCUIT DESIGN FOR QUANTITY JUDGMENT

The basic idea of using operational amplifiers to form a circuit for quantity judgment is to compare the input voltage with the reference voltage. The greater the number of surprise box changes, the stronger the system's anti-interference ability and the more stable its operation.

The voltage comparison unit detects the number of sub-surprise boxes connected, and its circuit design is shown in Figure 3. The voltage comparison unit includes a lower limit comparator, an upper limit comparator, an AND gate circuit, and resistors R1, R2, R3, R4, R5, R11, R15, R16, R17, and R18. The resistance value of resistor R11 is the same as that of a parallel resistor. Resistor R1 is connected to the power source and the parallel resistor R11. Resistor R2 is connected to the power source and the series resistor R3 before grounding. The other side of resistor R3 is connected to the positive end of the lower limit comparator, and the negative end of the lower limit comparator is simultaneously connected to the point where resistor R1 and resistor R11 are connected in series with the positive end of the upper limit comparator. Resistor R16 is connected to the power supply, and the negative connection of the upper limit comparator is grounded through resistor R17. The lower limit comparator and upper limit comparator are connected to the power supply through resistor R4 and resistor R18. Connect the resistors R5 and R15 in series to the two input terminals of the AND gate. The output terminal of the AND gate is connected to the center controller through a circuit, and the AND gate

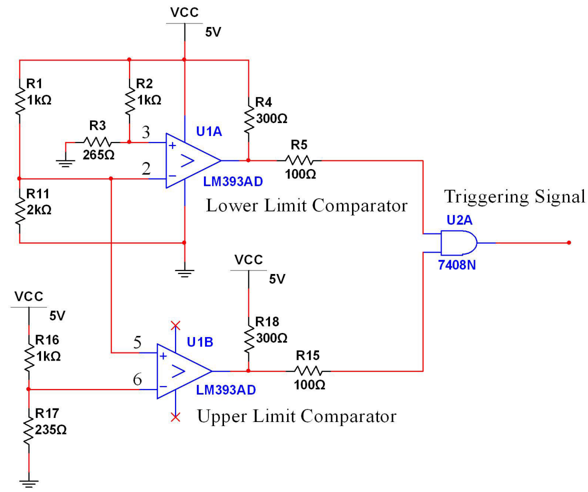

FIGURE 3. Circuit diagram of voltage comparison unit.

outputs a high-level signal to trigger the surprise box to enter the combined working mode. Turn on the color LED lighting mode, and the AND gate output is low. The surprise box operates independently, and the color LED recenters off. Adjust the resistance values of resistors R3 and R17 to ensure that the number of connected sub-surprise boxes equals the set value and that the gate generates a high level.

The customization function of surprise boxes is centered and achieved through the design of R3. Calculate the resistance range of R3 based on the preset number N of the sub-surprise boxes. Since N is an integer and the power supply voltage is set to VCC, the calculation steps for the resistance value of resistor R3 are as follows:

Step 1: Calculate the negative terminal voltage of the lower limit comparator when parallel N sub surprise boxes are connected

$$V_{2,N} = V_{CC}\frac{R_{11}/\,(N+1)}{R_{11}/\,(N+1)+R_1} \tag{1}$$

Step 2: Calculate the negative terminal voltage of the lower limit comparator when parallel N-1 sub surprise boxes are connected

$$V_{2,N-1} = V_{CC}\frac{R_{11}/N)}{R_{11}/N+R_1} \tag{2}$$

Step 3: According to the lower limit comparator, the positive terminal voltage meets the conditions

$$\begin{cases} V_3 & > V_{21} \\ V_3 & < V_{22} \\ V_3 & = V_{CC}\dfrac{R_3}{R_3+R_2} \end{cases} \tag{3}$$

Further calculations have shown that

$$\begin{cases} R_3 & > \dfrac{R_2 * R_{11}}{R_1(N+1)} \\ R_3 & < \dfrac{R_2 * R_{11}}{R_1 N} \end{cases} \tag{4}$$

Step 4: Calculate the value range of R3 and take R3 as the middle value of the range.

Step 5: Calculate the upper limit comparator positive terminal voltage when one center surprise box is connected in parallel with N sub surprise boxes

$$V_{5,N} = V_{CC}\frac{R_{11}/(N+1)}{R_{11}/(N+1)+R_1} \tag{5}$$

Step 6: Calculate the upper limit comparator positive terminal voltage when one center surprise box is connected in parallel with N+1 sub surprise boxes

$$V_{5,N+1} = V_{CC}\frac{R_{11}/(N+2)}{R_{11}/(N+2)+R_1} \tag{6}$$

Step 7: According to the upper limit, the negative terminal voltage of the comparator meets the conditions

$$\begin{cases} V_6 > V_{52} \\ V_6 < V_{51} \\ V_6 = V_{CC}\dfrac{R_{17}}{R_{17}+R_{16}} \end{cases} \tag{7}$$

Therefore, we have

$$\begin{cases} R_{17} > \dfrac{R_{16} * R_{11}}{R_1(N+2)} \\ R_{17} < \dfrac{R_{16} * R_{11}}{R_1(N+1)} \end{cases} \tag{8}$$

Step 8, calculate the value range of R17 and take R17 as the middle value of the range.

When cascading surprise boxes, the contact piece of the sub-surprise box is connected to the contact frame of the center surprise box, and the parallel resistor is connected to the center surprise box. The contact piece of the sub-surprise box is attached to the contact frame of the primary sub-surprise box. When the center surprise box is connected in parallel with N sub-surprise boxes, the lower limit comparator generates a high level. While the number of parallel connections is less than N, the lower limit comparator generates a low level. At the same time, when the center surprise box is connected in parallel with N sub-surprise boxes, the upper limit comparator generates a high level. When the number of parallel connections exceeds N, the upper limit comparator generates a low level. Only when the generates of the lower limit comparator and the upper limit comparator are both high levels can the outcome of the AND gate be high. Therefore, by outputting the high and low levels of the AND gate, the center surprise box can determine whether the number of connected sub-surprise boxes is exactly N; when the number of corresponding sub-surprise boxes is precisely equal to the set value N, the center surprise box enables the LED flashing function. Otherwise, the LED flashing function is turned off, and the center surprise box cannot trigger the hidden process.

The combination surprise box customization method formed is simple, and it only needs to adjust the resistance to achieve the function of triggering LED flashing by connecting different numbers of sub-surprise boxes, which

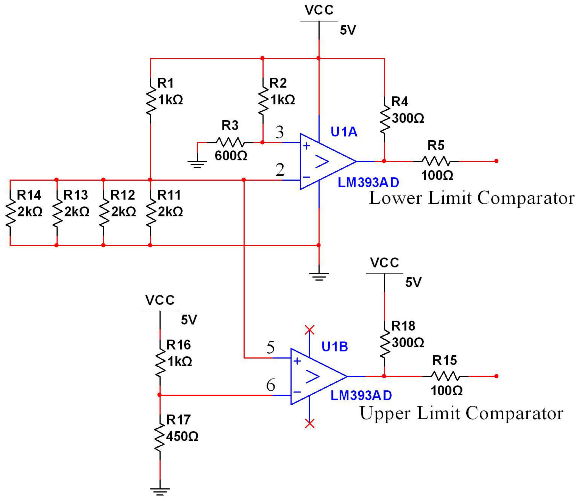

FIGURE 4. Four sub surprise boxes.

is of commemorative significance. Users can customize one center surprise box and one to N sub surprise box. Based on the number of customized sub-surprise boxes, resistor R3, and resistor R17 resistance values can be calculated and adjusted. Each surprise box can independently play music, achieving the function of a standard surprise box. However, when the set number of surprise boxes are connected, the unique process of lighting LED can be activated, which further increases the significance of the commemoration and the exceptional value as a gift.

III. PRACTICAL DESIGN CASES

The feasibility of the proposed method is demonstrated by designing different numbers of sub-surprise boxes and providing specific calculation processes.

Scenarios for customizing surprise boxes include university students customizing graduation souvenirs for dormitory mates, small teams of individuals with shared interests for anniversary gifts, and family mementos. It is preferable to have a customization quantity ranging from 2 to 9. Therefore, our examples choose the midpoint of these quantities, and the analysis and calculation methods remain the same for other values.

A. THE NUMBER OF SUB SURPRISE BOXES IS FOUR

When customizing four sub-surprise boxes for detachable surprise boxes, the key point is to calculate and adjust the certified resistance resistance R3 and R17. The number of connected sub-surprise boxes equals four, and the gate outputs a high level. The steps are as follows: The first step is selecting the commonly used comparator, such as LM393. As R3 and R17 are the focus of the design, and their calculation basis is provided in the following steps, the other resistance values are as follows: $R_1 = R_2 = R_{16} = 1000\Omega, R_4 = R_{18} = 300\Omega, R_5 = R_{15} = 100\Omega, R_{11} = R_{12} = R_{13} = R_{14} = 2000\Omega$, The power supply is $V_{CC} = 5V$.

In the case of connecting four sub-surprise boxes in series, the negative terminal of the lower limit comparator, i.e., the second pin voltage of the U1A chip, is

$$V_{2,N} = \frac{R_{11}/4}{R_{11}/4 + R_1} * V_{CC} = \frac{500}{500 + 1000} * 5(V) = 1.67(V) \tag{9}$$

The second step is to calculate the voltage of the negative terminal of the lower limit comparator, i.e., the second pin of the U1A chip, when two sub-surprise boxes are connected in series.

$$V_{2,N-1} = \frac{R_{11}/3}{R_{11}/3 + R_1} * V_{CC} = \frac{666.7}{666.7 + 1000} * 5(V) = 2(V) \tag{10}$$

The third step is to satisfy the following conditions for the value of R_3:

$$\begin{cases} V_3 & > 1.67(V) \\ V_3 & < 2(V) \\ R_2 & = 1000\Omega \end{cases} \tag{11}$$

Further calculations have shown that

$$\begin{cases} R_3 & > 501\Omega \\ R_3 & < 667\Omega \end{cases} \tag{12}$$

Step 4, take the middle value of the range, with R3 as 600Ω. In the case where the resistance value is set to the intermediate value, the permissible resistance error can be allowed to be about 11%. Therefore, the lower limit comparator only outputs a high level when 3 or more sub surprise boxes are connected in parallel;

Step 5, calculate the positive terminal voltage of the upper limit comparator U1B when four sub surprise boxes are connected in series, $V_{5,N} = 1.67(V)$.

Step 6, calculate the positive terminal voltage of the upper limit comparator U1B when four sub surprise boxes are connected in series, $V_{5,N+1} = 1.428(V)$.

Step 7, calculate the resistance value of R17. The value of R17 needs to meet the voltage of the sixth pin of the upper limit comparator

$$\begin{cases} V_6 & > 1.428(V) \\ V_6 & < 1.67(V) \\ R_{16} & = 1000\Omega \end{cases} \tag{13}$$

Further calculations have shown that

$$\begin{cases} R_{17} & > 399.8\Omega \\ R_{17} & < 501\Omega \end{cases} \tag{14}$$

Step 8, take the middle value of this range, with R17 as 450Ω, so the upper limit comparator can only output high levels when 3 or less sub surprise boxes are connected in parallel. In the case where the resistance value is set to the intermediate value, the permissible resistance error can be allowed to be about 11%.

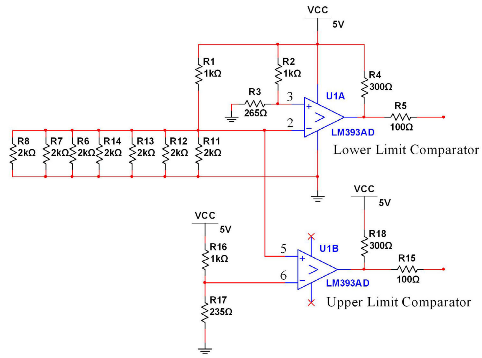

FIGURE 5. **Seven sub surprise boxes.**

The specific method for connecting surprise boxes is to align the contact pieces of any sub-surprise box with the guide hole of the center surprise box and insert them into contact with the contact frame of the center surprise box. According to this method, align the recentering sub-surprise box contact pieces with the guide hole of the previous sub-surprise box, insert them into contact with the contact frame of the sub-surprise box, and complete the connection of four sub-surprise boxes in sequence. Write a program for the center controller to detect the output level status of the AND gate in real-time. When a high-level signal is detected, it enters the combined working mode, a hidden function, and illuminates the color LED lighting. Otherwise, when the AND gate outputs a low level, the surprise box will be in independent working mode, and the color LED will recenter off.

B. THE NUMBER OF SUB SURPRISE BOXES IS SEVEN

Customize the detachable surprise box as one center and seven sub-surprise boxes. Similarly, it is necessary to calculate and adjust the resistance values of the certified resistors R3 and R17. Therefore, the gate outputs a high level when the number of connected sub-surprise boxes equals seven, as figure 5 shows. The specific steps are:

Step 1, select LM393 as the comparator model. Except for R3 and R17, the other resistance values are: $R_1 = R_2 = R_{16} = 1000\Omega, R_4 = R_{18} = 300\Omega, R_5 = R_{15} = 100\Omega, R_{11} = R_{12} = R_{13} = R_{14} = R_6 = R_7 = R_8 = R_9 = 2000\Omega,$

In the case of connecting seven sub surprise boxes in series, the voltage at the negative end of the lower limit comparator, the second pin of the U1A chip, is

$$V_{2,N} = \frac{R_{11}/8}{R_{11}/8 + R_1} * V_{CC} = \frac{250}{250 + 1000} * 5(V) = 1(V) \tag{15}$$

Step 2: In the case where one center surprise box is connected in parallel with seven sub surprise boxes, the voltage at the negative end of the lower limit comparator, the second pin of the U1A chip, is

$$V_{2,N-1} = \frac{R_{11}/7}{R_{11}/7 + R_1} * V_{CC} = \frac{285.7}{285.7 + 1000} * 5(V) = 1.11(V) \quad (16)$$

Step 3: The conditions that need to be met based on the value of R3 are

$$\begin{cases} V_3 & > 1(V) \\ V_3 & < 1.11(V) \\ R_2 & = 1000\Omega \end{cases} \quad (17)$$

Further calculations have shown that

$$\begin{cases} R_3 & > 250\Omega \\ R_3 & < 285\Omega \end{cases} \quad (18)$$

Step 4, taking the middle value of the range and selecting R3 as 265Ω, then the lower limit comparator only outputs a high level when seven or more sub surprise boxes are connected in parallel. In the case where the resistance value is set to the intermediate value, the permissible resistance error can be allowed to be about 6.7%. When the number of parallel sub surprise boxes is six or less, the lower limit comparator outputs a low level;

Step 5: When one center surprise box is connected in parallel with seven sub surprise boxes, the upper limit comparator U1B's positive terminal voltage, $V_{5,N} = 1(V)$.

Step 6: When one center surprise box is connected in parallel with seven sub surprise boxes, the upper limit comparator U1B's positive terminal voltage, $V_{5,N+1} = 0.909(V)$.

Step 7, therefore, the value of R17 needs to be such that the negative terminal of the upper limit comparator U1B, the voltage of the sixth pin in upper limit comparator, meets

$$\begin{cases} V_6 & > 0.909(V) \\ V_6 & < 1(V) \\ R_{16} & = 1000\Omega \end{cases} \quad (19)$$

Further calculations have shown that

$$\begin{cases} R_{17} & > 222\Omega \\ R_{17} & < 250\Omega \end{cases} \quad (20)$$

Step 8, take the middle value of the range, with R17 as 235Ω. In the case where the resistance value is set to the intermediate value, the permissible resistance error can be allowed to be about 6.4%. Therefore, the lower limit comparator only outputs a high level when seven or less sub surprise boxes are connected in parallel. When the number of parallel surprise boxes is 8 or more, the upper limit comparator outputs a low level.

Similarly, the lighting function designed to turn on colored LED is a hidden function, which can only be turned on when the center surprise box and seven sub-surprise boxes are all assembled. The serial connection method for surprise boxes is to first align the contact piece of any sub-surprise box with the guide hole of the center surprise box and insert it to make contact with the contact frame of the center surprise box, and then follow this method, Align the contact plates of the recentering sub surprise boxes with the guide holes of the previous sub surprise box and insert them into the contact frame of the sub surprise box, completing the connection of seven sub surprise boxes in sequence. The center controller will detect the output level status of the AND gate connected to them in real time. When a high-level signal is detected, it will enter the combined working mode and turn on the color LED lighting mode. Otherwise, if the output level of the AND gate is low, the surprise box will be in independent working mode, and the colored LED recenters off.

C. DESIGN EXAMPLE SUMMARY

By comparing the above two design examples, it is found that in theory, the number of sub-surprise boxes can be expanded to an infinite number. However, the more sub-surprise boxes there are, the smaller the allowable range of resistance fluctuations for feature resistors, necessitating the selection of high-precision resistors, which will increase manufacturing costs. Additionally, constrained by the limitations of available high-precision resistors in reality, there is a maximum accuracy limit. Therefore, in practical design, it is not feasible to have an infinite number of sub-surprise boxes.

The official documentation states that the LM393 has a typical processing speed of 1.3μs, including the processing time of the comparator itself, which is approximately 0.05μs. This means that the LM393 can provide a comparison result within 1.4μs from a change in quantity. In comparison, a typical interrupt handling time for a single-core 51 micro-controller ranges from tens to hundreds of microseconds, and this is under light load conditions. It's worth noting that the LM393's speed is equivalent to a data bus with a response speed of around 10M, but implementing such a high-speed bus would significantly increase the system cost.

IV. CONCLUSION

This article proposes a combined surprise box quantity determination circuit and structural design based on a comparator, instead of micro-controllers. The main contributions of this study can be summarized as follows:

(1) Design of a customizable surprise box structure: We introduce a surprise box structure that allows for a customizable number of surprise boxes, which can be cascaded without limitations. This design is simple, reliable, and offers a straightforward connection method.

(2) Calculation steps for resistance value determination: We provide specific calculation steps for determining the resistance value of surprise boxes when the number of surprise boxes is being determined. These steps ensure accurate and precise resistance value selection.

(3) Feasibility verification and implementation cases: We present specific implementation cases to validate the feasibility of the proposed method. Through these cases,

we demonstrate the practicality and effectiveness of our approach.

In conclusion, this study offers a novel approach to address the limitations of traditional surprise boxes. The proposed combined circuit and structural design provide customization options, accurate resistance value determination, and reliable performance. These findings pave the way for future research and advancements in surprise box technology.

REFERENCES

[1] M. Yu, J. Zhuge, M. Cao, Z. Shi, and L. Jiang, "A survey of security vulnerability analysis, discovery, detection, and mitigation on IoT devices," *Future Internet*, vol. 12, no. 2, p. 27, Feb. 2020.

[2] Y. Wei, X. Tong, and X. Xin, "A fixed-window level-crossing ADC with a single comparator," *J. Phys., Conf.*, vol. 2301, no. 1, 2022, Art. no. 012026. [Online]. Available: https://api.semanticscholar.org/CorpusID:250672462

[3] A. Sarker, M. Shamiul Amin, A. Bose, and N. Islam, "An optimized design of binary comparator circuit in quantum computing," in *Proc. Int. Conf. Informat., Electron. Vis. (ICIEV)*, May 2014, pp. 1–5.

[4] M. P. C. Varma and M. G. Venkateswarlu. (2019). *SCADA Based Automated Bottle Quality and Quantity Detection and Filling System By Using PLC*. [Online]. Available: https://api.semanticscholar.org/CorpusID

[5] J. Liu, "Investigation and research on consumer psychology of surprise box consumers," *Frontiers Bus., Econ. Manag.*, vol. 6, no. 1, pp. 1–4, 2022. [Online]. Available: https://api.semanticscholar.org/CorpusID:253427424

[6] R. Zhao and J. Xu. (2022). *New Marketing Inspired by surprise Box*. Advances in Social Science, Education and Humanities Research. [Online]. Available: https://api.semanticscholar.org/CorpusID:247215495

[7] Y. Zhang, H. Zhou, and J. Qin, "Research on the effect of uncertain rewards on impulsive purchase intention of surprise box products," *Frontiers Behav. Neurosci.*, vol. 16, pp. 1–14, 2022. [Online]. Available: https://api.semanticscholar.org/CorpusID:251571339

[8] Z. Wang and S. Ulukus, "Digital blind box: Random symmetric private information retrieval," in *Proc. IEEE Inf. Theory Workshop (ITW)*, Nov. 2022, pp. 95–100.

[9] G. Wang, X. Li, and L. Yang, "Dynamic coal quantity detection and classification of permanent magnet direct drive belt conveyor based on machine vision and deep learning," *Int. J. Pattern Recognit. Artif. Intell.*, vol. 35, no. 11, Sep. 2021, Art. no. 2152017.

[10] J. Sui, R. Dong, S. Liao, Z. Zhao, Y. Wang, and H. Zhang, "Janus metastructure based on magnetized plasma material with and logic gate and multiple physical quantity detection," *Ann. Phys.*, vol. 535, 2023, Art. no. 2200509. [Online]. Available: https://api.semanticscholar.org/CorpusID:256489916

[11] H. Yang and C. Fu. (2019). *Quantity Detection of Steel Bars Based on Deep Learning*. [Online]. Available: https://api.semanticscholar.org/CorpusID:208120482

[12] G. M. Abo-Hamad, D. K. Ibrahim, E. Aboul Zahab, and A. F. Zobaa, "Adaptive mho distance protection for interconnected transmission lines compensated with thyristor controlled series capacitor," *Energies*, vol. 14, no. 9, p. 2477, Apr. 2021.

[13] S. Munratiwar, Y. Saikrishna, and V. Jyothi, "Design of high speed 8-bit magnitude comparator for security application," in *Proc. IEEE Int. Conf. Distrib. Comput. Electr. Circuits Electron. (ICDCECE)*, Apr. 2022, pp. 1–6.

[14] T. Chouta, T. Graba, J.-L. Danger, J. Bringer, M. Berthier, Y. Bocktaels, M. Favre, and H. Chabanne, "Side channel analysis on an embedded hardware fingerprint biometric comparator & low cost countermeasures," in *Proc. 3rd Workshop Hardw. Architectural Support Secur. Privacy*, Jun. 2014, pp. 1–6. [Online]. Available: https://api.semanticscholar.org/CorpusID:18827417

[15] S. Sunkireddy, S. Thallapally, G. Avula, and B. S. G. Devi, "Design of high speed and area efficient N-bit digital comparator," *Int. J. Res. Appl. Sci. Eng. Technol.*, vol. 10, pp. 1522–1527, Nov. 2022. [Online]. Available: https://api.semanticscholar.org/CorpusID:253989086

[16] K. Anjalideep, H. Kumar, S. Srivastava, and V. K. Sharma, "QCA-based single-bit comparator circuit," in *Proc. 3rd Int. Conf. Smart Electron. Commun. (ICOSEC)*, Oct. 2022, pp. 328–332.

[17] (2020). *Design of Low Power Dynamic Comparator Using Reversible Logic*. [Online]. Available: https://api.semanticscholar.org/CorpusID:252067463

[18] S. Lee and Y. Kim, "High-speed comparator in 65-nm CMOS with rail-to-rail detection," in *Proc. IEEE Int. Conf. Consum. Electronics-Asia (ICCE-Asia)*, Oct. 2022, pp. 1–3.

[19] A. Berenguel Centeno, O. Ramos Terrades, J. Lladós Canet, and C. Cañero Morales, "Recurrent comparator with attention models to detect counterfeit documents," in *Proc. Int. Conf. Document Anal. Recognit. (ICDAR)*, Sep. 2019, pp. 1332–1337. [Online]. Available: https://api.semanticscholar.org/CorpusID:211026726

[20] Z. Guan, Y. Zhang, and Y. Lü, "Reversible logic gate cascade network based on series connection," in *Proc. Int. Conf. Comput. Intell. Secur.*, vol. 1, Dec. 2009, pp. 468–472.

[21] E. Akbari, M. Mollajafari, H. M. R. Al-Khafaji, H. Alkattan, M. Abotaleb, M. Eslami, and S. Palani, "Improved salp swarm optimization algorithm for damping controller design for multimachine power system," *IEEE Access*, vol. 10, pp. 82910–82922, 2022.

[22] M. Negahban, M. V. Ardalani, M. Mollajafari, E. Akbari, M. Talebi, and E. Pouresmaeil, "A novel control strategy based on an adaptive fuzzy model predictive control for frequency regulation of a microgrid with uncertain and time-varying parameters," *IEEE Access*, vol. 10, pp. 57514–57524, 2022.

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