IEEE Access
Multidisciplinary | Rapid Review | Open Access Journal

Received 22 February 2024, accepted 10 March 2024, date of publication 19 March 2024, date of current version 30 July 2024.

Digital Object Identifier 10.1109/ACCESS.2024.3378128

RESEARCH ARTICLE

A UHF Passive RFID Tag Front-End Design With a Novel True Random Number Generator

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ABSTRACT Among various wireless communication methods, the ultra-high frequency (UHF) passive Radio Frequency Identification (RFID) electronic tags are widely used due to their ability to transfer information without internal power supply. In this study, a low-power UHF passive RFID tag front-end with a novel structure including a true random number generator is designed and fabricated in standard 180nm CMOS technology. The proposed front-end circuit includes an analog front-end, an RF front-end, and an impedance matching network. The received RF energy is impedance-matched to the analog front-end, generating a power supply voltage for the RF front-end. The RF front-end performs signal demodulation and generates a reference clock. A novel true random number generator (TRNG) is designed in the proposed RF front-end to achieve signal anti-collision functionality. The experimental results indicate that the total power consumption of the RFID tag front-end is 8.67μW, and the TRNG circuit can produce a series of random number with 85.5% of credibility, which effectively improves the randomness of the communication keys.

INDEX TERMS Ultra-high frequency, RFID electronic tags, front end circuit, true random number generator.

I. INTRODUCTION

Radio Frequency Identification (RFID), as a non-contact data communication method, is widely used in access control and production management [1]. Ultra-high frequency passive RFID (UHFP-RFID) has become the main research direction due to its advantages such as long-distance transmission and high-speed communication [2]. A UHFP-RFID system mainly consists of an electronic tag, a reader, a middleware, and a host computer. The reader emits electromagnetic signals (energy) to drive the electronic tag and receives its internal data which are then decoded by the host computer through the middleware [3], [4]. An electronic tag usually comprises a front-end circuit, a digital baseband, and a non-volatile memory (NVM). The functions of the front-end circuit include converting radio frequency signals into energy to supply the front-end, powering the modulation/demodulation circuit, providing a clock for the digital baseband and NVM, and transmitting internal data back to the reader. Therefore, maximizing the efficiency of radio frequency energy conversion, improving the accuracy of signal modulation/ demodulation and clock precision, and enhancing the communication security are crucial in the front-end circuit design [5], [6].

Two approaches are typically used to optimize the utilization of received energy in the front-end circuit. A high-efficiency voltage multiplier can be employed to convert the high-frequency signal into the internal DC supply. Besides, low-power technologies, such as the current-starved structure, can be utilized to design modules of the front-end. In 2011, Chung et al. proposed a fully integrated ultra-low power UHFP-RFID tag consuming only 2.64μW [7]. The tag employs the low-threshold voltage Schottky diode to implement the voltage multiplier circuit. To reduce the dynamic power consumption, it uses a current-starved structure in the design of its oscillator. Most of its analog blocks are biased in the subthreshold region to reduce the static power consumption. In this research, some components like Schottky diodes are incompatible with certain processes, posing challenges in achieving seamless integration. Then in 2020, Li et al. added an automatic impedance matching circuit to a UHFP-RFID tag to ensure maximum power receiving and

The associate editor coordinating the review of this manuscript and approving it for publication was Harikrishnan Ramiah.

reduce the back-scattering loss obviously [8]. The circuit uses gate-cross structure in the voltage multiplier design to improve the energy efficiency. The tag totally consumes 4.8μW. The proposed automatic matching circuit improves circuit efficiency but increases system complexity. Additionally, the leak current of the gate-cross structure cannot be ignored.

To enhance the accuracy of signal processing and clock precision, calibration technologies can be employed to generate stable and accurate timing signals for the system. In 2019, Din et al. improved the accuracy of the clock generator in the tag by calibrating its frequency continuously [9]. This self-calibrating clock uses the downlink pulse-interval encoding symbols from the reader to make its error within $\pm$4%. The current mode demodulator inside can provide a larger dynamic range than the voltage mode demodulator. In 2022, Wang et al. applied a novel structure made up of a current mirror array and a counter to the calibration circuit of the on-chip clock [10]. The counter firstly calculates the number of clock cycles and compares it to the standard value. Then, the circuit changes oscillation frequency according to the results. The design consumes 7.65μW due to the dynamic power consumption and its on-chip clock error is within $\pm$2.5%. Although the accuracy of information has been improved, the designs above introduce additional modules to the circuit to calibrate the clock errors, increasing the complexity of the circuit and the dynamic power consumption of the entire front-end.

To improve the communication security, a true random number generator (TRNG) is necessary in the front-end circuit. Using the algorithm embedded in the digital baseband, the true random number generator can produce a jumbled set of signals to ensure the correctness and security of the communication. To generate the true random number, the noise of resistors can be simply amplified by an amplifier. But this method has a high-power consumption. In 2019, Wang et al. proposed a TRNG based on differential current starved ring oscillator [11]. The circuit utilizes the jitter noise of the oscillator and improves its thermal stability by using the tail current source. Then, in 2022, Mehra et al. designed a TRNG based on hexagonal ring oscillator [12]. The design takes advantages of the jitter and random phase noise provided by two hexagonal oscillators to produce highly random sequence. Nevertheless, the circuit itself consumes 1.27mW. These circuits both have a high-power consumption. In RFID systems, it is crucial to effectively manage power consumption at the μA level.

To solve the above-mentioned problems, this study presents a front-end circuit for the UHF passive RFID tag fabricated in the standard 0.18μm CMOS process. The circuit consists of a voltage multiplier, a voltage limiter, a demodulator, a low dropout regulator, a clock generator and a true random number generator. Some essential circuits such as power-on-reset module are also integrated in the design to control the digital baseband and minimize power consumption. The low-threshold voltage transistors are used to enhance the efficiency of voltage multiplier circuit. Furthermore, the current-starved structure is also utilized to reduce the dynamic power consumption of the ring oscillator. Then, a novel structure of the low-power true random number generator is designed.

TABLE 1. Key indexes for signal transmitted from reader to tag.

communication rate	modulation method	encoding method	operating frequency	modulation depth
40~160Kb/s	ASK	PIE/ Manchester	860~960MHz	80%~100%

TABLE 2. Key indexes for signal transmitted from tag to reader.

communication rate	modulation method	encoding method	anti collision
40~640Kb/s	ASK/PSK	Miller/FM0	slot-ALOHA

In this paper, we work on a UHFP-RFID tag front-end circuit design. In particular:

1) We design the low-power modules of the RFID tag front-end, including power-on-reset circuit, current-starved structure oscillator, to utilize the received power efficiently.

2) We design a novel true random number generator circuit where the high-speed clock is sampled by the low-speed clock to ensure the correctness and security of the communication.

The paper is organized as follows: section II describes the overall UHF passive RFID tag front-end structure and the signal path inside the tag. Section III shows the detailed structure of each module and analysis of the key modules. A brief introduction to impedance matching is in this part. Section IV shows the simulation results of the circuit. Section V presents the layout of the circuit and test results of the chip. Section VI and VII discuss and conclude this passage shortly.

II. RFID TAG FRONT END ARCHITECTURE

In the study, the ISO/IEC 18000 protocol is applied to design the system. ISO/IEC 18000 protocol is a communication protocol developed by a global non-profit industry standards organization. The protocol has made detailed provisions for the communication in 13.56MHz, 960MHz, 2.45GHz and other commonly used bands. Due to its wide application, we decide to adopt the UHF part of this protocol for the circuit design. Some important indexes of ISO/IEC 18000-6C protocol are shown in the tables below [13], [14], [15].

The overall architecture of the UHFP-RFID tag front-end is shown in Figure 1. The system is composed of a matching network, an RF front-end circuit and an analog front-end circuit. The RF front-end is used in signal processing and the analog front-end generates the supply voltage for the whole tag. Three parts of the front-end circuit work together to make the process of signal transmission efficient.

A. ANALOG FRONT END CIRCUIT

The UHFP-RFID tag analog front-end module converts the signal power to the DC voltage supply of the whole tag.

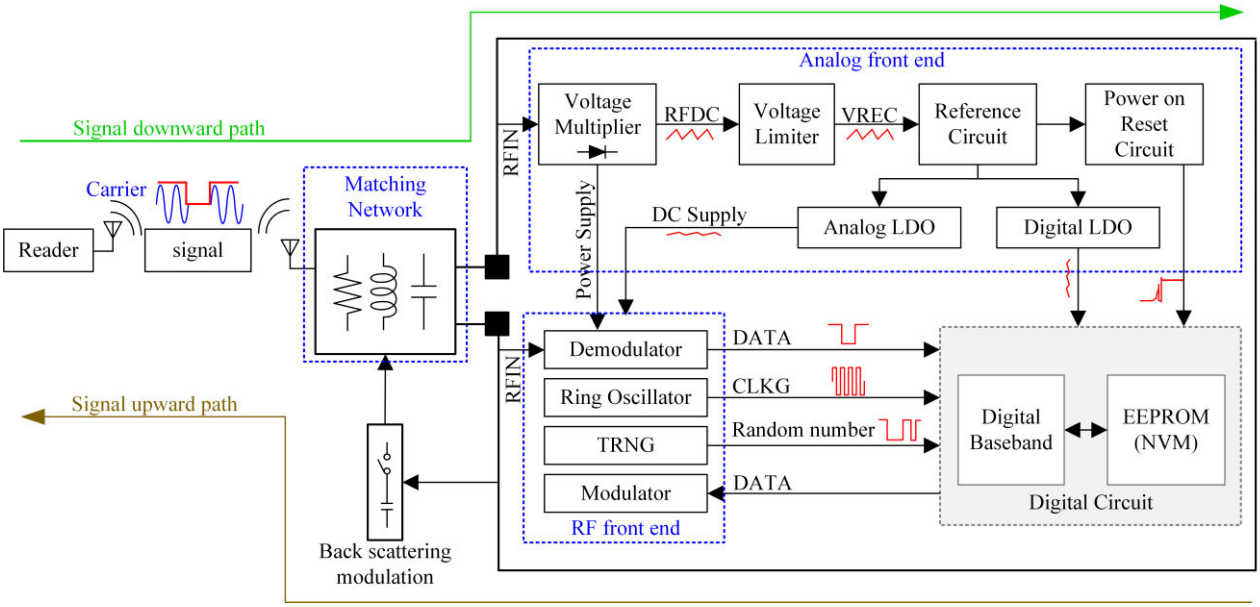

FIGURE 1. The architecture of the UHFP-RFID tag front end.

The circuit consists of a voltage multiplier, a voltage limiter, a reference circuit, two low dropout regulators for analog circuit and digital circuit respectively and a power-on-reset circuit. During the process of signal transmission, firstly, the voltage multiplier and the voltage limiter are used to convert the UHF signal received by the on-chip antenna into a voltage with ripples. Then, the reference circuit reduces the ripples of the voltage and turns it into an almost DC voltage due to its high common mode rejection ratio. After that, the low dropout regulator takes a further step to reduce the ripples and generates a steady DC voltage as the power supply of the tag. To avoid the interference between the analog signal chain and digital chain, two LDOs are designed to supply the analog circuit and digital circuit respectively.

B. RF FRONT END CIRCUIT

The UHFP-RFID tag RF front-end module is used to remove the high frequency carrier of the received signal and generate the necessary signals for the digital baseband. In the RFID systems, the signal path from the reader to the tag is called ''the downward path,'' and the signal path from the tag to the reader is called ''the upward path.'' In the downward path, firstly, the demodulator restores the signal to the low frequency and sends it to the digital baseband. Meanwhile, the ring oscillator begins to generate an inside clock for the digital baseband. Also, the TRNG circuit begins to work to ensure the correctness and security of the communication. By using these signals, the digital baseband reads the information stored in NVM and sends it to the reader through the upward path.

C. MATCHING NETWORK

During the process of ultra-high frequency signal transmission, it is necessary to consider the loss of signal energy. Considering the UHFP-RFID tag front-end as a two-port system, if the input impedance of the system cannot match the impedance of the antenna, the signal energy will be mostly reflected back to the reader. This cannot be acceptable because the tag itself is battery-less and the signal is the power source of the circuit. To keep the front-end receiving the maximum power, the conjugate resonance should be used as the matching network on the chip.

III. CIRCUIT IMPLEMENTATION

A. VOLTAGE MULTIPLIER AND VOLTAGE LIMITER

The voltage multiplier converts the ultra-high frequency signal to a relatively stable supply voltage. When the RFID tag is close to the reader, the tag will receive a huge amount of energy, thus generating a high voltage in the voltage multiplier circuit. To protect the device from the high voltage, a voltage limiter is used to limit the voltage to a relatively low level [16], [17]. Figure 2 shows the structure of a single-stage voltage multiplier and gives the key node voltage waveform. This structure can boost the input AC signal to a DC voltage, and the amplitude of the DC voltage is nearly twice as the peak-to-peak voltage of the input signal. For an N-stage voltage multiplier, the amplitude of output voltage can be described as follows:

$$V_{OUT} = 2N(V_{PP} - V_{TH}) \tag{1}$$

where N is the number of the stage of voltage multiplier, V_{PP} is the peak-to-peak voltage of the input signal, and V_{TH} is the threshold voltage of the diode.

Commonly, we tend to use the Schottky diode to implement this circuit, due to its ultra-low threshold voltage. However, many processes do not support integrating Schottky diode on the chip [8]. To solve this problem, we use the

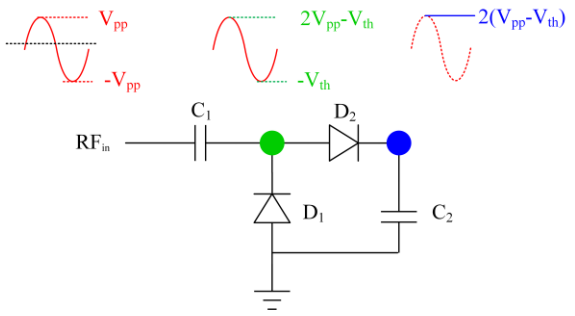

FIGURE 2. The single stage of voltage multiplier.

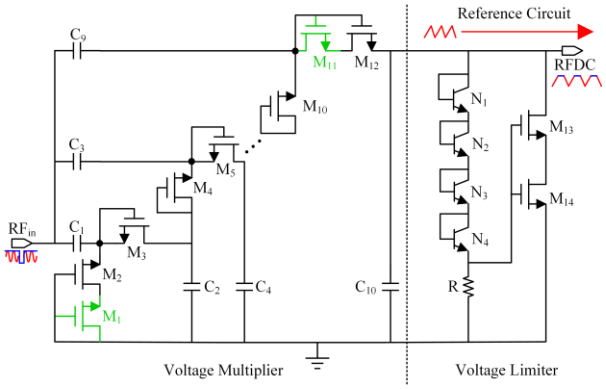

FIGURE 3. The structure of voltage multiplier and voltage limiter.

low-threshold voltage NMOS to complete the circuit. Its threshold voltage can be as low as 116mV.

Figure 3 shows the whole structure of the voltage multiplier and voltage limiter. The circuit is made up of 5-stage voltage multiplier and a clamp voltage limiter. Transistor M_1 and M_{11} are used to protect the circuit from the interference of the ground and insulate the high voltage in the circuit. If the peak voltage of the input signal is 700mV, then the module can boost it up to 5.5V without any load. When the output DC voltage is higher than the sum of the threshold voltage of the transistors $N_1 \sim N_4$, the clamp voltage limiter module begins to work. Transistor M_{13} and M_{14} turn on to reduce the voltage and limit the maximum output voltage to 3.3V. Because the capacitors in the circuit are charged and discharged periodically, the ripples of the output voltage can be excessively high, and it cannot be used as the supply voltage of the whole circuit.

B. REFERENCE CIRCUIT AND LDO CIRCUIT

Reference circuit is designed to reduce the ripples generated by voltage multiplier, and generate voltages and currents independent of the supply voltage. LDO circuit can generate the supply voltage of the whole system and increase the driving capacity of the power supply. This module provides the supply voltage to other modules on the chip.

Figure 4 gives a brief description of the structure of the reference circuit and LDO circuit. A start-up circuit is added to the reference circuit to ensure its normal operation. Figure 5

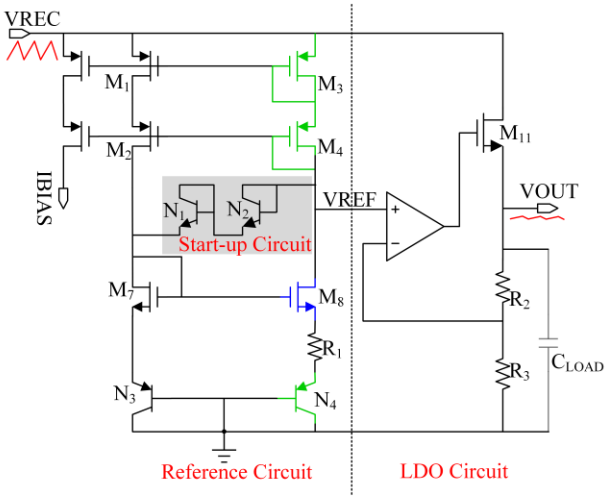

FIGURE 4. The structure of reference circuit and LDO circuit.

shows the equivalent circuit of highlight part in Figure 4. The relationship between the ΔVREC and ΔVREF can be described as follows:

$$\Delta V_{REF} = \Delta V_{REC} \times \frac{R + \frac{1}{gm_{(N_4)}}}{(\frac{1}{gm_{M_8}} + \frac{\frac{1}{gm_{M_{3,4}}}}{gm_{M_8} R_{o8}}) + R + \frac{1}{gm_{(N_4)}}} \approx \Delta V_{REC} \times \frac{1}{1 + \frac{1}{gm_{M_8}(R + \frac{1}{gm_{(N_4)}})}} \quad (2)$$

where gm_{M8} is the transconductance of M_8, R_{o8} is the output resistor of the small signal model of the M_8 transistor. Because of the high common mode rejection ratio of the reference circuit, through the equation (2), we can see the ripples of VREC has been reduced efficiently. The reference voltage is about 700mV. The module also generates a series of supply-independent current for the subsequent use.

Then the reference voltage is sent to the LDO circuit to generate the power supply for the tag. The LDO circuit is designed by using a negative feedback loop. The output voltage can be described as follows:

$$V_{OUT} = V_{REF} \times \frac{R_2 + R_3}{R_3} \quad (3)$$

From the equation, we can see the output voltage is relatively independent on the supply voltage. The output voltage of LDO circuit is about 1.1V and it is stored on a capacitor to provide supply power for other modules.

C. DEMODULATOR CIRCUIT

The function of the demodulator circuit is to remove the high-frequency carrier signal and restore the original signal back to the low frequency. Commonly, the circuit is implemented by using the envelope detection demodulator. Then, the signal will be sent to digital baseband for the subsequent signal processing [18].

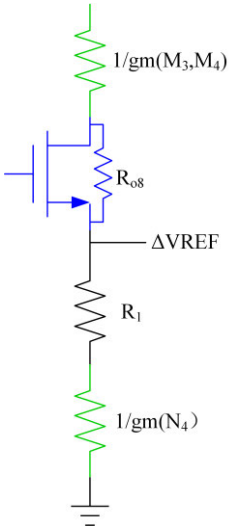

FIGURE 5. The equivalent circuit of highlight circuit in FIGURE 4.

Figure 6 shows the structure proposed in this study and the waveform of the key node. Firstly, the single stage voltage multiplier converts the input high-frequency signal to a DC voltage with ripples which contains the information of the original signal. Next, the envelope detector senses the ripples and the low pass filter reduces the amplitude of the ripples. Then, the average circuit continues to reduce the ripples. The hysteresis comparator compares the differences between the two nodes and restores the original signal to low frequency. Finally, the inverter chains improve the driving capability of the signal and send it to the digital baseband.

Figure 7 shows the structure of the hysteresis comparator in this design. Assuming the V_{ip} is at a relatively high level initially, M_2 is cut off. The current of IBIAS entirely flows into M_1 and the drain voltage of M_6 is pulled down to a low level. In this situation, the output voltage is up to the VLDO. When the voltage of V_{ip} begins to drop, the gate voltage of M_5 and M_6 keeps at a low level and the transistors are still cut off. The current of M_2 all flows to M_4. The current is determined by the copied current from the current mirror and the current from the transistor M_2. It can be seen from the analysis that when the current copied by the current mirror equals to the current flowing from M_2, the output voltage begins to reverse. A precise analysis can be seen from equation (4) ∼ (6) as follows:

$$I_{BIAS} = I_1 + I_2 \tag{4}$$

where I_1 and I_2 are the drain currents of M_1 and M_2 respectively.

$$\frac{I_3}{I_4} = \frac{\mu_P C_{OX}(\frac{W}{L})_3}{\mu_P C_{OX}(\frac{W}{L})_4} = K \tag{5}$$

where I_3 and I_4 are the drain currents of M_3 and M_4 respectively.

$$\beta_2 = \frac{1}{2}\mu_P C_{OX}(\frac{W}{L})_2 \tag{6}$$

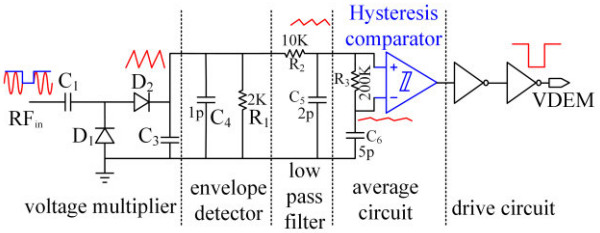

FIGURE 6. The structure of the demodulator circuit.

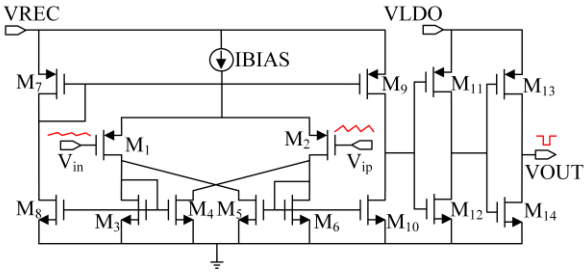

FIGURE 7. The structure of the hysteresis comparator.

The forward threshold voltage of the hysteresis comparator (V_+) can be calculated by equation (7) as follows:

$$V_+ = V_{GS2} - V_{GS1} = \sqrt{\frac{2I_{BIAS}}{\beta_2}} \bullet \frac{\sqrt{K}-1}{\sqrt{K}+1} \tag{7}$$

Similarly, the downward threshold voltage of the hysteresis comparator (V_-) can also be calculated. By simply changing the K value, we can make V_+ different from V_-, and realize the function of hysteresis comparator.

D. RING OSCILLATOR CIRCUIT

The ring oscillator is designed to generate a high frequency clock for the whole tag. The accuracy of the clock determines not only the speed of communication rate, but the compatibility of the design with the communication protocol [19]. According to the communication protocol, the frequency of the oscillation should be around 1.92MHz.

Figure 8 shows the structure of the ring oscillator in this design. It consists of a ring oscillator made up of 3-stage inverter, a current-starved structure and a drive circuit. The ring oscillator begins to work due to its inner noise. When the PMOS and NMOS transistors are switched on at the same time, the instantaneous current is extremely large. To prevent the large power consumption, tail current sources are added to the circuit to control its dynamic current. Drive circuit is used to increase its drive ability. A capacitor is used to control the oscillation frequency of the circuit. The relationship can be seen as follows [20]:

$$f = \frac{1}{2NT_D} \tag{8}$$

where N is the number of the stage of the ring oscillator, and T_D is the delay of each inverter.

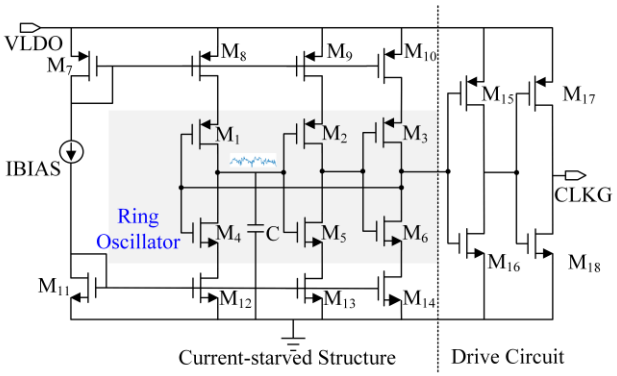

FIGURE 8. The structure of the ring oscillator.

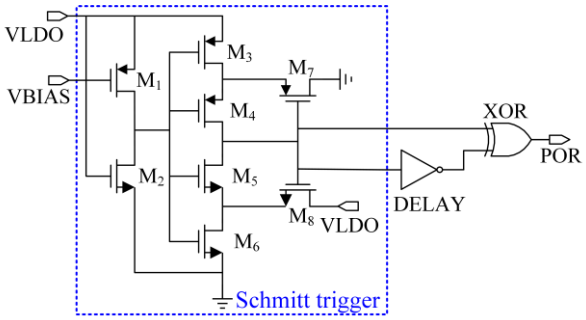

FIGURE 9. The structure of the power-on-reset circuit.

E. POWER-ON-RESET CIRCUIT

Power-on-reset circuit is mainly used to generate a negative pulse to initialize the digital baseband. When the output of voltage multiplier exceeds a certain voltage, the whole circuit is initialized by the pulse [21]. After the pulse, other circuits and digital baseband begin to work. Typically, the circuit is made by charging a specific capacitor. Figure 9 shows the structure of power-on-reset circuit proposed in this study.

In this structure, the circuit consists of a Schmitt trigger and an XOR gate circuit. Assuming the initial voltage of VLDO is 0, and transistor M_2 is cut off. The gate voltage of M_3 ~M_6 is pull up to VLDO. Since the supply voltage is relatively low, the gate voltage of M_7 and M_8 will change with the supply until transistor M_2 opens. At this time, transistors M_3 and M_4 will open and a negative pulse is generated at the output.

Simply, we can change the size of M_3, M_7 and M_6, M_8 to control the pulse width. The Schmitt trigger in this design can effectively avoid the circuit errors caused by the supply jitter due to its hysteresis. The whole tag is initialized by this signal.

F. TRUE RANDOM NUMBER GENERATOR CIRCUIT

In the whole RFID system, the reader is for transmitting the RF signal and accepting the high-frequency signal reflected by the tag. The tag is for receiving the signal of the reader and sending the information of baseband and NVM back to the reader. Mostly, the RFID communication mode is multi-access mode. However, when multiple tags appear in the same area, without signal processing, communication confusion will occur [22]. Consequently, it is necessary to introduce the anti-collision algorithm to the system, so that the reader and the tag can communicate one-to-one, thus ensuring the correctness and security of the communication.

The common anti-collision algorithm of RFID system is mainly based on time division multiplexing (TDMA). Only when the communication process is over, the algorithm will send instructions to make reader and tag unlocked. Then, the reader can go on communicating with other tags. Traditional ALOHA algorithm has a low throughput rate of 18.4%. So, this study uses slot-ALOHA algorithm as an anti-collision algorithm [13], [23]. Through statistical analysis, we can conclude the followed equations (9) ~ (10):

$$G = \sum_{i}^{n} \frac{\tau_n}{T} r_n \tag{9}$$

where τ_n is the transmission time of a data packet, r_n is the number of data packets sent in T, G is the average number of exchanged data packet in T. So, G represents the average number of the data packets transmitted between the reader and the tag in T.

$$\bar{S} = Ge^{-G} \tag{10}$$

where S is the channel throughput rate and $\bar{S}$ is the average throughput rate. We use 'S' to evaluate the ability of the system to process the transmitted data packet correctly. When S is equal to 1, it means there is no collision during the data transfer and when S is equal to 0, it means the system is unable to transmit information correctly due to the collision. So, $\bar{S}$ represents the average number of the data packets transmitted correctly between the reader and the tag in T. The relationship between $\bar{S}$ and G is shown in equation 10. From the equation, we can see when G is 1, S can go up to the maximum of 36.8%, and the channels are used more efficiently than the traditional ALOHA algorithm. This slot-ALOHA algorithm relies on a true random number generator to ensure tags communicate with the reader in turn.

The structure of true random number generator in this study is based on clock jitter. The schematic of this circuit is shown in Figure 10. There is clock jitter inside both the high-speed clock and the low-speed clock, which is reflected as phase noise on the signal. The high-speed clock is sampled by the low speed clock. Statistics show that when root mean square of the phase jitter of the low-speed clock and the period of the high-speed clock meet the following equation, the output signal VTRNG can be approximately seen as a random signal.

$$\frac{2\Delta_{rms}}{T} > 1 \tag{11}$$

where Δ_{rms} is the root mean square of the phase jitter of the low-speed clock, T is the period of the high-speed clock. We need to increase the jitter of low-speed clock and the

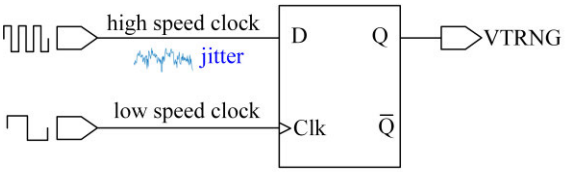

FIGURE 10. The schematic of the TRNG circuit.

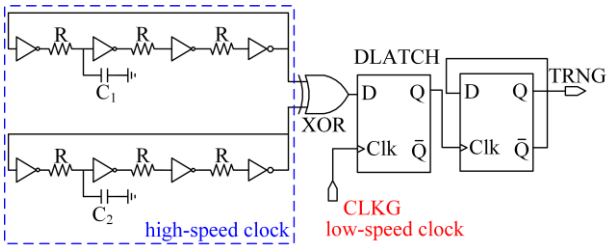

FIGURE 11. The structure of the TRNG circuit.

frequency of the high-speed clock to meet the equation. If this equation is satisfied, we can ensure that there is no obvious correlation between the output data, thus ensuring the unpredictability of all the data. Ideally, the duty cycle of the VTRNG must be about 50%.

The detailed circuit of the structure is presented in Figure 11. Because the ring oscillator itself is a positive feedback, the jitter noise will be continuously amplified. Meanwhile, to increase the thermal noise and reduce the frequency of the clock, resistances are introduced into the circuit. In this way, the phase error of the low-frequency clock is amplified, which can better satisfy the equation 11.

To ensure the duty cycle of the output is approximately 50%, XOR logic is added to the circuit [24]. Assuming that in the binary sequence, the probability of '1' is P and the probability of '0' is 1-P. To make the output of XOR gate be '1', its input must be '01' or '10', in which case the probability of output being '1' is shown as equation 11

$$2P(1-P) \tag{12}$$

Similarly, the probability of output being '0' is shown as equation 13

$$P^2 + (1-P)^2 \tag{13}$$

So, when there are n XOR gates, it can be concluded that the probability of output being '0' is shown as equation 14

$$0.5 + 2^{n-1}(P-0.5)^n \tag{14}$$

and the probability of output being '1' is shown as equation 15

$$0.5 - 2^{n-1}(P-0.5)^n \tag{15}$$

We can see that the XOR gate can ensure the 50% duty cycle of the output.

The circuit is triggered by the clock generated by ring oscillator and it introduces the jitters of high-frequency clock. The low-speed clock comes from the ring oscillator circuit and it is the signal of CLKG. The high-speed clock is also implemented by ring oscillator. It is different from the CLKG circuit in the value of passive component. In the design, the frequency of high-speed clock is 3MHz and the frequency of low-speed clock is 1.92MHz.

G. MATCHING NETWORK

In RFID system, the signal is transmitted between reader and tag through antenna. The antenna itself has a 50Ω impedance. If not matched properly, the energy will be mostly reflected back to the reader. It is necessary to make the input impedance of the tag equal to 50Ω through a matching network. For the tag front-end circuit, in order to maximize the received power, we often use the conjugate matching circuit to design the matching network. The circuit is implemented by pi-matching network shown in Figure 12.

IV. SIMULATION AND RESULT

The circuits are designed and simulated in Cadence Virtuoso. We use the power source whose amplitude is −12dBm to excite the whole circuits. The encoding method of the data is Manchester encoding, which uses the rising edge in a period to represent '1' and the falling edge to represent '0'.

A. VOLTAGE MULTIPLIER AND VOLTAGE LIMITER

In UHFP-RFID front-end circuit, the received signal is firstly converted into a DC voltage with ripples by voltage multiplier. Because of the charge and discharge of the load capacitors, the amplitude of the ripples is relatively large. To ensure the whole circuit to work efficiently, we set the output to be up to around 3V. Figure 13 shows the output of the module tested with an 800mV peak voltage of the input signal.

The blue line shows the output of the circuit without any load, and the red line shows the output with a 10μA load. From the result, we can see that the output voltage can be boosted higher than 3.4V without any load. Due to the voltage limiter, the output voltage is limited to no higher than 3.5V. With a 10μA load, the output voltage can be boosted up to 2.8V $\sim$ 3.3V. But the ripples of the output signal are about 270.3mV, which is too high to supply the whole system as a DC voltage. The efficiency of this circuit is about 34.8%. It is necessary to reduce the amplitude of ripples in the following circuits.

B. REFERENCE CIRCUIT AND LDO CIRCUIT

In this front-end, to save energy, the supply voltage of the module is about 1V$\sim$1.1V. Due to the high common mode rejection ratio, the ripples of the input voltage can be reduced significantly. Through the simulation, the common mode rejection ratio of this circuit can be up to 75dB. Figure 14

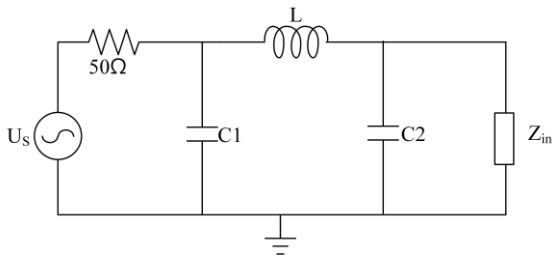

FIGURE 12. The structure of the matching network circuit.

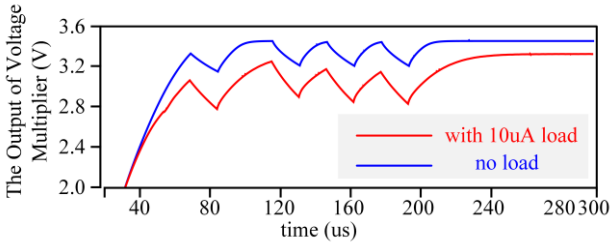

FIGURE 13. The simulation result of the voltage multiplier.

shows the simulation results of the LDO circuit and its ripples on the output voltage.

From the graph above, we can see the output voltage is stable at about 1.07V. The amplitude of the LDO output ripples is around 19mV. Compared with the output of voltage multiplier, the ripples have already been sharply reduced. It can be used as the power supply of the system.

C. DEMODULATOR CIRCUIT

The demodulator circuit is used to remove the high-frequency carrier, and restores signal to low frequency. Then, the output signal is sent to digital baseband for communication. The input signal itself has a lead code to provide initial power for the circuit. The lead code does not contain any useful information. Figure 15 shows the simulation result of the demodulator circuit.

From the picture, we can see, apart from the lead codes, the carrier is removed and the input signal is restored to low frequency. Because of the large capacitors and resistors in the circuit, there is a delay of the demodulation. At tt corner, the delay is about 0.5μs. The delay is acceptable to the system.

D. RING OSCILLATOR CIRCUIT

According to the communication protocol ISO/IEC18000-6C, the data transfer rate from the tag to the reader should at least 640Kbps. According to the communication protocol, the tolerance of the ring oscillator frequency should be within $\pm$15%. To fit the rate of baseband, the frequency of this ring oscillator is designed to be 1.92MHz. Figure 16 shows the Monte Carlo simulation result of the oscillator frequency (100 points).

From the Monte Carlo simulation result, we can see the average of the result is 1.90367MHz. About 94% of the

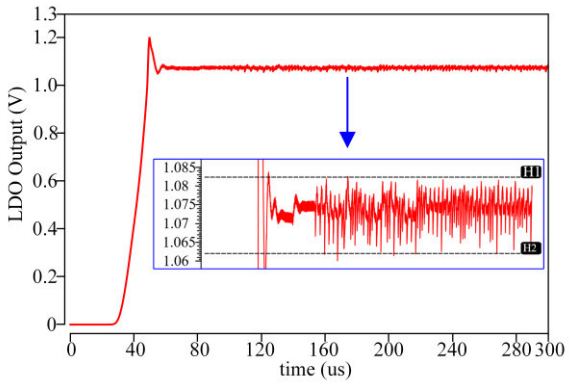

FIGURE 14. The simulation result of LDO and its ripples.

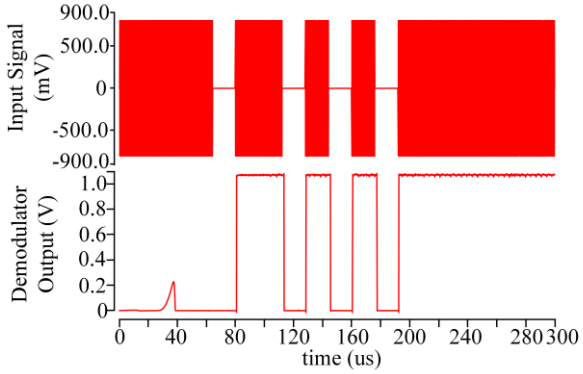

FIGURE 15. The simulation result of demodulator circuit.

sample is within the error, and the typical frequency of the output signal lies in 1.73478MHz $\sim$ 2.07256MHz. The simulation results can meet the requirement of the design.

Figure 17 shows the waveform of the ring oscillation frequency with temperature. From the graph, we can see there is a downward trend of both ff corner (2.12MHz $\sim$ 1.98MHz) and tt corner (1.97MHz $\sim$ 1.91MHz). The ss corner see an opposite trend (1.68MHz $\sim$ 1.71MHz) from $-10°$ to 40°. The frequency of the ring oscillator of different corners and temperatures can also meet the requirement.

E. POWER-ON-RESET CIRCUIT

The power-on-reset circuit is to generate a negative pulse to initialize the tag. The pulse width of the signal is designed to be more than 4μs. Figure18 shows the result of output waveform of this module.

From the result, we can see the circuit starts to generate a negative pulse when the power supply is higher than 811mV. The power-on-reset signal generates from 42.1us to 51.273us and it can last 9.173μs. It ends the reset before the meaningful signal arrives. It can meet the demand of the RFID tag front-end.

F. TRUE RANDOM NUMBER GENERATOR CIRCUIT

According to the analysis mentioned above, we can see that the key point of the TRNG is its duty cycle. Ideally, the

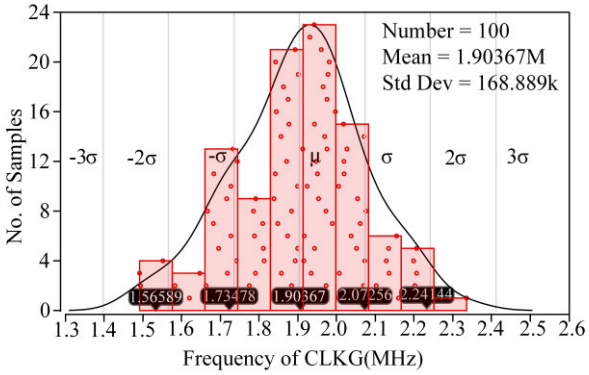

FIGURE 16. The Monte Carlo result of the ring oscillator.

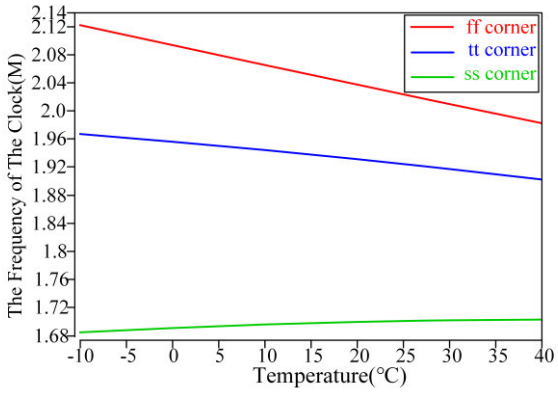

FIGURE 17. The simulation results of temperature and corner.

duty cycle should be 50% to ensure the correctness of the communication process. Theoretically, the error should be within ±5%. Figure 19 shows the Monte Carlo simulation result of the output signal duty cycle (100 points). The TRNG circuit consumes only about 529nA.

From the simulation, we can see that the average of the duty cycle is 50.2907%. The typical duty cycle of the output is about 46.6352% ∼53.9461%. 91% of the sample is within the error. The TRNG is reliable for the system.

G. MATCHING NETWORK

The matching network is designed to match the impedance of the antenna (50Ω) and ensures the circuit to receive the maximum power. By simulation, the input impedance of the system is 22.64-j55Ω. In the circuit, we use the pi-matching network to complete the match. The circuit is shown in Figure 20.

H. CORNER SIMULATION RESULTS

Besides the results of simulation mentioned above, to ensure the system can work correctly, we also need to simulate the circuit under different corners ff, tt, ss. Different corners can bring different mismatches to the circuit. The results are concluded in the table3.

From the table3, the circuit can work well under all corners. The results are all within the error. The whole system is relatively reliable and can work efficiently.

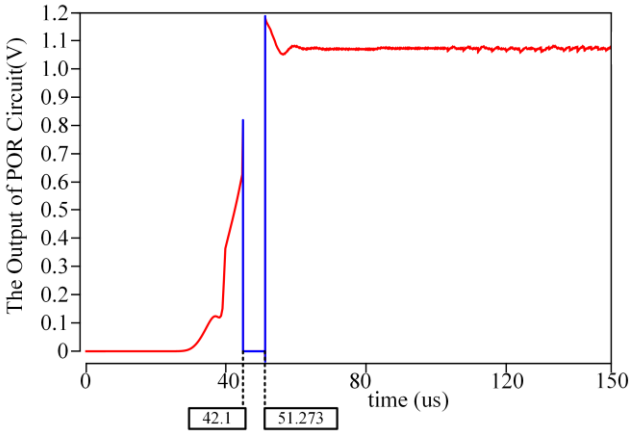

FIGURE 18. The simulation result of POR.

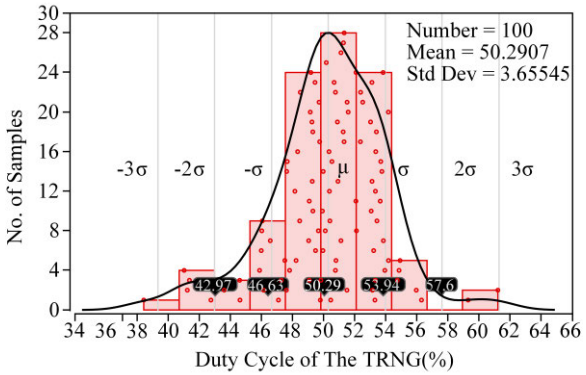

FIGURE 19. The Monte Carlo result of the TRNG.

TABLE 3. The simulation result of different corners.

	tt corner	ff corner	ss corner
demodulation delay (μs)	0.5	0.467	0.74
LDO ripples (mV)	19	24	17
clock frequency (MHz)	1.893	2.02	1.716
POR pulse width (μs)	9.17	4.28	9.23
TRNG duty cycle (%)	50.28	52.28	48.8

I. POWER CONSUMPTION

In the front-end circuit, besides the function of the circuit, we also show concerns on the power consumption. We need to make the power consumption of each module as low as possible. Figure 21 shows the power consumption of the main modules. We can see the analog LDO circuit consumes the most energy due to its heavy loads. The total power consumption of the system is about 8.12 μA.

V. TEST AND RESULT

After detailed simulation, we begin to test the function of RFID tag. Figure 22 shows the micro photograph of the chip. In this experiment, we use RF signal generator RIGOL-DSG836 and square wave generator RIGOL-DG832 to generate the modulated ultra-high frequency signal. Then, we use Agilent-N9916A to measure the input impedance and S11 parameter of the chip. The waveform of voltage

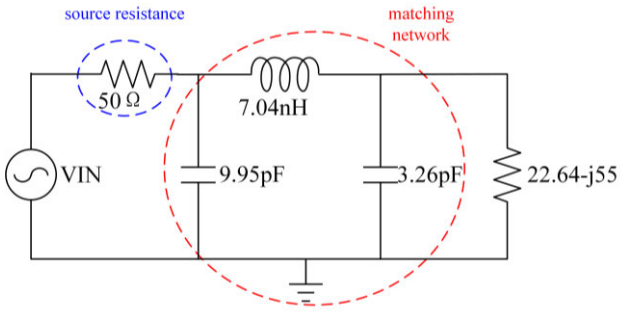

FIGURE 20. The circuit of matching network.

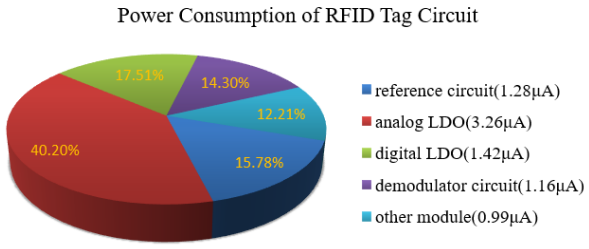

FIGURE 21. The power consumption of RFID tag modules.

multiplier, LDO, demodulator circuit, and TRNG in the circuit is shown in RIGOL-MSO5074. Figure 23 shows the environment of the test.

A. MATCHING NETWORK

In the system, the signal power is firstly received by the matching network. To reduce the power loss, the input impedance should match the impedance of the antenna. In the experiment, we use the conjugate matching to achieve the matching network. We test the input impedance and S11 parameter of the chip by using Agilent-N9916A. Figure 24 shows the test result of parameter S11 and Figure 25 shows the input impedance in Smith Chart.

The input impedance of the chip is 16.2-j233Ω and is marked 'A' in the Fig.25. We also use the matching circuit shown in Fig.12 to achieve impedance matching. Due to the input power and the parasitic parameter on PCB, the impedance is different from the simulation, and we change the value of capacitor and inductor due to the test results. Ideally, the value of C_1 is 33pF, the value of C_2 is 3.5pF, and the value of L is 7.6nH. But the impedance is related to the input power, we change the values around the ideal value. Finally, the value of C_1 is 27pF, the value of C_2 is 3.5pF, and the value of L is 9.4nH.

From the graphs above, we can clearly see that the value of S11 parameter at 960MHz is about −38.56dB and the equivalent input impedance is 51.5-j0.8Ω, thus effectively reducing the return loss of the input signal. In this matching, the energy of input source is received by the circuit at its maximum power point.

B. VOLTAGE MULTIPLIER AND LDO CIRCUIT

In the system, we use the high frequency RF signal generator RIGOL-DSG836 to test the system. The amplitude of the input signal is −10.3dBm and its peak-to-peak voltage is 500mV, and it is modulated by a pulse signal whose duty cycle is 65%. The depth of the modulation is 100% and we use the amplitude modulation to process the input signal. The outputs of the voltage multiplier and LDO are displayed in RIGOL-MSO5074 and shown in Figure 26.

In the graph, the blue line shows the output voltage of voltage multiplier and the red line shows the output voltage of LDO circuit. From the picture, we can see the amplitude of ripples of the voltage multiplier is about 469.65mV and LDO circuit can reduce the ripples to 55.467mV under the condition mentioned above. The output voltage of the LDO is about 1.05V. The circuit can effectively reduce the ripples and generate a DC power for the whole system.

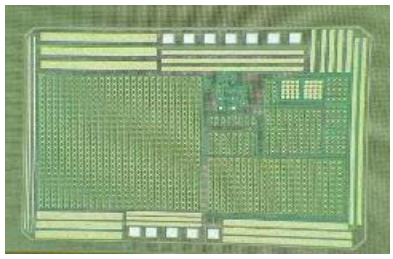

FIGURE 22. The chip of the designed RFID tag.

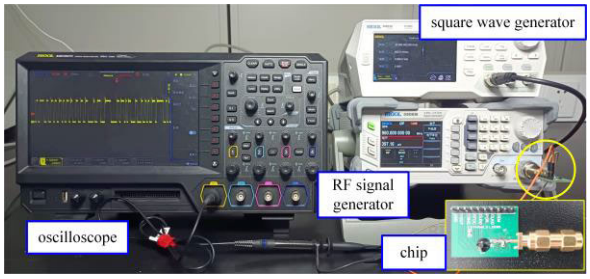

FIGURE 23. The test environment of the designed RFID tag.

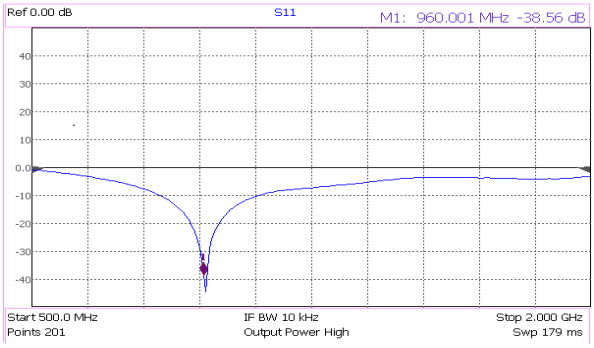

FIGURE 24. The test result of the S11 parameter.

C. DEMODULATOR CIRCUIT

The demodulator circuit in the system is used to remove the high frequency carrier and then restore the original signal to the low frequency band. In the test, we use RIGOL-DSG836 and RIGOL-DG832 to generate a high

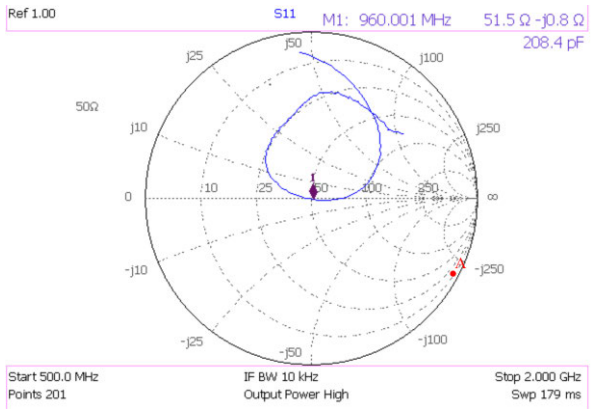

FIGURE 25. The test result of the input impedance in Smith Chart.

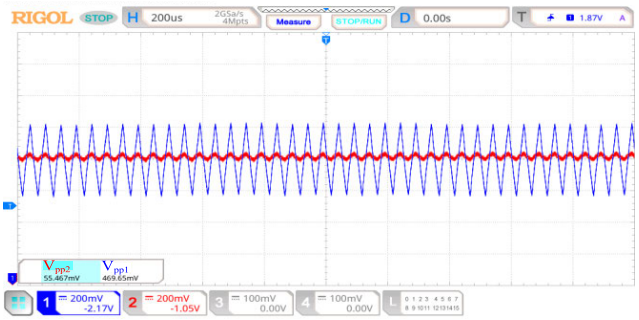

FIGURE 26. The test result of the voltage multiplier and LDO.

frequency RF input signal which is modulated by a square wave signal. We assume that the square wave signal is 50KHz and its duty cycle is 65%. The output of the demodulator circuit is displayed in RIGOL-MSO5074 and shown in Figure 27.

From the picture, we can see that the high frequency carrier has been removed and the signal is restored to low frequency. Although the down edge of signal is relatively slow, due to the large parasite capacitance of I/O pad, it will not affect the next process. The demodulator circuit can extract the original signal from the received signal.

D. TRUE RANDOM NUMBER GENERATOR CIRCUIT

The true random number generator in the circuit is used to generate the digital signal in chaos. The anti-collision algorithm is designed to avoid the situation that two tags communicate at the same time. Ideally, the duty cycle of the output signal should be 50%, within a ±5% error. In the system, we use RIGOL-DSG836 to generate input RF signal for the system. The output of the TRNG circuit is displayed in RIGOL-MSO5074 and shown in Figure 28.

It can be seen clearly from the graph that the output of the TRNG is disordered. The duty cycle of the waveform is around 51.964%, which is within the range of error.

To ensure the reliability of the circuit, we choose 200 points randomly to test its duty cycle. The test result is shown in Figure 29. From the bar chart, we can see that 85.5% of the test points is within the error.

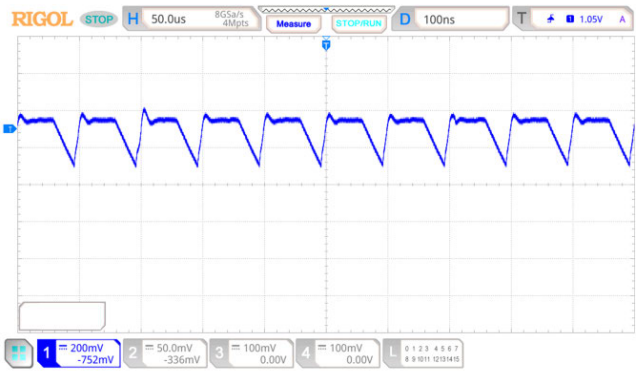

FIGURE 27. The test result of the voltage multiplier and LDO.

TABLE 4. Performance comparisons.

	[25]	[26]	[27]	This work
Process	0.13μm	0.35μm	0.18μm	0.18μm
Freq (MHz)	900~960	868~900	860~960	860~960
Standard supported	EPC-gen2	N.A.	EPC-gen2	ISO/IEC 18000-6C
Tag type	Passive	Passive	Passive	Passive
Chip size (mm^2)	1.1	2.24	1.1	2.5
Power (μW)	71	37.5	12	8.67
Supply voltage (V)	1.3	1.4	1/0.5	1.07
Clock freq (MHz)	1.92	0.48	2.3	1.92
Sensitivity(dBm)	-12	-6	N.A.	-10.3
Efficiency	47%	N.A.	35%	34.8%

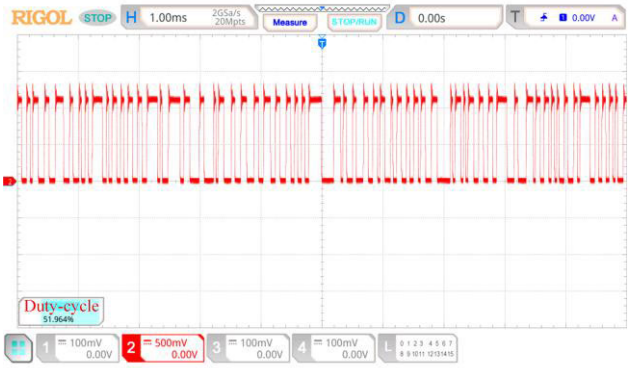

FIGURE 28. The test waveform of TRNG.

VI. DISCUSSION

This study proposed a low power consumption UHFP-RFID tag front-end circuit with a novel TRNG based on ISO/IEC 18000-6C protocol. Comparisons of this work's performance with some of other works are listed in Table 4.

From the table, we can see that the power consumption of this work has an advantage over other works due to a lower inner supply voltage. Compared to work [27], the inside clock frequency is a bit lower. The chip size of this work is similar to work [26], while larger than other works.

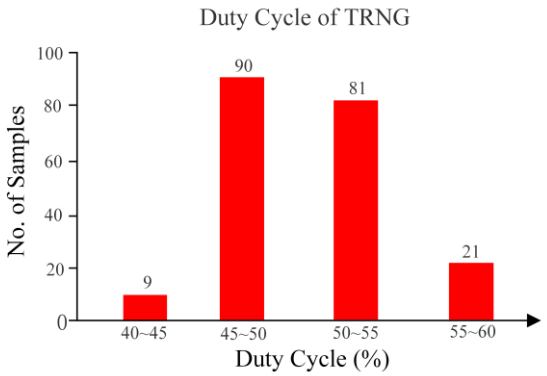

FIGURE 29. The test result of TRNG (200 points).

In the design, we use the NMOS transistors with a low threshold voltage, which can significantly improve the efficiency of the voltage multiplier. However, they have a large leakage current and a large conduction power consumption, leading to non-ideal effects on the substrate. We can use the advanced processing technology or leakage current suppression structure to reduce the leakage.

Usually, the output of the demodulation circuit is directly connected to the digital baseband, with a load of fF-level node capacitance. To measure its waveform, the output is connected to the IO pad, with a large pF-level parasitic capacitance of the node. The drive current of the circuit module is very low to reduce dynamic power consumption. Therefore, the output signal edge falls slowly.

The low-power design structure proposed in this article can also be applied to the design of other power conversion and energy management systems. We can use the current-starved structure to design the on-chip clock of the PWM modulation in a DC-DC system. The low threshold voltage transistors can be employed in the charge pump and DC-DC module to boost the efficiency of the circuit.

VII. CONCLUSION

This paper proposed a UHFP-RFID tag front-end circuit with a novel TRNG for ISO/IEC 18000-6C protocol. In this study, we use the low power design such as current-starved structure and power-on-reset module to minimize its power consumption. We also design a novel TRNG circuit where the high-speed clock is sampled by a low-speed clock to ensure the correctness and security of the communication. Measured results shows that the input impedance of circuit is about 51.5-j0.8Ω after matching. The LDO circuit can effectively reduce the ripples of voltage multiplier from 469.65mV to 55.467mV. The demodulator circuit can remove the high frequency carrier of the signal and restore the original circuit to the low frequency band. The TRNG module can produce a series of random number with 85.5% of credibility. The chip has a power consumption of 8.67μW and its size is 25mm^2. In the future, this work has a broad application prospects in wireless communication systems such as electronic monitoring, data acquisition and logistics control [28].

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