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RESEARCH ARTICLE

Design of Enhancement Mode β-Ga_2O_3 Vertical Current Aperture MOSFETs With a Trench Gate

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ABSTRACT In this article, enhancement-mode (E-mode) operation is achieved by employing a trench gate on the β-Ga_2O_3 current aperture vertical MOSFETs via Sentaurus TCAD simulation. The performance of the trench gate β-Ga_2O_3 MOSFETs was investigated with different structure parameters, such as trench gate depth, channel doping concentration, and drift layer doping concentration and thickness. The transistor with a trench gate recess (Gr) of 130 nm obtained a high on/off current ratio of 10^8, an on-current density of 65 A/cm^2, a low specific on-resistance ($R_{on,sp}$) of 42.5 mΩ·cm^2, and a breakdown voltage (BV) of 488 V for an E-mode operation. With the thickness of the drift layer increasing to 9.2 μm, BV is improved to 721 V, $R_{on,sp}$ keeps a low value of 43.5 mΩ·cm^2 due to the trench gate structure, and the transfer characteristic maintains the same. The thermal characteristics of the proposed MOSFET were studied and the device stability with high temperature was analyzed. The transistor with Gr = 130 nm can keep working in E-mode operation at T = 500 K. The performance of the transistor exhibits its great potential as a high-voltage switch device for power electronic applications.

INDEX TERMS Beta-phase gallium oxide (β-Ga_2O_3), enhancement-mode, trench gate, vertical power MOSFET, current aperture, specific on-resistance, breakdown voltage, thermal characteristics.

I. INTRODUCTION

In the past decade, beta-phase gallium oxide (β-Ga_2O_3) has attracted extensive research as an ultra-wide bandgap semiconductor material owing to its outstanding material properties, including a high breakdown field of 8 MV/cm [1], a large Baliga's figure of merit (FOM) which is over three times of GaN and ten times of 4H-SiC [2], [3], and a low intrinsic carrier concentration allowing for high-temperature operations [4]. Huang's chip area manufacturing FOM shows a cost advantage of large size β-Ga_2O_3 bulk crystals over three times of GaN and five times of 4H-SiC [2], [5]. At present, no p-type Ga_2O_3 has been reported due to the difficulty for single-crystal oxide semiconductors to form shallow acceptor states [6], and self-trapped holes [7] which results in very low hole mobility and associated high effective hole mass [8]. It is challenging to implement enhancement-mode (E-mode) β-Ga_2O_3 MOSFETs since the absence of p-type doping causes no inversion layer. To make n-channel accumulation mode devices, different approaches have been developed to fabricate E-mode β-Ga_2O_3 MOSFETs, one of which is to decrease the channel thickness to fully deplete the channel under zero gate bias voltage [9], such as β-Ga_2O_3 on insulator (GOOI) field effect transistors [10], [11], [12] and gate recess process [13], [14], [15]. From our review work of trench gate β-Ga_2O_3 MOSFETs [16], the trench gate process was mostly adopted in the planar device structure, and no vertical single trench gate β-Ga_2O_3 MOSFET was reported. The design of the vertical trench gate β-Ga_2O_3 power MOSFETs was developed via Sentaurus TCAD in this work. A trench gate was applied on a depletion mode (D-mode) current aperture vertical MOSFET to realize E-mode operation. The material-dependent physical models for the simulation were introduced. The static characteristics of the transistors were

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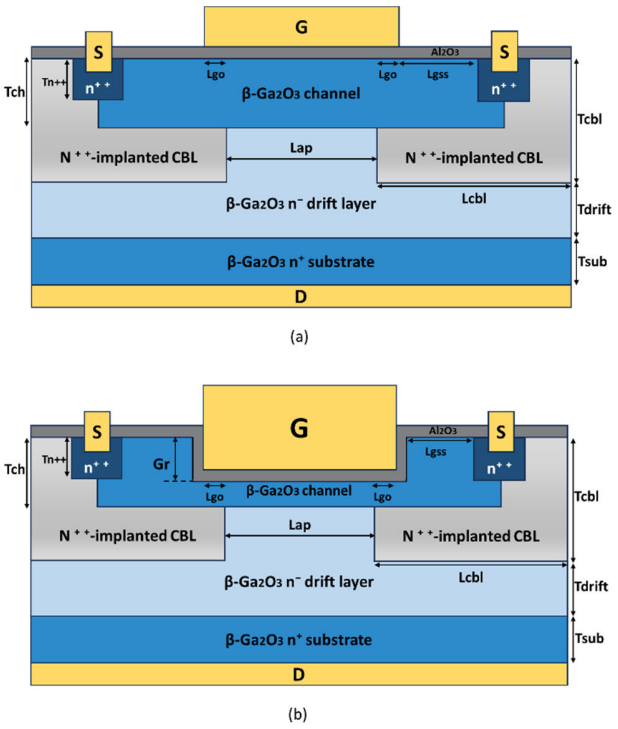

FIGURE 1. Schematic cross-sectional view of (a) planar gate [23], and (b) trench gate β-Ga_2O_3 MOSFET.

investigated, and the dependence of the device performance on different device parameters and temperatures was analyzed.

II. DEVICE DESIGN AND DESCRIPTION

A. CURRENT APERTURE VERTICAL β -Ga_2O_3 MOSFET

The first current aperture vertical electron transistors (CAVETs) were developed on AlGaN/GaN by Ben-Yaacov et al. [17] for RF power application for dispersion-free performance. The AlGaN/GaN CAVETs exhibit the advantage of the large electric field region being buried under the gate into the bulk, and a high voltage switch for power electronics application [18], [19], [20]. For ultra-wide bandgap semiconductors, based on the successful work of β-Ga_2O_3 doping with shallow donors (Si) [21] and deep acceptors (Mg, N) [22], Wong et al. demonstrated the first current aperture vertical β-Ga_2O_3 power MOSFETs in D-mode [23] and E-mode [24] operations, and both devices are with a planar gate. Figure 1 (a) depicts the schematic structure of D-mode β-Ga_2O_3 current aperture MOSFET [23], which was used for the simulation calibration in this work. The source contact is separated from the drain contact by an electron barrier, N-ion-implanted β-Ga_2O_3, called a current blocking layer (CBL), and the gate-modulated current flows vertically through a well-defined opening called the aperture.

B. TRENCH GATE STRUCTURE

The trench gate process is one of the effective solutions to make n-channel accumulation mode β-Ga_2O_3 devices to implement E-mode. Our review work summarized the recent progress of trench gate β-Ga_2O_3 MOSFETs [16]. The trench gate was mostly used in the planar device structure, and only one vertical D-mode trench gate MOSFET was demonstrated by Sasaki et al. [25] with a structure similar to vertical β-Ga_2O_3 FinFETs. Wong et al. [24] demonstrated the E-mode planar gate β-Ga_2O_3 current aperture MOSFET by reducing the implanted channel of the D-mode device using the n_{access} regions. Different from the method Wong et al. used, this work applied a single trench gate on the D-mode planar gate β-Ga_2O_3 MOSFET, as shown in Figure 1 (b), to realize E-mode operation and investigate the impact of the trench gate on DC performance.

III. SIMULATION SETUP AND CALIBRATION

Sentaurus TCAD device simulator was employed in this work. The physical models for β-Ga_2O_3 device simulation with material-dependent parameters are elaborated in this section, and the calibrated curves are presented as well.

A. TEMPERATURE AND DOPING DEPENDENT MOBILITY MODEL

In doped semiconductors, the carrier mobility is affected by carrier density and temperature [26], [27]. The increasing active doping concentration causes more carrier scattering on ionized impurities and degrades mobility. At high temperatures, the increased phonon concentration leads to the carrier scattering increasing to lower the mobility. In Sentaurus, the mobility model can be specified with Arora model, as a function of doping concentration and temperature [28]. The electron mobility (μ_n) can be written as:

$$\begin{aligned} \mu_n &= \mu_{min} + \mu_d/[1 + ((N_{A,0} + N_{D,0})/N_0)^{A^*}] \\ \mu_{min} &= A_{min}\cdot(T/300\text{K})^{\alpha_m},\ \mu_d = A_d\cdot(T/300\text{K})^{\alpha_d} \\ N_0 &= A_N\cdot(T/300\text{K})^{\alpha_N},\ A^* = A_a\cdot(T/300\text{K})^{\alpha_a} \end{aligned} \quad (1)$$

where $N_{A,0}$ and $N_{D,0}$ are the active donor and acceptor concentrations; T is the temperature; $A_{min} = 13cm^2/Vs$, $A_d = 235cm^2/Vs$, $A_N = 1.1 \times 10^{18}cm^{-3}$, $A_a = 0.78$, $\alpha_m = -0.57$, $\alpha_d = 0.78$, $\alpha_N = 2.4$, and $\alpha_a = -0.146$ are the material-dependent parameters for β-Ga_2O_3 electron mobility, which was calibrated with the experimental data at the room temperature of $T = 300$K by Park et al. [29]. We modified the exponent parameter α_d from 0.78 to -2.13 to calibrate the temperature-dependent electron mobility with the experimental results obtained by Ma et al. [30]. As shown in Figure 2, the electron mobility decreases as the temperature increases, and the curve of the corrected Arora model with $\alpha_d = -2.13$ matches the measured data with $N_{A,0} = 7.5 \times 10^{16}cm^{-3}$ and $N_{D,0} = 2.4 \times 10^{17}cm^{-3}$ [30].

B. HIGH-FIELD SATURATION MOBILITY MODEL

At low electric fields, the carrier drift velocity is proportional to the electric field, and the low-field mobility is constant. However, in high electric fields, the velocity increases sub-linearly to a saturation speed as the electric field rises, which degrades the mobility. For β-Ga_2O_3, the theoretical

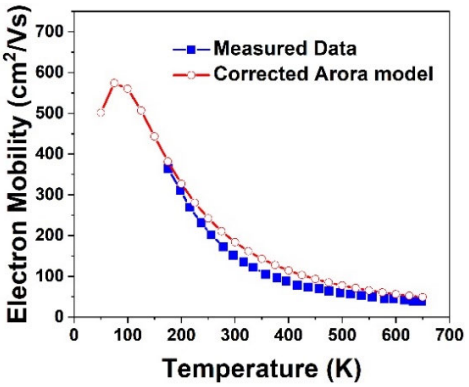

FIGURE 2. Temperature-dependent electron mobility of β-Ga_2O_3 with $N_{A,0} = 7.5 \times 10^{16}\text{cm}^{-3}$ and $N_{D,0} = 2.4 \times 10^{17}\text{cm}^{-3}$.

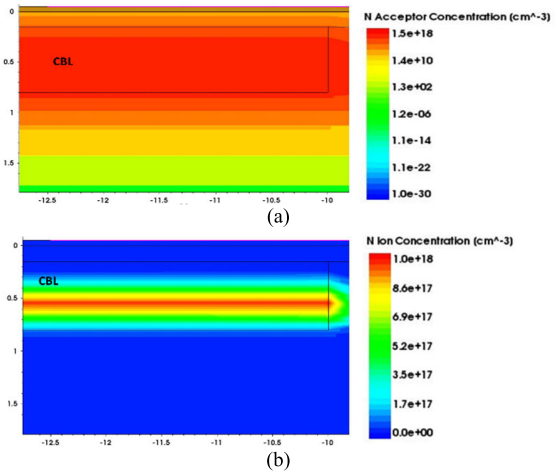

FIGURE 3. Nitrogen (a) acceptor and (b) ion concentration in one of the CBLs.

estimation of the electron saturation velocity by Ghosh and Singisetti [31] is $1.0 \sim 2.0 \times 10^7 cm/s$, and the saturation velocity at low temperature of 50 K based on the measured velocity-field profile is evaluated above $1.1 \times 10^7 cm/s$ by Zhang et al. [32]. The high-field saturation mobility (μ_{n_hf}) can be simulated with the Caughey-Thomas model [33] given in the following expression:

$$\mu_{n\_hf}(E) = \mu_n / [1 + (\mu_n \times E / v_{sat})^{\beta}]^{1/\beta} \tag{2}$$

where E is the electric field, $v_{sat} = 1 \times 10^7 cm/s$ is the saturation velocity, and $\beta = 0.37$ is the fitting parameter.

C. IMPACT IONIZATION MODEL

Besides mobility, impact ionization is also an important high-field effect. In power devices, as the electric field increases further, inter-band transitions and electron ionization become significant and could cause the device breakdown. To obtain impact ionization rate G_{ii}, the formulas given in (3) was used in the simulation:

$$G_{ii} = (\alpha_n |\boldsymbol{J_n}| + \alpha_p |\boldsymbol{J_p}|)/q \tag{3}$$

where q is the charge of an electron; $|\boldsymbol{J_n}|$ and $|\boldsymbol{J_p}|$ are the electron and hole current density vectors; α_n and α_p are the electron and hole ionization coefficient, which can be calculated by the equation (4) and (5) respectively:

$$\alpha_n(E) = \gamma a_n exp(-\gamma b_n / E) \tag{4}$$

$$\alpha_p(E) = \gamma a_p exp(-\gamma b_p / E) \tag{5}$$

$$\gamma = \frac{\tanh(\frac{\bar{h}\omega_{op}}{2k \cdot 300\text{K}})}{\tanh(\frac{\bar{h}\omega_{op}}{2kT})} \tag{6}$$

where k is the Boltzmann constant; $\bar{h}\omega_{op} = 63meV$ is the optical phonon energy; $a_n = a_p = 7.6 \times 10^5 cm^{-1}$ and $b_n = b_p = 2.1 \times 10^7 V/cm$ are the fitting parameters for β-Ga_2O_3 [34].

D. INCOMPLETE IONIZATION MODEL

In the nitrogen-doped β-Ga_2O_3, the deep acceptors have relatively large ionization energy compared to thermal energy, which means the dopants cannot be fully ionized, so incomplete ionization must be considered in the simulation. When the N doping concentration N_{AN0} is less than $1 \times 10^{22} cm^{-3}$, the density of ionized N acceptors, N_{AN}, can be given by Fermi–Dirac distribution:

$$N_{AN} = N_{AN0} / (1 + 2exp(\frac{E_{AN} - E_{Fp}}{kT})) \tag{7}$$

where E_{AN} is the N acceptor ionization energy in β-$Ga_2O_3$and the experimental data of 87 meV obtained by Liu et al. [35] is adopted for the simulation; E_{Fp} is the quasi-Fermi energy. For the case of $N_{AN0} > 1 \times 10^{22} cm^{-3}$, the acceptors are assumed to be completely ionized, which is out of the range of this work.

E. CALIBRATION

The planar gate β-Ga_2O_3 current aperture MOSFET shown in Figure 1 (a) is the referenced MOSFET for simulation setup and calibration. Table 1 lists the structural parameters of the device [23]. According to the secondary ion mass spectrometry (SIMS) depth profiles of N and Si in the gate-CBL overlap region of the referenced device [23], the Gaussian doping was applied in the CBLs, and the uniform doping was used in the channel region since the Si ions are uniformly distributed there. The channel and drift layer Si doping concentration were adapted to 1.1×10^{18} cm^{-3} and 8.0×10^{15} cm^{-3} respectively to best match the experimental data. In CBLs, the N Gaussian doping peak concentration of 1.5×10^{18} cm^{-3} and the corresponding N ion peak concentration of 1.0×10^{18} cm^{-3} shown in Figure 3 (a) and (b) respectively indicate the model of incomplete ionization of N acceptor was implemented successfully.

Figure 4 presents the calibrated DC characteristics of the planar gate β-Ga_2O_3 MOSFET. Both the output characteristics in Figure 4 (a) and transfer characteristics in Figure 4 (b) of the device match the experimental data [23]. At the drain voltage (V_D) of 20 V and gate voltage (V_G) of 5 V, the drain current density (I_D) reaches 0.43 kA/cm^2 normalized to the

TABLE 1. Device parameters for simulation [23].

Parameter	Value
Nch, Channel Si doping concentration	1.1×10^{18} cm^{-3}
n++ source Si doping concentration	5.0×10^{19} cm^{-3}
CBLs N Gaussian doping peak concentration	1.5×10^{18} cm^{-3}
Ndrift, Drift layer Si doping concentration	8.0×10^{15} cm^{-3}
Substrate Sn doping concentration	3.0×10^{18} cm^{-3}
Tch, channel depth	0.15 µm
Tn++, n++ source depth	0.1 µm
Tal2o3, Al_2O_3 gate dielectric thickness	50 nm
Tcbl, CBL outside edge depth	0.8 µm
Tdrift, drift layer depth under CBL	4.2 µm
Tsub, substrate depth	600 µm
Tsmi, metal depth inbedded in n++ source	50 nm
Tsm/Tdm, source/drain electrodes depth	0.25 µm
Tgm, gate electrode depth	0.295 µm
Lcbl, one CBL length	37.5 µm
Lch, channel length	55 µm
Ln++, n++ source length	20 µm
Lg, gate length	25 µm
Lgo, the gate–CBL overlap length	2.5 µm
Lap, aperture length	20 µm
Lgss, gate–source spacing	5 µm
Lsm, source contact length	15 µm
Wsm, source contact width	200 µm
Wap, aperture width	200 µm
Wn++, n++ source width	220 µm
Wch, channel width	240 µm
Wcell, device cell width	260 µm

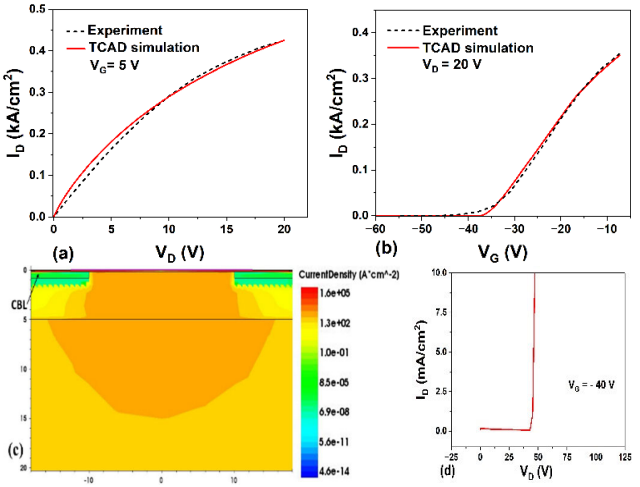

FIGURE 4. Calibrated (a) output and (b) transfer characteristics of the planar gate β-Ga_2O_3 MOSFET with the experimental data [23]. (c) Current density at V_D = 20 V and V_G = 5 V. (d) Off-state breakdown I-V characteristic at V_G = − 40 V.

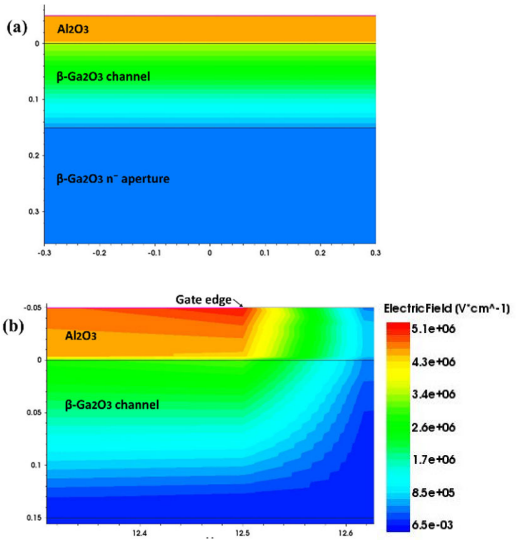

FIGURE 5. Electric field distribution (a) above the current aperture and (b) under the gate edge of planar gate β-Ga_2O_3 MOSFET at V_G = − 40 V and V_D = 47 V.

area of the channel (1.32×10^{-4} cm^2). The threshold gate voltage (V_T) is −38 V for a D-mode operation. The current density shown in Figure 4 (c) demonstrates the CBL regions obstruct the current as expected. As presented in Figure 4 (d), the off-state breakdown I-V characteristic of the device was calculated at $V_G = -40$ V by the external resistor method [36]. The simulated breakdown voltage (BV) of 48 V was obtained at $I_D = 10^{-3}$ A/cm^2 [23], comparable to the experimental BV of 25 V. As shown in Figure 5 (a), at $V_G = -40$ V and $V_D = 47$ V, the electric field near the Al_2O_3/β-Ga_2O_3 interface above the current aperture is 3.7 MV/cm and 3.4 MV/cm in Al_2O_3 and β-Ga_2O_3respectively. The largest electric field of 5.1 MV/cm is located at the surface of the Al_2O_3layer near the gate edge shown in Figure 5 (b). Electron ionization coefficient α_n illustrated in Figure 6 (a) presents the strong distribution of ionized electrons under the gate oxide, which is consistent with the electric field distribution in β-Ga_2O_3. Impact ionization rate G_{ii} shown in Figure 6 (b) displays the highest generation rate of 4.3×10^{17} cm^{-3}/s in the β-Ga_2O_3 channel under the gate edge due to the peak electric field, and the G_{ii} distribution in the drift layer is consistent with the current density shown in Figure 6 (c).

IV. SIMULATION RESULTS AND DISCUSSION

A. EFFECT OF TRENCH GATE DEPTH

Based on the well-calibrated planar gate β-Ga_2O_3 MOSFET model, different depths of trench gate recess (Gr) were applied to the device. The trench gate simulation results are summarized in Table 2. Figure 7 illustrates the dependence of DC characteristics of trench gate β-Ga_2O_3 MOSFET on the variation of Gr. As shown in Figure 7 (a), the threshold voltage of V_T increases as Gr turns deeper, whereas the drain current density of I_D normalized to the area of the channel (1.32×10^{-4} cm^2) at $V_D = 20$ V, $V_G = 5$ V decreases due to the reducing of the channel depth. At Gr = 130 nm, V_T reaches the positive value of 0.74 V for a fully depleted channel for an E-mode operation, and $I_D = 0.065$ kA/cm^2 is over five times larger than $I_D = 0.012$ kA/cm^2 of the reported E-mode planar gate β-Ga_2O_3 MOSFET [24]. At the deepest Gr = 145 nm, V_T raises to 2.5 V, and $I_D = 0.03$ kA/cm^2 is twice that of the reported device in [24]. Normalized

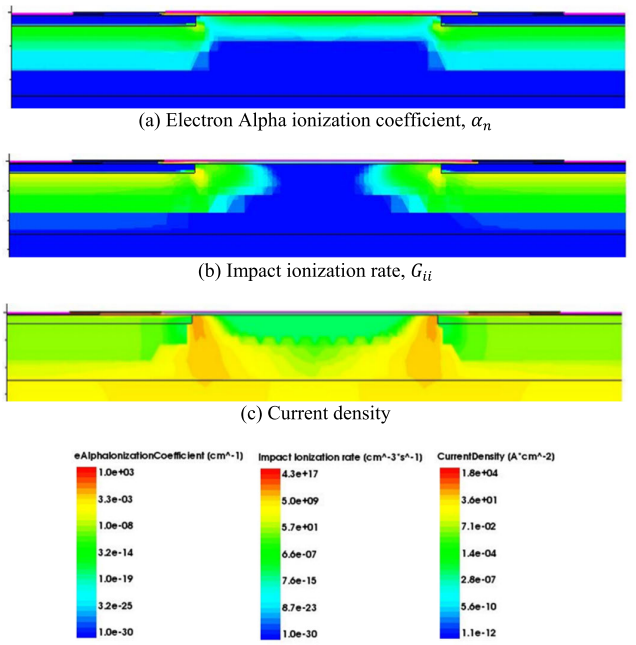

FIGURE 6. (a) Electron Alpha ionization coefficient, (b) impact ionization rate, and (c) current density of the planar gate β-Ga_2O_3 MOSFET at V_G =− 40 V and V_D = 47 V.

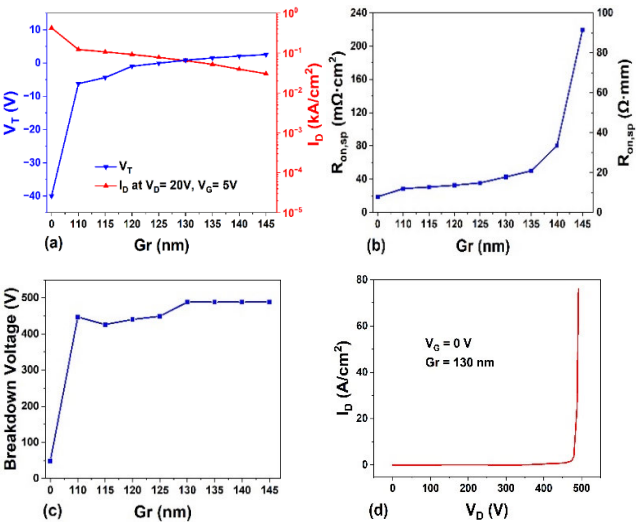

FIGURE 7. DC characteristics of trench gate β-Ga_2O_3 MOSFET: (a) V_T and I_D at V_D = 20 V, V_G = 5 V, (b) $R_{on,\,sp}$ and (c) BV at different Gr. (d) Off-state breakdown I-V characteristic at V_G = 0 V with Gr = 130 nm.

to the channel length of 55 μm, the drain current density of 154.9 mA/mm at Gr =130 nm is larger than those of the reported E-mode planar β-Ga_2O_3 trench gate MOSFET in [16]. The output characteristics of the trench gate β-Ga_2O_3 MOSFET with Gr = 130 nm shown in Figure 8 (a) exhibit a clear current modulation feature. As shown in Figure 8 (b), the current flow pattern of trench gate MOSFET is different from that of the planar gate MOSFET shown in Figure 4 (c) because of the narrower channel.

TABLE 2. Summary of the simulation results of the trench gate β-Ga_2O_3 vertical MOSFETs.

Gr (nm)	V_T (V)	I_D (kA/cm²)	$R_{on,sp}$ (mΩ·cm²)	$R_{on,sp}$ (Ω·mm)	BV (V)
0	-40	0.425	18.8	7.8	48
110	-6.2	0.122	28.6	11.9	447
115	-4.37	0.107	30.4	12.7	426
120	-0.98	0.092	32.6	13.6	440
125	-0.05	0.078	35.5	14.8	449
130	0.74	0.065	42.5	17.7	488
135	1.53	0.052	50.0	20.8	488
140	2.07	0.039	80.2	33.4	488
145	2.54	0.030	219.8	91.6	488

The differential specific on-resistance ($R_{on,sp}$) near V_D = 0 V normalized to the area and length of the channel are scaled on the left and right axis of Figure 7 (b), respectively. As Gr grows deeper, $R_{on,sp}$ increases since the drain current gets smaller. Among the transistors from Gr = 130 nm to Gr = 145 nm with positive V_T, the one with Gr = 130 nm obtains the lowest $R_{on,sp}$ of 42.5 mΩ·cm² or 17.7 Ω·mm, which is smaller than 135 mΩ·cm² reported in the E-mode planar gate β-Ga_2O_3 MOSFET [24]. The BV for different gate recesses is presented in Figure 7 (c). Trench gate recess makes BV jumps from 48 V of the D-mode planar gate structure (Gr = 0 nm) to over 440 V at Gr = 110 nm, and reaches a stable value of 488 V for Gr ≥ 130 nm for an E-mode operation, which is larger than the BV of 263 V reported in the E-mode planar gate β-Ga_2O_3 MOSFET [24], and the off-state breakdown I-V characteristic at V_G = 0 V with Gr = 130 nm is shown in Figure 7 (d). Figure 9 presents the electric field distribution at V_G = 0 V and V_D = 487 V for the transistor with Gr = 130 nm. The electric field near the Al_2O_3/β-Ga_2O_3 interface above the current aperture shown in Figure 9 (a) is 1.8 MV/cm and 1.7 MV/cm in Al_2O_3 and β-Ga_2O_3 respectively, half of those of the D-mode MOSFET shown in Figure 5 (a). The high electric field of 5.1 MV/cm under the planar gate edge of the D-mode MOSFET shown in Figure 5 (b) is alleviated to 0.4 MV/cm at the trench bottom corner shown in Figure 9 (b). The reduction of the electric field leads to an enhancement of the breakdown voltage and a decrease in the hot electron effect.

B. EFFECT OF CHANNEL DOPING CONCENTRATION

The transfer characteristics of the trench gate β-Ga_2O_3 MOSFET with Gr = 130 nm at different channel doping concentrations (N_{ch}) are shown in Figure 10 (a). The threshold voltage and the $R_{on,sp}$ near V_D = 0 V decrease as N_{ch} increases. The transistors with $N_{ch} \geq 2 \times 10^{18}$ cm^{-3} operate in D-mode due to more electrons in the channel, and a higher drain current causes lower $R_{on,sp}$. As shown in Figure 10 (c), a small $R_{on,sp}$ = 26.3 mΩ·cm² was obtained for the device with $N_{ch} = 3 \times 10^{18}$ cm^{-3}. The transistors with N_{ch} lower than 2×10^{18} cm^{-3} operate in E-mode with higher V_T, but when N_{ch} decreases to 2×10^{17} cm^{-3}, $R_{on,sp}$ sharply increases to over 500 mΩ·cm² owing to the abruptly dropped

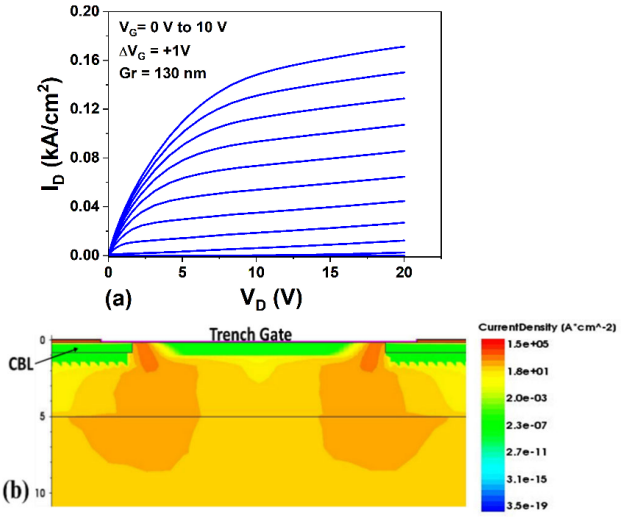

FIGURE 8. (a) Output characteristics and (b) current density at V_D = 20 V, V_G = 5 V of β-Ga_2O_3 MOSFET at Gr = 130 nm.

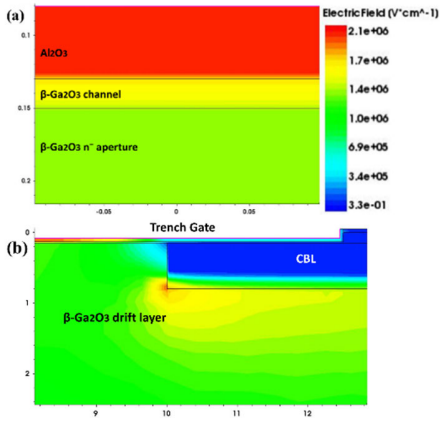

FIGURE 9. Electric field distribution (a) above the aperture and (b) at the trench gate bottom corner of β-Ga_2O_3 MOSFET with Gr = 130 nm at V_G = 0 V and V_D = 487 V.

drain current. As discussed in the previous subsection *A*, the trench gate β-Ga_2O_3 MOSFET at Gr = 130 nm with N_{ch} = 1.1 × 10^{18} cm^{-3} operates in E-mode with V_T = 0.74 V and $R_{on,sp}$ = 42.5 mΩ·cm^2. This threshold voltage was obtained by the linear extrapolation of the transfer curve to the V_G axis. Another method to define the threshold voltage is $V_T = V_G$ at $I_D = I_{on}/10^5$ [24], and a V_T of 0.31 V was obtained for this transistor. Figure 10 (b) shows the on/off current ratio (I_{on}/I_{off}) greater than 10^8 with an off-state I_D = 0.21 μA/cm^2, and this normally off trench gate β-Ga_2O_3 MOSFET can be used as a power switching device.

C. EFFECT OF CURRENT APERTURE LENGTH

Figure 11 illustrates the dependence of the DC performance of the trench gate β-Ga_2O_3 MOSFET on the length of the current aperture (L_{ap}) with Gr = 130 nm and the length of the trench gate (L_g) fixed at 25 μm. As L_{ap} increases

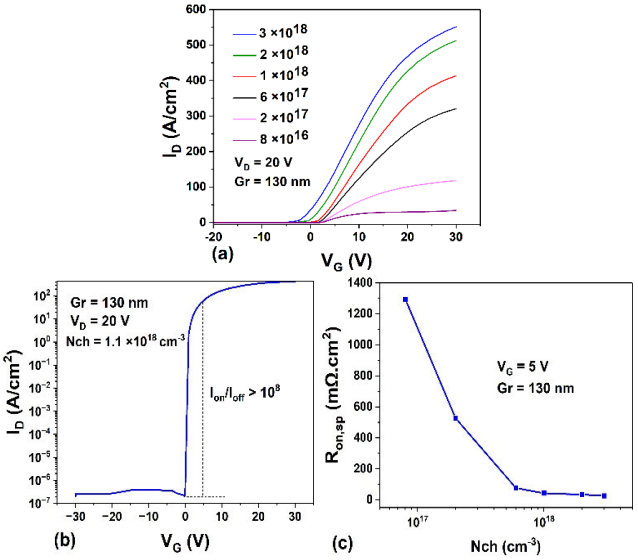

FIGURE 10. (a) (b) Transfer characteristics and (c) $R_{on,sp}$ of the trench gate β-Ga_2O_3 MOSFET with Gr = 130 nm at different channel doping concentration.

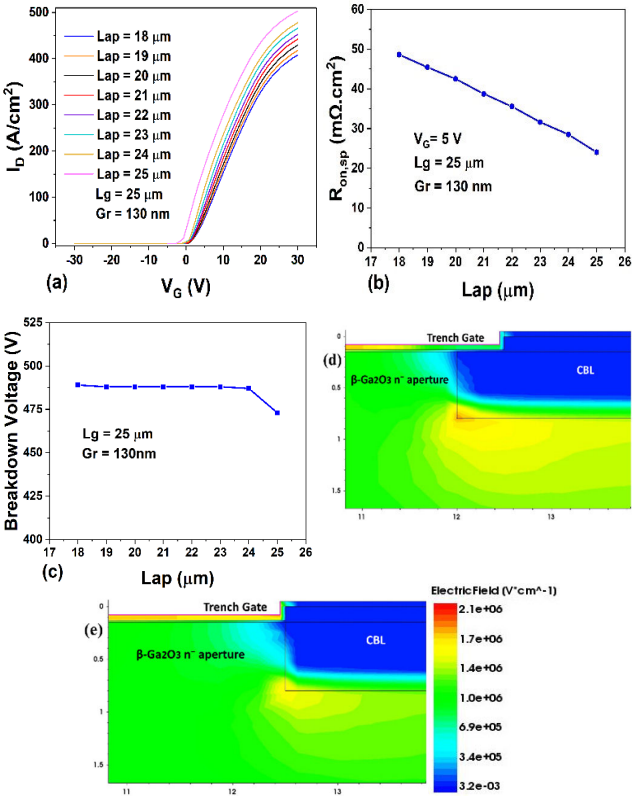

FIGURE 11. (a) Transfer characteristics, (b) $R_{on,sp}$ and (c) BV at different L_{ap}. Electric field at the trench gate bottom corner of (d) L_{ap} = 24 μm at V_G = -1 V and V_D = 487 V, and (e) L_{ap} = 25 μm at V_G = − 3 V and V_D = 470 V.

from 18 μm to 25 μm, the gate–CBL overlap length (L_{go}), as denoted in Figure 1, decreases from 3.5 μm to 0 μm. Figure 11 (a) presents a stable E-mode transfer characteristic in the L_{ap} range of 18 μm to 21 μm. The transistor turns to

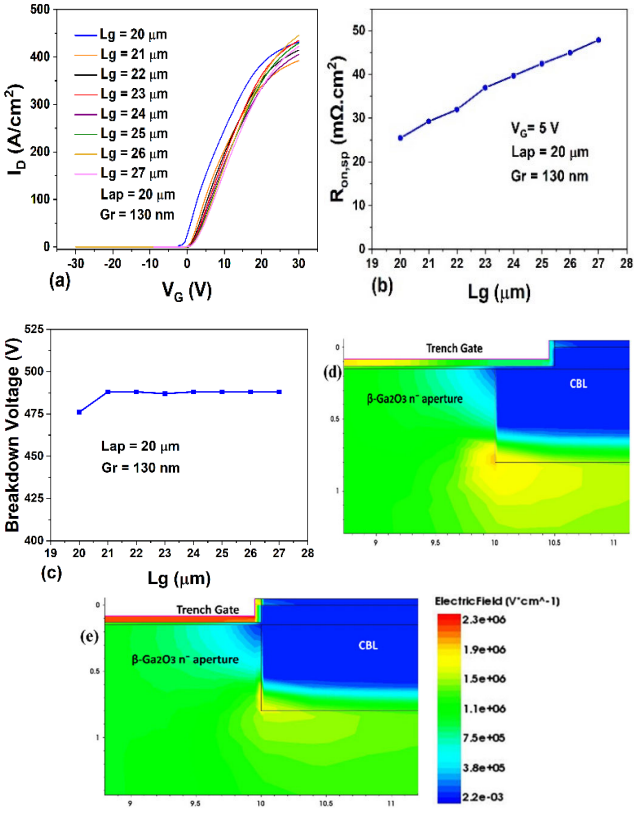

FIGURE 12. (a) Transfer characteristics, (b) $R_{on,sp}$ and (c) BV at different L_g. Electric field at the trench gate bottom corner of (d) $L_g = 21\ \mu m$ at $V_G = 0$ V and $V_D = 487$ V, and (e) $L_g = 20\ \mu m$ at $V_G = -4$ V and $V_D = 470$ V.

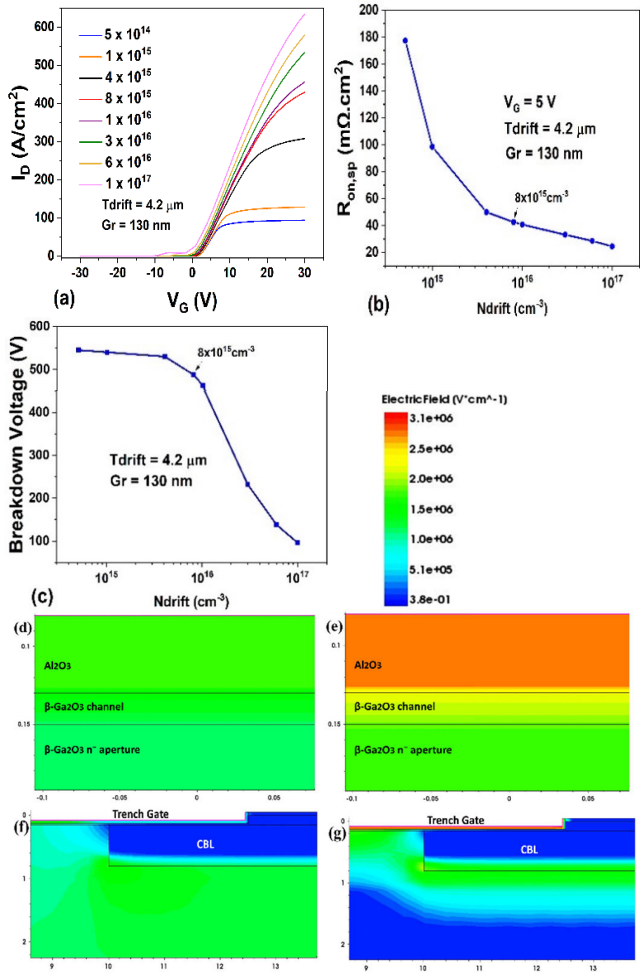

FIGURE 13. (a) Transfer characteristics, (b) $R_{on,sp}$ and (c) BV at different N_{drift}. Electric field distribution above the aperture for (d) $N_{drift} = 5\times10^{14}$ cm^{-3} at $V_G = 1$ V and $V_D = 540$ V, and (e) $N_{drift} = 1\times10^{17}$ cm^{-3} at $V_G = -11$ V and $V_D = 95$ V. Electric field distribution at the trench gate bottom corner for (f) $N_{drift} = 5\times10^{14}$ cm^{-3} at $V_G = 1$ V and $V_D = 540$ V, and (g) $N_{drift} = 1\times10^{17}$ cm^{-3} at $V_G = -11$ V and $V_D = 95$ V.

D-mode operation when L_{ap} is greater than 21 μm because of the wider current path in the aperture. Consequently, $R_{on,sp}$ becomes smaller with increasing L_{ap}, and the value of $R_{on,sp}$ decreases from 48.6 m$\Omega\cdot$cm^2 at $L_{ap} = 18\ \mu$m to 24.1 m$\Omega\cdot$cm^2 at $L_{ap} = 25\ \mu$m as shown in Figure 11 (b). The influence of L_{ap} on BV is shown in Figure 11 (c). The BV keeps a value of 488 V from $L_{ap} = 18\ \mu$m to $L_{ap} = 24\ \mu$m and drops to 473 V at $L_{ap} = 25\ \mu$m because the electric field at the trench bottom corner increases from 0.8 MV/cm to 1.7 MV/cm as shown in Figure 11 (d) and (e) respectively. Based on the simulation results, L_{ap} from 18 μm to 21 μm can be considered for the design of E-mode operation for the trench gate β-Ga_2O_3 MOSFET with Gr = 130 nm and $L_g = 25\ \mu$m.

D. EFFECT OF TRENCH GATE LENGTH

The effect of the length of the trench gate on the DC performance of the β-Ga_2O_3 MOSFET with Gr = 130 nm and $L_{ap} = 20\ \mu$m is shown in Figure 12. When L_g increases from 20 μm to 27 μm, L_{go} increases from 0 μm to 3.5 μm. The threshold voltage of the trench gate β-Ga_2O_3 MOSFET has a small dependence on L_g in the range of 21 μm to 27 μm as shown in Figure 12 (a), and the transistor keeps in E-mode operation. At $L_g = 20\ \mu$m or $L_{go} = 0\ \mu$m, the gate-CBL overlap decreases to zero resulting in a wider current path similar to the case in subsection *C*, and the transistor operates in D-mode for this gate length. Accordingly, $R_{on,sp}$ turns larger with increasing L_g, and the value of $R_{on,sp}$ raises from 25.5 m$\Omega\cdot$cm^2 at $L_g = 20\ \mu$m to 47.9 m$\Omega\cdot$cm^2 at $L_g = 27\ \mu$m as shown in Figure 12 (b). The BV shown in Figure 12 (c) exhibits less dependence on L_g in the range of 21 μm to 27 μm with BV = 488 V. At $L_g = 20\ \mu$m, the BV drops to 475 V since the electric field at the trench bottom corner increases from 0.8 MV/cm at $L_g = 21\ \mu$m to 2 MV/cm at $L_g = 20\ \mu$m as shown in Figure 12 (d) and (e) respectively. Based on the above results, L_g from 21 μm to 27 μm can be considered for the design of E-mode operation for the trench gate β-Ga_2O_3 MOSFET with Gr = 130 nm and $L_{ap} = 20\ \mu$m.

E. EFFECT OF DOPING CONCENTRATION OF DRIFT LAYER

The influence of the drift layer doping concentration (N_{drift}) on the transfer characteristics is investigated and presented in Figure 13 (a) for the trench gate β-Ga_2O_3 MOSFET with Gr = 130 nm and the thickness of drift layer (T_{drift}) of 4.2 μm,

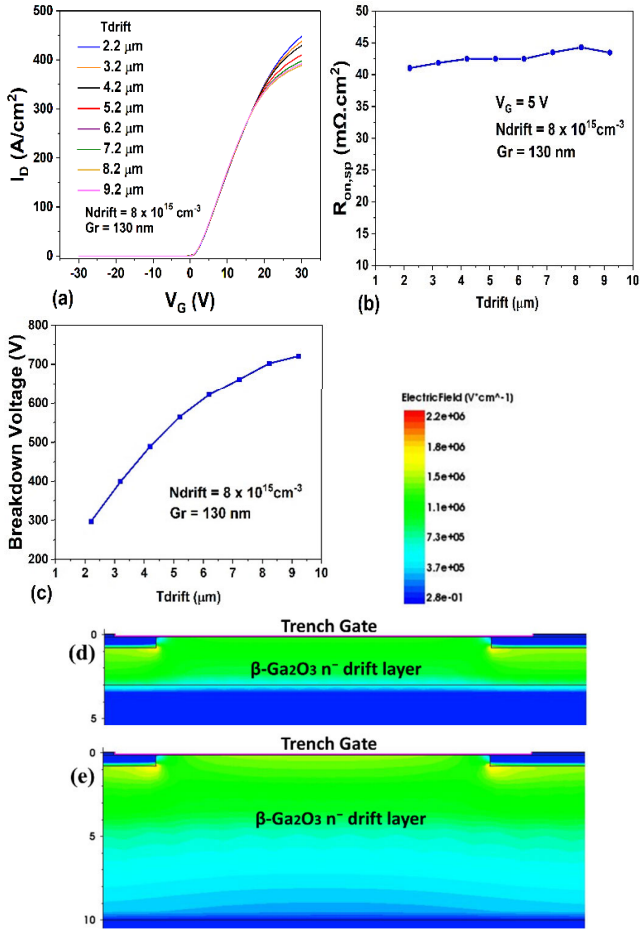

FIGURE 14. (a) Transfer characteristics, (b) $R_{on,sp}$ and (c) BV at different T_{drift}. Electric field distribution for (d) T_{drift} = 2.2 μm at V_G = 0 V and V_D = 295 V, and (e) T_{drift} = 9.2 μm at V_G = 0 V and V_D = 720 V.

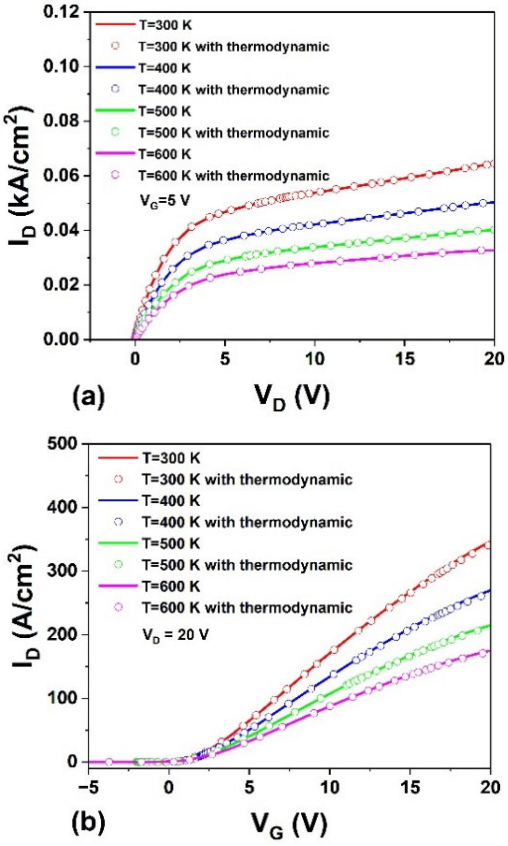

FIGURE 15. (a) Output and (b) transfer characteristics of trench gate β-Ga_2O_3 MOSFET with Gr = 130 nm at different temperatures.

the threshold voltage decreases as N_{drift} increases, and maintains positive with $N_{drift} < 1 \times 10^{16}$ cm^{-3} for an E-mode operation. $R_{on,sp}$ drops from 177.3 mΩ·cm^2 to 24.5 mΩ·cm^2 as N_{drift} increases from 5×10^{14} cm^{-3} to 1×10^{17} cm^{-3} as illustrated in Figure 13 (b) since the drain current increases. For power devices, N_{drift} and T_{drift} are important design parameters for breakdown voltage. The influence of N_{drift} on BV shown in Figure 13 (c) is expected. BV decreases as N_{drift} increases, which is similar to the case for Si, SiC [37] and GaN [38]. For the transistor with $N_{drift} = 5 \times 10^{14}$ cm^{-3}, the electric field at $V_G = 1$ V and $V_D = 540$ V above the current aperture is 1.6 MV/cm and 1.5 MV/cm in Al_2O_3 and β-Ga_2O_3 as shown in Figure 13 (d), and 0.6 MV/cm at the trench bottom corner as shown in Figure 13 (f). At $N_{drift} = 1 \times 10^{17}$ cm^{-3}, the electric field at $V_G = -11$ V and $V_D = 95$ V above the current aperture is 2.4 MV/cm and 2.2 MV/cm in Al_2O_3 and β-Ga_2O_3 as shown in Figure 13 (e), and 2.8 MV/cm at the trench bottom corner as shown in Figure 13 (g), which causes the lower breakdown voltage.

F. EFFECT OF THICKNESS OF DRIFT LAYER

The dependence of T_{drift} on DC performance and BV of the trench gate β-Ga_2O_3 MOSFET with Gr = 130 nm and $N_{drift} = 8 \times 10^{15}$ cm^{-3} is analyzed in this subsection. As T_{drift} increases, the threshold voltage shown in Figure 14 (a) is maintained at 0.74 V, and $R_{on,sp}$ illustrated in Figure 14 (b) fluctuates around 42 mΩ·cm^2. As shown in Figure 14 (c), with T_{drift}increasing from 2.2 μm to 9.2 μm, BV is improved from 296 V to 721 V. The $R_{on,sp}$ at $T_{drift} = 9.2$ μm is 43.5 mΩ·cm^2, only 1 mΩ·cm^2 higher than the $R_{on,sp}$of 42.5 mΩ·cm^2 at T_{drift} = 4.2 μm discussed in subsection *A*. The trench gate structure in the current aperture MOSFET contributes to the low $R_{on,sp}$ without increasing as the BV does. At T_{drift} = 8.2 μm, the transistor achieves the BV of 702 V and $R_{on,sp}$ of 44 mΩ·cm^2, surpassing the BV of 263 V and $R_{on,sp}$ of 135 mΩ·cm^2 with the same drift layer thickness reported in the E-mode planar gate β-Ga_2O_3 MOSFET [24]. The electric field distribution for T_{drift} = 2.2 μm at $V_G = 0$ V and $V_D = 295$ V and $T_{drift} = 9.2$ μm at $V_G = 0$ V and $V_D = 720$ V are presented in Figure 14 (d) and (e), respectively. The growth of the thickness of the drift layer increases the depletion width, causing an increase in the breakdown voltage [37].

G. EFFECT OF TEMPETURE

β-Ga_2O_3 is a significant semiconductor material for high-temperature electronics. A low intrinsic carrier concentration

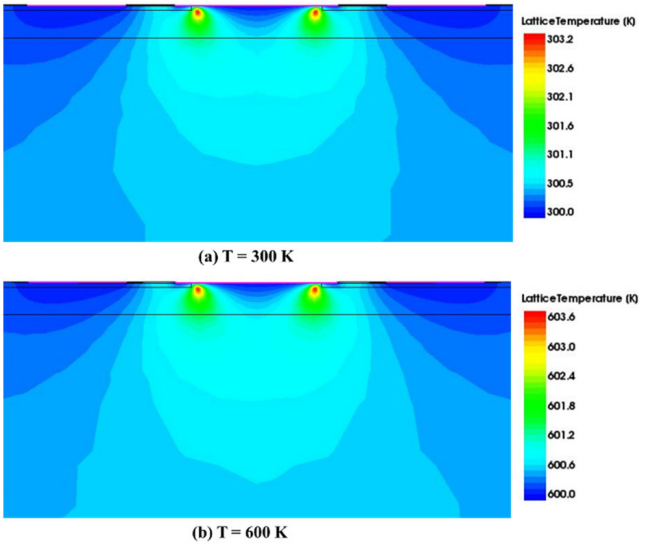

FIGURE 16. Lattice temperature distribution at (a) T = 300 K and (b) T = 600 K in the trench gate β-Ga_2O_3 MOSFET with Gr = 130 nm at V_G = 5 V and V_D = 20 V.

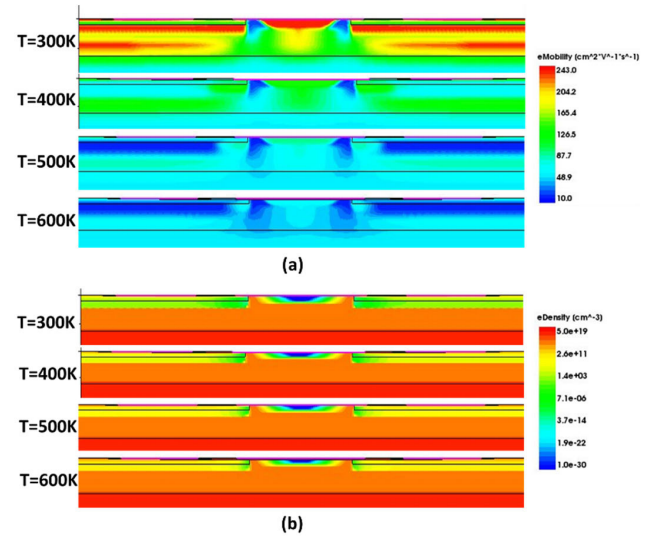

FIGURE 17. (a) Electron mobility and (b) electron density distribution at T = 300 K, 400 K, 500 K and 600 K.

in β-Ga_2O_3 at high temperatures sustains the modulation capability of transistors. The temperature-dependent performance of the proposed trench gate β-Ga_2O_3 MOSFET is investigated in this subsection. The low thermal conductivity of β-Ga_2O_3 is in the range of 11–27 W/mK at room temperature [39], [40]. In this work, 14.7 W/mK in the direction [001] was used, and at high temperatures, the thermal conductivity follows a $\sim$ 1/T relationship [39]. Figure 15 illustrates the output and transfer characteristics of the trench gate β-Ga_2O_3 MOSFET with Gr = 130 nm at different temperatures. At V_G = 5 V and V_D = 20 V, the simulation results with the thermal conductivity used in the thermodynamic model are the same as those without considering the effect of thermal exchange, because the temperature-dependent electron mobility model works dominantly, and the maximum lattice temperatures in the device caused by self-heating at V_D = 20 V are only three degrees higher than the minimum ones both for T = 300 K and T = 600 K as shown in Figure 16. The maximum temperatures exist at the edge of the CBLs owing to the electric field spreading through the structure. When the temperature increases, the drain current decreases due to the reduced electron mobility displayed in the color contour of Figure 17 (a). At the elevated temperature, the increased phonon concentration results in increased carrier scattering, which lowers electron mobility. Consequently, the electron density slightly increases at the high temperature as shown in Figure 17 (b), and $R_{on,sp}$ increases from 42.5 mΩ·cm^2 at T = 300 K to 94.7 mΩ·cm^2 at T = 600 K. The threshold voltage shown in Figure 15 (b) slightly decreases from 0.74 V at T = 300 K to 0.65 V at T = 400 K, and the device keeps E-mode operation at T = 500 K with V_T = 0.42 V. At T = 600 K, the transistor goes into D-mode operation with $V_T = -0.09$ V.

V. CONCLUSION

Trench Gate β-Ga_2O_3 current aperture vertical power MOSFETs were designed and investigated using Sentaurus TCAD simulation in this article. The effect of different device parameters, such as trench gate depth, channel doping concentration, and drift layer doping concentration and thickness, on the DC performance of the transistors were presented and analyzed to provide more design space for the trench gate β-Ga_2O_3 MOSFET. The transistor with Gr = 130 nm obtains a BV of 488 V, an on-current density I_D of 65 A/cm^2, a $R_{on,sp}$ of 42.5 mΩ·cm^2, a high I_{on}/I_{off} of 10^8, and a V_T of 0.74 V for an E-mode operation. With T_{drift}increasing to 9.2 μm, BV is improved to 721 V, $R_{on,sp}$ is 43.5 mΩ·cm^2, only 1 mΩ·cm^2 higher than the $R_{on,sp}$at T_{drift} = 4.2 μm, and the transfer characteristic keeps the same. The thermal performance of the trench gate β-Ga_2O_3 MOSFET with Gr = 130 nm was investigated, and the transistor still works in E-mode operation at T = 500 K. The trench gate technique was proved effective in implementing E-mode operation in the vertical β-Ga_2O_3 power MOSFET, and the performance of the transistors shows its potential as a high voltage power switching device.

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