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RESEARCH ARTICLE

A Soft-Switched Boost Converter Based LED Driver With Reduced Input Current Ripple

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ABSTRACT This paper proposes a soft-switched paralleled boost converter based LED driver for street lighting application. Output of paralleled boost converter (BC) in the form of full-bridge feeds a buck-boost converter (BBC). The outputs of paralleled BC and BBC are added to power LED lamps. The paralleled boost converters help in reducing the source current ripple with small inductors and also can handle large power. Regulation of the load voltage is achieved by BBC which handles small power without significantly affecting the overall efficiency. Soft switching of the devices in boost converters is achieved with a ZVS inductor resulting in high efficiency. PWM based dimming control is employed. The LED driver can be fed from batteries, ultra-capacitor, etc. A prototype of 65 W DC-DC converter for LED lighting is developed. The experimental results are in good agreement with simulation results. The proposed converter offers high efficiency of 93.42%, reduced source current ripple, and dimming control. Efficiency of the proposed converter with SiC MOSFETs is around 95% at all voltage variations.

INDEX TERMS Synchronous boost converter, ripple cancellation, synchronous rectification, zero voltage switching, LED lighting, buck-boost converter, lighting control, LED driver.

I. INTRODUCTION

Illumination with LEDs is becoming very common for various applications. In comparison to the conventional lighting sources, LEDs offer numerous advantages. It includes long life time, fast response, saving in energy and environment friendly. LEDs are shock resistant and offer wide chromatic variety. Now-a-days, LEDs are used in residential lighting, traffic signaling, emergency lighting systems, automotive lights, etc [1], [2].

Most of the LED drivers proposed in the recent years include powering LEDs from ac mains [3], [4], and DC supply which include renewable sources [5], [6], [7], automotive applications [8], [9] and batteries [10]. The life time of LED is high. Hence, LED drivers without electrolytic capacitors are preferred which results in higher reliability [11]. AC powered LED drivers are available as single-stage, two-stage or integrated converter topologies. In general, they consist of a rectifier circuit followed by one or more DC-DC converters. Single-stage LED drivers use a DC-DC converter which provides output current regulation and power factor correction (PFC). Two-stage LED drivers consist of a PFC circuit and a DC-DC converter. In integrated LED drivers, one or more switching devices of PFC and DC-DC converter circuits are shared, to reduce component count, cost and size of the converter [12].

DC powered LED drivers are using single-stage, two-stage or partial power-stage configurations. DC-DC converter based current regulators are used in single-stage LED drivers. In two-stage converters two DC-DC converters are connected in cascade. First converter supplies regulated dc voltage to second converter. Second converter regulates the current in LED load. The overall efficiency of this type of LED driver is reduced due to cascade connection of the converters. Component count, size and cost of the system are increased [13], [14]. In partial power-stage configuration, two converters are used. One of the converters processes larger portion of the output power whereas the other converter handles a smaller portion of it and provides output voltage regulation. An LED driver based on fly-back converter has been proposed in [15].

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LED load is connected across fly-back converter and a dc source which are connected in series. Hence, the dc source supplies major portion of the output voltage. Whereas the converter processes less power to regulate the load current. Hence the losses in the converter are reduced and the driver efficiency is improved. However, during low and medium power operation the efficiency of the driver is reduced. LED load is connected across this series combination. In [16], a Switched capacitor Boost hybrid serial output LED driver has been proposed. Boost converter and switched-capacitor converters assembly are providing the output voltage. About 50% of the power is handled by switched-capacitor converter and boost converter handles remaining power to regulate the output voltage.

Boost converter is useful in increasing operating voltage of LEDs to higher value, when the source is battery, DC micro-grid or ultra-capacitors. This is helpful in reducing the total load current for a given output power. Interleaved operation is useful in higher power applications. It provides high efficiency and lower complexity. Interleaving also lowers ripple in input current and output voltage. This also results in reduction in size of passive components with ripple cancellation [17]. Effective frequency is doubled and reliability is increased by distribution of power losses evenly. Also, it is modular in nature, based on the necessity, additional converters can be added in parallel. In the recent times, many LED drivers with interleaved operation of DC-DC converters are presented [18], [19], [20], [21]. Lossless switching based converters can be used to replace hard switched converters. Soft switching enables increasing switching frequency and will reduce the converter volume and weight. Interleaved boost converters (IBC) are used in some LED drivers. The performance of IBC with soft switching overcomes the drawbacks of a traditional boost converter [22], [23]. Despite this, boost diode conduction loss still occurs, lowering the power conversion efficiency. Hence instead of using a diode, synchronous rectifier is proposed in [24].

Use of LEDs for street lighting offers reduced electric energy consumption, improved light quality and life span of lamps. LEDs are suitable for battery / ultra-capacitor fed street lighting system, due to their superior energy efficiency, lower operating voltage, higher luminous efficiency and compactness.

Desirable features of a DC powered street lighting LED system are:

a) multiple outputs
b) relatively larger power
c) reduced component count
d) high efficiency
e) dimming operation for energy efficiency and
f) load current regulation.

In this paper, a DC-DC converter topology suitable for battery fed street lighting LED system is presented. This topology consists of a DC-DC full-bridge paralleled boost converter (FBPBC) along with buck-boost converter at the output stage for regulation of LED current. Proposed converter offers ZVS operation of devices of both boost converters. Parallel operation enables input ripple current cancellation. It provides dimming control, output voltage regulation and increased efficiency due to reduced losses. Since, source ripple current cancellation can be achieved, this converter can be operated from battery with better performance. In this paper, the source is taken as a battery. By reducing the source current ripple, the battery performance will also be improved.

The salient features of the proposed LED Driver are:

a) ZVS operation of boost converters
b) Input ripple cancellation
c) Dimming control
d) High efficiency and
e) Output current regulation

The organization of the paper is as follows: Section II describes the proposed converter configuration, operating principle and modes of operation. Section III describes detailed analysis and Section IV describes control and design aspects. The dimming of LED lamp is discussed in Section V. Section VI presents simulation and experimental results. Section VII presents major conclusions.

II. PROPOSED LED DRIVER CIRCUIT

Fig. 1*a* shows the proposed converter circuit for powering LEDs for street lighting application. It consists of a full-bridge two phase synchronous boost converter operated in parallel and a buck-boost converter (BBC). It comprises of dc source (V_{DC}), five MOSFETs (S_1, S_2, S_{d1}, S_{d2}, and S_{bb}), diode D_3, inductors L, L_1 and L_2 and capacitors C_{o1} and C_{o2}. D_1, D_2, D_{d1} and D_{d2} are body diodes of S_1, S_2, S_{d1} and S_{d2} respectively. C_1, C_2, C_{d1} and C_{d2} are output capacitors of S_1, S_2, S_{d1} and S_{d2} respectively.

The full-bridge has two synchronous boost converters (SBC) operated in parallel at a phase shift of 180^0 with a fixed duty cycle of 0.5. L_1, S_1 and S_{d1} are forming one SBC whereas L_2, S_2 and S_{d2} form another SBC. Components used in each converter are identical in order to obtain interleaving operation. Gate pulses of S_1 and S_{d1} are complementary to each other. Similarly, gate pulses of S_2 and S_{d2} are complementary to each other. Auxiliary inductor 'L' is connected between two legs of FBPBC to incorporate soft-switching for reducing switching losses in S_1, S_{d1}, S_2 and S_{d2}. Filter capacitor 'C_{o1}' is connected at the output of full-bridge converter (FBPBC). V_{o1} is the output voltage of full-bridge boost converter which is fed to BBC which consists of L_3, S_{bb}, D_1 and output filter capacitor C_{o2}. V_{o2} is the output voltage of BBC.

LED lamp load is connected across positive output terminal of FBPBC and negative output terminal of BBC as shown in Fig. 1*a*. LED lamp is formed by connecting two LED strings in parallel. Each string consists of 20 LEDs in series. PWM dimming is employed to control the illumination level. V_o is the LED lamp voltage. Due to polarity reversal nature of BBC, output voltages of FBPBC and BBC are added and LED lamp voltage is given as $V_o = V_{o1} + V_{o2}$.

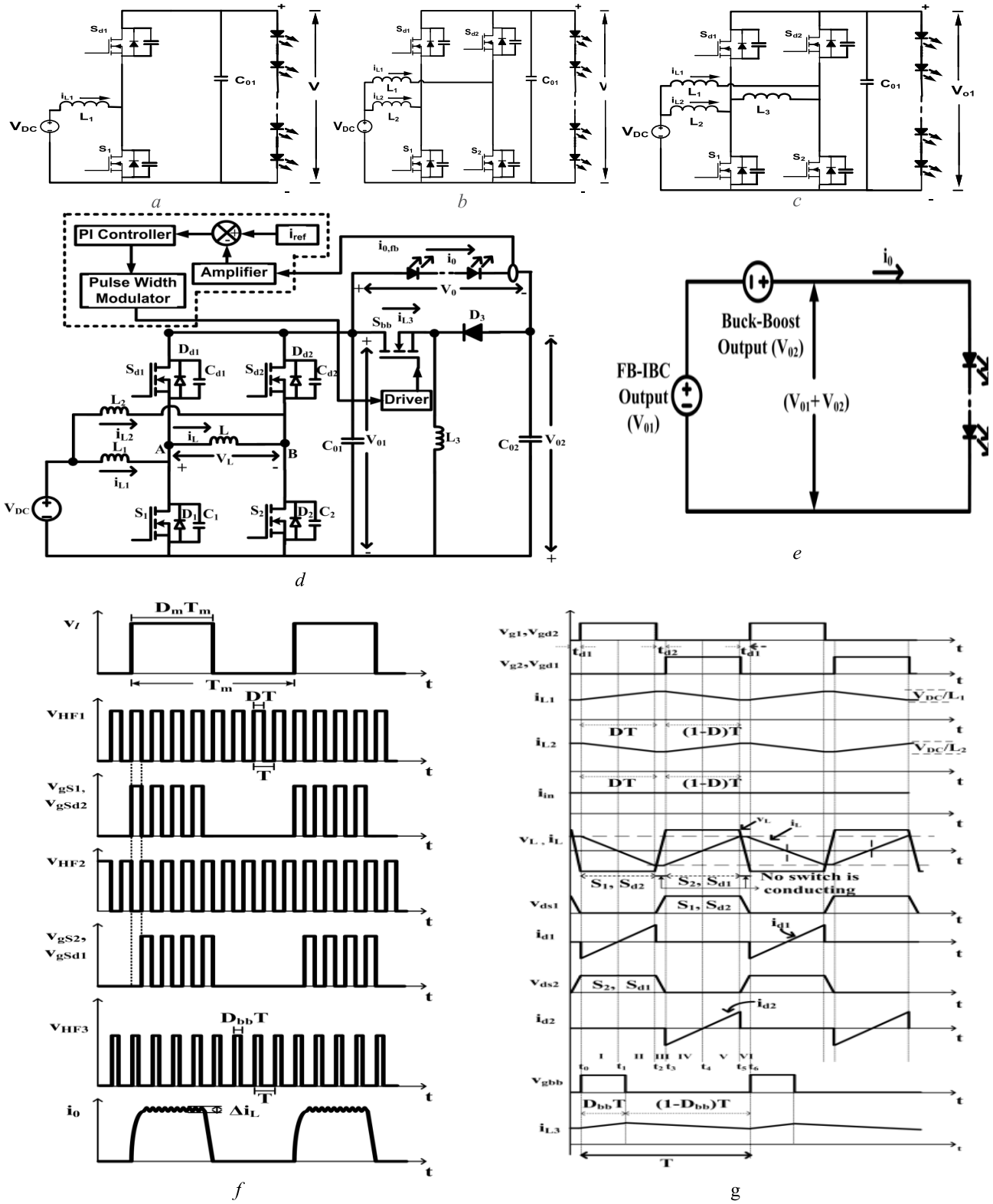

FIGURE 1. Proposed Converter Configuration and waveforms (a-c) Development of fundamental structure of proposed LED Driver (d)Proposed FBPBC based LED Driver (e) Equivalent circuit (f) Gate pulses with dimming control and LED lamp current (g) Operating waveforms.

Hence, the proposed LED driver is represented with the equivalent circuit shown in Fig. 1*b*. The development of proposed LED driver is shown in Fig. 1*a*. Output voltage V_o is represented as the addition of voltages supplied by two voltage sources representing the output voltage of FBPBC (V_{o1}) and BBC (V_{o2}) respectively. V_{o1} supplies major portion of the output voltage to the LED load and V_{o2} is utilized in regulating the LED voltage by compensating

the variation in output voltage due to supply voltage fluctuations.

V_{o2} is controlled by adjusting duty-ratio of BBC switch S_{bb}. Dimming control waveforms and operating waveforms of the proposed converter are presented in Fig. 1f and Fig. 1g respectively.

Fig. 1*f* illustrates the DPWM control scheme. The control signals of FBPBC and buck-boost converter are synchronised with that of a low frequency signal. As illustrated in Fig. 1*f*, the pulses to switches S_1- S_{d2}, S_2- S_{d1} are obtained by combining a low frequency (200 Hz) pulse v_l with the high frequency (100 kHz) pulses v_{HF1} and v_{HF2} respectively. And, v_{HF3} and v_l are used to control the switch S_{bb}. FBPBC and buck-boost converter are turned-off during off duration of the low frequency pulse. During this time, LED turns-off and powered again in next cycle when switches are switched-on. Low frequency PWM controls the average LED current to control LED brightness.

High frequency PWM controls the current in LED lamp. Dimming is achieved from 20% to 80% by varying the on-period of low frequency signal. Total average load current of LEDs is varied from 200 mA to 1A. The LED dimming regulation is shown in Fig. 1*f*.

In each working cycle, the synchronous full-bridge IBC operates in six different modes. Equivalent circuits for various modes are presented in Figs. 2 and 3. Modes of operation for S_1-ON and S_2-ON are explained in detail in this section. Energy flow from input (V_{DC}) to output by switching S_1 and S_2 alternately along with S_{d2} and S_{d1} respectively is explained.

A. S_1 AND S_{d2} ARE ON

1) MODE - I (t_0- t_1)

Switches S_1, S_{d2} are turned-on with ZVS at instant t_0. Inductor L_1 starts energizing and the current i_{L1} through L_1 increases linearly. Inductor L_2 is de-energized and current i_{L2} through it decreases linearly with the same slope. During this interval, voltage across ZVS inductor L, $V_L = -V_{o1}$ and current i_L decreases. Current in S_1, $i_{S1} = i_{L1} - i_L$, which is small. Power is transferred to the output from the source through L_2 and S_{d2}. S_{d2} conducts a current which is sum of i_L and i_{L2} i.e., $-(i_L + i_{L2})$. When $i_L = 0$, this mode is completed.

2) MODE - II (t_1- t_2)

S_1 and S_{d2} are on and S_2 and S_{d1} are off in this interval. The current i_L through ZVS inductor decreases linearly to negative from zero. i_{L1} continues to increase linearly to peak value until S_1 and S_{d2} are turned-off. Similarly, i_{L2} continues to decrease linearly to minimum value. At instant t_2, this mode ends.

3) MODE - III (t_2- t_3)

S_1 and S_{d2} are turned-off at zero voltage. During this interval, all switches are in off-state. $\frac{(i_{L1}+i_L)}{2}$ charges C_1(output capacitor of S_1) and discharges C_{d1}. $\frac{(i_L - i_{L2})}{2}$ charges C_{d2} and discharges S_2. Body diodes of S_2 and S_{d1} conduct. S_2 and S_{d1} are switched-on with ZVS. Current in inductor L_1 decreases linearly and current in inductor L_2 increases linearly. Capacitor C_2 discharges from V_{DC} to 0; C_{d1} discharges from V_{o1} to 0 and C_1 charges from 0 to V_{DC}; C_{d2} charges from 0 to V_{o1}.

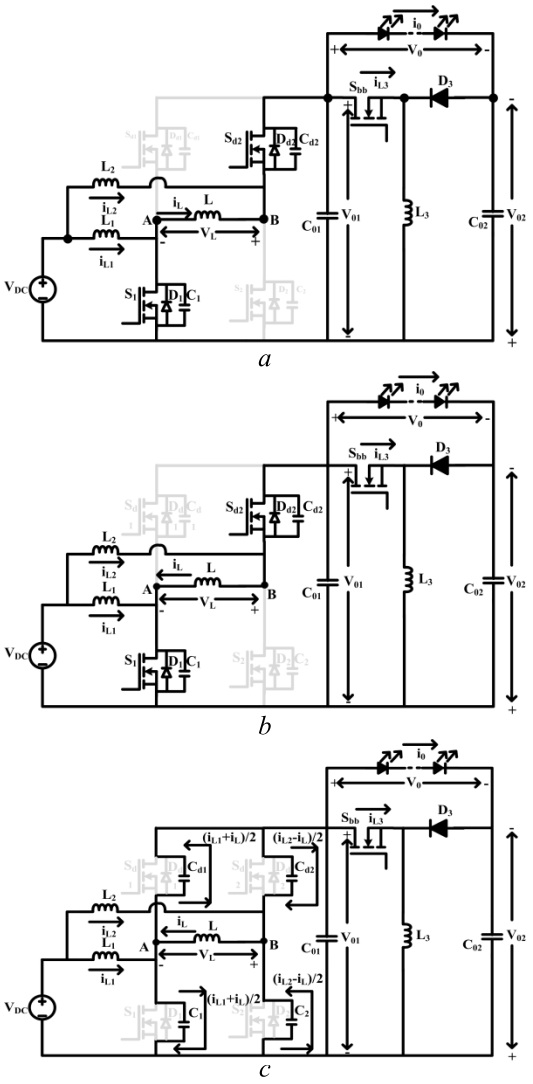

FIGURE 2. Equivalent circuits when S_1 is ON (a) Mode-I (b) Mode-II (c) Mode-III.

B. S_2 AND S_{d1} ARE ON

1) MODE - IV (t_3- t_4)

S_2, S_{d1} are turned-on with ZVS at instant t_3. Inductor L_2 is energized and i_{L2} increases linearly. Inductor L_1 is de-energized and i_{L1} decreases linearly with the same slope. voltage across ZVS inductor L, $V_L = +V_{o1}$ and current i_L increases through S_2. Current $(i_{L2}+i_L)$ flows through S_2 which is small. Power is transferred to the output from the source through L_1 and S_{d1}. S_{d1} conducts the difference of currents i_L and i_{L1}. When $i_L = 0$, the mode is completed.

2) MODE - V (t_4- t_5)

S_2, S_{d1} are on and S_1, S_{d2} are off. This mode of operation is similar to Mode-IV. But, the current, i_L through ZVS

inductor increases linearly to positive from zero. Current i_{L2} continuous to increase linearly to peak value until S_2, S_{d1} are turned-off. Similarly, i_{L1} continues to decrease linearly to minimum value. At t_5, this mode is completed.

3) MODE - VI (t_5- t_6)

S_2 and S_{d1} are turned-off at zero voltage. During this interval, all switches are in off state. $\frac{(i_{L2}+i_L)}{2}$ charges C_2 and discharges C_{d2}, $\frac{(i_L-i_{L1})}{2}$ charges C_{d1} and discharges C_1. Body diodes of S_1 and S_{d2} start conducting. S_1 and S_{d2} are switched-on with ZVS. The current in inductor L_2 starts decreasing linearly and current in inductor L_1 starts increasing linearly. Capacitors C_1 and C_{d2} discharge from V_{o1} to 0 and capacitors C_2 and C_{d1} charges 0 to V_{o1}. L_2, S_{d2} and L_1, S_{d1} alternately transfer energy from the source to the output, producing voltage V_{o1} across capacitor C_{o1}. Buck-boost converter is fed from V_{o1}.

III. ANALYSIS OF THE PROPOSED CONVERTER

Converter operation is analysed during different intervals of time with the following assumptions:

1) Semiconductor switches S_1, S_2, S_{d1}, S_{d2}, S_{bb} and diodes are ideal.
2) Boost inductors L_1 and L_2 are equal.
3) Boost converters are identical. Both boost and buck-boost converters are operating in CCM.
4) Output capacitors C_{o1} and C_{o2} are of large values resulting in negligible output voltage ripple.

A. During (t_0-t_2)

The LED lamp is powered from both voltages V_{o1} and V_{o2}. When S_1 and S_{d2} are switched on, current flows through the path $V_{DC}^{+}\rightarrow L_2 \rightarrow S_{d2}\rightarrow C_{01}\rightarrow V_{DC}^{-}$. Figs. 2*a* and 2*b* show corresponding equivalent circuits that represent this duration.

Inductor L_1 voltage is

$$v_{L1} = V_{DC} = L_1\frac{di_{L1}}{dt}, \quad t_0 \le t \le t_2 \tag{1}$$

Current through L_1 is

$$\begin{aligned} i_{L1}(t) &= \frac{1}{L_1}\int_{t_0}^{t} v_{L1}(t)dt + i_{L1}(t_0) \\ &= \frac{V_{DC}}{L_1}(t-t_0) + i_{L1}(t_0), t_0 \le t < t_2 \end{aligned} \tag{2}$$

At $t = t_0$, inductor current is $i_{L1}(t_0)$. $i_{L1}(t)$ reaches its maximum value at $t = t_2$, i.e.,

$$i_{L1}(t_2) = \frac{V_{DC}}{L_1}(t_2-t_0) + i_{L1}(t_0) \tag{3}$$

S_1 is on for a period of ($t_2 - t_0$). Hence, it is written from (3) as

$$i_{L1}(t_2) = \frac{V_{DC}}{L_1}DT + i_{L1}(t_0) \tag{4}$$

where 'T' is switching period and 'D' is the duty ratio of S_1.

Current ripple in L_1 is calculated using (4) as

$$\Delta i_{L1} = i_{L1}(t_2) - i_{L1}(t_0) = \frac{V_{DC}}{L_1}DT \tag{5}$$

Voltage across inductor L_2 is calculated as

$$v_{L2} = V_{DC} - V_{o1} = L_2\frac{di_{L2}}{dt}, t_0 \le t < t_2 \tag{6}$$

where V_{o1} is output voltage of FBPBC.

Current through inductor L_2 is calculated as follows

$$\begin{aligned} i_{L2}(t) &= \frac{1}{L_2}\int_{t_0}^{t} v_{L2}(t)dt + i_{L2}(t_0) \\ &= \frac{V_{DC}-V_{o1}}{L_2}(t-t_0) + i_{L2}(t_0), t_0 \le t < t_2 \end{aligned} \tag{7}$$

At $t = t_0$, current in inductor L_2 is $i_{L2}(t_0)$. $i_{L2}(t)$ reaches its minimal value at $t = t_2$.

$$i_{L2}(t_2) = \frac{V_{DC}-V_{o1}}{L_2}(t_2-t_0) + i_{L2}(t_0) \tag{8}$$

S_{d2} is on for a period of ($t_2 - t_0$). Now, (3) can be written as

$$i_{L2}(t_2) = \frac{V_{DC}-V_{o1}}{L_2}DT + i_{L2}(t_0) \tag{9}$$

where 'T' is switching period and 'D' is the duty ratio of S_{d2}.

From (9), ripple current in inductor L_2 is given by

$$\Delta i_{L2} = i_{L2}(t_2) - i_{L2}(t_0) = \frac{V_{DC}-V_{o1}}{L_2}DT \tag{10}$$

The source current i_{DC} is expressed as

$$\begin{aligned} i_{DC}(t) &= i_{L1}(t) + i_{L2}(t) \\ &= \frac{V_{DC}}{L_1}DT + i_{L1}(t_0) + \frac{V_{DC}-V_{o1}}{L_2}DT + i_{L2}(t_0) \\ &= \left[\frac{V_{DC}}{L_1} + \frac{V_{DC}-V_{o1}}{L_2}\right]DT + i_{L1}(t_0) + i_{L2}(t_0) \end{aligned} \tag{11}$$

$i_{L1}(t_0)$ and $i_{L2}(t_0)$ can be considered as k_1 and k_2. Since L_1 and L_2 are equal, (11) can be rewritten as

$$i_{DC}(t) = \left[\frac{2V_{DC}}{L} - \frac{V_{o1}}{L}\right]DT + k_1 + k_2$$

For a duty ratio of 50%; $V_{o1} = 2V_{DC}$, hence

$$i_{DC}(t) = k_1 + k_2 \tag{12}$$

Equation (12) shows that with interleaving, source current is constant which indicates ripple cancellation.

Voltage across ZVS inductor (L), is $-V_{o1}$ during the interval. i_L decreases linearly as it approaches the negative value.

It can be expressed as

$$\begin{aligned} i_L(t) &= -\frac{V_L}{L}(t-t_0) + i_L(t_0) \\ &= -\frac{V_{o1}}{L}(t-t_0) + i_L(t_0), \quad t_0 \le t < t_2 \end{aligned} \tag{13}$$

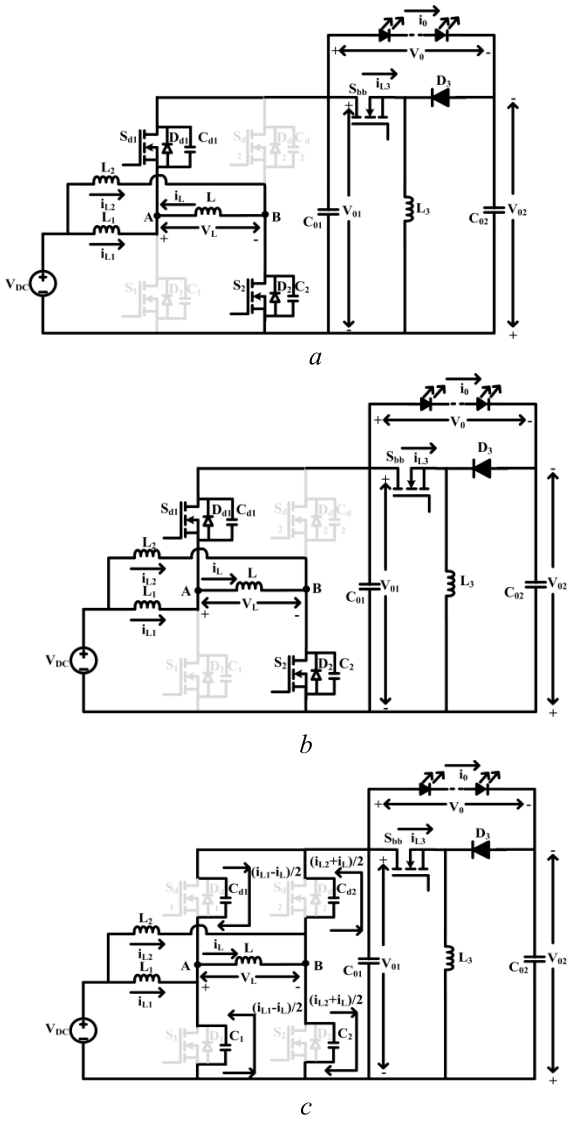

FIGURE 3. Equivalent circuits when S_2 is ON (a) Mode-IV (b) Mode-V (c) Mode-VI.

B. During (t_3 –t_5)

In this interval, S_1 & S_{d2} are switched-off. S_2 & S_{d1} are switched-on. Energy stored in inductor L_1 circulates current in path $V_{DC}^{+}\rightarrow L_1 \rightarrow S_{d1}\rightarrow C_{01}\rightarrow V_{DC}^{-}$. Equivalent circuits are depicted in Fig. 3*a* and 3*b*.

Voltage across L_1 is

$$v_{L1} = V_{DC} - V_{o1} = L_1\frac{di_{L1}}{dt}, \quad t_3 \le t < t_5 \tag{14}$$

Current in Inductor L_1 is

$$\begin{aligned} i_{L1}(t) &= \frac{1}{L_1}\int_{t_3}^{t} v_{L1}(t)dt + i_{L1}(t_3) \\ &= \frac{V_{DC}-V_{o1}}{L_1}(t-t_3) + i_{L1}(t_3), \quad t_3 \le t < t_5 \end{aligned} \tag{15}$$

$i_{L1}(t)$ reaches its minimal value at $t = t_5$.

$$i_{L1}(t_5) = \frac{V_{DC}-V_{o1}}{L_1}(t_5-t_3) + i_{L1}(t_3) \tag{16}$$

($t_5 - t_3$) is the on duration of S_2. With the assumption that dead times t_{d1} and t_{d2} are insignificant, (16) is expressed as

$$i_{L1}(t_5) = \frac{V_{DC}-V_{o1}}{L_1}(1-D)T + i_{L1}(t_3) \tag{17}$$

From (17), ripple current in L_1 is

$$\Delta i_{L1} = i_{L1}(t_5) - i_{L1}(t_3) = \frac{V_{DC}-V_{o1}}{L_1}(1-D)T \tag{18}$$

Voltage across inductor L_2 is

$$v_{L2} = V_{DC} = L_2\frac{di_{L2}}{dt}, t_3 \le t < t_5 \tag{19}$$

Current in inductor L_2 is

$$\begin{aligned} i_{L2}(t) &= \frac{1}{L_2}\int_{t_3}^{t} v_{L2}(t)dt + i_{L2}(t_3) \\ &= \frac{V_{DC}}{L_2}(t-t_3) + i_{L2}(t_3), \quad t_3 \le t < t_5 \end{aligned} \tag{20}$$

$i_{L1}(t)$ reaches its maximum value at $t = t_5$.

$$i_{L2}(t_5) = \frac{V_{DC}}{L_2}(t_5-t_3) + i_{L2}(t_3) \tag{21}$$

$$i_{L1}(t_5) = \frac{V_{DC}-V_{o1}}{L_1}(1-D)T + i_{L1}(t_3) \tag{22}$$

From (22), ripple current in inductor is

$$\Delta i_{L2} = i_{L2}(t_5) - i_{L2}(t_3) = \frac{V_{DC}}{L_2}(1-D)T \tag{23}$$

The input source current i_{DC} can be derived in similar manner as (11) and reiterated as

$$\begin{aligned} i_{DC}(t) &= i_{L1}(t) + i_{L2}(t) \\ &= \left[\frac{2V_{DC}}{L} - \frac{V_{01}}{L}\right](1-D)T + k_1 + k_2 \end{aligned} \tag{24}$$

$V_L = V_{o1}$ during the interval. Current i_L varies linearly and is written as

$$\begin{aligned} i_L(t) &= \frac{V_L}{L}(t-t_3) + i_L(t_3) \\ &= \frac{V_{o1}}{L}(t-t_3) + i_L(t_3), \quad t_3 \le t < t_5 \end{aligned} \tag{25}$$

From (5) and (10), under steady-state, the change in inductor currents i_{L1} and i_{L2} during single switching period, T, is zero.

$$[i_{L1}(t_2) - i_{L1}(t_0)] + [i_{L1}(t_5) - i_{L1}(t_3)] = 0 \tag{26}$$

(or)

$$\begin{aligned} &[i_{L2}(t_2) - i_{L2}(t_0)] + [i_{L2}(t_5) - i_{L2}(t_3)] \\ &= 0 \\ &\Rightarrow \frac{V_{DC}}{L_1}DT + \frac{V_{DC}-V_{o1}}{L_1}(1-D)T = 0 \end{aligned} \tag{27}$$

$$\Rightarrow V_{o1} = \frac{V_{DC}}{(1-D)} \tag{28}$$

Equations related to buck-boost converter can be derived as described in the following sections:

C. DURING ON-PERIOD OF S_{bb}

Voltage across inductor L_3 is expressed as

$$v_{L3} = V_{o1} = L_3 \frac{di_{L3}}{dt} \Rightarrow \frac{di_{L3}}{dt} = \frac{V_{o1}}{L_3} \tag{29}$$

Inductor current waveform is depicted in Fig. 1*c*.

Considering duty-ratio of S_{bb} as D_{bb}, (29) can be rewritten as

$$\Delta i_{L3} = \frac{V_{o1}}{L_3} D_{bb} T \tag{30}$$

D. DURING OFF-PERIOD OF S_{bb}

Voltage across inductor L_3 is expressed as

$$v_{L3} = V_{o2} = L_3 \frac{di_{L3}}{dt} \Rightarrow \frac{di_{L3}}{dt} = \frac{V_{o2}}{L_3} \tag{31}$$

Inductor current waveforms are depicted in Fig. 1*d*.

During off-time of S_{bb}, (31) can be rewritten as

$$\Delta i_{L3} = \frac{V_{o2}}{L_3}(1 - D_{bb})T \tag{32}$$

Under steady-state condition,

$$\begin{aligned} &(\Delta i_{L3})_{ON} + (\Delta i_{L3})_{OFF} \\ &= 0 \\ &\Rightarrow \frac{V_{o1}}{L_3} D_{bb} T + \frac{V_{o2}}{L_3}(1 - D_{bb})\, T = 0 \\ &\Rightarrow V_{o2} = -V_{o1}\left[\frac{D_{bb}}{(1 - D_{bb})}\right] \end{aligned} \tag{33}$$

LED load is connected across outputs of FBPBC and buck-boost converters. Hence, LED load voltage V_o is the combination of voltage supplied by FBPBC (V_{o1}) and the buck-boost converter (V_{o2}). Hence from (28) and (33)

$$V_o = V_{o1} + V_{o2} V_o = \frac{V_{DC}}{(1 - D)} + V_{o1}\left[\frac{D_{bb}}{(1 - D_{bb})}\right] \tag{34}$$

Duty-ratios of boost converters (D) are fixed at 50% to achieve source ripple current cancellation. It also steps-up the source voltage. Controlling duty ratio (D_{bb}) of buck-boost converter, regulates the LED current.

Voltage gain of FBPBC is given by

$$G_1 = \frac{V_{o1}}{V_{DC}} = \frac{1}{(1 - D)} \tag{35}$$

Voltage gain of the buck-boost converter is given by

$$G_2 = \frac{V_{o2}}{V_{o1}} = \frac{D_{bb}}{(1 - D_{bb})} \tag{36}$$

The overall gain of the proposed converter is given by

$$G = \frac{V_o}{V_{DC}} = \frac{1}{(1 - D)}\left[\frac{1}{(1 - D_{bb})}\right] \tag{37}$$

IV. DESIGN ASPECTS OF PROPOSED CONVERTER

The design of the proposed converter involves selection of power MOSFETs, inductors, and output capacitors. In a paralleled design, the inductors and power MOSFETs should be same ratings in both networks. Duty-cycle and the peak currents are to be considered for design of these components. Since, the output power of synchronous FBPBC is provided through two power paths, design of components is to be arrived by considering half the output power.

The instantaneous current of L_1 can be expressed as

$$i_{L1}(t) = \begin{cases} \frac{\Delta i_{L1}}{DT} t + I_{L1min}, & 0 \le t < DT \\ \frac{\Delta i_{L1}}{(1 - D)\, T}(t - DT) + I_{L1max}, & DT \le t < T \end{cases} \tag{38}$$

The same holds good for inductor L_2.

Instantaneous current in the switches can be expressed as

$$i_{s1}(t) = \begin{cases} i_{L1}(t) - i_L(t), & 0 \le t < DT \\ 0, & DT \le t < T \end{cases} \tag{39}$$

Hence,

$$i_{s1}(t) = \begin{cases} \frac{V_{DC}}{L_1} * t + i_{L1}(t_0) + \frac{-V_{o1}}{L} * t + i_L(t_0), \\ \qquad 0 \le t < DT \\ 0, \quad DT \le t < T \end{cases}$$

$$i_{sd1}(t) = \begin{cases} 0 & 0 \le t < DT \\ (-i_{L1}(t) + i_L(t)), & DT \le t < T \end{cases} \tag{40}$$

$$i_{s2}(t) = \begin{cases} 0, & 0 \le t < DT \\ i_{L2}(t) + i_L(t), & DT \le t < T \end{cases} \tag{41}$$

$$i_{s2}(t) = \begin{cases} 0, \quad 0 \le t < DT \\ \frac{V_{DC}}{L_2} * t + i_{L2}(t_3) + \frac{V_{o1}}{L} * t + i_L(t_3), \\ \qquad DT \le t < T \end{cases}$$

$$i_{sd2}(t) = \begin{cases} -(i_{L2}(t) + i_L(t)), & 0 \le t < DT \\ 0, & DT \le t < T \end{cases} \tag{42}$$

A. ZVS CONDITION

Transition instants that occur for a switching cycle are S_{d1off} to S_{1on}; S_{1off} to S_{d1on}; S_{d2off} to S_{2on} and S_{2off} to S_{d2on}.

At t = 0,

$$i_{Sd1,turn-off} = \frac{I_{L,max} - I_{L1,min}}{2} > 0 \tag{43}$$

$$i_{S1,turn-on} = -\left(\frac{I_{L,max} - I_{L1,min}}{2}\right) < 0 \tag{44}$$

$$i_{S2,turn-off} = \frac{I_{L2,max} + I_{L,max}}{2} > 0 \tag{45}$$

$$i_{Sd2,turn-on} = -\left(\frac{I_{L2,max} + I_{L,max}}{2}\right) < 0 \tag{46}$$

At t = t_2

$$i_{S1,turn-off} = \frac{I_{L1,max} + I_{L,max}}{2} > 0 \quad (47)$$

$$i_{Sd1,turn-on} = -(\frac{I_{L1,max} + I_{L,max}}{2}) < 0 \quad (48)$$

$$i_{Sd2,turn-off} = \frac{I_{L,max} - I_{L2,min}}{2} > 0 \quad (49)$$

$$i_{S2,turn-on} = -(\frac{I_{L,max} - I_{L2,min}}{2}) < 0 \quad (50)$$

Boost inductors L_1 and L_2 can provide currents of proper sign for ZVS turn-on and turn-off of S_{d1}, S_1 and S_{d2}, S_2 at the end of their energizing durations respectively. But it is not so when they transfer energy to the output. This problem is overcome using ZVS inductor 'L'. The ZVS inductor current i_L is having half-wave symmetry. It possesses the property of $i_L(t) = -i_L(t+T/2)$. The FBPBC inductor currents i_{L1} and i_{L2} will satisfy the property of $i_{L1}(t) = i_{L2}(t+T/2)$. Hence, ZVS condition is as represented by (43). ZVS inductor 'L' always provides proper turn-on and turn-off currents for all devices (S_1, S_2, S_{d1}, S_{d2}) to facilitate ZVS. Hence, the magnitudes of $I_{L,max}$ or $I_{L,min}$ should be more than magnitude of $I_{L1,min}$ or $I_{L2,min}$. In the proposed configuration, the ZVS peak current is 2.8A; the values of minimum and maximum boost inductor currents are 1.3A and 2A respectively.

The output capacitor of each MOSFET must be charged or discharged within the interval provided for dead time for ZVS operation. Hence, the charge required for each MOSFET is calculated as

$$Q = \int_0^{V_{01}} C_1(V_{ds})\, dV_{ds} = \int_{V_{01}}^{0} C_1(V_{ds})\, dV_{ds} \quad (51)$$

It can be assumed that linear charging and discharging of output capacitances of MOSFETs occurs with constant current ($I_1/2$) during ZVS interval. The current (I_1) can be expressed during dead time (t_d) as

$$I_1 = \frac{2C_1V_{o1}}{t_d} = \frac{2Q}{t_d} \quad (52)$$

The ZVS inductor along with the boost inductors L_1 and L_2 will provide the ZVS commutation currents as shown from (43) to (50). Boost inductors with lower values can be selected since ripple cancellation is possible. But this results in higher peak currents. Due to this, the conduction losses will increase. Hence, there should be a tradeoff for obtaining a good efficiency while designing the boost inductors.

From the waveforms of the FBPBC at nominal input voltage of 24V, I_1 is taken as 4.1A, V_{01} is 48V, t_d = 200ns. The Capacitance C_1 is calculated as 8.54nF. C_{0ss} of the device is 0.295nF. Hence, an additional capacitance of 8.24nF is required. C_1 is taken as C_{d1}. Similarly, other leg capacitance can also be calculated.

B. SWITCH CURRENTS AND CRITICAL INDUCTANCE

The maximum switch current can be determined from minimum input voltage, $V_{DC(min)}$. $I_{o1(max)}$ can be obtained considering 100% efficiency of paralleled boost converter.

$$P_{o1} = P_{in}V_{o1,min}I_{o1,max} = V_{DC,min}I_{DC,max}$$

$$I_{o1,max} = \frac{V_{DC,min}I_{DC,max}}{V_{o1,min}} \quad (53)$$

Boost inductor ripple current is required to calculate maximum current in the switch.

$$\text{Inductor ripple current} = \Delta i_{L1} = \Delta i_{L2} = \frac{V_{DC,min} * D}{f_s * L_1} \quad (54)$$

where D is fixed at 0.5

$L_1 = L_2$ = boost inductor value

The maximum current in the boost inductors is given by

$$I_{L1max} = \frac{\Delta i_{L1}}{2} + \frac{I_{o1,max}}{2(1-D)} \quad (55)$$

$$I_{L2max} = \frac{\Delta i_{L2}}{2} + \frac{I_{o1,max}}{2(1-D)} \quad (56)$$

Maximum Switch Current (I_{Smax})

$$I_{S1,max} = I_{L1,max} + I_{L,max} \quad (57)$$

$$I_{S2,max} = I_{L2,max} + I_{L,max} \quad (58)$$

The maximum and minimum currents in inductor L_1 or L_2 can be determined by their corresponding average currents and their ripple currents as

$$I_{L1,max} = I_{L1} + \frac{\Delta i_{L1}}{2} \quad (59)$$

$$I_{L1,min} = I_{L1} - \frac{\Delta i_{L1}}{2} \quad (60)$$

Similarly, $I_{L2,max}$ and $I_{L2,min}$ can be obtained.

The maximum average boost inductor current is given by

$$I_{L1,2max(avg)} = \frac{I_{L1,2max} + I_{L1,2min}}{2} \quad (61)$$

The maximum output of FBPBC is given by

$$I_{L1,2max(avg)} = \left\lceil \frac{I_{o1max}}{2(1-D)} \right\rceil \quad (62)$$

The average inductor current is obtained as 1.65A. Each boost converter contributes 0.825A.

C. BOOST INDUCTOR CALCULATION

The chosen inductance value should be higher such that the ripple current is low. But due to ripple cancellation effect of paralleled boost, lower inductance can be used. Allowing ripple in inductor current of 20% to 40% of FBPBC output current,

$$\text{Ripple current, } \Delta i_L = (0.2\ to\ 0.4) i_{o1max} \quad (63)$$

Equation (28) is obtained by considering the boost inductor current to be continuous. Boundary condition for CCM and DCM can be obtained by making I_{L1min} to zero. Hence, the critical value of boost inductor L_{1cr} is expressed as

$$L_{1cr} = \frac{V_{DC(min)}D}{\Delta i_L * f_s} \quad (64)$$

where f_s is the switching frequency. For the proposed converter, the critical inductance is obtained as 163.63 μH.

For continuous conduction, the boost inductance should be greater than critical inductance, i.e., $L_1 > L_{1cr}$.The boost inductor value for switching frequency f_s can be expressed as

$$L_{1,2} = \frac{V_{DC} * (V_{01} - V_{DC})}{\Delta i_L * f_s * V_{01}} \tag{65}$$

where V_{DC} is the input voltage to the FBPBC. V_{01} is the output of FBPBC.

For 100 kHz of switching frequency, $V_{DC} = 24$V, D = 0.5, T = 10μs. Limiting peak ripple inductor current to (20)-(40) % of average inductor current, inductor value obtained from preceding equation is L_1& $L_2 = 200\mu$H.

D. MAGNETIC DESIGN

The boost inductors, ZVS inductor and buck-boost inductors are designed based on their respective peak current values. The peak currents carried by inductors L_1 and L_2 is 2A, inductor L is 2.8A and L_3 is 1A.

Peak energy stored in the inductors are

$$E = \frac{1}{2}LI_{max}^2$$
$$E_{L1,2} = \frac{1}{2}L_{1,2}I_{1,2max}^2; = 4x10^{-4}J$$
$$E_L = \frac{1}{2}LI_{max}^2; = 1.96x10^{-4}J$$
$$E_{L3} = \frac{1}{2}LI_{3max}^2 = 1x10^{-4}J$$

The inductor core area is calculated as

$$A_p = A_w A_c = \frac{2E}{K_w K_c J B_m}$$

K_w is chosen as 0.6; flux density (B_m) = 0.2T for Ferrite core; current density (J) = 2A/mm^2.

A_p for L_1&L_2, L, L_3 are calculated as 2777 mm^4, 1361 mm^4, 694 mm^4 respectively.

EE Cores of dimension 30/15/7 for L_1& L_2, 25/9/6 for L and L_3 are chosen by comparing A_p value from data sheet based on the inductor values and currents carried by them.

Number of turns (N) of inductor coil is calculated as

$$N = \frac{LI_{max}}{A_c B_m}$$

Number of turns for L_1& L_2, L, L_3 are chosen as 33, 18 and 25 respectively. A small air gap is introduced in the core in order to avoid saturation at peak value.

E. OUTPUT CAPACITANCE (C_{o1})

The output capacitance can be obtained as

$$C_{o1} = \frac{I_{01} * D}{f_s \Delta V_{o1}} \tag{66}$$

where I_{o1} is the output current and ΔV_{o1} is allowable ripple in output voltage.

The buck-boost inductor value L_{bb} is obtained from (31) as

$$\Delta i_{L3} = \frac{V_{o1}}{L_3} D_{bb} T$$

For 100 kHz of switching frequency, with $V_{o1} = 48$V, $D_{bb} = 0.27$, T = 10μs, the value of inductor from above equation is found to be $L_3 = 220\mu$H.

F. INPUT RIPPLE

The proposed FBPBC is operated in continuous current mode of operation. This enables lower input ripple current compared to other converter configurations [25], [26]. By operating two boost converters in interleaving mode, boost inductor currents cancel each other, thereby minimizing the input ripple current further. Hence, the size of boost inductor can be reduced. Also, the stress on input and output capacitors is reduced which increases the reliability. Ripple current of a boost inductor is given by

$$\Delta i_{L1} = \Delta i_{L2} = \frac{V_{DC} * D}{f_s * L_{1,2}}$$

Since boost converters are operated at 0.5 duty cycle, theoretically, the input current is ripple free.

G. POWER LOSS CALCULATION

The major power losses in the proposed converter are the conduction losses in switches, boost inductors, ZVS inductor, switch and diode of buck-boost converter.

Conduction losses:

Conduction losses of inductive elements are given as

$$P_{con,ind} = I_{L1}^2 r_{L1} + I_{L2}^2 r_{L2} + I_L^2 r_L = 0.95 \text{ W}$$
$$P_{core,ind} = 1.88 \text{ W} \tag{67}$$

where I_{L1}, I_{L2} and I_L are the rms currents and r_{L1}, r_{L2}, r_L are parasitic resistances of L_1, L_2 and L respectively.

Conduction losses of switches of FBPBC is given by

$$P_{con,SIBC} = (I_{s1}^2 + I_{s2}^2 + I_{sd1}^2 + I_{sd2}^2) r_{dson1} = 0.959 \text{ W} \tag{68}$$

where I_{s1}, I_{s2}, I_{sd1}, I_{sd2} are the rms currents of S_1, S_2, S_{d1} and S_{d2} respectively and r_{dson1} is the on-state resistance of these devices. Switching losses are neglected.

Switching and Conduction loss of buck-boost switch S_{bb} is given by

$$P_{(con+sw),BB} = I_{sbb}^2 r_{dson2} = 0.411 \text{ W} \tag{69}$$

where I_{sbb} is the rms current of S_{bb} and r_{dson2} is the on-state resistance of S_{bb}.

Power loss in diode D_3 is given by

$$P_{con,diode} = V_f I_{o2} = 0.36 \text{ W} \tag{70}$$

where V_f is the forward voltage drop and I_{o2} is the output current of buck-boost converter.

The conduction loss in inductor L_3 is

$$P_{con,L3} = I_{L3}^2 r_{L3} \tag{71}$$

where I_{L3} is the rms current and r_{L3} is the parasitic resistance of L_3.

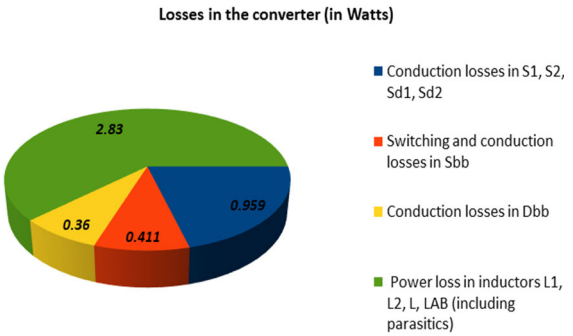

FIGURE 4. Loss analysis of the converter.

H. LED LOAD AND OUTPUT VOLTAGE

The equivalent circuit of LED load can be used to calculate the number of LEDs and LED strings required for a given output power. Two parallel strings of LEDs are used as load. 20 LEDs are connected in series in one string. The on- resistance of each LED is 1.86 Ω and forward voltage is 2.32V. Hence, the LED lamp is operated at 65 V, 1 A (0.5 A in each string) and 65W. $V_0 = 65\ V$

Output voltage of FBPBC is calculated with (29) as

$$V_{o1} = \frac{V_{DC}}{(1-D)}$$

Hence, for $V_{DC} = 24V$ and $D = 50\%$, V_{o1} will be 48V.

From (34), voltage across LED lamp is expressed as

$$V_o = \frac{V_{DC}}{(1-D)} + V_{o1}\left[\frac{D_{bb}}{(1-D_{bb})}\right]$$

I. STATE SPACE EQUATIONS

For paralleled boost converter,

$$\begin{bmatrix} \frac{di_{L1}}{dt} \\ \frac{di_{L2}}{dt} \\ \frac{dv_{C1}}{dt} \end{bmatrix} = \begin{bmatrix} 0 & 0 & \frac{(1-D_1)}{L_1} \\ 0 & 0 & \frac{D_1}{L_2} \\ \frac{(1-D_1)}{C_1} & \frac{D_1}{C_1} & \frac{-1}{RC_1} \end{bmatrix} \begin{bmatrix} i_{L1} \\ i_{L2} \\ v_{C1} \end{bmatrix} + \begin{bmatrix} \frac{(2D_1-1)}{L_1} \\ \frac{(1-2D_1)}{L_2} \\ 0 \end{bmatrix} v_{DC}$$

$$v_{01} = \begin{bmatrix} 0 & 0 & 1 \end{bmatrix} \begin{bmatrix} i_{L1} \\ i_{L2} \\ v_{C1} \end{bmatrix}$$

For buck-boost converter,

$$\begin{bmatrix} \frac{di_{L3}}{dt} \\ \frac{dv_{C2}}{dt} \end{bmatrix} = \begin{bmatrix} 0 & \frac{-(1-D_2)}{L_3} \\ \frac{(1-D_2)}{C_2} & \frac{-1}{RC_2} \end{bmatrix} \begin{bmatrix} i_{L3} \\ v_{C2} \end{bmatrix} + \begin{bmatrix} \frac{D_2}{L_3} \\ 0 \end{bmatrix} v_{DC}$$

$$v_{02} = \begin{bmatrix} 0 & 1 \end{bmatrix} \begin{bmatrix} i_{L3} \\ v_{C2} \end{bmatrix}$$

$$v_0 = v_{01} + v_{02}$$

$$\mathrm{R}_1 = \text{Equivalent load on} v_{01} = \left(\frac{R}{1+k}\right)$$

$$\mathrm{R}_2 = \text{Equivalent load on} v_{02} = \left(\frac{k.R}{1+k}\right)$$

$$k = \left(\frac{V_{01}}{V_{02}}\right)$$

R = LED load on the converter.

V. DIMMING CONTROL AND SALIENT FEATURES OF PROPOSED FBPBC

In most of the lighting applications, dimming is essential for energy saving and human need [27]. It can be achieved by amplitude control of LED current referred as Amplitude

Modulation (AM) or by varying the average LED current referred as PWM diming [28], [29], [30], [31]. As there is a risk of colour variation of light with current control, PWM dimming is commonly preferred over AM dimming. Dimming is done at a lower frequency. The switches are turned OFF with that of low frequency pulse so as to incorporate dimming into proposed configuration. Dimming is to be done at low frequency to avoid a colour change or apparent flickers in the lighting [32]. A double PWM (DPWM) control strategy is implemented to simultaneously regulate amplitude and average current.

The salient features of the proposed FBPBC are:

a) The boost configurations operating out of phase are uncontrolled and operate always at 50% duty cycle. This helps in simplicity of the control circuit and ZVS is ensured for wider range of operation. Feedback is only required with buck-boost configuration at its output.
b) For applications such as industrial/factory lighting, higher wattages and multiple units are required. This requires higher voltages as well. As boost configurations exist in the input stage, it can provide higher voltages at the output with lower currents. This will also reduce conduction losses.
c) This configuration can be extended for multiple outputs also with independent control of each output. Additional buck-boost configurations can be added for multiple outputs with independent control.

There are several high-power applications for LED lighting such as a) Street lighting (100 W), b) LCD Back light (150 W), c) High Bay light (300 W) and d) Flood Lighting (500 W). The proposed configuration offers following advantages for such applications:

a) The efficiency of the proposed configuration will be considerably higher for higher power applications as mentioned above.
b) For high power applications, the source current as well as source current ripple are expected to be higher. This configuration cancels the source current ripple completely. This is very much helpful in reduction in size of the inductors as higher current ripples can be allowed.

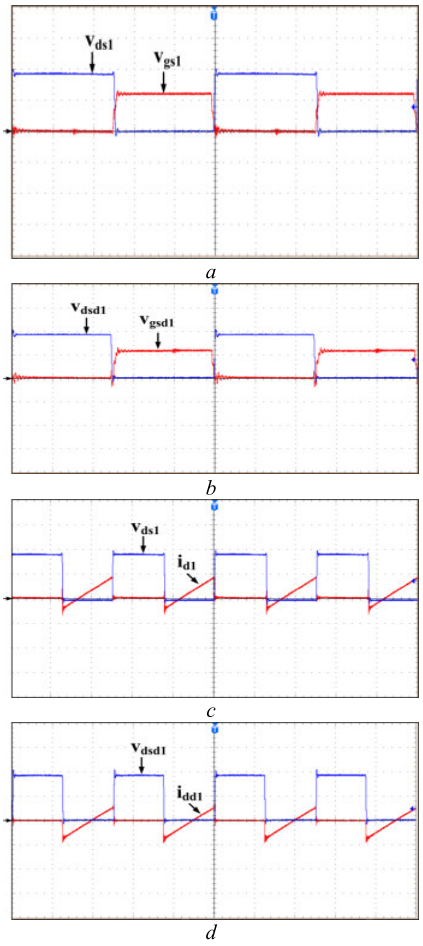

FIGURE 5. Experimental waveforms showing ZVS for rated input voltage $V_{DC} = 24V$ (v_{ds}: 25 Volts/div; v_{gs}: 10 Volts/div; i_d: 5 Amp/div; time: 2 μs/div).

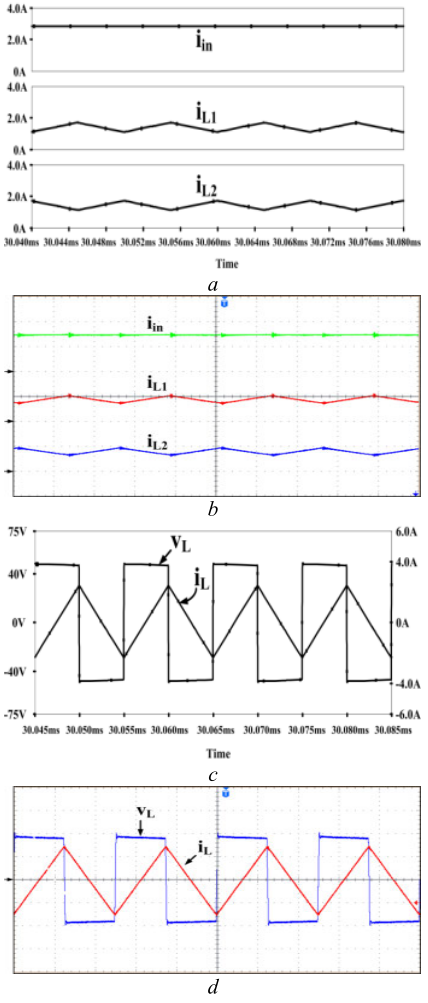

FIGURE 6. Simulation and experimental waveforms for inductor currents, source current indicating ripple cancellation and current through ZVS inductor at nominal input voltage $V_{DC} = 24V$ (i_{L1}, i_{L2}, i_L, i_{DC} : 2 Amp/div; v_L: 25 Volts/div; time: 4 μs/div).

c) Proposed configuration doubles the input voltage which is helpful for higher voltage operation of the load for higher power ratings.
d) Efficiency will be further enhanced with the use of SIC based device.

VI. SIMULATION AND EXPERIMENTAL RESULTS

A 65 W prototype of the proposed configuration is designed and experimentally tested. Components used are listed in Table 1. PSpice ORCAD software is used for simulation. The cost analysis of the proposed configuration is provided in Table 2. Simulation and experimental results are in good agreement. FBPBC is powered with input voltage of 24V switching at 100 kHz. For 24 V of input, Figs. 5*a* and b show experimental waveforms of voltage across switch (V_{ds}) & gate signals of S_1 & S_{d1} respectively. Figs. 5*c* and b indicate experimental waveforms for current through switch and voltage across S_1 and S_{d1} for same input voltage. These waveforms indicate ZVS operation of FBPBC.

ZVS operation: It can be seen that after V_{ds1} falls, gate pulse is applied, giving ZVS turn-on for S_1. Similarly, V_{ds1} rises after the gate pulse is removed giving ZVS turn-off for S_1. Same operation can be observed for S_{d1} in Fig. 5*b* giving ZVS turn-on and turn-off. There is another method to observe ZVS operation. In Fig.5*c*, i_{d1} is negative before V_{ds1} falls. Negative device current (i_{d1}) discharges the output capacitance of S_1 before turn-on.

Then the anti-parallel diode starts conducting keeping device voltage close to zero. It results in ZVS turn-on by the application of gate pulse. Same operation is shown for S_{d1} in Fig.5*d*. S_1, S_2, S_{d1}, S_{d2} are switched-on and switched-off at zero voltage. Switching losses are decreased with ZVS, resulting in increased efficiency.

Figs. 6*a* and b indicate simulation and experimental waveforms of currents through FBPBC inductors and source current for nominal input. For the devices of left-leg and right-leg of FBPBC i.e., (S_1, S_{d1}) and (S_2, S_{d2}), have a off-state voltage of 48 V. Their voltage fall and rise times are 0.2 μsecs and 0.1 μsecs respectively. Turn-on and turn-off currents of S_1 and S_{d1} are (2A, 4A) and (3A, 3A) respectively. Figs. 6*a* and b show negligible ripple in input current. Peak currents of boost inductors is 2 A with ripple current of 0.8 A

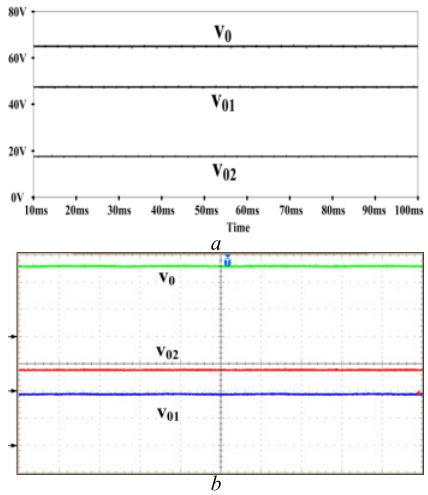

FIGURE 7. Simulation and experimental waveforms for FBPBC, buck-boost Converter, LED lamp voltage at nominal input voltage V_{DC} = 24V (voltage: 25 Volts/div; time: 4 μs/div).

each. The ZVS inductor current (i_L) has a peak value of 2.8 A. This helps in aiding ZVS operation of devices of FBPBC. When i_L is rising (S_{d1}, S_2 on) L_1 discharges, transferring energy to the output (v_{o1}). Under this condition, currents i_{L1} and i_L are in opposite direction through S_{d1}. Hence switch current reduces resulting in lower conduction loss. When S_{d1} is turned-off, the difference of these two currents helps in achieving ZVS of S_{d1} and S_1. During this interval, with S_{d1} and S_2 on, i_{L2} and i_L flow though S_2 also. When S_2 is turned-off, sum of i_{L2} and i_L help in charging capacitor across S_2 and discharging the capacitor across S_{d2} resulting ZVS operation. In the next interval, S_{d2} and S_1 are conducting. L_1 is energized. At the end of this interval, i_L reaches negative peak and directions of i_L and i_{L2} have opposite signs. Difference of these two currents flows through S_{d2}. Also, at the time of turn-off of S_{d2} this difference of currents helps in achieving ZVS of S_{d2} and S_2. ZVS inductor voltage and current are shown in Figs. 6*c* and d.

Simulation and experimental waveforms for output voltages of FBPBC, buck-boost converter and LED lamp voltage are shown in Figs. 7*a* and b. It can be observed that FBPBC supplies majority of voltage to the LEDs, while buck-boost converter supplies the remaining voltage and power. The total voltage required for LED lamps is the sum of both voltages. Rated LED load current is obtained at buck-boost duty-cycle (D_{bb}) of 27.6% at nominal input voltage. At nominal input voltage of 24 V, FBPBC produces $V_{o1} = 48$ V and buck-boost converter produces output voltage of $V_{o2} = 17$ V. A total of 65 V is applied across LED load.

Considering variation in input voltage by $\pm 10\%$, there is a reduction of 2.4 V. The input voltage is $V_{DC} = 21.6$ V. Duty cycle of S_{bb} (D_{bb}) is adjusted accordingly such that load voltage remains constant and load current is maintained at rated value. The required value of D_{bb} is 35.2%. Figs. 8*a* and b show waveforms for gate signals and drain to source voltage (V_{ds}) of S_1 and S_{d1} for -10% variations in input voltage. ZVS

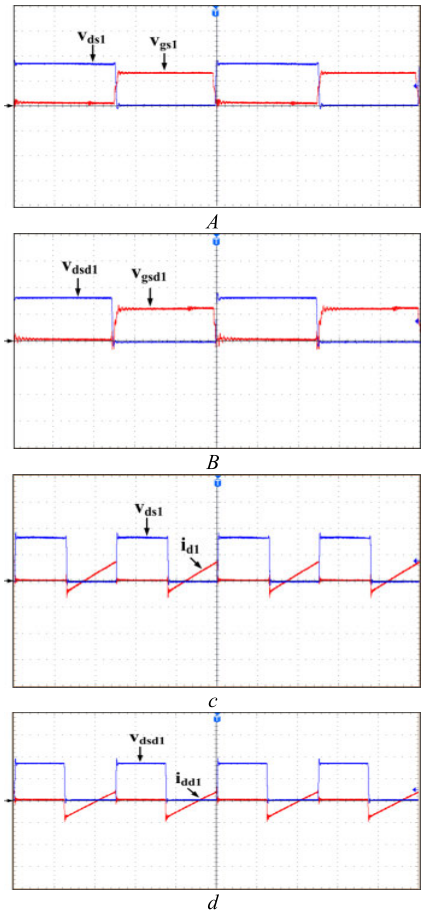

FIGURE 8. Experimental waveforms showing ZVS for -10% input voltage fluctuations i.e., $V_{DC} = 21.6$V (v_{ds}: 25 Volts/div; v_{gs}: 10 Volts/div; i_d: 5 Amp/div; time: 2 μs/div).

TABLE 1. Parameters of proposed configuration.

Parameters	Values
Source voltage, v_{DC}	24 V
Total LEDs	40 (2 parallel string)
LED operating current, i_o	1 A (0.5 A each string)
Power Rating of LED load	65W
Switching frequency, f_s	100 kHz
Duty-cycle of FBBC switches	0.5
Boost Inductors; L_1, L_2	200 µH
ZVS Inductor, L	50 µH
Output Capacitors; C_{o1}, C_{o2}	10 µF
Buck-Boost Inductor, L_{bb}	200 µH
Output Voltage V_o	65 V
Duty ratio of switch S_{bb}	0 to 1
Switching devices used	MOSFET IRF540N
Diode D_3	MBR 20200

is still attained in both switches. Figs. 8*c* and d show current waveforms of these devices.

Fig. 9*a* and b are waveforms under simulation and experimentation for currents through inductor and source currents of FBPBC for -10% variations in input voltage. Here also ripple cancellation exists. These figures show waveforms of ZVS operation, v_L, i_L, i_{L1}, i_{L2} for -10% variation of source voltage.

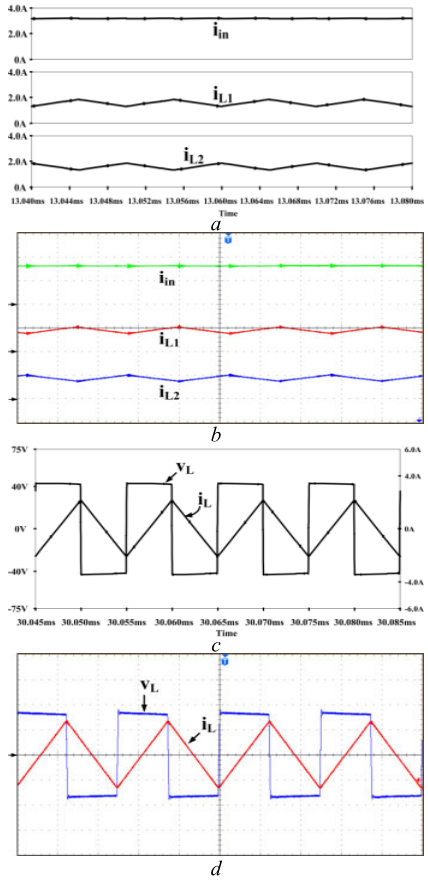

FIGURE 9. Simulation and experimental waveforms for inductor currents, source current indicating ripple cancellation and current through ZVS inductor for −10% input voltage variation i.e., $V_{DC} = 21.6V$ (i_{L1}, i_{L2}, i_L, i_{DC}: 2 Amp/div; v_L: 25 Volts/div; time: 4 μs/div).

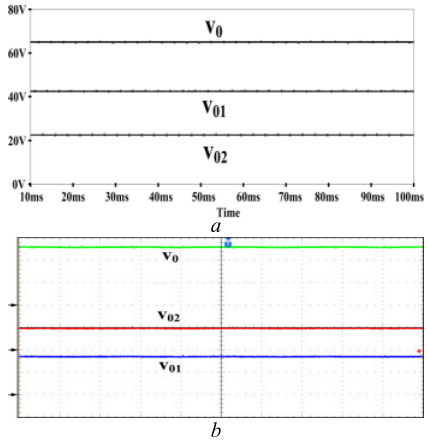

FIGURE 10. Simulation and experimental waveforms of FBPBC, buck-boost Converter, LED lamp voltage for −10% input voltage variation i.e., $V_{DC} = 21.6V$ (voltage: 25 Volts/div; time: 4 μs/div).

TABLE 2. Cost analysis of proposed configuration.

Component	Required Rating	No.	Unit Price ($)	Amt
IRF540N	IRF540NPBF	5	1.35	6.75
MBR20200	MBR20200CTF	1	0.89	0.89
	200 uH/3 A	3	2.48	7.44
Inductor	47 uH/ 2 A	1	1.74	1.74
	10 uF/100 V (FILM)	2	1.62	3.24
Capacitor	(Electrolytic)	2	0.94	1.88
MOSFET Driver	IR2110PBF	2	3.68	7.36
	TLP250H(TP1,F)	1	1.82	1.82
			Total Cost ($)	31.12

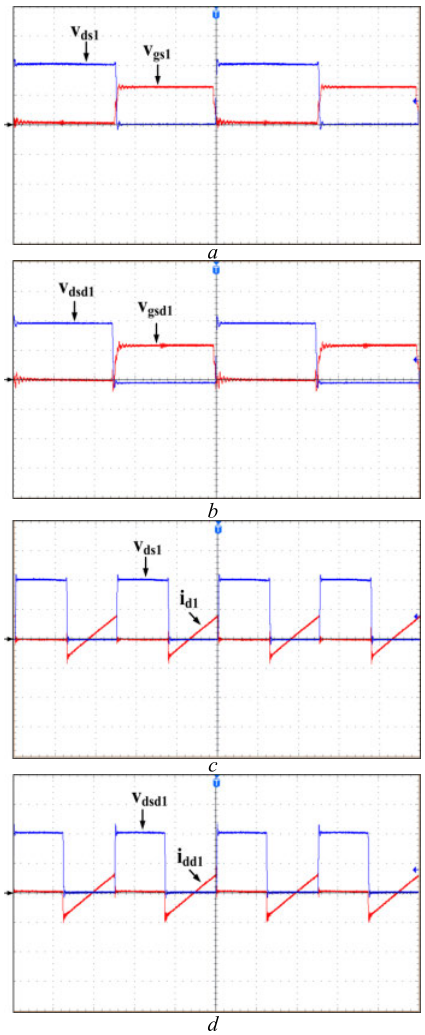

FIGURE 11. Experimental waveforms showing ZVS for +10% input voltage variations i.e., $V_{DC} = 26.4V$ (v_{ds}: 25 Volts/div; v_{gs}: 10 Volts/div; i_d: 5 Amp/div; time: 2 μs/div).

Fig. 10*a* and *b* indicate the corresponding simulation and experimental results for output voltages of FBPBC, buck-boost converter and LED lamp voltage for −10% source voltage fluctuations. Waveforms of v_{o1}, v_{o2}, and v_o under −10% variation of the input voltage are shown. For input voltage of 21.6 V, $v_{o1} = 43.2$ V and $v_{o2} = 21.8$ V, making total voltge of $v_o = 65$ V for the LED load.

Now let us consider a +10% input fluctuation. The input voltage will be $V_{DC} = 26.4V$. The buck-boost converter has to attenuate for the enhanced source voltage by 2.4V. The

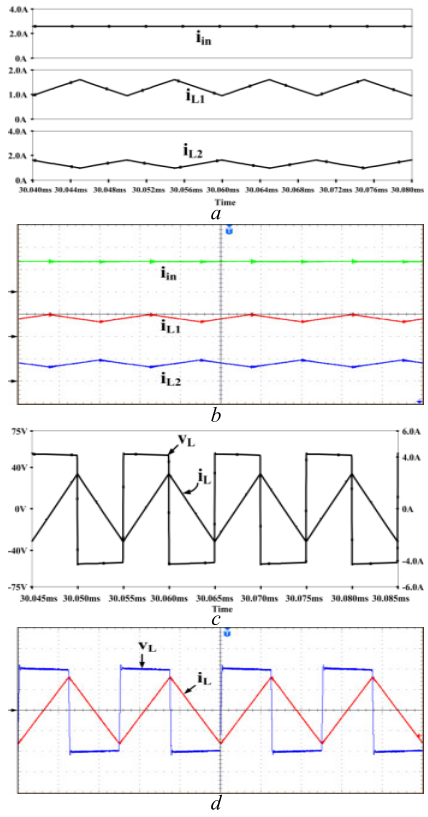

FIGURE 12. Simulation and experiment waveforms of inductor currents and source current indicating ripple cancellation and current through ZVS inductor for +10% input voltage variation i.e., $V_{DC} = 26.4V$ (i_{L1}, i_{L2}, i_L, i_{DC}: 2 Amp/div; v_L: 25 Volts/div; time: 4 μs/div).

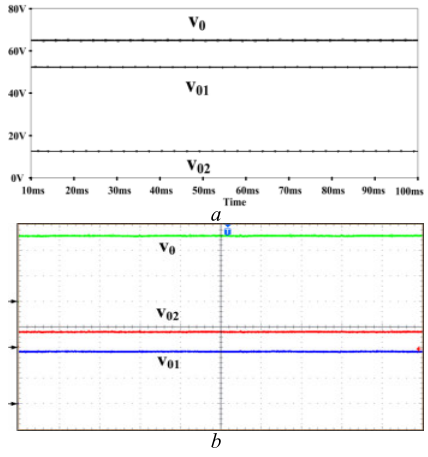

FIGURE 13. Simulation and experimental waveforms of FBPBC, buck-boost converter, LED lamp voltage for +10% input voltage variations i.e., $V_{DC} = 26.4V$ (voltage: 25 Volts/div; time: 4 μs/div).

duty-cycle of S_{bb} is modified accordingly, and the LED load receives the rated current. D_{bb} is 20.1%.

Figs. 11*a* and *b* show experimental waveforms for voltage across switch (V_{ds}) & gate signals of S_1 & S_{d1} for +10% variations in input voltage. ZVS is still attained in both switches, according to the results. Figs. 11*c* and d indicate experimental waveforms for current through switch and voltage across S_1 & S_{d1} for +10% variations in input voltage.

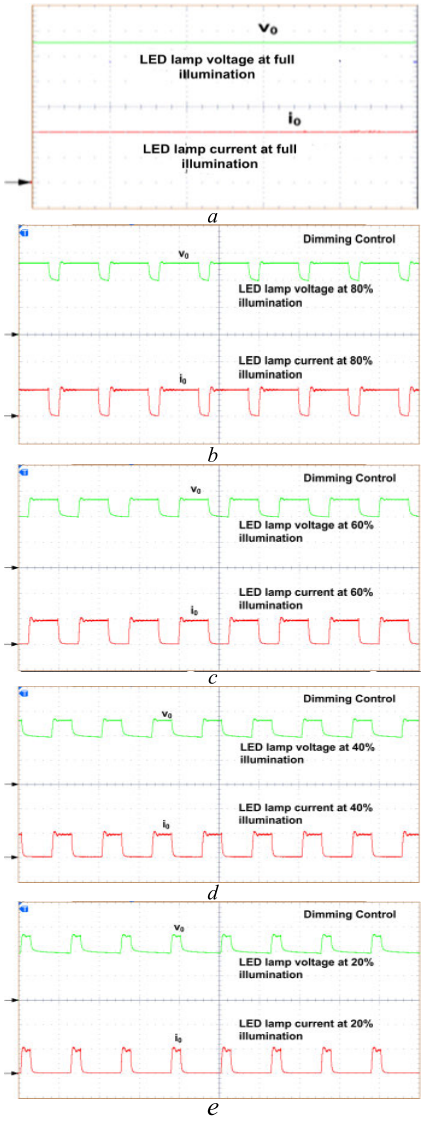

FIGURE 14. Experimental waveforms of LED lamp voltage and current at full illumination and various dimming levels for rated input voltage (V_o: 25 Volts/div; i_0: 1 Amp/div; time: 4 μs/div).

Figs. 12*a* and *b* indicate simulation and experimental waveforms of currents through inductor and source current of FBPBC for +10% variations in input voltage. The ripple in input current has been found to be significantly reduced. Figs. 12*c* and *d* indicate the corresponding simulation and experimental results for ZVS inductor voltage and current for +10% variations. Experimental waveforms of i_{L1}, i_{L2}, and i_L are in agreement with simulation results.

Figs. 13*a* and *b* indicate the corresponding simulation and experimental waveforms for output voltages of FBPBC, buck-boost converter and LED lamp voltage for +10% input fluctuations. It shows v_{o1}, v_{o2}, and v_o under +10% variation of the input voltage. For input voltage of 26.4 V, $v_{o1} = 52.8V$ and $v_{o2} = 12.2$ V, making total voltage of $v_o = 65$ V for the LED load.

Fig. 14*a* shows experimental waveforms of LED voltage and current at maximum illumination for nominal input

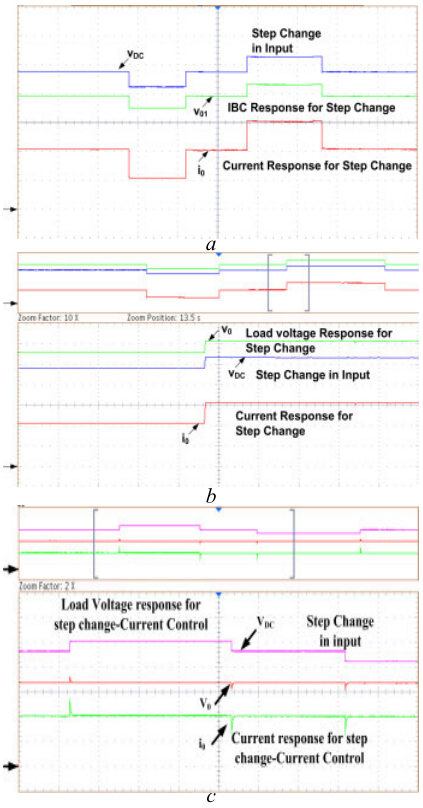

FIGURE 15. Dynamic response: (a), (b) Open loop performance of the LED driver for step change in input voltage, (c) Closed loop performance of the LED driver for step change in input voltage implementing current control (V_{DC}: 5 Volts/div; V_o: 20 Volts/div; i_0: 0.5 Amp/div).

voltage. The load voltage is controlled using buck-boost converter, which handles small power. As a result, the converter's total efficiency is high. At maximum illumination, the efficiency is determined as 93.42%.

Fig. 14*b* shows experimental waveforms of LED voltage and current at 80% of illumination. Similarly, Figs. 14 *c* to *e* show experimental waveforms of LED voltage and current at 60%, 40%, and 20% of illumination respectively. At all dimming levels, high efficiency is achieved. It shows that response of LED current for different illumination levels are with negligible overshoot. Also, simulation and experimental results are in good agreement. LED current remains constant at all levels of illumination but the average LED current is varied.

For a step change in input voltage, the paralleled boost converter voltage and current response, the overall load voltage and current response in open loop are shown in Fig. 15*a* and *b* respectively. It is observed that the output voltage and current follow very closely for step change. The closed loop performance of the LED driver is shown in Fig. 15c by sensing the current through LED lamp with a sensing resistor. Duty cycle of buck-boost converter is controlled for constant current in LED for a step change in input voltage. The current response shows that the current though LEDs is controlled.

Fig. 16*a* shows the variation of buck-boost converter duty-cycle (D_{bb}) with input voltage (V_{DC}) variations. Fig. 16*b*

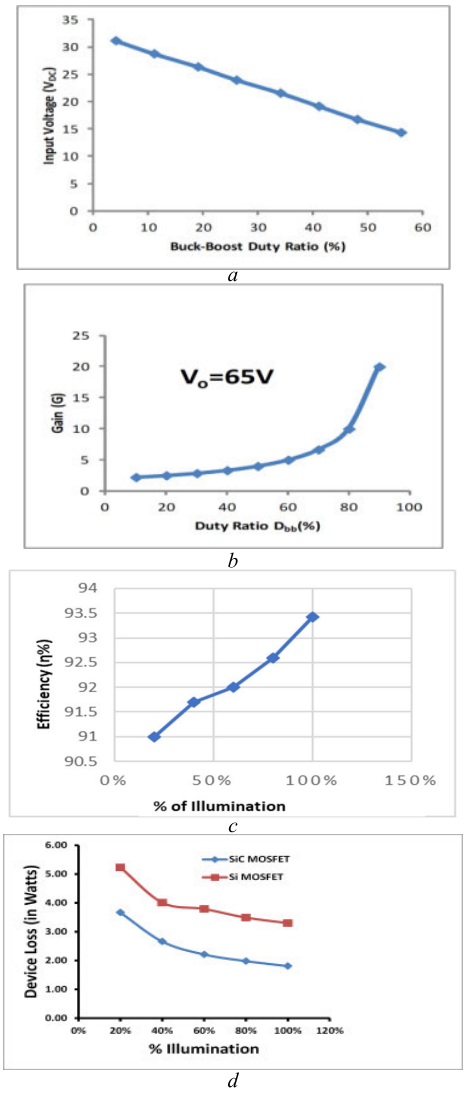

FIGURE 16. (a) Input voltage vs buck-boost converter duty-cycle (D_{bb}) (b) Voltage gain vs D_{bb} (c) Efficiency (η %) (d) Comparison of device loss of the proposed converter at various dimming levels using Si and SiC MOSFET.

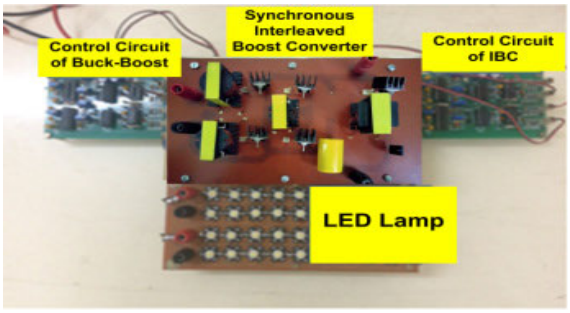

FIGURE 17. Experimental setup of the proposed converter.

shows the converter Gain versus D_{bb} variation. This indicates a control of D_{bb} for input voltage variations. In the range of $\pm$ 10% variation of the input voltage, buck-boost converter duty-cycle varies almost linearly to regulate the load voltage and current of LED load. This is same with gain vs. duty-cycle variation also.

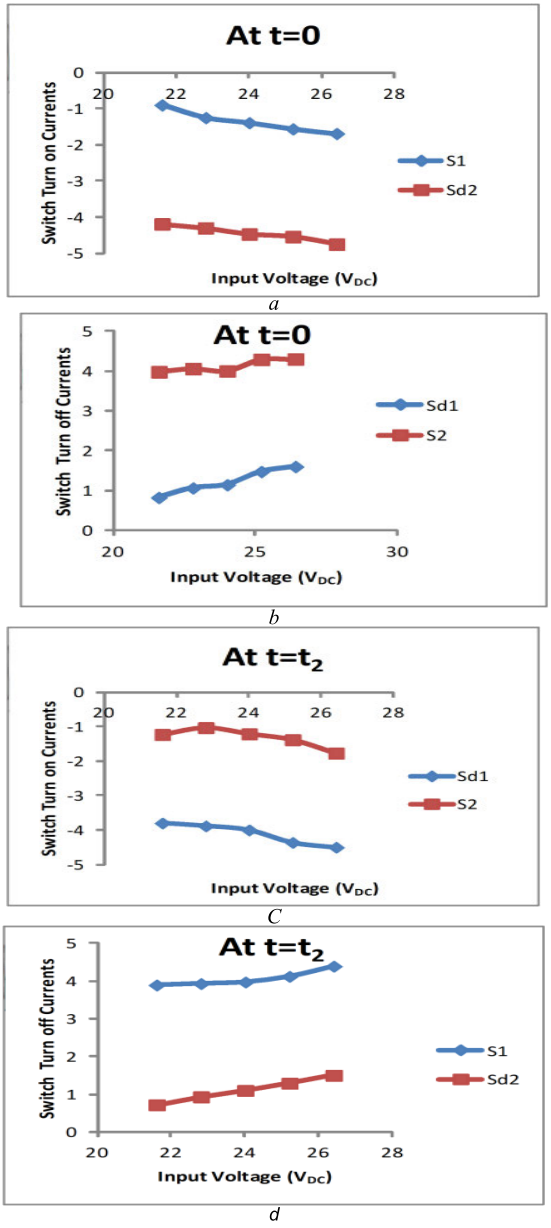

FIGURE 18. Switch turn-on and turn-off currents at t = 0, t = t_2 (a) At t = 0, turn-on currents of S_1, S_{d2}, (b) At t = 0, turn-off currents of S_{d1}, S_2, (c) At t = t_2, turn-on currents of S_{d1}, S_2, (d) At t = t_2, turn-on currents of S_1, S_{d2}.

Fig.16*c* shows the variation of efficiency vs. level of illumination. Minimum and maximum efficiencies obtained are 91% and 93.42%. These are reasonably high.

Fig. 17 shows the experimental setup of the proposed converter. FBPBC converter and buck-boost converter of the proposed LED driver are implemented with IRF 540N MOSFETs. Low drop diode MBR20200 is used in buck-boost converter. Driver circuits are built using UC 3875 control ICs and TLP250H ICs. The LED load consists of two strings of 20 LEDs each.

Figs. 18*a* and *b* show the switch turn-on and turn-off currents of switches (S_1, S_{d2}); (S_{d1}, S_2) respectively at t = 0.

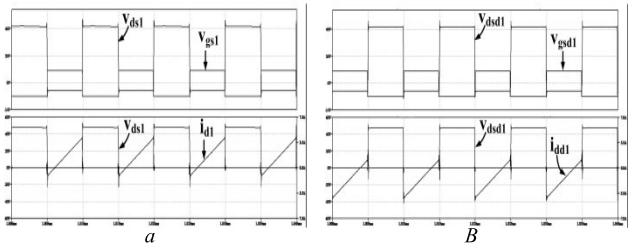

FIGURE 19. Simulation waveforms showing ZVS with SiC MOSFET for rated input voltage V_{DC} = 24V (v_{ds}: 20 Volts/div; v_{gs}: 20 Volts/div; i_d: 3.5 Amp/div; time: 2 μs/div).

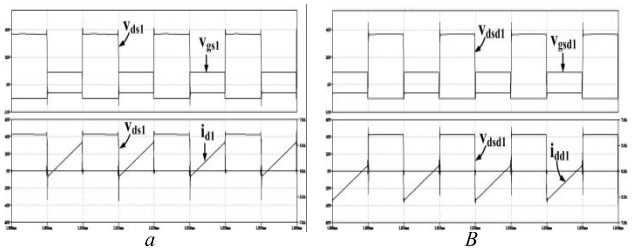

FIGURE 20. Simulation waveforms showing ZVS with SiC MOSFET for −10% input voltage fluctuations i.e., V_{DC} = 21.6V (v_{ds}: 20 Volts/div; v_{gs}: 20 Volts/div; i_d: 3.5 Amp/div; time: 2 μs/div).

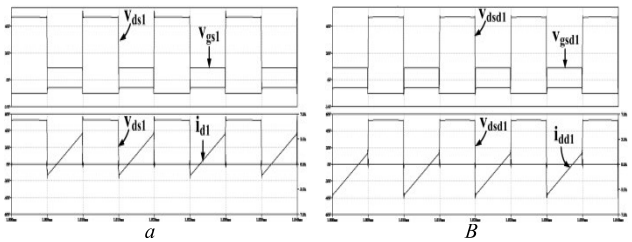

FIGURE 21. Simulation waveforms showing ZVS with SiC MOSFET for +10% input voltage fluctuations i.e., V_{DC} = 26.4V (v_{ds}: 20 Volts/div; v_{gs}: 20 Volts/div; i_d: 3.5 Amp/div; time: 2 μs/div).

Turn-on currents of S_1 and S_{d2} are shown for the entire range of variation of the input voltage. As the duty-cycle of devices of FBPBC is fixed but turn-on currents can vary with input voltage variation. It can be noticed that these currents remain negative in the entire range of input voltage variation and ZVS is ensured. Turn-on current of S_1 is smaller than that of S_{d2}. Turn-on current of S_1 is due to i_{L1} and i_L and is difference of these currents. Whereas, turn- on current of S_{d2} is due to i_{L2} and i_L which are of same sign obtained by their addition. Hence it is larger. Similarly, Fig. 18*b* shows the turn-off currents of S_{d1} an S_2. These are shown for input voltage variation. Turn-off currents for both devices are positive ensuring ZVS turn-off.

Turn-on current of S_1 and turn-off current of S_{d1} are same and of opposite sign. Also, turn-on current of S_{d2} and turn- off current of S_2 are same in magnitude and opposite in sign. These can be observed in the figures. Similarly, Figs. 18*c* and *d* show the switch turn-on and turn- off currents of switches (S_{d1}, S_2); (S_1, S_{d2}) respectively at t = t_2. Fig. 18*c* shows turn- on currents of S_{d1} and S_2 at t = t_2. These are negative in the entire range of input variation ensuring ZVS

TABLE 3. Comparison of existing converters with proposed led driver.

Resonant topology	[39]	[35]	[40]	[37]	[34]	[41]	Proposed topology
Switching Devices	6	4	2	1	3	2	5
Diodes	-	2	6	5	3	2	**1**
Inductors	3	3	0	1	3	1	4
Capacitors	4	3	1	4	4	3	**2**
Transformer	0	1	2	1	1	1	**0**
Output Power (P_0)	20W	120 W	210W	38W	30W	40W	65W
Efficiency	>85%	87%	90%	>90%	92%	>94%	**>93%** (Si MOSFET) **>95%** (SiC MOSFET)
Switching frequency	2 MHz	150 kHz	-	40 kHz	120 kHz	114 kHz	100kHz
Source current Ripple	No ripple cancellation	Equal to peak of tank current	Considerable Ripple, No ripple cancellation	No ripple cancellation	No ripple cancellation	No ripple cancellation	**Ripple Cancellation**
Source Voltage	8 to 18V	400 V	$220V_{ac}$	9 to 16 V	9 to 16 V	400V	24V
No. of LED lamps	4	1	1	1	1	1	1 (Multiple loads can be added as per requirement)
Switching device Voltage stress	$2V_{DC}$	Supply voltage	$>V_{in,peak}$	$V_0/(1+n)$	$V_{DC}/(1-D)$	Supply voltage	$2V_{DC}$

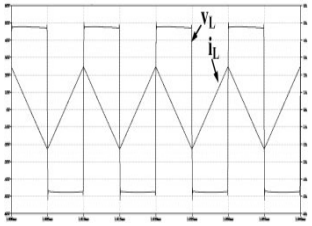

FIGURE 22. Simulation waveform of current through ZVS inductor at nominal input voltage V_{DC} = 24V using SiC MOSFET (v_L: 10 Volts/div; time: 5 μs/div).

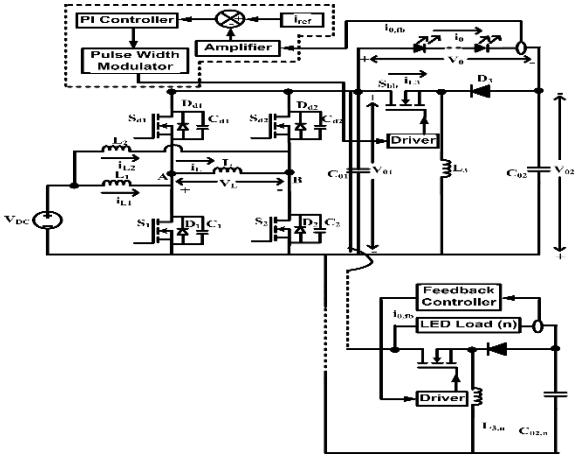

FIGURE 23. Proposed Converter with multiple loads.

turn-on. For S_{d1}, value of turn-on current is large as i_{L1} and i_L are of same sign. For S_2 turn-on current is small as i_{L2} and i_L have opposite sign. Fig.18*d* shows switch turn-off currents of S_{d2} and S_1.

For S_{d2} it is small as i_L and i_{L2} are of opposite sign and subtractive. For S_1 it is large as i_L and i_{L1} are of same sign and additive.

Significant advantages of using SiC device (C3M0015065K) in the proposed converter:

1. Small values of rise time and fall time resulting in reduced switching losses and possibility of operating at higher switching frequencies.

2. Small on-state resistance (15 mΩ) resulting in lower conduction losses. Total device losses are found be approximately, 1.8 W for the proposed converter at full illumination, increasing the overall efficiency.

3. Small dead time ($T_d = 0.1\ \mu s$) is required between the devices of same leg.

4. As the ZVS capacitor can be calculated as $C_{oss} = [(I_{sw,turn-off}).T_d]/(2.V_{DC})$, it can be noticed that with smaller values of dead time, smaller snubber capacitors are required.

Also, the reliability of the system improves as these devices can withstand higher operating temperature than silicon based MOSFETs.

The proposed configuration can be extended for multiple outputs also with independent control of each output. Additional buck-boost configurations can be added for multiple outputs with independent control as shown in Fig. 23. A relative comparison of multiple output LED drivers available in the literature and the proposed converter is provided in Table 3.

It can be observed from Table 3 that some of the existing topologies have low efficiency, high component count, absence of input current ripple cancellation etc. Most of them are using transformers. Whereas the proposed converter offers ripple current cancellation and higher efficiency of >95% with SiC MOSFETs. No transformer is used in

the proposed converter. For high power applications, the component count of the proposed converter is not high.

VII. CONCLUSION

This research work proposes an efficient and compact driver circuit for LED Street-lighting application. It is a combination of synchronous boost converter and buck-boost converter. A 65W prototype of LED driver has been simulated and experimentally verified. Majority of the power is supplied by FBPBC, while the buck-boost converter handles the remaining power. Buck-boost converter is also helpful in regulating the LED current. Paralleled operation enables the input ripple cancellation which is advantageous with battery or ultra-capacitor as DC source.

The boost converter has high efficiency, lower input and output ripple, and a higher power density. It is also useful in increasing overall power rating by additional blocks. By replacing the diodes by SR MOSFETs, the converter efficiency has significantly improved. The converter configuration uses an auxiliary inductor to obtain ZVS. This reduces switching losses. Efficiency of 93.42% is obtained for full illumination with Si MOSFET and above 95 % with SiC MOSFET. Even at reduced lamp power levels with dimming, high efficiencies are observed.

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