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RESEARCH ARTICLE

Mechanism and Analytical Model for Switching Transient Process in SiC 3L-ANPC Converter

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ABSTRACT Silicon carbide three-level active neutral point clamped converters (SiC 3L-ANPC) have emerged as promising solutions for medium-voltage high-capacity applications. However, compared to traditional two-level converters, they exhibit a relatively higher presence of stray parameters. The combined impact of high dv/dt, di/dt and multiple stray parameters during the switching transient process can lead to non-ideal behaviors, including voltage and current overshoots, along with oscillations. These issues contribute to increased switching losses and limitations in power handling. Therefore, a thorough evaluation of the switching transient process becomes imperative to ensure the proper design and protection of 3L-ANPC converters. An analytical model is proposed in this article that accurately characterizes the switching transient process of SiC 3L-ANPC converters. The model is developed based on a comprehensive analysis of the switching transient mechanism. By focusing on specific pivotal moments within the transient process, the model significantly reduces computational time. Moreover, these distinct moments carry explicit physical significance and possess universal applicability. Experimental results validate the effectiveness of the proposed model, showcasing a maximum calculation error of less than 6% for transient overshoots. The insights presented in this article provide guidance for designing circuit parameters in SiC 3L-ANPC converters, aiding in the mitigation of overvoltage issues.

INDEX TERMS SiC MOSFET, switching transient, 3L-ANPC, analytical model, parasitic parameters.

I. INTRODUCTION

In the rapidly advancing realm of power electronics, the silicon carbide (SiC) power devices have revolutionized converter design by offering high switching speeds and minimized switching losses [1], [2]. Concurrently, the three-level active neutral point clamped (3L-ANPC) converter has garnered significant attention owing to its compelling attributes, including low device voltage requirements, superior output power quality, and minimal electromagnetic interference [3], [4], [5]. The SiC 3L-ANPC power converter embodies a dual advantage paradigm. Consequently, it has emerged as a focal point in international research endeavors [6], [7] and stands as a highly competitive solution within the global aviation sector for medium-voltage, large-capacity, high-performance power converters [8], [9].

However, within the high-speed switching transient process of SiC devices, non-ideal behaviors such as voltage/current overshoots and oscillations have emerged as significant impediments, impeding the enhancement of converter performance. This challenge is particularly prominent in the context of 3L-ANPC converter, where the transient commutation circuit presents notably greater intricacy than that of a two-level circuit. Multiple commutation circuits exhibit coupling, each involving numerous switches, connecting lines, and parasitic parameters, intensifying the severity of switching transient non-ideal behaviors [10]. In contrast to Si IGBT, SiC MOSFET demonstrates distinct characteristics including reduced reverse transfer capacitance and larger output capacitance, leading to elevated dv/dt and di/dt and

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exacerbated voltage and current overshoots. These factors contribute to intricate interactions between the switching transient and the parasitic parameters within both the device and circuit, resulting in diverse electromagnetic transient process behaviors. Therefore, it becomes indispensable to understand the processes and the mechanisms of switching transients in SiC 3L-ANPC converters for further elevating the application potential of SiC power devices and facilitating the efficient, high-quality, and highly reliable utilization. Subsequently, efforts should be directed towards managing the short time-scale switching transient behaviors and regulating them within controllable states.

Extensive analysis and research have been dedicated to exploring the switching transient process of the SiC MOSFETs, leading to significant advancements. The majority of research on switching transients has primarily centered around discrete devices [11], [12], [13], [14], switch-diode combination circuits [15], [16], [17], switch-switch combination circuits [18], [19], [20], [21], or two-level converters [22]. However, different articles propose varying hypotheses concerning the current rise and voltage drop stages in SiC MOSFETs. For instance, in [15], the proposition is that during SiC MOSFET turn-on, current increases precede voltage decrease. This perspective suggests that the drain-source voltage remains relatively stable until the current reaches the load current threshold. Conversely, [20] contends that the current rise and voltage drop occur simultaneously and should not be treated as distinct events. Such contrasting viewpoints in assumptions can yield disparate outcomes when modeling switch transients. Furthermore, the intricate topology of the 3L-ANPC circuit exacerbates the divergence between these results.

Several studies have explored the switching transient behavior of SiC 3L-ANPC converters [10], [23], [24], [25]. In [23], an analysis of the commutation circuits of 3L-ANPC converters is conducted, delving into the on and off characteristics of power devices in different commutation circuits. However, the conclusion is derived from double-pulse experiments, lacking the establishment of a corresponding mathematical model and exhibiting a relatively weak theoretical foundation. Reference [24] presents an analytical model for the drain-source overvoltage of SiC MOSFETs in 3L-ANPC converters. Nevertheless, this analytical model is presented in matrix form, making it less intuitive in reflecting the influence of diverse parasitic parameters on voltage overshoot. Both [10] and [25] propose control methods to mitigate the switching transient non-ideal behavior of SiC 3L-ANPC converters, yet there is an absence of analysis on the mechanism behind this non-ideal behavior. Currently, for SiC 3L-ANPC converters, there exists a dearth of a comprehensive analytical model that elucidates the coupling effects between different circuits and establishes the relationship between SiC MOSFET overvoltage, overcurrent, and parasitic parameters.

The predominant approach in current research involves circuit simulation or numerical models. However, these method lacks intuitive depiction of the coupling between transient voltage/current overshoot and system elements, limiting its applicability in engineering practices. Moreover, short-time scale system-level simulations encounter challenges such as prolonged simulation durations and frequent convergence issues. Hence, it is crucial to investigate the quantitative relationship between the switching transient process and system elements in SiC 3L-ANPC converters. This entails establishing an analytical model of the switching transients and achieving a quantitative evaluation of voltage/current overshoots by directly substituting parameters.

In response to these challenges, this article presents an analytical model aimed at understanding the switching transient process within SiC 3L-ANPC converters, derived from an in-depth comprehension of commutation mechanisms. The proposed model employs a piecewise linearization approach, effectively segmenting the SiC MOSFETs' switch transient process into distinct stages based on the external circuit status. By calculating specific circuit states at certain times, this model accurately forecasts the entire switch transient process, markedly improving computational efficiency. Experimental validation demonstrates the model's efficacy in precisely predicting the switching transient process of the configured SiC 3L-ANPC setup, with a maximum calculation error of less than 6% for transient overshoots. Compared to circuit simulation methods, this proposed model offers a clearer depiction of coupling relationships and significantly enhances calculation speed. This enhancement establishes a robust scientific foundation for subsequent investigations into non-ideal transient behavior of switches and facilitates optimization in design practices.

The rest of this paper is organized as follows. In section II, the commutation mechanism of 3L-ANPC and the generation mechanism of non-ideal behaviors in switching transients are discussed. Then, the analytical model for the switching transient process of SiC 3L-ANPC converters is presented in section III. Analytical and experimental results are given in section IV. Guidance for the design of circuit parameters in SiC 3L-ANPC converters is also offered to facilitate the mitigation of overvoltage issues. Eventually, section V includes the conclusion of this paper.

II. MODULATION STRATEGY AND NON-IDEAL BEHAVI-ORS OF SIC 3L-ANPC CONVERTER

Fig. 1 illustrates the schematic diagram of the three-phase 3L-ANPC circuit, where S_{Xn} (X ∈ (A, B, C) and n ∈ (1, 2, …, 6)) represents a SiC MOSFET in Kelvin package. Specifically, S_{X1} and S_{X2} form the upper bridge arm, while S_{X3} and S_{X4} constitute the lower bridge arm, and S_{X5} and S_{X6} compose the output bridge arm. C_{bank_1} and C_{bank_2} represent the bus capacitors, respectively. L_{stray_1} and L_{stray_2} denote the positive and negative DC bus parasitic inductances, including the parasitic inductance of the neutral line. Furthermore, R_{load} and L_{load} represent the load resistance and inductance parameters, respectively. The blue box in the lower left corner indicates the equivalent circuit diagram of

TABLE 1. Typical modulation schemes and switching modes for 3L-ANPC converters.

Modulation Scheme	Output positive voltage (P state)	Output zero voltage (0 state)	Output negative voltage (N state)	Features
Opposite-side Clamping Method	S_1, S_3, S_5 are turned on	S_1, S_3, S_6 are turned on (0^+ state, used when outputting positive voltage) S_2, S_4, S_5 are turned on (0^- state, used when outputting negative voltage)	S_2, S_4, S_6 are turned on	S_5-S_6 is a high-frequency switch pair in full cycle complementary with severe uneven heating
Same-side Clamping Method	S_1, S_3, S_5 are turned on	S_2, S_3, S_5 conducted (0^+ state, used when outputting positive voltage) S_2, S_3, S_6 are turned on (0^- state, used when outputting negative voltage)	S_2, S_4, S_6 are turned on	S_1-S_2 and S_4-S_3 are complementary high-frequency switching pairs in the positive and negative halves, respectively
Full-path Clamping Method	S_1, S_3, S_5 are turned on	S_1, S_3, S_5, S_6 are turned on	S_2, S_4, S_6 are turned on	S_1-S_2-S_5-S_6 and S_4-S_3-S_5-S_6 are complementary high-frequency switching pairs in the positive and negative halves, respectively, with high switching loss

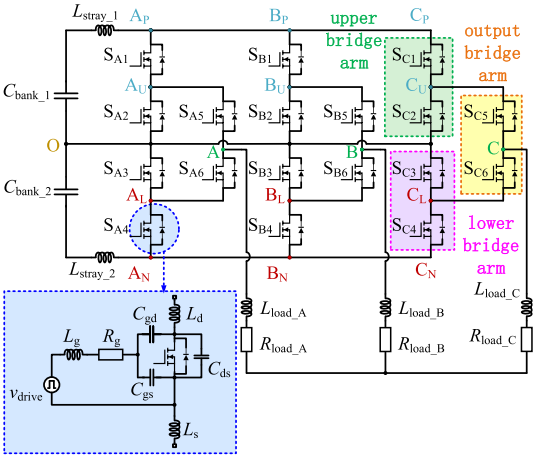


FIGURE 1. Schematic diagram of a three-phase 3L-ANPC converter.

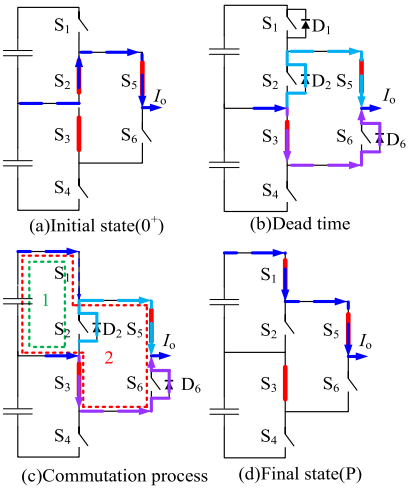


FIGURE 2. Schematic diagram of the commutation from 0^+ state to P state by the same-side clamping method.

the SiC MOSFET, taking into account the primary parasitic parameters. This equivalent circuit includes R_g, which represents the total gate drive resistance, and C_{gd}, C_{gs}, and C_{ds}, which represent the junction capacitances. Additionally, L_d, L_s, and L_g correspond to the drain, source, and gate parasitic inductances, respectively. These parasitic inductances incorporate the device lead inductance and external line parasitic inductance.

The 3L-ANPC converter can produce three output levels—positive (P), negative (N), and zero (0)—using four current branches and employing multiple methods for zero level operation [26], [27]. Considering the variations in zero level current paths, three prevalent modulation strategies are commonly employed in 3L-ANPC converters: the opposite-side clamping method, the same-side clamping method, and the full-path clamping method [26], as delineated in Table 1. Notably, in the switching process from the 0^+ state to the P state using the opposite-side clamping method, S_2 remains inactive. The load current switches from S_3-S_6 to S_1-S_5, involving only one commutation loop. Conversely, both the same-side and full-path clamping methods encompass two simultaneous commutation loops for the same switching transient process. For instance, considering the same-side clamping method illustrated in Fig. 2, the conducting switch is depicted by the red short wire for clarity.

Initially, S_2, S_3, and S_5 are turned on, while the remaining switches are turned off, directing the load current I_o through S_2 and S_5. Assuming that the SiC MOSFET's on-state resistance is lower than the body diode resistance, the shunt between the body diode of S_6 and S_3 is deemed negligible. The sequential transition from the 0^+ state to the P state unfolds in two steps: first, S_2 deactivates, followed by a dead time, after which S_1 activates. When S_2 switches off, the load current divides into two paths: D_2-S_5 and S_3-D_6, each carrying approximately $I_o/2$, as depicted in Fig. 2(b). S_1 activation triggers commutation processes—short loop commutation from D_2 to S_1 and long loop commutation from S_3-D_6 to S_1-S_5—occurring concurrently, as depicted in Fig. 2(c). These commutation processes are interconnected through variations

TABLE 2. Physical meaning of the segmentation points in S_{A1} turn-on process.

Segmentation Points	Physical Meaning
t_0	The gate drive voltage v_{drive} abruptly changes from V_L to V_H
t_1	The gate source voltage v_{gs_A1} reaches the threshold voltage V_{th}
t_2	The short commutation loop completes the commutation, i.e. i_{d_A2} reaches 0
t_3	The long commutation loop completes the commutation, i.e. $i_{d\ A6}$ reaches 0
t_4	v_{ds_A6} beyond v_{ds_A2}
t_5	$i_{d\ A6}$ reaches 0
t_6	i_{d_A2} reaches 0

in S_1 voltage and current, introducing complexity into the 3L-ANPC converter's commutation involving five devices in the bridge arm. This complexity starkly contrasts with the commutation transient of the two-level converter.

When the converter's output current $I_o > 0$, the transition from the 0^+ state to the P state involves the cutoff of D_2 and D_6. Consequently, S_2 and S_6 can act as SiC MOSFET output capacitors, causing terminal voltage overshoots and oscillations due to capacitor charge and discharge effects. These charging and discharging currents influence the S_1 branch, resulting in corresponding overshoots and oscillations in its current. Conversely, during the transition from the P state to the 0^+ state, S_1 simulates an output capacitor, causing voltage overshoots in S_1 and current overshoots in the S_2 and S_6 branches. When the DC power supply transfers energy to the load via the inverter during the transition from the 0^+ state to the P state, the resulting switching transient experiences more pronounced voltage and current overshoots compared to the transition from the P state to the 0^+ state. These effects are mirrored during transitions between the N state and 0^- state.

The previously stated conclusion presumes a positive output voltage with the load current exiting the converter. However, in cases involving inductive or capacitive loads, there can be a phase shift between the current and voltage waveforms. This phase difference can alter the occurrence of non-ideal behavior during the switching transient if the output voltage opposes the direction of the load current. For example, consider Fig. 2, where if the load current I_o flows from the load back into the converter during the 0^+ state, the freewheeling stage after S_2 deactivation routes I_o through the parasitic diode D_1 rather than D_2. Consequently, transient non-ideal behavior is observed in the voltages of S_2 and S_6, as well as the current in S_1. Subsequently, during the S_1 activation process, the commutation occurs solely within S_1, specifically between the body diode and the MOSFET channel, thereby minimizing evident non-ideal behavior.

III. ANALYTICAL MODEL FOR SWITCHING TRANSIENT PROCESS IN SIC 3L-ANPC CONVERTER

The analytical model proposed for the SiC 3L-ANPC converter's switching transient process relies on a piecewise linear model [15]. The methodology involves several key steps: Initially, a thorough understanding of the switching mechanism allows for a logical segmentation of the transient process, enabling approximations of linear changes in voltage and current within defined stages. This segmentation ensures that each transition point holds distinct physical significance. Equivalent transient commutation circuits are formulated for these stages, utilizing Kirchhoff's law to establish a system of differential equations. The subsequent step leverages the linear assumption by substituting dv, di, and dt with Δv, Δi, and Δt within each stage. This substitution leads to difference equations, simplifying the definition of the duration Δt for every stage. Solving each stage involves incorporating Δt back into the difference equations, facilitating the derivation of analytical formulas for the final voltage and current values within each stage. Additionally, maintaining the linear assumption enables the derivation of analytical formulas for the voltage and current at specific moments within these stages.

To mitigate errors caused by oversimplification of the nonlinear junction capacitances and transconductance of SiC MOSFETs, this article adopts the junction capacitances and transconductance models proposed in [20]:

$$C_{xss}(v_{ds}) = \frac{C_{0xss} - C_{hxss}}{1 + (v_{ds}/V_b)^r} + C_{hxss}, \quad x = o, i, r \tag{1}$$

$$g_{fs}(i_d) = k_1 k_2 \left(\frac{i_d}{k_1}\right)^{1-1/k_2} \tag{2}$$

where C_{hxss} and C_{0xss} represent the capacitance values at high and zero voltages, respectively, and V_b, r, k_1, and k_2 need to be fitted based on the device datasheet [28]. The nonlinear capacitance and transconductance values are calculated as the average of integrals within each stage, allowing for a better representation of the dynamic characteristics during the switching transient process in the SiC 3L-ANPC converter.

A. TURN-ON MODEL

This section provides a clear focus on deriving the turn-on model, specifically using the turn-on process of S_{A1} as a detailed example. The schematic diagram displaying voltage and current waveforms is shown in Fig. 3. Traditional studies on SiC MOSFET turn-on processes often segment it

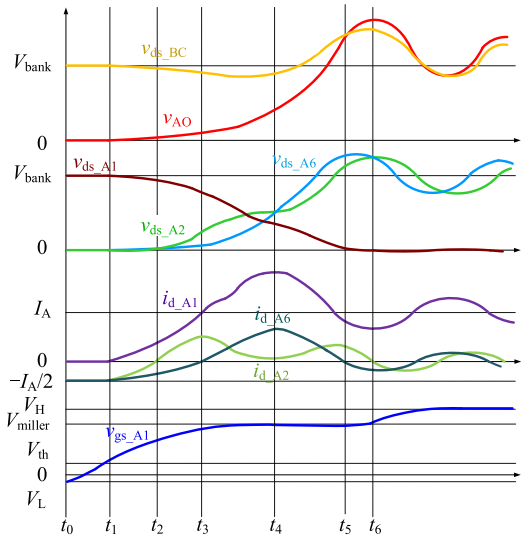


FIGURE 3. Schematic diagram of voltage and current waveforms during the turn-on process of S_{A1}.

into delay, current rise, and voltage drop stages, primarily centered on device behavior. However, within the 3L-ANPC converter, solely relying on S_{A1}'s behavior for stage division is inadequate due to concurrent changes in S_{A2} and S_{A6} transitioning from freewheeling to cutoff. Therefore, the proposed analytical model in this article delineates stages based on equivalent circuit changes, considering the overall circuit behavior. The transient process is segmented into 5 stages, with stage 4 further subdivided into 3 sub-stages to refine the segmented linear model. Each segmentation point is defined with explicit physical significance, outlined comprehensively in Table 2.

At t_0, phase A is in the state depicted in Fig. 2(b), where the load current I_A is flowing through the branches D_{A2}-S_{A5} and S_{A3}-D_{A6}. The drain-source voltage $v_{ds\_A2(t0)}$ and $v_{ds\_A6(t0)}$ can be approximated as the negative value of the renewal diode voltage drop, denoted as $-V_{DB}$, and $v_{ds\_A1(t0)}$ can be calculated as the difference between the upper bus voltage V_{bank} and $v_{ds\_A2(t0)}$, i.e., $V_{bank} + V_{DB}$. Each stage's modeling approach will be described in detail, considering the simplified transient circuit.

Stage 1 (t_0 - t_1): This is the turn-on delay stage. At t_0, the gate drive voltage of S_{A1}, v_{drive}, transitions from V_L to V_H. Consequently, the gate-source voltage v_{gs_A1} starts to increase exponentially from V_L to the threshold voltage V_{th}, reaching this threshold at t_1. In practical engineering, the parasitic inductance L_g of the gate loop is typically designed to be small, and the rate of change of current i_{g_A1} is not significant. Therefore, the impact of L_g on the switching transient voltage and current can be considered negligible. The transient equivalent circuit of the S_{A1} gate loop during this stage is illustrated in Fig. 4, where C_{iss_A1} represents the input capacitor of S_{A1}.

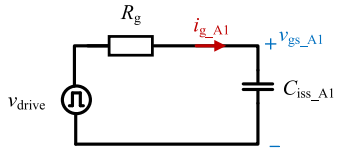


FIGURE 4. Transient equivalent circuit of 3L-ANPC in S_{A1} turn-on process: Stage 1.

The kinetic model of this stage is shown in (3) and (4):

$$v_{drive} = R_g i_{g\_A1} + v_{gs\_A1} \tag{3}$$

$$i_{g\_A1} = C_{iss\_A1} \frac{dv_{gs\_A1}}{dt} \tag{4}$$

The duration of this stage is solved by combining (3) and (4):

$$t_1 - t_0 = R_g C_{iss\_A1} \ln\left(\frac{V_H - V_L}{V_H - V_{th}}\right) \tag{5}$$

During the turn-on delay stage, the voltage and current on the power circuit maintain the same values as at time t_0. This means that there is no significant voltage or current variation on the power circuit.

Stage 2 (t_1 - t_2): During this stage, the conductive channel width of S_{A1} begins to increase, causing a drop in v_{ds_A1}. The short commutation loop formed by S_{A1} and D_{A2} is synchronized with the long commutation loop formed by S_{A1}, S_{A5}, D_{A6}, and S_{A3}. Assuming that I_A is equally shared between the two commutation loops at t_1, and if the parasitic inductance of the long commutation loop is m times that of the short loop, the commutation rate of the former will be approximately $1/m$ of that of the latter. At t_2, the current in the short commutation loop (i_{d_A2}) is fully commuted, while approximately $1/m$ of the current in long commutation loop (i_{d_A6}) is commuted.

The transient equivalent circuit for this stage is shown in Fig. 5, which includes L_1 and L_2 as the total parasitic inductance of the drain and source of S_{A1} and S_{A2}, respectively. L_{3_1}, L_{3_2}, and L_{3_3} represent the total parasitic inductance of the drain and source of S_{A5}, S_{A6}, and S_{A3}, respectively. L_4 represents the parallel equivalent parasitic inductance of the upper half bridge arm of phases B and C. L_3 is defined as the sum of L_{3_1}, L_{3_2}, and L_{3_3}. The direction of the current flowing into the drain of the SiC MOSFET is defined as the positive direction of the branch current.

The junction capacitances and parasitic inductances in the two commutation loops for phase A are mainly considered in Fig. 5, while ignoring the effect of the on-state resistances of S_{A3} and S_{A5}. During the turn-on transient of S_{A1}, the inductive voltage on the upper bus inductor L_{stray_1} will impact the terminal voltage of the upper bridge arm of phases B and C due to the rapid change of i_{d_A1}, and then excite oscillation currents for charging and discharging of their junction capacitors. The majority of the oscillation currents in phases B and C flow directly back to the bus capacitor through the neutral point, having less impact on the lower half bridge arm and the output bridge arm. So only two switches of phases B and C are considered in Fig. 5, respectively.

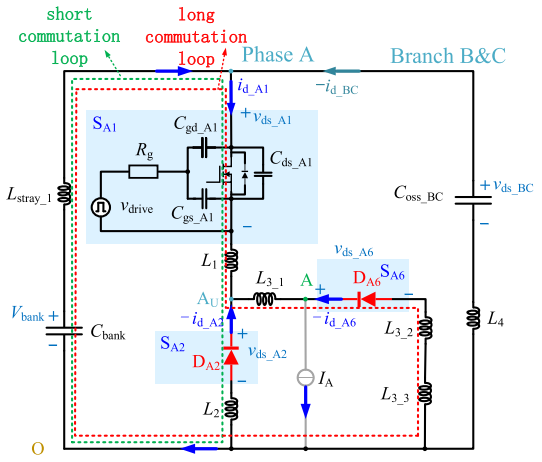


FIGURE 5. Transient equivalent circuit of 3L-ANPC in S_{A1} turn-on process: Stage 2.

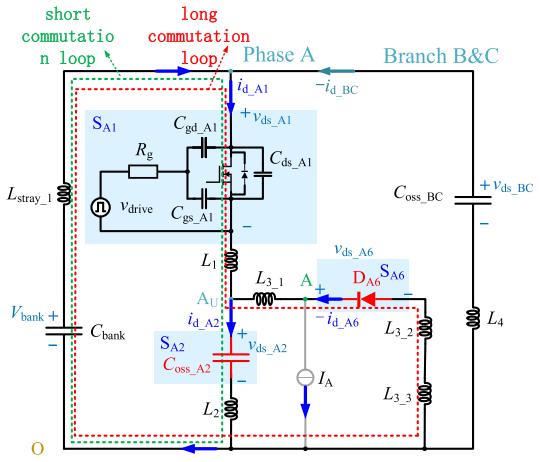


FIGURE 6. Transient equivalent circuit of 3L-ANPC in S_{A1} turn-on process: Stage 3.

Furthermore, regardless of whether phases B and C are in the P, N, 0^+, or 0^- states, only one SiC MOSFET will be turned on in the upper bridge arm of both phases, while the other one behaves as an output capacitor. In this article, the parallel branches of the upper bridge arms of phases B and C are equivalently represented by a new branch "B&C", where C_{oss_BC} represents the equivalent capacitance of the upper bridge arm branches of phases B and C, approximately twice the output capacitor of SiC MOSFET. The current i_{d_BC} represents the total transient current flowing through the upper bridge arms of phases B and C.

The gate current of S_{A1}, i_{g_A1}, can be expressed by (6) and (7):

$$i_{g\_A1} = \frac{V_H - V_{gs\_A1}}{R_g} \tag{6}$$

$$i_{g\_A1} = C_{iss\_A1}\frac{dv_{gs\_A1}}{dt} - C_{gd}\frac{dv_{ds\_A1}}{dt} \tag{7}$$

The combination of (6) and (7) results in (8):

$$V_H - v_{gs\_A1} = R_g C_{iss\_A1}\frac{dv_{gs\_A1}}{dt} - R_g C_{gd}\frac{dv_{ds\_A1}}{dt} \tag{8}$$

For the short commutation loop, there is:

$$V_{bank} = v_{ds\_A1} + (L_1 + L_{stray\_1})\frac{di_{d\_A1}}{dt} + v_{ds\_A2} + L_2\frac{di_{d\_A2}}{dt} + L_{stray\_1}\frac{di_{d\_BC}}{dt} \tag{9}$$

For the long commutation loop, there is:

$$V_{bank} = v_{ds\_A1} + (L_1 + L_{stray\_1})\frac{di_{d\_A1}}{dt} + v_{ds\_A6} + L_3\frac{di_{d\_A6}}{dt} + L_{stray\_1}\frac{di_{d\_BC}}{dt} \tag{10}$$

For the "B&C" brunch, there are:

$$V_{bank} = v_{ds\_BC} + L_{stray\_1}\frac{di_{d\_A1}}{dt} + (L_4 + L_{stray\_1})\frac{di_{d\_BC}}{dt} \tag{11}$$

$$i_{d\_BC} = C_{oss\_BC}\frac{dv_{ds\_BC}}{dt} \tag{12}$$

For S_{A1}, there is:

$$v_{gs\_A1(t_2)} = \frac{i_{d\_A1(t_2)} - i_{d\_A1(t_1)}}{g_{fs}} + v_{gs\_A1(t_1)} \tag{13}$$

The quadratic equation with respect to the parameter (t_2-t_1) is obtained by combining (8)-(13) and replacing all the differential terms with difference terms (e.g. dv_{ds_A1} is replaced by $v_{ds\_A1(t2)} - v_{ds\_A1(t1)}$:

$$A_1(t_2 - t_1)^2 + B_1(t_2 - t_1) + C_2 = 0 \tag{14}$$

The solution of (14) provides the duration of stage 2, where the specific parameter values are listed in Table 6 in the Appendix. By substituting the time duration back into (8)-(13), the values of voltage and current at t_2 can be determined. Then, based on the assumption of linearity, the voltage and current at any moment between t_1 and t_2 can be calculated. For example, the analytical formulas of i_{d_A1} and v_{ds_A1} are as shown in (15) and (16).

$$i_{d\_A1(t)} = \frac{A_1(m+1)I_A}{(-B_1 + \sqrt{B_1^2 - 4A_1C_1})m}(t - t_1) \tag{15}$$

$$v_{ds\_A1(t)} = -\frac{4A_1^2((m+1)(L_1 + L_{stray}) + mL_2)I_A}{(-B_1 + \sqrt{B_1^2 - 4A_1C_1})^2 m}(t - t_1) + V_{bank} + V_{DB} \tag{16}$$

Stage 3(t_2 - t_3): At t_2, i_{d_A2} reaches 0, and subsequently, S_{A2} is represented in the transient equivalent circuit as the MOSFET output capacitor C_{oss_A2}. As C_{oss_A2} charges, the voltage v_{ds_A2} gradually increases. Meanwhile, D_{A6} continues to conduct until t_3. Fig. 6 illustrates the transient equivalent circuit for this stage.

For S_{A1}, there is:

$$v_{gs\_A1(t_3)} = \frac{i_{d\_A1(t_3)} - i_{d\_A1(t_2)}}{g_{fs}} + v_{gs\_A1(t_2)} \tag{17}$$

For S_{A2}, there is:

$$i_{d\_A2} = C_{oss\_A2}\frac{dv_{ds\_A2}}{dt} \tag{18}$$

By combining equations (8)-(12), (17) and (18), and replacing all the differential terms in the equation with difference terms, a quadratic equation with respect to the parameter (t_3-t_2) can be derived as follows:

$$A_2(t_3-t_2)^4 + B_2(t_3-t_2)^3 + C_2(t_3-t_2)^2 + D_2(t_3-t_2) + E_2 = 0 \tag{19}$$

The non-negative real number solution of this equation represents the duration stage 3. The calculation of voltage and current at any moment between t_2 and t_3 follows a similar procedure as the previous stage and does not need to be repeated. The specific parameter values in (19) can be found in Table 6 in the Appendix.

Stage 4(t_3 - t_6): The transient equivalent circuit for this stage is illustrated in Fig. 7. At t_3, D_{A6} stops freewheeling, and then it can be represented as an output capacitor C_{oss_A6}. v_{gs_A1} enters Miller platform, while v_{ds_A1} continues to decrease, and i_{d_A1} exhibits an initial overshoot before entering into oscillation at t_4. At t_3, C_{oss_A2} has been charging for some time, while C_{oss_A6} has just started charging, resulting in a charge imbalance between them. Since the C_{oss_A2} branch and the C_{oss_A6} branch are connected in parallel, this charge imbalance leads to mutual charging and discharging behavior, resulting in higher frequency oscillations of i_{d_A2} and i_{d_A6}. The coupling effect of C_{oss_A2} and C_{oss_A6} is the most significant difference in switch transient behavior between the 3L-ANPC circuit and the two-level circuit.

In this stage, the behavior of each voltage and current becomes more complex. To enhance the accuracy of the segmented linear model, this stage is further divided into three sub-stages.

Sub-stage 4.1(t_3 - t_4): The terminal voltage of capacitor C_{oss_A6} is approximately zero at t_3, which gives it a high charge absorption capacity. It not only absorbs charge from the bus capacitor C_{bank} but also absorbs charge from capacitor C_{oss_A2}. As a result, the current i_{d_A2} decreases while i_{d_A6} increases. As the voltage difference between v_{ds_A2} and v_{ds_A6} decreases, the rate at which C_{oss_A6} absorbs charge from C_{oss_A2} slows down. At t_4, $v_{ds\_A2} = v_{ds\_A6}$, and the charge absorption between them temporarily stops. At this point, the rate of change of currents i_{d_A2} and i_{d_A6} can be approximated as zero.

Sub-stage 4.2(t_4 - t_5): Although $v_{ds\_A2} = v_{ds\_A6}$ at t_4, i_{d_A2} and i_{d_A6} are not equal, indicating that C_{oss_A2} and C_{oss_A6} are not charging at the same rate. As a result, there is a voltage difference between v_{ds_A2} and v_{ds_A6} again. This time, C_{oss_A2} absorbs charge from C_{oss_A6}, leading to an increase in i_{d_A2} and a decrease in i_{d_A6}. Eventually, i_{d_A6} drops to 0 at t_5, while v_{ds_A6} reaches its peak. At t_5, S_{A1} is nearly fully turned on, and as an approximation, v_{ds_A1} drops to $V_{miller} - V_{th}$.

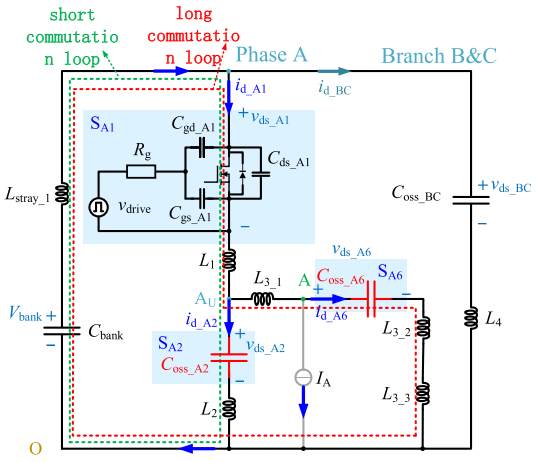


FIGURE 7. Transient equivalent circuit of 3L-ANPC in S_{A1} turn-on process: Stage 4.

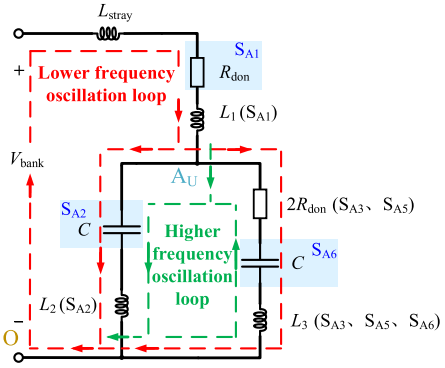


FIGURE 8. Transient equivalent circuit of 3L-ANPC in S_{A1} turn-on process: Stage 5.

Sub-stage 4.3 (t_5 - t_6): At t_6, i_{d_A2} drops to 0 and v_{ds_A2} reaches its peak. In this article, S_{A1} is considered fully turned on at t_6, and v_{ds_A1} drops to $I_A \times R_{don}$, where R_{don} represents the on-state resistance of the SiC MOSFET and I_A is the output current of phase A. Although v_{ds_A6} starts to decay and oscillate from t_5, this article still assumes linearity for v_{ds_A6} in this sub-stage to simplify the equation-solving process.

Within the three sub-stages of stage 4, for S_{A1}, there are:

$$v_{gs\_A1(t_{k+1})} = \frac{i_{d\_A1(t_{k+1})} - i_{d\_A1(t_k)}}{g_{fs}} + v_{gs\_A1(t_k)} \quad (k = 3, 4, 5) \tag{20}$$

For S_{A6}, there is:

$$i_{d\_A6} = C_{oss\_A6}\frac{dv_{ds\_A6}}{dt} \tag{21}$$

Combining (8)-(12), (18), (20), and (21), and replacing all the differential terms in the equation with difference terms, the quadratic equations with respect to the parameters (t_4-t_3), (t_5-t_4), and (t_6-t_5) are obtained:

$$A_k(t_{k+1}-t_k)^4 + B_k(t_{k+1}-t_k)^3 + C_k(t_{k+1}-t_k)^2$$

$$+ D_k(t_{k+1} - t_k) + E_k = 0(k = 3, 4, 5) \tag{22}$$

The non-negative real number solutions of the equation correspond to the durations of the respective sub-stages. The calculation of voltage and current at any moment between t_3 and t_6 follows a similar procedure as the previous phase and will not be reiterated. The specific parameter values in (22) can be found in Table 6 in the Appendix.

Stage 5 (after t_6): This is the oscillation stage of turn-on process. After t_6, the gate voltage v_{gs_A1} of S_{A1} continues to exponentially increase to V_H. The voltages v_{ds_A2}, v_{ds_A6}, v_{AO}, and v_{ds_BC} start to decay and exhibit oscillations.

In order to analyze the oscillation frequency in the complex topology of the 3L-ANPC, this article simplifies the analysis by ignoring the energy exchange between phases. Instead, the focus is placed on the energy exchange between the junction capacitances and the parasitic inductances within each phase. The transient equivalent circuit for the oscillation stage is shown in Fig. 8, where $C_{oss\_A2} \approx C_{oss\_A6} \approx C$.

The equivalent impedance of the circuit in Fig. 8 can be represented as:

$$Z_{eq} = \frac{1}{2j\omega C} + j\omega(L_1 + L_{stray\_1} + \frac{L_2 + L_3 - 2\omega^2 L_2 L_3 C}{4 - 2\omega^2(L_2 + L_3)C}) \tag{23}$$

According to (23), a total of four solutions of the resonant frequency can be obtained, of which two negative ones are invalid, and two positive ones are the actual resonant frequency, in (24) and (25), as shown at the bottom of the next page.

Among these frequencies, f_1 is the lower oscillation frequency, resulting from the combination of inductance and capacitance components in the red loop in Fig. 8. The variation direction of each branch current under f_1 is the same. On the other hand, f_2 is a higher oscillation frequency, mainly occurring in the green loop of Fig. 8, with S_{A2} and S_{A6} experiencing opposite changes. In Fig. 8, the output voltage v_{AO} can be approximated as the voltage between point A_U and point O, and its oscillation peaks and valleys are primarily determined by f_1. Part of the higher frequency oscillation current will "leak" into the lower frequency oscillation loop, causing the waveform of v_{AO} to appear as a non-standard attenuation sine wave. However, the higher frequency vibration amplitude of v_{AO} is relatively low. Therefore, the output voltage analytical model proposed in this article mainly focuses on considering oscillations with f_1 as the resonant frequency. This choice minimizes the computational complexity of the model while capturing the main oscillation trend effectively.

The equivalent resistance of the circuit in Fig. 8 can be determined as follows:

$$R_{eq} = 2R_{don}\frac{|Z_{2//6}|^2}{|Z_6|^2} + R_{don} \tag{26}$$

where Z_6 represents the total impedance of the S_{A6} branch, and $Z_{2//6}$ represents the impedance of the parallel branch consisting of S_{A2} and S_{A6}.

Therefore, the expression for v_{AO} can be obtained as follows:

$$v_{AO} = V_{bank} + (v_{AO(t_6)} - V_{bank})e^{-\frac{R_{eq}}{2L_{eq}}(t-t_6)}\cos(2\pi f_1(t - t_6)) \tag{27}$$

where L_{eq} refers to the equivalent inductance in (23).

Similarly, the analytical expressions for v_{ds_A2}, v_{ds_A6} and v_{ds_BC} can be derived using similar methods.

B. TURN-OFF MODEL

In contrast to the turn-on process, the turn-off process of the 3L-ANPC does not involve a state change of the switching device from the current-continuing diode to the output capacitor. As a result, the number of stages in the turn-off process is relatively small. Fig. 9 illustrates the schematic waveforms of each voltage and current during the turn-off process, using the example of S_{A1} turn-off.

At t_0', phase A is in the P state, and I_A flows to the load through S_{A1}-S_{A5}. $v_{ds\_A1(t0')}$ is equal to $R_{don} \times I_A$, and $v_{ds\_A2(t0')}$ and $v_{ds\_A6(t0')}$ are equal to the upper bus voltage V_{bank}. In this article, the turn-off transient process of 3L-ANPC is divided into three stages and the segmentation points are shown in Table 3, all of which also have clear physical meaning.

Stage 1 (t_0' -t_1'): This is the turn-off delay stage. At t_0', the gate drive voltage of S_{A1} v_{drive} transitions from V_H to V_L. Simultaneously, the gate-source voltage v_{gs_A1} exponentially decreases from V_H and reaches the Miller voltage V_{miller} at t_1'. During this stage, all other voltages and branch currents on the power side remain unchanged. Therefore, the turn-off delay process can still be described by (3) and (4).

The time duration of this stage is solved by combining (3) and (4), as shown in (28):

$$t_1' - t_0' = R_g C_{iss\_A1} \ln(\frac{V_H - V_L}{V_{miller} - V_L}) \tag{28}$$

Stage 2 (t_1' -t_2'): During this stage, S_{A1} experiences a voltage rise, following the same transient equivalent circuit as shown in Fig. 7. In the drive loop, v_{gs_A1} decreases approximately linearly from V_{miller} to V_{th}. In the power loop, v_{ds_A2} and v_{ds_A6} decrease from the upper bus voltage V_{bank} to approximately 0, while v_{ds_A1} increases from $R_{don} \times I_A$ to its peak value, and i_{d_A1} decreases from I_A to 0. Throughout this stage, v_{ds_A2} and v_{ds_A6} exhibit significant variations, while the influence of parasitic inductors L_2 and L_3 on the transient behavior is relatively small. Therefore, this article assumes that the currents i_{d_A2} and i_{d_A6} are equal until t_2'.

The quadratic equation with respect to the parameter (t_2' - t_1') can be derived by combining (8)-(12), along with (18) and (21), and replacing all the differential terms with their corresponding difference terms:

$$A_1'(t_2' - t_1')^2 + B_1'(t_2' - t_1') + C_2' = 0 \tag{29}$$

The solution of (29) provides the duration of this stage. Similarly to the turn-on process, this duration is then used

TABLE 3. Physical meaning of the segmentation points in S_{A1} turn-off process.

Segmentation Points	Physical Meaning
t_0'	The gate drive voltage v_{drive} abruptly changes from V_H to V_L
t_1'	The gate source voltage v_{gs_A1} reaches the Miller voltage V_{miller}
t_2'	i_{d_A1} reaches 0

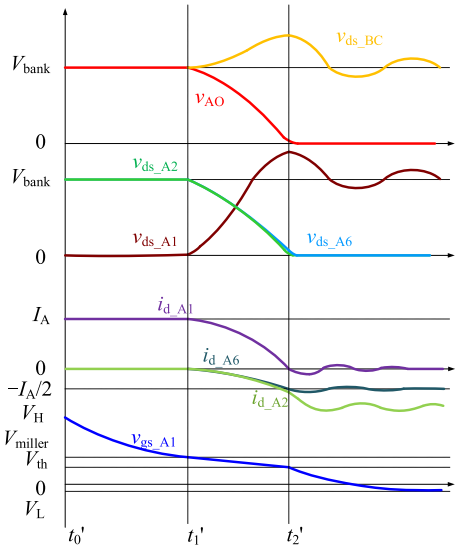


FIGURE 9. Schematic diagram of voltage and current waveforms during the turn-off process of S_{A1}.

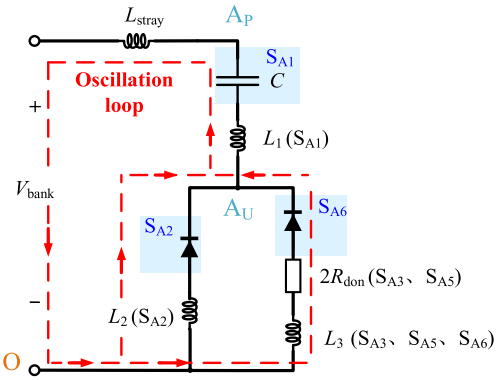


FIGURE 10. Transient equivalent circuit of 3L-ANPC in S_{A1} turn-off process: Stage 3.

to substitute back into the difference form of the equations, allowing for the determination of the voltages and currents at t_2'. By assuming linearity, the voltage and current at any moment within this stage can be calculated. The specific parameters in (29) are taken as follows:

$$\begin{cases} A_1' = (V_L - \dfrac{V_{miller} + V_{th}}{2}) \\ B_1' = R_g(C_{gd}V_{bank} - C_{iss\_A1}(V_{th} - V_{miller})) \\ C_1' = R_g(2L_1 + 2L_{stray} + L_2)C_{gd}I_A \end{cases} \tag{30}$$

Stage 3 (aftert_2'): This is the oscillation stage of turn-off process. The transient equivalent circuit is shown in Fig. 10. In the power loop, v_{ds_A1} experiences a significant overshoot and oscillation. On the other hand, v_{ds_A2} and v_{ds_A6} reach the diode on-state voltages $-V_{DB}$ after t_2', resulting in smaller and negligible voltage oscillations. In the drive loop, v_{gs_A1} exponentially decreases from V_{th} to V_L.

By neglecting the resistance term in Fig. 10, the resonant frequency is determined as follows:

$$f' = \frac{1}{2\pi\sqrt{(L_1 + L_{stray} + \frac{L_2L_3}{L_2+L_3})C}} \tag{31}$$

Then the equivalent resistance is calculated as:

$$R_{eq}' = (2R_{don} + R_{DB})\frac{|Z_{2//6}|^2}{|Z_6|^2} + R_{DB}\frac{|Z_{2//6}|^2}{|Z_2|^2} \tag{32}$$

where Z_2 represents the total impedance of the S_{A2} branch, and R_{DB} represents the diode forward conduction resistance.

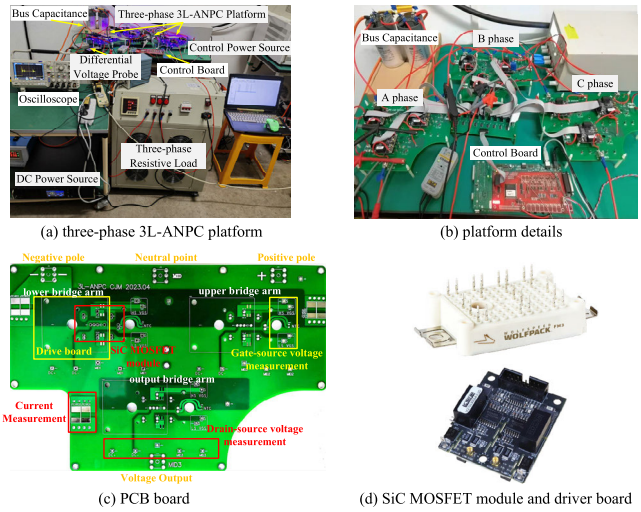
Hence, the analytical expression for v_{ds_A1} can be given as:

$$v_{ds\_A1} = V_{bank} + (V_{ds\_A1(t_2')} - V_{bank})e^{-\frac{R_{eq}'}{2L_{eq}}(t-t_2')} \times \cos(2\pi f'(t - t_2')) \tag{33}$$

Similarly, the analytical expression for v_{ds_BC} can be approximated.

$$f_1 = \frac{1}{2\pi}\sqrt{\frac{2(L_1 + L_{stray}) + (L_2 + L_3) - \sqrt{2^2(L_1 + L_{stray})^2 + (L_2 - L_3)^2}}{2C\left((L_1 + L_{stray})(L_2 + L_3) + L_2L_3\right)}} \tag{24}$$

$$f_2 = \frac{1}{2\pi}\sqrt{\frac{2(L_1 + L_{stray}) + (L_2 + L_3) + \sqrt{2^2(L_1 + L_{stray})^2 + (L_2 - L_3)^2}}{2C\left((L_1 + L_{stray})(L_2 + L_3) + L_2L_3\right)}} \tag{25}$$



(a) three-phase 3L-ANPC platform (b) platform details

(c) PCB board (d) SiC MOSFET module and driver board

FIGURE 11. Experimental platform of 3L-ANPC converter.

TABLE 4. Circuit parameters.

Parameters	Value	Parameters	Value
L_{stray} /nH	117.5552	C_{iss} /nF	6.6
L_1 /nH	15.0279	C_{oss} /nF	0.29~7
L_2 /nH	30.9861	C_{rss} /nF	0.019~2.5
L_3 /nH	111.1774	R_g /Ω	2
L_4 /nH	143.3677	g_{fs} /S	0~10

It should be noted that the analytical model proposed in this article may require slight adjustments based on the actual application scenarios. When the load current or the relationship between L_2 and L_3 changes, the sequence of events may differ slightly from the schematic diagram in Fig. 3. For example, v_{ds_A2} may peak after the zero-crossing point of i_{d_A6}, resulting in changes in the sequence of t_5 and t_6 in Fig. 3. However, in such cases, the segmentation points of stages can be appropriately adjusted, resulting in a substantial reduction in the calculation error.

IV. EXPERIMENTAL VERIFICATION

The three-phase 3L-ANPC platform is designed for experimental verification, as shown in Fig. 11. The SiC MOSFETs CAB016M12FM3 rated at 1200V, 78A from Wolfspeed are used. The parasitic parameters in the circuit are extracted by ANSYS Q3D, as shown in Table 4.

Experiments are carried out under the conditions of $R_g = 12\Omega$ and $R_g = 3\Omega$ respectively. The experimental and the analytical results under different operational conditions are compared in Fig. 12 to Fig. 15, when the bus voltage $2V_{bank} = 700$V and the load current $I_A = 10$A.

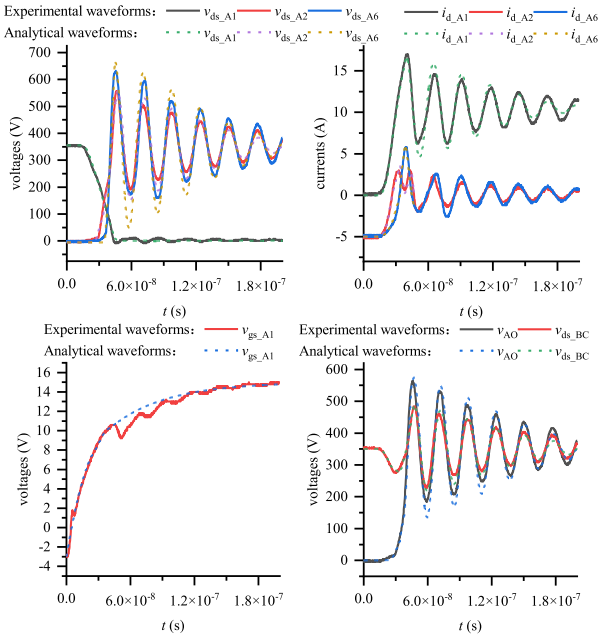


FIGURE 12. Experimental and analytical results in S_{A1} turn-on process under $R_g = 12\Omega$.

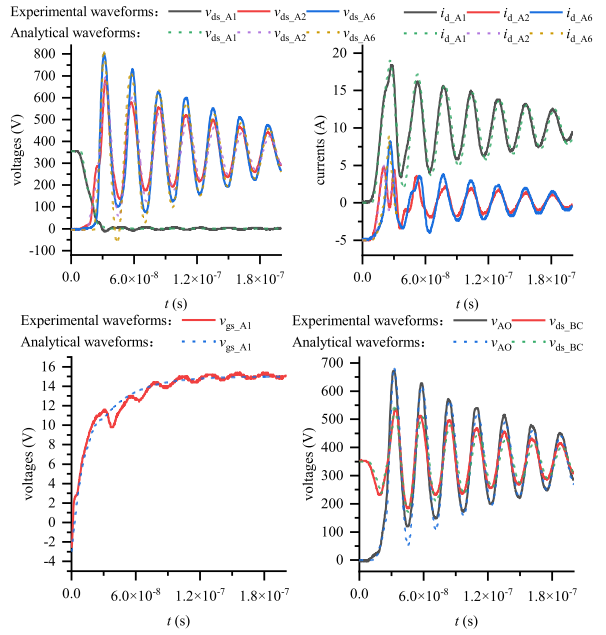


FIGURE 13. Experimental and analytical results in S_{A1} turn-on process under $R_g = 3\Omega$.

Fig. 13 and Fig. 14 present the experimental and analytical waveforms for the S_{A1} turn-on process, while Fig. 15 and Fig. 16 illustrate the waveforms for the S_{A1} turn-off process. The assessed voltages and currents encompass v_{ds_A1}, v_{ds_A2}, v_{ds_A6}, i_{d_A1}, i_{d_A2}, i_{d_A6}, v_{gs_A1}, v_{AO}, and v_{ds_BC}, among others. Table 5 provides the calculation errors for each peak, demonstrating that the maximum error is below 6%. The results indicate an agreement between the proposed

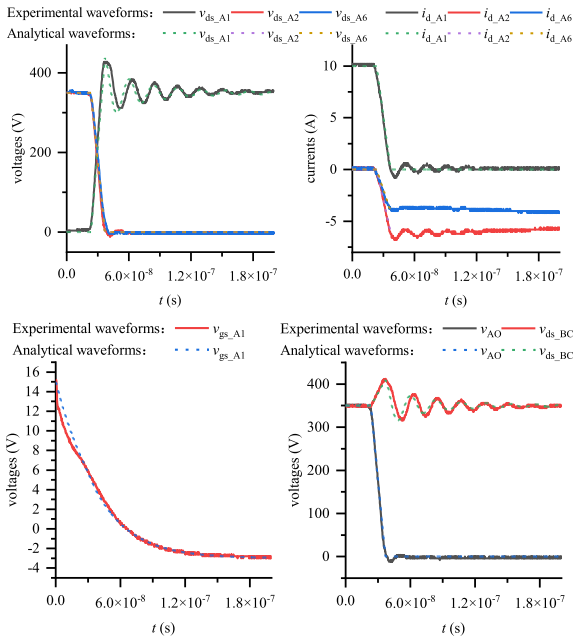


FIGURE 14. Experimental and analytical results in S_{A1} turn-off process under $R_g = 12\Omega$.

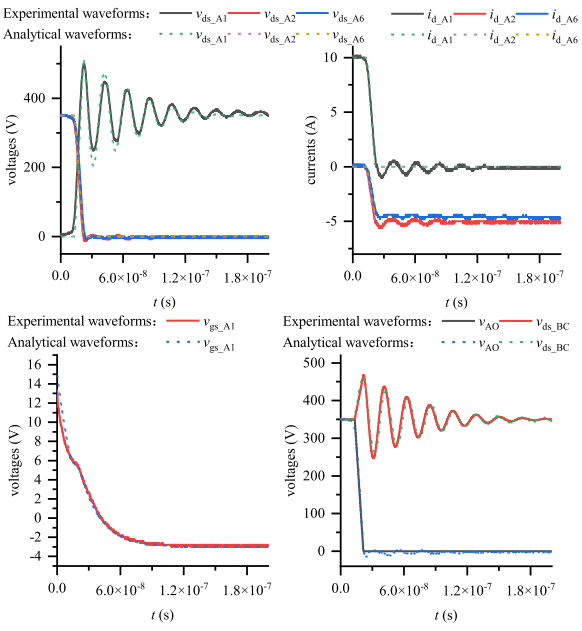


FIGURE 15. Experimental and analytical results in S_{A1} turn-off process under $R_g = 3\Omega$.

analytical model and the experimental findings, affirming the correctness and validity of the proposed model in capturing the switching transient process of the 3L-ANPC. The proposed analytical model offers several significant advantages, including fast calculation speed, intuitive coupling relationships, and easy applicability. For example, when using Pspice for circuit simulation, simulating a fundamental cycle of an aviation 400Hz AC power supply takes approxi-

TABLE 5. Calculation errors.

Parameters		Overshoot Multiplier		Error	
		$R_g = 3\Omega$	$R_g = 12\Omega$	$R_g = 3\Omega$	$R_g = 12\Omega$
S_{A1} turn-on process	v_{ds_A2}/V	1.897	1.588	2.02%	1.44%
	v_{ds_A6}/V	2.280	1.797	5.22%	4.78%
	v_{AO}/V	1.908	1.608	3.23%	1.58%
	v_{ds_BC}/V	1.508	1.374	1.21%	2.11%
	i_{d_A1}/A	1.820	1.680	3.33%	3.53%
S_{A1} turn-off process	v_{ds_A1}/V	1.405	1.211	2.45%	1.87%
	v_{ds_BC}/V	1.322	1.177	4.47%	1.98%

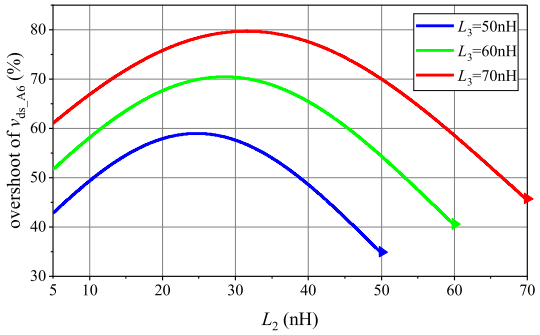


FIGURE 16. Experimental and analytical results in S_{A1} turn-off process under $R_g = 3\Omega$.

mately 28 minutes, with an average of 29 seconds for each switching cycle (f_{sw} = 25kHz). On the other hand, the proposed analytical model achieves a computation time of only 0.02 seconds per switching cycle. This represents a substantial improvement in computational efficiency, being approximately 1500 times faster than the circuit simulation.

Furthermore, the experimental results reveal insights regarding the voltage stress and output voltage distortion during the turn-on and turn-off transient processes in the 3L-ANPC converter. Firstly, it is observed that the turn-on transient process causes higher device voltage stress and more severe output voltage distortion compared to the turn-off transient process under the same driving resistance. Additionally, it is found that the voltage stress on the output bridge arm devices is greater than that on the upper and lower bridge arm devices. This is attributed to the fact that the output bridge arm devices are situated in the long commutation loop, where the parasitic inductance is significantly higher. As a result, the impact on the output bridge arm devices is more pronounced.

Significantly, the voltage stress experienced by the output bridge arm device in the 3L-ANPC converter is influenced not only by the parasitic inductance of the long commutation loop but also by the parasitic inductance of the short com-

TABLE 6. Equation coefficients for each stage in turn-on process.

Stage	Equation coefficients	
Stage 2	$A_1 = 2g_{fs}V_H - 2g_{fs}V_{gs\_A1(t1)} - I_{d\_A1(t2)}$	(A1)
	$B_1 = -2R_gC_{iss\_A1}i_{d\_A1(t2)}$	(A2)
	$C_1 = -4g_{fs}R_gC_{gd}((L_1 + L_{stray\_1})I_{d\_A1(t2)} + L_2(I_{d\_A2(t2)} - I_{d\_A2(t1)}))$	(A3)
Stage 3	$A_2 = 2g_{fs}V_H - 2g_{fs}V_{gs\_A1(t2)} - I_{d\_A6(t3)}$	(A4)
	$B_2 = -2R_gC_{iss\_A1}(I_{d\_A6(t3)} + I_A - I_{d\_A1(t2)}) - 2g_{fs}R_gC_{gd}(2V_{ds\_A1(t2)} - 2V_{bank} + V_{ds\_A6(t3)} + V_{ds\_A6(t2)})$	(A5)
	$C_2 = 4(2g_{fs}V_H - 2g_{fs}V_{gs\_A1(t2)} - I_A + I_{d\_A1(t2)})L_2C_{oss\_A2} + 4L_3C_{oss\_A2}I_{d\_A6(t2)}$ $-4g_{fs}R_gC_{gd}((L_1 + L_{stray\_1})(I_A - I_{d\_A1(t2)}) - L_3I_{d\_A6(t2)})$	(A6)
	$D_2 = -8R_gC_{iss\_A1}C_{oss\_A2}(L_2(I_A - I_{d\_A1(t2)}) - L_3I_{d\_A6(t2)})$ $-8g_{fs}R_gL_2C_{gd}C_{oss\_A2}(2V_{ds\_A1(t2)} - 2V_{bank} + V_{ds\_A6(t3)} + V_{ds\_A6(t2)})$	(A7)
	$E_2 = -16g_{fs}R_gC_{gd}C_{oss\_A2}(L_2(L_1 + L_{stray\_1})(I_A - I_{d\_A1(t2)})$ $-L_3(L_1 + L_{stray\_1} + L_2)I_{d\_A6(t2)})$	(A8)
Stage 4	$A_3 = -(g_{fs}R_gC_{gd} + C_{oss\_A2} + C_{oss\_A6})(V_{ds\_A6(t3)} - V_{ds\_A2(t3)})$	(A9)
	$B_3 = 4(g_{fs}V_H - g_{fs}V_{gs\_A1(t3)} + I_{d\_A2(t3)})(L_2C_{oss\_A2} - L_3C_{oss\_A6})$ $-2R_gC_{iss\_A1}(C_{oss\_A2} + C_{oss\_A6})(V_{ds\_A6(t3)} - V_{ds\_A2(t3)})$ $-4(g_{fs}R_gC_{gd} + C_{oss\_A2} + C_{oss\_A6})L_2I_{d\_A2(t3)}$	(A10)
	$C_3 = 4(C_{oss\_A2}V_{ds\_A2(t3)} + C_{oss\_A6}V_{ds\_A6(t3)})(L_2C_{oss\_A2} - L_3C_{oss\_A6})$ $-4g_{fs}R_gC_{gd}(2V_{ds\_A1(t3)} - 2V_{bank} + V_{ds\_A6(t3)})(L_2C_{oss\_A2} - L_3C_{oss\_A6})$ $-8R_gC_{iss\_A1}(C_{oss\_A2} + C_{oss\_A6})L_2I_{d\_A2(t3)} + 8R_gC_{iss\_A1}I_{d\_A2(t3)}(L_2C_{oss\_A2} - L_3C_{oss\_A6})$ $-4g_{fs}R_gC_{gd}((L_1 + L_{stray\_1})(C_{oss\_A2} + C_{oss\_A6}) + L_3C_{oss\_A6})(V_{ds\_A6(t3)} - V_{ds\_A2(t3)})$ $-4(g_{fs}R_gC_{gd} + C_{oss\_A2} + C_{oss\_A6})(L_2C_{oss\_A2}V_{ds\_A2(t3)} - L_3C_{oss\_A6}V_{ds\_A6(t3)})$	(A11)
	$D_3 = -8R_gC_{iss\_A1}(C_{oss\_A2} + C_{oss\_A6})(L_2C_{oss\_A2}V_{ds\_A2(t3)} - L_3C_{oss\_A6}V_{ds\_A6(t3)})$ $+8R_gC_{iss\_A1}(C_{oss\_A2}V_{ds\_A2(t3)} + C_{oss\_A6}V_{ds\_A6(t3)})(L_2C_{oss\_A2} - L_3C_{oss\_A6})$ $+16g_{fs}R_gC_{gd}((L_1 + L_{stray\_1})I_{d\_A2(t3)} + L_3I_{d\_A6(t3)})(L_2C_{oss\_A2} - L_3C_{oss\_A6})$ $-16g_{fs}R_gC_{gd}((L_1 + L_{stray\_1})(C_{oss\_A2} + C_{oss\_A6}) + L_3C_{oss\_A6})L_2I_{d\_A2(t3)}$	(A12)
	$E_3 = 16g_{fs}R_gC_{gd}(L_1 + L_{stray\_1})(C_{oss\_A2}V_{ds\_A2(t3)} + C_{oss\_A6}V_{ds\_A6(t3)})(L_2C_{oss\_A2} - L_3C_{oss\_A6})$ $+16g_{fs}R_gL_3C_{gd}C_{oss\_A6}V_{ds\_A6(t3)}(L_2C_{oss\_A2} - L_3C_{oss\_A6})$ $-16g_{fs}R_gC_{gd}((L_1 + L_{stray\_1})(C_{oss\_A2} + C_{oss\_A6}) + L_3C_{oss\_A6})(L_2C_{oss\_A2}V_{ds\_A2(t3)} - L_3C_{oss\_A6}V_{ds\_A6(t3)})$	(A13)
	$A_4 = (2g_{fs}V_H - 2g_{fs}V_{gs\_A1(t4)} - I_A + I_{d\_A1(t4)})C_{oss\_A6} - g_{fs}R_gC_{gd}I_{d\_A6(t4)} - (C_{oss\_A2}I_{d\_A6(t4)} - C_{oss\_A6}I_{d\_A2(t4)})$	
	$B_4 = -2R_gC_{iss\_A1}(C_{oss\_A2}I_{d\_A6(t4)} - C_{oss\_A6}(I_{d\_A6(t4)} + 2I_{d\_A2(t4)}))$ $-4g_{fs}R_gC_{gd}C_{oss\_A6}(V_{ds\_A1(t4)} - V_{bank} + V_{ds\_A6(t4)})$	(A14)
	$C_4 = 4(2g_{fs}V_H - 2g_{fs}V_{gs\_A1(t4)} - I_A + I_{d\_A1(t4)})L_2C_{oss\_A2}C_{oss\_A6} - 4C_{oss\_A2}C_{oss\_A6}(L_2I_{d\_A2(t4)} - L_3I_{d\_A6(t4)})$	(A15)
	$-4g_{fs}R_gC_{gd}C_{oss\_A6}((L_1 + L_{stray\_1})(I_A - I_{d\_A1(t4)}) - L_3I_{d\_A6(t4)}) - 4g_{fs}R_gL_2C_{gd}C_{oss\_A2}I_{d\_A6(t4)}$ $-4g_{fs}R_g(L_1 + L_{stray\_1})C_{gd}(C_{oss\_A2}I_{d\_A6(t4)} - C_{oss\_A6}I_{d\_A2(t4)})$	(A16)
	$D_4 = 8R_g(L_2 + L_3)C_{iss\_A1}C_{oss\_A2}C_{oss\_A6}I_{d\_A6(t4)}$ $-16g_{fs}R_gL_2C_{gd}C_{oss\_A2}C_{oss\_A6}(V_{ds\_A1(t4)} - V_{bank} + V_{ds\_A6(t4)})$	(A17)
	$E_4 = -16g_{fs}R_gL_2C_{gd}C_{oss\_A2}C_{oss\_A6}((L_1 + L_{stray\_1})(I_A - I_{d\_A1(t4)}) - L_3I_{d\_A6(t4)})$ $-16g_{fs}R_g(L_1 + L_{stray\_1})C_{gd}C_{oss\_A2}C_{oss\_A6}(L_2I_{d\_A2(t4)} - L_3I_{d\_A6(t4)})$	(A18)
Stage 5	$A_5 = i_{d\_A2(t5)}$	(A19)
	$B_5 = C_{oss\_A2}(2V_{ds\_A1(t5)} - 4V_{bank} + 4V_{ds\_A2(t5)} + 2V_{ds\_A1(t5)})$	(A20)
	$C_5 = -4(L_1 + L_{stray\_1} + L_2)C_{oss\_A2}I_{d\_A2(t5)} + 4(L_1 + L_{stray\_1} + L_3)C_{oss\_A6}I_{d\_A2(t5)}$	(A21)
	$D_5 = 8L_3C_{oss\_A2}C_{oss\_A6}(V_{ds\_A1(t5)} - 2V_{bank} + 2V_{ds\_A2(t5)} + V_{ds\_A1(t5)})$ $+16(L_1 + L_{stray\_1} + L_3)C_{oss\_A2}C_{oss\_A6}(V_{ds\_A2(t5)} - V_{ds\_A6(t5)})$	(A22)
	$E_5 = -16(L_1L_3 + L_{stray\_1}L_3 + L_1L_2 + L_{stray\_1}L_2 + L_2L_3)C_{oss\_A2}C_{oss\_A6}I_{d\_A2(t5)}$	(A23)

mutation loop. Fig. 15 illustrates the relationship between the overshoot percentage of v_{ds_A6} (with respect to V_{bank}) and the values of L_2 and L_3. It can be observed that the overshoot of v_{ds_A6} is affected by the values of L_2 and exhibits a non-monotonic behavior. Specifically, as L_2 increases, the overshoot of v_{ds_A6} initially increases, reaches a maximum value when L_2 is approximately equal to $L_3/2$, and then decreases. The minimum voltage overshoot occurs when L_2 is equal to L_3. Considering the typical design objective of limiting parasitic inductance in a circuit, this article disregards the case where L_2 exceeds L_3. The findings in Fig. 15 emphasize that the design of the 3L-ANPC converter should not only focus on restricting the parasitic inductance of the commutation loops but also aim to ensure that the values of L_2 and L_3 deviate significantly from the $L_2 = L_3/2$ relationship. By deviating from this relationship, the voltage overshoot and related stress on the output bridge arm device can be effectively minimized, promoting the reliable operation of the 3L-ANPC converter.

V. CONCLUSION

In this paper, the switching mechanism of 3L-ANPC converter is investigated. The focus is on analyzing the non-ideal behaviors during switching transients and understanding their generation mechanisms. An analytical model for the switching transient process in SiC 3L-ANPC converter is developed. Based on the theoretical analysis, simulation, and experimental study, the following conclusions have been drawn:

1) In the same-side and full-path clamping method employed in the 3L-ANPC converter, both long and short commutation loops are present which introduce additional complexities to the switching transient behavior of the converter. During the switching transient, electromagnetic energy is exchanged not only between the parasitic inductances and junction capacitances within the individual commutation loop but also between the junction capacitances in both commutation loops. This energy transfer between the different elements results in intricate dynamics of voltage and current waveforms across multiple switching devices.
2) When comparing the turn-on process with the turn-off process in the 3L-ANPC converter, it is observed that the former results in more severe voltage stress. Furthermore, in the 3L-ANPC topology, the output bridge arm devices experience greater voltage stress compared to the upper and lower bridge arm devices. This is mainly due to their location in the long commutation loop, which exhibits higher parasitic inductance. It is important to note that the voltage stress experienced by the devices in both commutation loops is influenced not only by the parasitic parameters of their respective commutation loops but also by the parasitic parameters of the other commutation loop. This introduces a non-monotonic relationship between the voltage stress and the parasitic parameters. In particular, when the parasitic inductance of the short commutation loop, represented by L_2, is approximately equal to half of the parasitic inductance of the long commutation loop, represented by L_3, it has the greatest influence on the voltage stress of the output bridge arm devices. Therefore, in the design process, it is crucial to deviate from this relationship as much as possible to mitigate the voltage stress on the output bridge arm devices.
3) The analytical model proposed in this paper for the switching transient process of SiC 3L-ANPC converters exhibits high accuracy, with a maximum error in peak calculation of less than 6%. In comparison to circuit simulation methods and numerical iterative calculations, the modeling approach presented in this paper offers several advantages. Firstly, it provides clearer and more intuitive coupling relationships between variables, allowing for a better understanding of the system dynamics during switching transients. Additionally, the calculation speed of the proposed model is significantly faster, enabling quick evaluation and analysis of system performance. The analytical model serves as a tool for conducting quantitative assessments of the impact of non-ideal behavior during switching transients on overall system performance. It also facilitates research on methods to suppress such non-ideal behavior, system optimization design, verification of design schemes, determination of safe operating points, and adjustment of protection thresholds. By using the model, design and application processes can be made more informed, reducing the potential for blind design decisions and enhancing the overall efficiency and reliability of the system.

APPENDIX

See Table 6.

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