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RESEARCH ARTICLE

Control of Utility Interfacing Modular High Frequency AC Link Converter Based on Fundamental Current Estimation

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ABSTRACT This work proposes a cell-to-cell voltage balance and flexible power sharing control strategy for 1-phase utility interfacing 1-phase modular high frequency AC link (HFAC-L) converter. Input series-output parallel (ISOP) configuration having cascaded multilevel front end converter (CMFEC) in the first stage and dual active bridge (DAB) converter in the second stage is the topology of focus in this work. This topology is extensively used in the solid state transformer (SST). Flexible power sharing is accomplished by estimating the high frequency link (HF-link) fundamental current component of each cell. No high bandwidth current sensors are used. Moreover, this scheme also incorporates parametric estimation of each HF-link inductor. This feature makes it robust to gradual ageing related parametric variation. Irrespective of the number of cells, this strategy requires only two low bandwidth current sensors, for grid current and load current measurements. Compared to erstwhile approaches, this flexible power sharing strategy allows for controlled zero power (phase-shedding/plug-out) operation of a cell while still regulating its DC link voltage. The proposed strategy also makes the subsequent phase-addition/plug-in process seamless without the need for pre-charge circuits. This scheme can also be reconfigured to operate in output current regulation mode. These features are validated through experiments performed on a 1.6 kW laboratory prototype.

INDEX TERMS Active front end converter, dual active bridge converter, estimation, modular high frequency AC link converter, observer, parameter identification, solid state transformer (SST), sensorless.

I. INTRODUCTION

High frequency AC link (HFAC-L) converter has been among the most scrutinized and promising power electronics solutions of the last decade. This topology has invited attention from both industry and academia. The high frequency link (HF-link) of the HFAC-L converter houses the much discussed dual active bridge (DAB) converter. It is extensively adopted in another solution of great contemporary interest, the solid state transformer (SST) [1], [2]. The modular HFAC-L composed of cascaded multilevel front-end converter (CMFEC) followed by DAB forms the core power processing and utility interfacing circuitry of the most popular type-D (three-stage) variants of SSTs [3], [4]. As a case study, this research focuses on type-D SST applications since it is the most preferred choice for many industrial applications such as traction system and medium voltage distribution system, because of its weak line-load dynamic coupling resulting in better load and line side disturbance rejection performance [5], [6], [7], [8], [9], [10].

Modular configurations allows scalability, use of standard low-power semiconductor devices, and improved reliability. For high input voltage and power applications of modular SSTs, the input series output parallel (ISOP) configuration is preferred [11]. The grid interfacing CMFEC in the first stage converts medium voltage AC (MVAC) from the grid to medium voltage DC (MVDC). The second stage uses modular dual active bridge (MDAB) converters to convert MVDC to LVDC. These first two stages of the three-stage Type-D SST denoted as modular HFAC-L are the focus of

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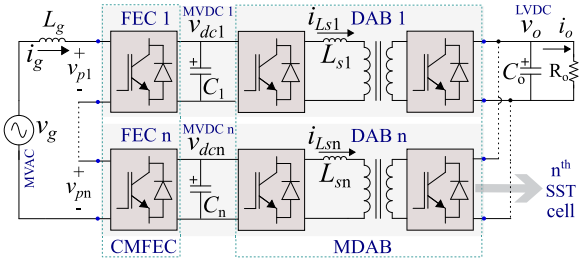
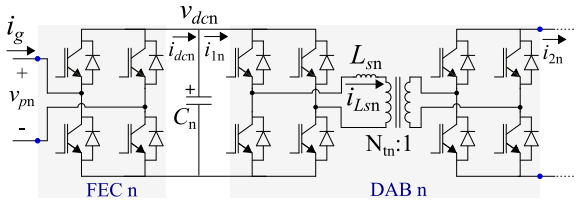
TABLE 1. List of key abbreviations.

Abbreviation	Definition
HFAC-L	high frequency AC link
SST	solid state transformer
CMFEC	cascaded multilevel front end converter
DAB	dual active bridge
HF-Link	high frequency link
ISOP	input series output parallel
MVAC	medium voltage AC
MVDC	medium voltage DC
LVDC	low voltage DC
HBW	high bandwidth
GA	generalised average
SPS	single phase shift



(a) Modular HFAC-L converter in ISOP configuration.



(b) Circuit diagram of n^{th} cell.

FIGURE 1. Circuit diagram of modular 1-phase HFAC-L converter used in a type-D SST topology.

TABLE 2. List of main symbols.

Symbol	Definition
v_g	1-phase MVAC grid voltage
v_{dcn}	MVDC voltage of n^{th} cell
v_o	LVDC side output voltage
v_{pn}	pole voltage of n^{th} cell FEC
v_{pT}	summation of all FEC pole voltges
i_g	grid current
i_{dcn}	DC-link output current of n^{th} cell FEC
i_{1n}	DC-link input current of n^{th} cell DAB
i_{2n}	DC-link output current of n^{th} cell DAB
i_{Lsn}	HF-link current of n^{th} cell
i_o	LVDC side load current
$\langle v_o \rangle_0$	zeroth Fourier coefficient of v_o
$\langle i_{Lsn} \rangle_1$	fundamental Fourier coefficient of i_{Lsn}
$\langle i_{Lsn} \rangle_1^I$	imaginary part of $\langle i_{Lsn} \rangle_1$
$\langle i_{Lsn} \rangle_1^R$	real part of $\langle i_{Lsn} \rangle_1$
i_{pken}	estimated peak of i_{Lsn}
L_g	grid interfacing inductance
L_{sn}	HF-link inductance of n^{th} cell
N_{tn}	HF-link turns ratio of n^{th} cell
C_n	MVDC-link capacitance of n^{th} cell
C_o	LVDC side capacitance
R_o	output load resistance
d_n	modulation-duty-function of n^{th} cell FEC
$d_{\varphi n}$	phase-shift-duty-ratio of n^{th} cell DAB
x_d	d-axis component of variable x. $x \in [v_g, i_g, d_n]$
x_q	q-axis component of variable x. $x \in [v_g, i_g, d_n]$
y_e	estimation of y. $y \in [L_{sn}, \langle i_{Lsn} \rangle_1, \langle i_{Lsn} \rangle_1^I, \langle i_{Lsn} \rangle_1^R]$
w_g	grid angular frequency
w	angular frequency of DAB
k_n	Inner current loop gain of n^{th} cell DAB

this work. Fig. 1 shows this modular topology with its first two stages in ISOP configuration.

Cell to cell power and MVDC voltage balance in the modular HFAC-L stage of SSTs are two imperative requirements for any control scheme. Power and voltage imbalance stems primarily from the cell to cell parameter mismatch in the high frequency (HF) link inductance values and transformer turns ratio values in the DAB stage. More importantly, the variation in HF-link inductance value is more of a concern as it can vary due to ageing related factors, where as the turns ratio is a fixed designed physical parameter which only depends on the number of turns [12]. Although parametric mismatch are also bound to be present in device resistances, HF link transformers and MVDC capacitors, it is the HF link inductor that most significantly affects the throughput power in the DAB stage. An imbalance in power or voltage leads to an unequal distribution of IGBT switch stress, uneven heat dissipation and undesirable grid current distortion.

Table 1 lists the two main categories of control strategies for balancing power and voltage [13]. The first category, strategy A, focuses on achieving voltage balance in the CMFEC stage and power balance in the DAB stage [14], [15], [16], [17], [18]. The second category, strategy B, involves realizing both voltage and power balance through the DAB stage [19], [20], [21], [22], [23], [24].

One of the earliest work adopting strategy A is reported in [14]. The major limitation of this work is the requirement of expensive high bandwidth (HBW) current sensors and high sampling rate ADCs to measure and sample each HF link inductor currents. To eliminate the need of these HBW sensors, a coordinated control is proposed in [15] and [16], by generating DAB phase shift compensation from FEC

TABLE 3. Broad categorisation of power and voltage balance control strategies.

Strategy	Stage	Control Input	Balance Objective
A	CMFEC	Equal/Unequal duty	MVDC balance
	DAB	Phase shift	Power balance
B	CMFEC	Only Equal duty	- - -
	DAB	Phase shift	MVDC & Power balance

duty ratio by linking their active components. However, the MVDC link dynamic performances for these approaches are slow with settling time more than 50 grid cycles. In [17], three phase power balance and MVDC balance controller are employed in CMFEC, while assigning common phase shift for all DABs. Parametric uncertainty in the HF link inductor is not addressed. In [18], an improved fault tolerant scheme based on strategy A is presented. However, it assumes equal parametric values across all DABs. A model predictive control approach is proposed in [25]. It achieves power balancing for ISOP-DAB converters in a power electronic traction transformer (PETT) without using HBW current sensors. However, it assumes the knowledge of the HF link inductance values and does not address parametric uncertainties due to ageing.

One of the earliest work based on strategy B is reported in [19], where a common duty cycle is used for all FECs. However, parametric variation in the DAB stage is not addressed. Power balance strategy in the DAB stage is widely adopted for DAB converters connected in ISOP mode [26], [27], [28]. A double control loop for DAB stage based on dual phase shift PWM technique is proposed in [20]. Voltage balancing technique for PETT application and for modular smart transformer is proposed in [21] and [22] respectively. These strategies involve assigning same duty cycle to all FECs in CMFEC stage to control the summation of MVDCs and regulating individual MVDC in the DAB stage. This control structure is very simple to implement. However, the impact of load disturbance on dynamic response of MVDCs remains a concern as both MVDCs and LVDC are being regulated by same central control structure. Furthermore, DAB stage parametric variation in SST cells is not considered in [22] during validation. In [24], a nonlinear control strategy is developed that aims to decouple all control objectives allowing fast stabilization of MVDCs and LVDC without any interactive coupling.

In all these schemes, falling under strategy B, the control structure is based on the reduced order model of DAB, which does not consider HF link inductor current (i_{Ls}) as a state variable. Hence, it does not facilitate direct control of this variable and the current regulation. Moreover, as all FEC modules in CMFEC are assigned with a common modulation duty cycle, which inherently limits this control strategy in its use of the entire degrees of freedom that the topology has to offer. One of the fallout is its inability to execute flexible power sharing. Flexible power sharing includes equal power sharing, controlled unequal power sharing and zero power sharing (phase-shedding/plug-out operation). Zero power sharing capability in a controlled manner can be very useful in contingency situations where a particular cell has to be phased out or shutdown. This capability may also be beneficial during low load periods. Certain cells can be temporarily deactivated from sharing power so that remaining cells operate close to their rated power [29]. Recently, attempts have been made to improve the dynamics of MVDC voltages by introducing power-linked model predictive control (PLPC) [30] with modification in strategy B. However, no experimental results are demonstrated regarding unequal or zero power sharing. Predictive control for fault tolerant condition is proposed in [31] and [32]. Sharing unequal power while still maintaining MVDCs is demonstrated experimentally but transient performance are not presented.

Quite a few works have been reported using observer-based techniques for control. Employing nonlinear disturbance observer, current sensorless control of a single cell DAB is put forward in [33], to estimate the load current. However, the HF-link inductor current is not included in the dynamic model. The direct and quadrature component of HF-link current is estimated using a terminal DC-link current sensor and reduced order observer in [34]. Based on generalised average (GA) modelling of a single cell DAB [35], an observer based high bandwidth current sensorless dual loop control for a single cell DAB is presented in [36]. However, these methods can not be directly extended to modular SST application. Cell-to-cell HF-link parameter identification and parameter uncertainty due to ageing are the main challenges while implementing current sensorless power balance control in a modular SST.

The key contribution of the proposed method compared to erstwhile approaches are described sequentially. This method provides a direct control handle on the fundamental component of DAB inductor current without the need of measuring it. It can be configured for both voltage and current regulation. This makes the flexible power sharing feasible. If one cell power becomes zero, the control algorithm automatically adjusts the modulation duty cycle of the FEC module of that cell to zero, while increasing power in other cells. During this phase-shedding operation of a particular cell, MVDC link voltage is still regulated tightly by the

TABLE 4. Comparison of control schemes for modular HFAC-link converter in ISOP configuration.

Reference	Strategy	Control of i_{Ls} fundamental component	HBW Sensor	Controlled flexible power sharing	Approx. MVDC settling time ∗
[14]	A	Yes	Yes	Both equal, unequal and zero ◇	4-5
[15], [16]	A	No	No	Only equal	> 50
[17]	A	No	No †	Only equal	12
[18]	A	No	No †	Both equal, unequal and zero ◇	NA
[19]	B	No	No †	Only equal	NA
[20]	B	No	No	Only equal	25 §
[21]	B	No	No	Only equal	28
[22]	B	No	No †	Only equal	3
[24]	B	No	No	Only equal	12 §
[25]	MPC	No	No †	Only equal	NA
[30]	PLPC	No	No	Only equal	3
[31]	PLPC	No	No	Both equal, unequal and zero ◇	NA
Proposed	A	Yes	No	Both equal, unequal and zero ◇	3-4

◇ Zero power sharing = Phase-shedding/plug-out operation. ∗ In grid cycles (For sudden load variation), § For power reversal.
† Equal/Known inductance in DAB HF-Link, NA - Not available.

proposed control scheme by only making its current flow zero, for zero power transfer. Hence, during subsequent phase-addition (plug-in) operation, this zero power sharing cell can be quickly reactivated as its MVDC link voltage is already precharged. One big advantage is it does not require any additional MVDC capacitor precharging circuit, helping to achieve fast phase-addition dynamics. Comparison of the proposed control scheme with other approaches, highlighting its key contributions is presented in Table 4.

The rest of this article is organized as follows. In Section II, modelling and control of HFAC-link converter for SST application is discussed. The step by step working procedure of the proposed control scheme is presented in Section III. Experimental validation of the proposed control scheme is presented in Section IV. Finally, this work is summarized and concluded in Section V.

II. MODELLING AND CONTROL OF MODULAR SST

The mathematical modelling and control of modular SST is presented in this section. The modelling techniques adopted for CMFEC and modular DAB are dq-frame modelling and generalised average (GA) modelling respectively. Control scheme for the CMFEC with proposed feed-forward compensation, proposed sensorless fundamental envelope estimation based power balance control by modular DAB and online inductance estimation of each DAB are discussed sequentially.

A. CONTROL SCHEME FOR THE CMFEC STAGE

Three control objectives are set for this stage. These are - grid side (MVAC side) unity power factor (UPF) operation, regulation of the total summation of MVDC voltages, MVDC voltage balance. Fig. 2 shows the overall scheme.

To meet the grid side objective, traditional dq-model based 1-phase vector control scheme has been employed [14]. This has been implemented in the 1-phase system by generating an imaginary orthogonal phase using the second order generalised integrator (SOGI) [37]. The orthogonal axes are α and β, which, are subsequently transformed to the rotating dq frame. The corresponding dynamic equations are [14],

$$\begin{bmatrix} \dot{i}_{gd} \\ \dot{i}_{gq} \end{bmatrix} = \begin{bmatrix} -\frac{r_g}{L_g} & \omega_g \\ -\omega_g & -\frac{r_g}{L_g} \end{bmatrix} \begin{bmatrix} i_{gd} \\ i_{gq} \end{bmatrix} - \begin{bmatrix} \frac{\sum_{k=1}^{n} d_{dn} v_{dcn}}{L_g} \\ \frac{\sum_{k=1}^{n} d_{qn} v_{dcn}}{L_g} \end{bmatrix} + \begin{bmatrix} \frac{v_{gd}}{L_g} \\ \frac{v_{gq}}{L_g} \end{bmatrix}, \tag{1}$$

$$\dot{v}_{dcn} = \frac{1}{C_n}\Big[d_n i_g - i_{1n}\Big], \tag{2}$$

where, x_d, x_q are the d-axis, q-axis components of the variable x, and $x \in \big[v_g, i_g, d_n\big]$. The grid side voltage and current drawn from the grid are denoted by v_g and i_g respectively. v_{dcn} and d_n are MVDC voltage and modulation duty ratio of n^{th} FEC cell respectively. L_g is the grid interfacing inductance and r_g is its parasitic resistance. ω_g is the angular grid frequency. The MVDC link capacitance of the n^{th} cell is represented as C_n.

Initially v_g is aligned with the d-axis by making $v_{gq} = 0$, using SOGI based phase locked loop (PLL). This makes the d-axis and q-axis component correspond to the active and reactive power respectively. Grid current reactive component

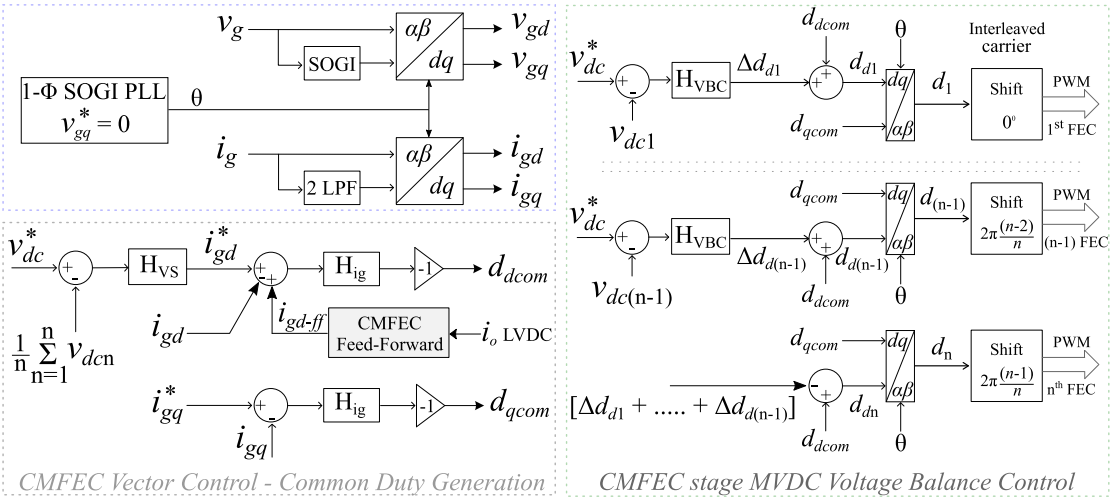


FIGURE 2. Control scheme for the CMFEC stage with proposed feed-forward compensation.

reference is zero for UPF operation ($i^*_{gq} = 0$). The outer voltage loop maintains the summation of MVDC voltage ($\sum v_{dcn}$) constant by regulating the average value directly. The inner current loop generates the active(d_{dcom}) and reactive(d_{qcom}) component of the common duty ratio(d_{com}). Subsequently, to achieve the objective of MVDC voltage balancing, this common active component is added to the output of the dedicated voltage balance controller (H_{VBC}) for each cell to generate the modified duty ratio specific to each cell [14]. For the n^{th} FEC cell, this component is denoted as (d_{dn}).

Carrier interleaved sine triangle unipolar PWM technique is also employed, which helps in achieving multilevel operation of CMFEC. Here, phase shift of the n^{th} FEC cell carrier is $2\pi(n-1)/n$. The exception to this, is the case of 2 cells, where carriers are shifted by 90°.

1) PROPOSED FEED-FORWARD COMPENSATOR FOR CMFEC

Whenever there is a sudden load fluctuation at the LVDC side, it also directly impacts the MVDC voltages. This, in turn, affects both grid side and load side operations. Hence, if the MVDC voltages can be tightly regulated, the disturbance rejection capability of the entire scheme gets enhanced. To do this, a feed forward compensation is proposed. A feed-forward term is derived which links DAB load side i_o to CMFEC grid side i_{gd} in the following manner. The total pole voltage (v_{pT}) of CMFEC can be expressed as,

$$v_{pT} = nd_{com}v_{dc,avg} = \sum_{k=1}^{n} d_k v_{dck}. \tag{3}$$

Once the voltage balance is achieved, it leads to the expressions shown in (4). The active component d_{dcom} of the common duty ratio is the average of the active components of each cell. Hence, sum of all Δd_{dn} is zero.

$$d_{dcom} = \frac{1}{n}\left[\sum_{k=1}^{n} d_{dk}\right] \quad \text{and} \quad \sum_{k=1}^{n} \Delta d_{dk} = 0. \tag{4}$$

Neglecting the switching frequency harmonics, a relation between i_{gd} and i_o is derived as,

$$i_{dcn} = d_{dn}i_{gd} = i_{1n} = i_{2n}/N_{tn} = i_o/(nN_{tn}), \tag{5}$$

$$i_{gd} = i_o/(nN_{tn}d_{dcom}), \tag{6}$$

where i_{dcn}, i_{1n} and i_{2n} are FEC DC-link output current, DAB DC-link input current and DAB DC-link output current in n^{th} cell. d_{dn} is replaced with d_{dcom} to consider the average effect on all cells and for simplicity during hardware realization. Hence, the relation presented in (6) is used to derive the feed-forward term. To capture the dynamic relation between i_{gd} and i_o, (6) is linearised by adding a small perturbation to arrive at

$$\tilde{i}_{gd} = \frac{1}{nN_{tn}D_{dcom}}\tilde{i}_o - \frac{I_o}{nN_{tn}{D_{dcom}}^2}\tilde{d}_{dcom}. \tag{7}$$

Here, the first term links the perturbation in i_o with the perturbation in i_{gd}. This is the feed-forward term (i_{gd-ff}), which is reproduced as,

$$\tilde{i}_{gd-ff} = \frac{1}{nN_{tn}D_{dcom}}\tilde{i}_o. \tag{8}$$

D_{dcom} is the nominal value of common active component of CMFEC duty ratio at full load. Nominal value of D_{dcom} can be derived as,

$$D_{dcom} = \frac{1}{nN_{tn}}\left[\frac{V_{gd}}{V_o}\right]. \tag{9}$$

The feed-forward term i_{gd-ff} is added to the inner active current control loop of CMFEC vector control, for fast dynamic response of MVDC voltages during load transients.

B. PROPOSED SENSORLESS POWER BALANCE CONTROL

The power (p_n) transferred in the n^{th} cell with single phase shift (SPS) modulation is,

$$p_n = \frac{N_{tn}v_o v_{dcn}}{2f_s}\frac{1}{L_{sn}}d_{\varphi n}(1-d_{\varphi n}), \tag{10}$$

where, the turns ratio, HF-link inductance and phase shift duty ratio of n^{th} DAB are denoted as N_{tn}, L_{sn} and $d_{\varphi n}$ respectively and f_s is the switching frequency of each DAB [14], [15].

It is the difference in L_s value from one cell to another which is primarily responsible for unequal sharing of active power. Maintaining the power balance by ensuring equal throughput power delivery across all cells irrespective of parametric variation in L_s and output voltage (v_o) regulation are the control objectives. These are met in this proposed current sensorless scheme by using the estimated value of the fundamental component of the high frequency link inductor current(i_{Ls}). A prerequisite is estimation of L_{sn} in each cell, which would be discussed in the subsequent subsection. Here, the power balance strategy is presented assuming that L_{sn} has been estimated with acceptable accuracy.

In this work, HF-link current fundamental component estimation based power balance strategy is derived with the help of online parameter identification and updation. The state observers are designed to estimate DAB current fundamental envelopes, thereby controlling these to achieve power balance. The GA modelling based small signal model of n^{th} DAB cell is presented in (11), as shown at the bottom of the next page, where the state variables are $\langle v_o\rangle_0$, $\langle i_{Lsn}\rangle_1^R$ and $\langle i_{Lsn}\rangle_1^I$ [36].

The Fourier series of i_{Ls} is dominated by its fundamental frequency term. Thus controlling its active power component in each DAB cell leads to power balance across the cells. Executing this without using high bandwidth current sensors is the primary motivation of this scheme. Fundamental harmonic approximation is applied in this analysis. The fundamental component of active power (p_{fund_n}) in n^{th} DAB cell is derived and shown in (12).

$$\begin{aligned} p_{fund\_n} &= 2\left[\langle v_{prin}\rangle_1^R\langle i_{Lsn}\rangle_1^R + \langle v_{prin}\rangle_1^I\langle i_{Lsn}\rangle_1^I\right] \\ &= -\frac{4}{\pi}\langle v_{dcn}\rangle_0\langle i_{Lsn}\rangle_1^I. \end{aligned} \tag{12}$$

$\langle v_{prin}\rangle_1^R$ and $\langle v_{prin}\rangle_1^I$ are the real and imaginary part of fundamental component, derived from the complex Fourier series expansion of v_{prin} (primary side switching pole voltage of the n^{th} DAB cell), where,

$$\langle v_{prin}\rangle_1^R = 0 \quad \text{and} \quad \langle v_{prin}\rangle_1^I = -\frac{2}{\pi}\langle v_{dcn}\rangle_0. \tag{13}$$

It is evident from (12) that $\langle i_{Lsn}\rangle_1^I$ is the active power component of inductor current and hence is chosen as a control variable along with v_o. The block diagram of proposed estimation based control scheme is shown in Fig. 3. Essentially, it is a dual loop control consisting of outer voltage and inner current control loop. The outer loop regulates v_o. The H_{VO} controller generates the current reference for all DAB modules. Subsequently, the inner loop comparator compares $\langle i_{Ls}^*\rangle_1^I$ reference with the estimated $\langle i_{Lsen}\rangle_1^I$, acquired from n^{th} DAB cell observer block. Finally, the current controller (H_{iLs}) generates phase shift duty ratio $d_{\varphi n}$ for the n^{th} DAB module.

A feed-forward compensation term is added to each of the inner current control loop of modular DAB. The feed-forward term ($i_{Ls1I-ff}$) is derived as

$$i_{Ls1I-ff} = \left[\left\{\frac{1}{n}\sum_{k=1}^{n}\langle i_{Lsen}\rangle_1^I\right\} - I_{Ls1I\_nom}\right], \tag{14}$$

where, I_{Ls1I_nom} can be obtained as

$$I_{Ls1I\_nom} \approx \frac{\pi}{2\cos\Phi_{nom}} \times \frac{I_o}{n}. \tag{15}$$

Φ_{nom} is the nominal full rated phase shift angle between the two H-bridges of DAB.

The observer block is also shown in Fig. 3. For the chosen ISOP configuration, all DAB modules have the same output voltage v_o, as their outputs are connected in parallel. Due to the cell to cell parametric variation, the generated error between measured v_o and estimated v_{oen} in the n^{th} DAB observer is different across the cells. Hence the error minimizing observer gain matrix is different for each DAB, depending on the estimation error. $\mathbf{K_{en}}$ is the observer gain matrix for n^{th} DAB. Mathematical model of n^{th} DAB module full order state observer is given in (16), where $\mathbf{x}_{en} = \left[\langle v_{oen}\rangle_0 \quad \langle i_{Lsen}\rangle_1^R \quad \langle i_{Lsen}\rangle_1^I\right]^T$, are the estimated state variables corresponding to n^{th} DAB.

$$\begin{aligned} \dot{\mathbf{x}}_{en} = (\mathbf{A}_n - \mathbf{K_{en}}\mathbf{C}_n)\mathbf{x}_{en} + \mathbf{B_{1n}}d_{\varphi n} + \mathbf{B_{2n}}v_{dcn} \\ + \mathbf{B_{3n}}i_N + \mathbf{K_{en}}v_o. \end{aligned} \tag{16}$$

Depending on different $d_{\varphi n}$ and L_{sn} values, the estimated state $\langle i_{Lsen}\rangle_1^I$ will be different for the different DAB modules. This $\langle i_{Lsen}\rangle_1^I$ is provided as the feedback input to the n^{th} DAB inner current control loop. Inner H_{iLs} controller will generate different $d_{\varphi n}$ for different DAB cells according to the difference in $\langle i_{Lsen}\rangle_1^I$ feedback, to obtain power balance in modular SST.

This control scheme also allows current mode control for current regulation. This is possible due to presence of the inner current control loop. During current control, the outer voltage loop can be deactivated and the LVDC side load current reference (i_o^*) can be directly provided with a multiplication factor C_k as shown in Fig. 3. C_k is obtained as,

$$C_k = \pi/(2n\cos\Phi_{nom}). \tag{17}$$

Moreover, if a particular cell has to be deactivated, the corresponding gain k_n (shown in Fig. 3) can be set to zero by using the act_n input. This enables phase-shedding operation of that cell, as experimental demonstrated.

C. ONLINE ESTIMATION OF INDUCTANCE VALUES

In this subsection the online estimation of each DAB cell inductance value is discussed. Parameter identification schemes of a single cell DAB are presented in [12], [36], and [38]. In this work inductance estimation scheme for output parallel connected DABs in modular SST is derived. Equating the active current input of n^{th} DAB cell with

the active current output of its series connected n^{th} FEC cell, forms the basis of modular SST inductance estimation scheme.

The n^{th} FEC cell output current (i_{dcn}) can be written as

$$i_{dcn} = i_g d_n = (i_{gd} + j i_{gq})(d_{dn} + j d_{qn}) = (i_{gd} d_{dn} - i_{gq}.d_{qn}) + j(i_{gd} d_{qn} + i_{gq} d_{dn}). \quad (18)$$

Due to the UPF operation at grid side, the reactive component of current $i_{gq} = 0$. Using this in (18), the active component of i_{dcn} can be obtained as,

$$i_{dcn\_active} = i_{gd} d_{dn}. \quad (19)$$

From the throughput power expression of a DAB converter for SPS PWM technique, the input active current of DAB module in n^{th} cell can be found as

$$i_{1n} = \frac{N_t v_o}{2 f_s L_{sn}} d_{\varphi n}(1 - d_{\varphi n}), \quad (20)$$

where N_t is turns ratio and f_s is DAB switching frequency. Equating (19) with (20), the inductance value in n^{th} DAB module can be calculated as

$$L_{sn} = \frac{N_t v_o}{2 f_s d_{dn} i_{gdn}} d_{\varphi n}(1 - d_{\varphi n}). \quad (21)$$

During realization of the control scheme, the inductance estimation loop is incorporated as shown in Fig. 3. It has been explained in details in the step by step working subsection, that once L_s values of each cells are estimated with reasonable accuracy, it automatically leads to equalization of the duty cycles in FEC modules. Achievement of this indicates completion of the estimation process. The peak of i_{Ls} can also be tracked easily and it can be used as an overcurrent marker.

D. CONTROLLER DESIGN PROCEDURE

Controller design process of the proposed control strategy is provided in this subsection. The observer design procedure using the pole placement method is discussed in [39] and [40]. The switching frequency of each DAB, in this work is 20kHz. The observer poles are placed one decade below the switching frequency at around 2kHz. The inner current loop is designed such that its poles are about 5 times slower than that of observer poles. The outer voltage loop is designed in such a way that the inner current control loop is 5 times faster than that of the outer voltage loop. The phase margin was targeted to be around 70°. The control schematic block diagram is shown in Fig. 4.

From the small signal model, the three transfer functions $G_{vo,d\varphi}$, $G_{iLs1R,d\varphi}$ and $G_{iLs1I,d\varphi}$ are derived and are presented in (22), (23) and (24), as shown at the bottom of the next page. For inner current controller H_{iLs} design, the Bode plot of $G_{iLs1I,d\varphi}$ (inner plant), H_{iLs} and I_{OLTF} (inner open loop gain transfer function) is shown in Fig. 5. A PI controller can achieve the targeted bandwidth and phase margin. Bode plot of $G_{vo,iLs1I}$ is also shown in Fig. 6. The closed loop transfer function of inner current loop combined with $G_{vo,iLs1I}$ is denoted as G_{OPLANT}, which is given in (25).

$$G_{OPLANT} = \frac{G_{iLs1I,d\varphi} H_{iLs}}{1 + G_{iLs1I,d\varphi} H_{iLs}} G_{vo,iLs1I} \quad (25)$$

Design of outer H_{VO} controller is done with a design target of nearly 70° of phase margin and 400 rad/sec of bandwidth. A PI controller can be used but the bandwidth will be lesser. PI controller combined with a lead compensator can also be used to eliminate the steady state error and to give required phase boost for obtaining the required phase margin. Bode plot of G_{OPLANT}, outer open loop transfer function (O_{OLTF}) and outer H_{VO} controller is shown in Fig. 7. Using similar approach the controllers for CMFEC stage can also be derived.

III. STEP BY STEP WORKING OF THE CONTROL SCHEME

The complete operation of this proposed scheme is discussed in a sequential manner in this section to facilitate understanding of the entire scheme. These are represented by a flowchart shown in Fig. 8. In terms of occurrence of successive events, working of the scheme can be divided into three steps.

The first step of this proposed control strategy starts with energizing the system with CMFEC based voltage balance control. This ensures MVDC voltage balance by making $v_{dc1} = v_{dc2} = .. = v_{dcn}$. For the DAB stage, different cells may have different inductance values due to plant uncertainty, which are unknown at this point. However, design of each DAB module state observer block is done with the assumption that L_s for every cell is equal to the nominal/nameplate rating (L_{snom}) that is $L_{s1} = L_{s2} = .. = L_{sn} = L_{snom}$. Hence the same nominal control inputs are also given initially as input to all the observer block, which is

$$\underbrace{\begin{bmatrix} \dot{\tilde{v}}_o\rangle_0 \\ \dot{\tilde{i}}_{Lsn}\rangle_1^R \\ \dot{\tilde{i}}_{Lsn}\rangle_1^I \end{bmatrix}}_{\dot{\tilde{\mathbf{x}}}_n} = \underbrace{\begin{bmatrix} -1/n & -\frac{4N_{sin}}{\pi C_o} & -\frac{4N_{cos}}{\pi C_o} \\ \frac{2N_{sin}}{\pi L_{sn}} & -\frac{R_{sn}}{L_{sn}} & \omega \\ \frac{2N_{cos}}{\pi L_{sn}} & -\omega & -\frac{R_{sn}}{L_{sn}} \end{bmatrix}}_{\mathbf{A}_n} \underbrace{\begin{bmatrix} \tilde{v}_o\rangle_0 \\ \tilde{i}_{Lsn}\rangle_1^R \\ \tilde{i}_{Lsn}\rangle_1^I \end{bmatrix}}_{\tilde{\mathbf{x}}_n} + \underbrace{\begin{bmatrix} \frac{4}{C_o}\left[N_{sin} I_{Ls1In} - N_{cos} I_{Ls1Rn}\right] \\ \frac{2N_{cos}}{L_{sn}} V_o \\ -\frac{2N_{sin}}{L_{sn}} V_o \end{bmatrix}}_{\mathbf{B_{1n}}} \underbrace{\tilde{d}_{\varphi n}}_{u_{1n}} - \underbrace{\begin{bmatrix} 0 \\ 0 \\ \frac{2}{\pi L_{sn}} \end{bmatrix}}_{\mathbf{B_{2n}}} \underbrace{\tilde{v}_{dcn}}_{u_{2n}} - \underbrace{\begin{bmatrix} \frac{1}{nC_o} \\ 0 \\ 0 \end{bmatrix}}_{\mathbf{B_{3n}}} \underbrace{\tilde{i}_N}_{u_{3n}} \quad (11)$$

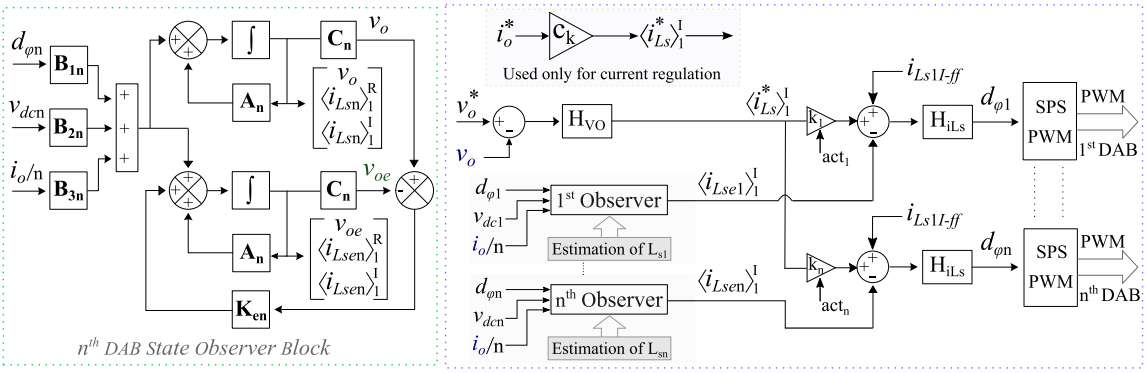


FIGURE 3. Observer based power balance control in modular DAB stage.

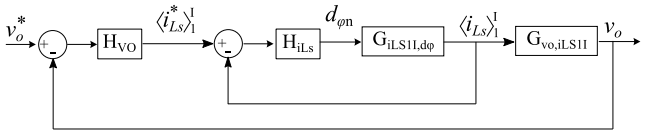


FIGURE 4. Schematic of control block.

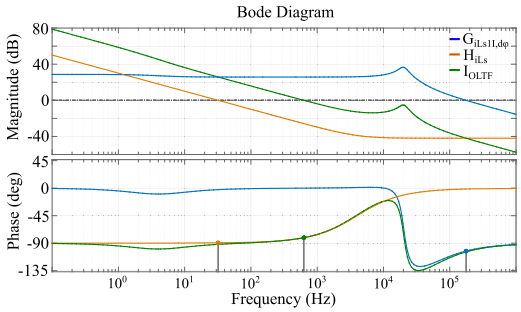


FIGURE 5. Plots of inner plant, controller, open loop gain transfer function.

$d_{\varphi 1} = d_{\varphi 2} = .. = d_{\varphi n} = d_{\varphi nom}$. As a result the observer output of every block is also the same. Thus $\langle i_{Lse1}\rangle_1^I = \langle i_{Lse2}\rangle_1^I = .. = \langle i_{Lsen}\rangle_1^I$. Since the same estimated values are given as feedback to each of their corresponding inner current loop, the H_{iLs} current controllers in each inner loop generates the same phase shift duty ratio, that is $d_{\varphi 1} = d_{\varphi 2} = .. = d_{\varphi n}$. Consequently, for cell to cell variation of L_s, power balance cannot be achieved at this stage. A direct impact of this power unbalance is manifested in the unequal modulation duty ratio of each FEC stage, that is $d_1 \neq d_2 \neq .. \neq d_n$. This is certain to occur as voltage balance is achieved but the active component of the current differs cell to cell. Given that all the FEC cells share the same input side current i_g, this is the only possible outcome at this point unless all L_s are equal.

In step-2, the values of inductances are estimated in each DAB using (21). These values are updated in the corresponding state observer block to estimate $\langle i_{Lse}\rangle_1^I$ of each DAB.

TABLE 5. Simulation parameters.

Parameter	Value
L_{s1}, L_{s2}, L_{s2}	215, 250, 285 μH
C_o	470 μF
C_1, C_2, C_3	2.2 mF
N_{tn}	4:5
Rated V_{dcn}	320 V
Rated V_o	400 V
Rated v_g (RMS)	575 V, 50 Hz
L_g	14 mH
P_t	3.6 kW

In step-3, the estimated state $\langle i_{Lse}\rangle_1^I$ from every observer block will be different if difference exists in the values of L_s across cells. These estimated values are given as feedback to their corresponding inner current loop. Estimation of inductances with good accuracy inherently leads to a good estimation of $\langle i_{Lse}\rangle_1^I$. This in turn leads to minimization of the current error in each loop and subsequently meeting the target of power balance across cells. If L_s are different across cells, then an obvious outcome is that $d_{\varphi 1} \neq d_{\varphi 2} \neq .. \neq d_{\varphi n}$. Also once both voltage balance and power balance are realised, duty ratio of all FEC cells which were unequal at the beginning of step-1, now becomes equal. Thus at the end of step-3, $d_1 = d_2 = .. = d_n$. After the power balance is achieved, the inductance estimation block can be deactivated and can be reactivated when the duty cycle in the FEC stage becomes unequal. This implementation method can effectively address parametric uncertainty caused by ageing.

IV. RESULTS AND DISCUSSION

A. SIMULATION RESULT

The initial analysis was conducted using PLECS simulation software with a 3.6 kW modular SST having 3 number of cells. The simulation parameters are given in Table. 5.

To bring the effect of parametric uncertainty three inductors with ± 15% variation in inductance values were

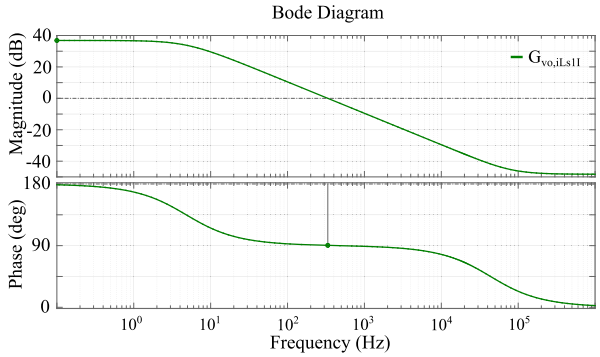


FIGURE 6. Bode plot of $G_{vo,iLs1I}$.

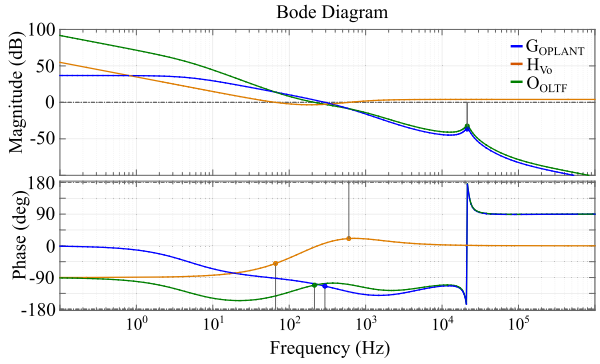


FIGURE 7. Plots of outer plant, controller, open loop gain transfer function.

considered. These HF-link inductance values were estimated and updated in the corresponding state observer block. The simulation result showing the multilevel interleaving operation is presented in Fig. 9a. i_g is in phase with v_g. Due to 3 number of cells there are $(2\times3+1=7)$ number of levels present in the v_{pT} waveform. The balanced HF-link inductor currents in the 3 cells are shown in Fig. 9b. These steady

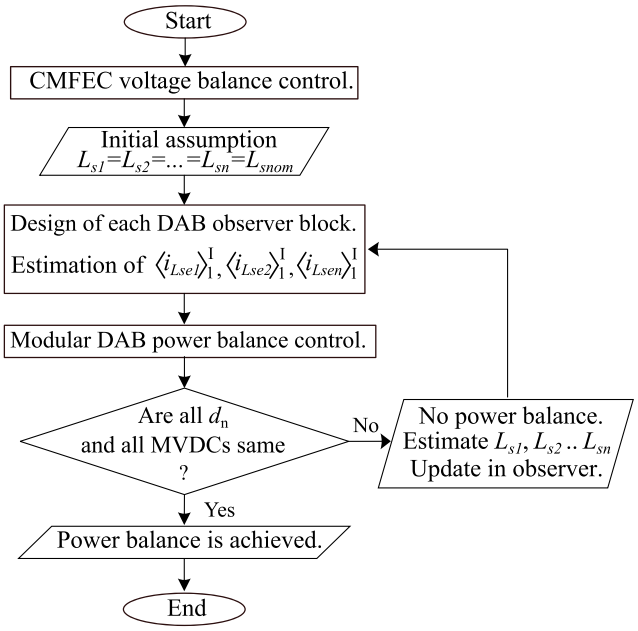


FIGURE 8. Control scheme flowchart showing step by step working.

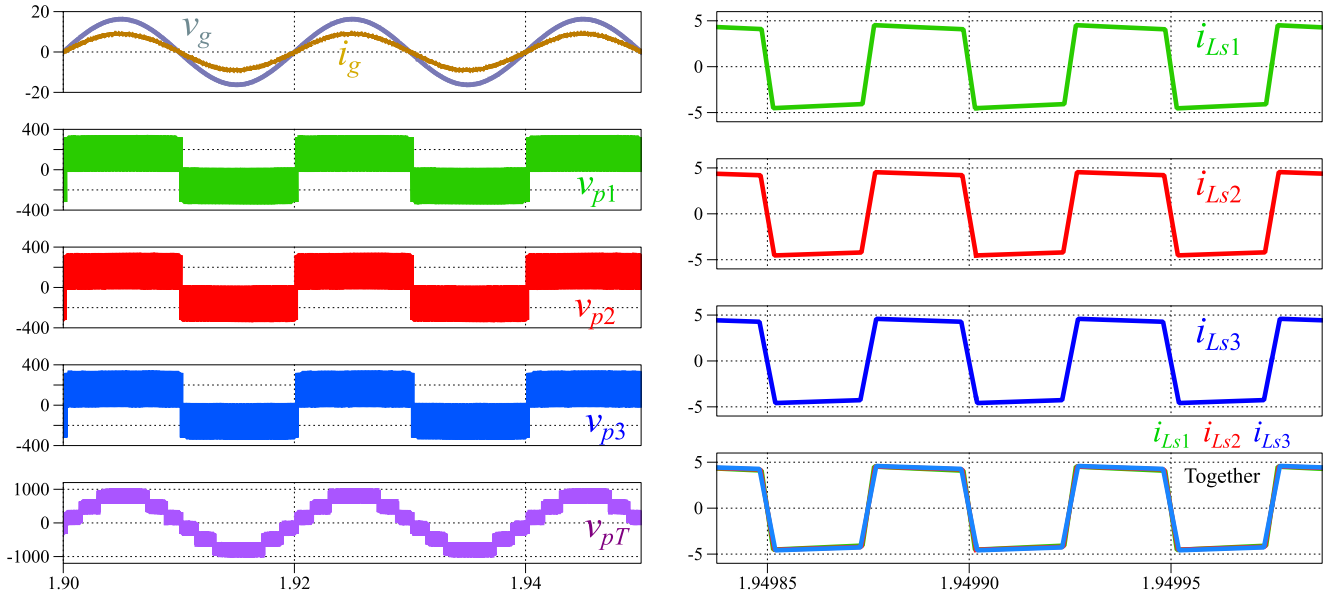
state simulation results display the voltage and power balance operation of 3 cell modular SST.

Next simulation was performed to test the dynamic performance of the proposed control method by introducing the load disturbance. A 50% step decrease in load current i_o is given at 2 sec as load disturbance. Similarly, a 50% step load increase in i_o is given at 2.5 sec. The simulation result corresponding to this is illustrated in Fig. 10. The settling time of v_{dc1}, v_{dc2} and v_{dc3} MVDC voltages are less than 2 grid cycles with overshoot/undershoot less than 2%. The settling time of v_o is around 10ms and overshoot/undershoot less than 4%. During these transients v_g and i_g remain in phase showing the UPF operation throughout.

$$G_{vo,d\varphi}=\frac{\langle\hat{v}_o\rangle_0}{\hat{d}_\varphi}=\frac{\begin{array}{c}4N_t(-I_{LS1R}((s^2+\omega^2)L_s^2+2L_sR_ss+R_s^2)\pi cos(\pi D_\varphi)\\ +I_{LS1I}((s^2+\omega^2)L_s^2+2L_sR_ss+R_s^2)\pi sin(\pi D_\varphi)+(2L_sN_tV_o\omega))R_o\pi\end{array}}{((sC_oR_o+1)((s^2+\omega^2)L_s^2+2L_sR_ss+R_s^2)\pi^2+(8N_t^2R_o(sL_s+R_s)))} \tag{22}$$

$$G_{iLs1R,d\varphi}=\frac{\langle\hat{i}_{Ls}\rangle_1^R}{\hat{d}_\varphi}=\frac{\begin{array}{c}2N_t(-4((I_{LS1I}s+I_{LS1R}\omega)L_s+I_{LS1I}R_s)N_tR_o\pi cos(\pi D_\varphi)^2+(-4N_tR_o((-I_{LS1I}\omega\\ +I_{LS1R}s)L_s+I_{LS1R}R_s)\pi sin(\pi D_\varphi)+((L_ss+R_s)(C_oR_os+1)\pi^2+8N_t^2R_o)V_o)\\ cos(\pi D_\varphi)+4\pi(-\omega L_s\pi V_o(C_oR_os+1)sin(\pi D_\varphi)/4+I_{LS1I}N_tR_o(L_ss+R_s)))\pi\end{array}}{((C_oR_os+1)((s^2+\omega^2)L_s^2+2L_sR_ss+R_s^2)\pi^2+8N_t^2R_o(L_ss+R_s))} \tag{23}$$

$$G_{iLs1I,d\varphi}=\frac{\langle\hat{i}_{Ls}\rangle_1^I}{\hat{d}_\varphi}=\frac{\begin{array}{c}-2N_t(4N_tR_o((-I_{LS1I}\omega+I_{LS1R}s)L_s+I_{LS1R}R_s)\pi cos(\pi D_\varphi)^2-4(((I_{LS1I}s\\ +I_{LS1R}\omega)L_s+I_{LS1I}R_s)N_tR_osin(\pi D_\varphi)-\omega L_s\pi V_o(C_oR_os+1)/4)\pi cos(\pi D_\varphi)\\ +((L_ss+R_s)(C_oR_os+1)\pi^2+8N_t^2R_o)V_osin(\pi D_\varphi)+4I_{LS1I}L_sN_t\pi R_o\omega)\end{array}}{((C_oR_os+1)((s^2+\omega^2)L_s^2+2L_sR_ss+R_s^2)\pi^2+8N_t^2R_o(L_ss+R_s))} \tag{24}$$



(a) Multilevel operation of CMFEC.

(b) Balanced HF-link currents.

FIGURE 9. Simulation results showing multilevel interleaving operation, UPF operation of CMFEC and balanced HF-link currents in 3 cells.

To validate the controlled zero power sharing operation of a particular cell, next simulation was performed. The simulation result corresponding to this is presented in Fig. 11. Before $t = 3$ sec, each cell was carrying 800 watt to supply a total load demand of 2400 watt. At 3 sec, the 3rd cell was turned off by making its inner current loop gain $k_3 = 0$, for the phase-shedding operation. Due to this, the power flowing in the 3rd cell becomes zero by making i_{Ls3} zero. The power in remaining cells (cell1 and cell2) is increased from individual 800 watt to rated 1200 watt with the increase in i_{Ls1} and i_{Ls2}. The MVDC voltages v_{dc1}, v_{dc2} and v_{dc3} are maintained at 320 volt. At $t = 3.9$ sec, the 3rd cell is reactivated by making $k_3 = 1$, for phase-addition operation. As v_{dc3} is still regulated, precharging circuit is not required for power flow resumption in 3rd cell. The proposed control strategy makes the phase-shedding and phase-addition operation seamless.

B. EXPERIMENTAL RESULT

A hardware prototype of 1.6-kW modular SST with 2 number of cells was used for experimental validation. This is shown in Fig. 12. System parameters for experiment are given in the Table 6. Isolated ISO5852S gate driver ICs were used to drive the discrete IGBT switches (IKQ50N120CT2) used in the power stage of SST. Two current sensors were installed to measure output current i_o and grid current i_g. The bandwidth of these sensors used during experiments are provided in Table 7. DSP micro-controller TMS320F28377S and SPARTAN-6 FPGA were used as the digital control platform.

The nominal/nameplate rating of two DAB cell inductances is 150 μH. However, to bring the effect of the parametric uncertainty, two inductors with values $130\mu H$ and $177\mu H$ were selected as L_{s1} and L_{s2} respectively. Hence, the inductance values for the experiment were chosen with a variation of $\pm 15\%$ from the nominal value. The HF-link transformer were designed for a turns ratio of 0.8 in the two cells. Initially, the aim was to validate the voltage

TABLE 6. Experiment parameters.

Parameter	Symbol	Value
DAB 1, 2 inductance	L_{s1}, L_{s2}	130, 177 μH
LVDC Capacitance	C_o	470 μF
MVDC 1, 2 Capacitance	C_1, C_2	2.2 $\pm$10% mF
DAB Switching frequency	f_{DAB}	20 kHz
FEC Switching frequency	f_{FEC}	4 kHz
HF link turns ratio	N_{tn}	4:5
Rated MVDC voltage	V_{dcn}	205 V
Rated LVDC voltage	V_o	255 V
Grid input voltage (RMS)	v_g	220 V, 50 Hz
Grid interfacing inductance	L_g	6 mH
Load Resistance	R_o	40 Ω
Total power	P_t	1.6 kW

TABLE 7. Bandwidth of sensors used in this work.

Measured Parameter	Sensor*	Bandwidth
v_g, v_o, v_{dc1}, v_{dc2}	HA025T01	Low – 200 kHz
i_g, i_o	VH1K0T01	Low – 200 kHz

* Make - Electrohms Private Limited

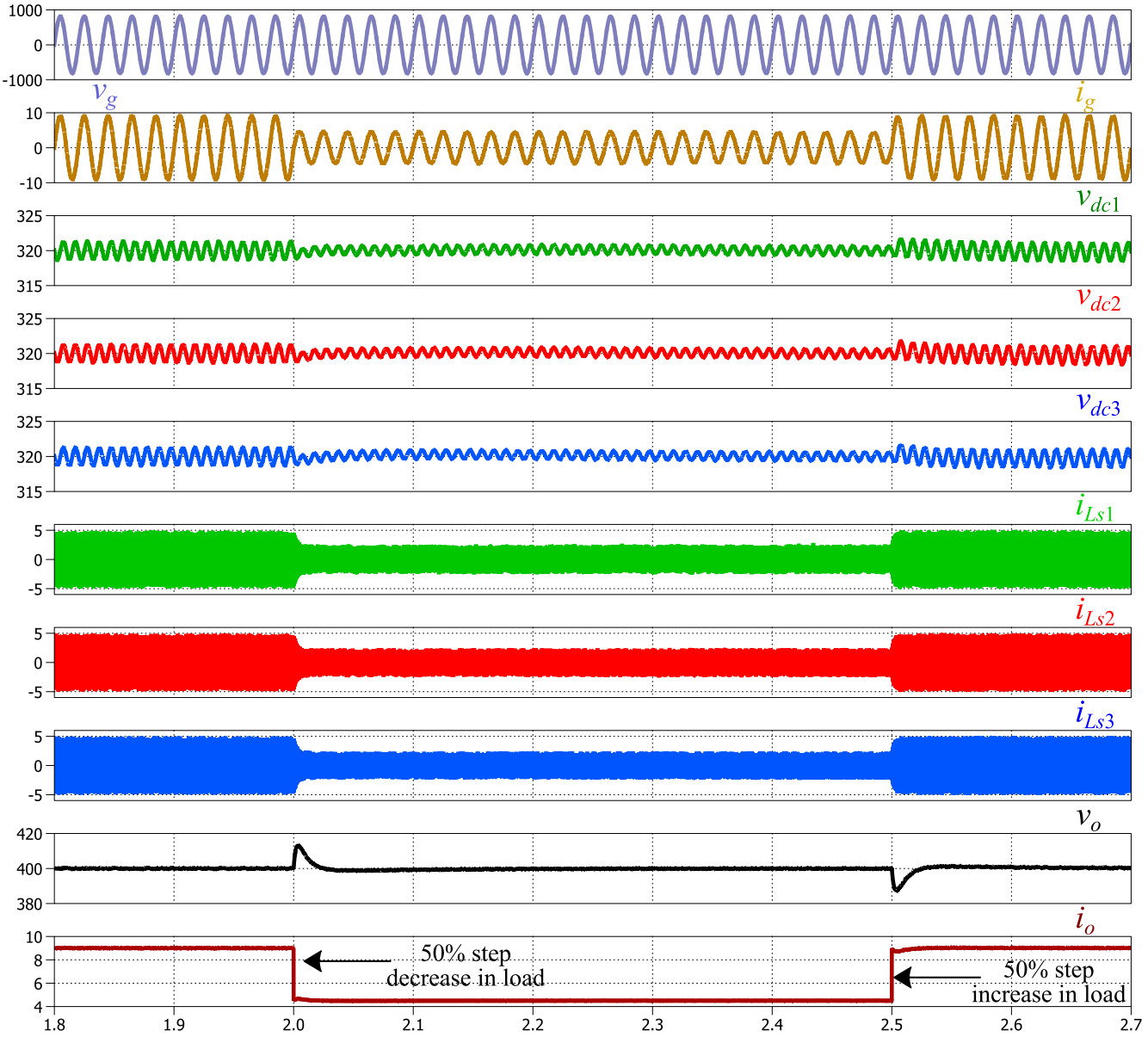


FIGURE 10. Simulation result showing voltage and current transients due to 50% step increase and decrease in load current.

balance control in the CMFEC stage without activating the L_s estimation blocks. The experimental results are illustrated in Fig. 13. The carrier signals of FEC1 and FEC2 were phase shifted from each other by 90° to realize carrier based interleaving PWM. Multilevel operation is achieved where v_{p1} and v_{p2} switched pole voltages of FEC1 and FEC2 are of 2 levels, whereas, total switched pole voltage v_{pT} is of 5 level. The corresponding results are shown in Fig. 13a. The experimental result showing UPF operation, where v_g and i_g are in same phase, is presented in Fig. 13b. The two MVDC voltages are also shown, where the peak to peak ripple voltages are around 3.5%. The two MVDC voltages v_{dc1} and v_{dc2} are both equal to 205 volt. This validates the voltage balance control irrespective of unequal inductances in DAB stage. The dynamic performance of this voltage balance control was tested by introducing a line voltage variation in v_g. The value of v_g was changed in a ramp like manner from 200 V to 265 V as shown in the Fig. 13c. The disturbance is rejected in both MVDC voltages with variation within ±5% during the transient. As v_g is increased, i_g starts reducing accordingly without losing the UPF operation throughout this transient period. This is evident from Fig. 13c.

To separately examine the effectiveness of the proposed power balance scheme, the estimation blocks were activated. The experimental results are presented in Fig. 14. It can be observed from Fig. 14a, in the absence of power balance control, the two DAB inductor currents i_{Ls1} and i_{Ls2} are

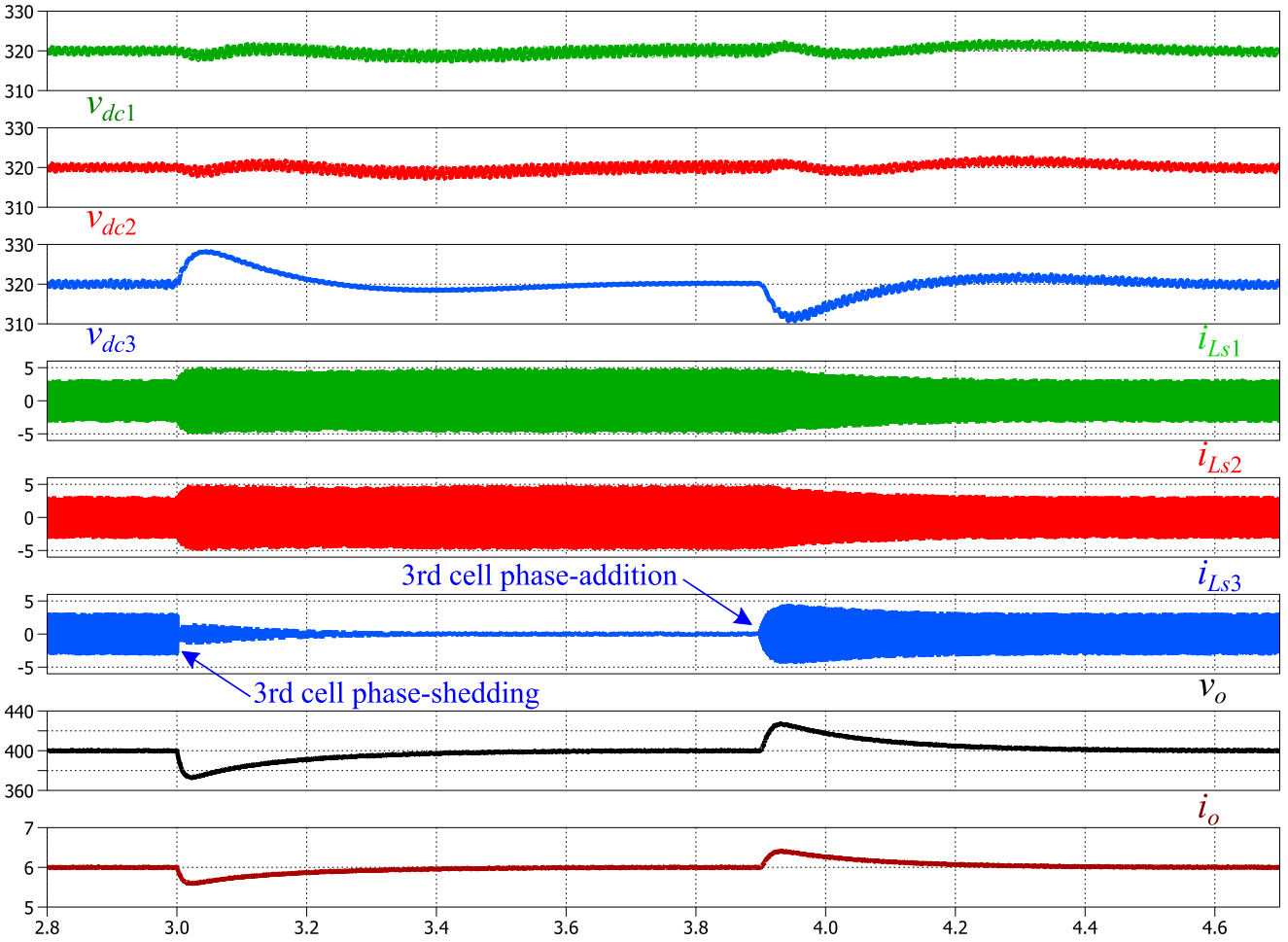


FIGURE 11. Simulation result showing voltage and current transients during phase-shedding and phase-addition operation of cell3.

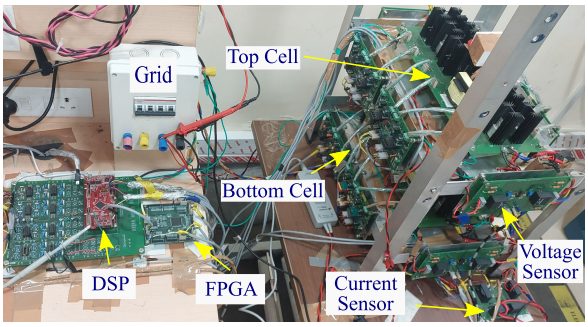
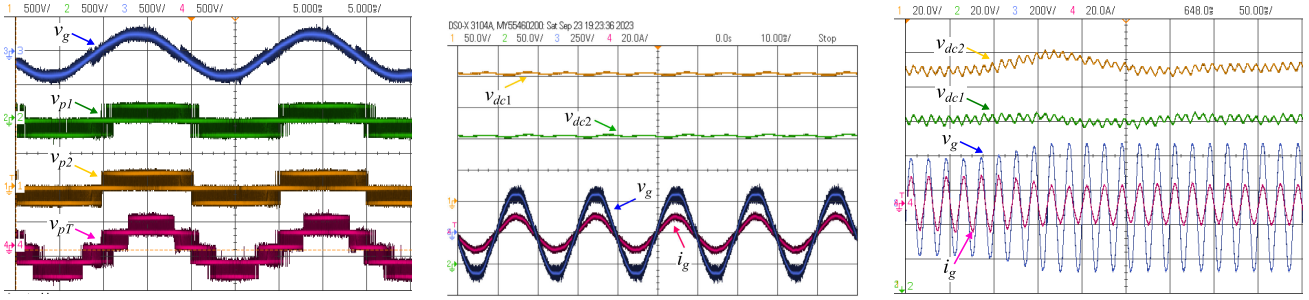


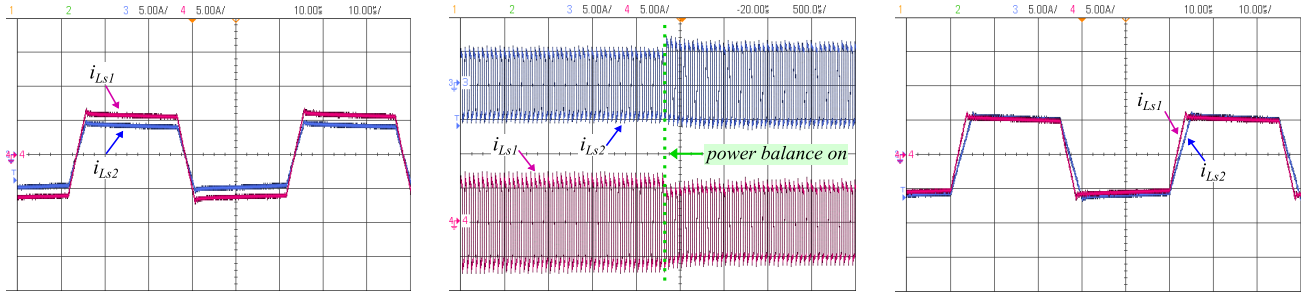
FIGURE 12. Hardware prototype.

unequal. As expected i_{Ls1} is greater than i_{Ls2} because actual inductance value of L_{s1} is lesser than L_{s2}. It was found that $i_{Ls1,rms}$ and $i_{Ls2,rms}$ were about 113.5% and 86.5% respectively of the values expected under power balance. The fundamental harmonic active component $\langle i_{Lse1}\rangle_1^I$ and $\langle i_{Lse2}\rangle_1^I$ of two DAB cells were estimated to be same, as state observers for both DAB cells were designed at same nominal inductance value. This made the corresponding phase shift duty ratio generated by inner H_{iLs} current controller same for both DAB cells, ($d_{\varphi 1} = d_{\varphi 2}$), hence there was no power balance. Subsequently, activating the proposed online inductance estimation scheme, the values of L_{s1} and L_{s2} were estimated using the expression in (21). The estimated inductance values were found out to be $L_{s1e} = 135\mu H$ and $L_{s2e} = 184\mu H$. The percentage error of inductance value estimation was found to be within $\pm 5\%$. Once the estimation was done, these estimated inductance values were updated in their corresponding state observer blocks. Consequently, the observer blocks estimated $\langle i_{Lse1}\rangle_1^I$ and $\langle i_{Lse2}\rangle_1^I$, which were now different and fedback to the inner current loop. The outer H_{VO} voltage controller generated the same reference i^*_{Ls1I} for inner current loops. The inner H_{iLs} controller generated different $d_{\varphi 1}$ and $d_{\varphi 2}$ for two DAB cells to minimize error between $\langle i_{Lse1}\rangle_1^I$, $\langle i_{Lse2}\rangle_1^I$ and the reference. Once the same fundamental active components $\langle i_{Lse1}\rangle_1^I$ and $\langle i_{Lse2}\rangle_1^I$ are made equal, this in turn made i_{Ls1} and i_{Ls2} nearly equal, as the fundamental component is dominant. Finally, power balance was achieved. The experimental result validating this is presented in Fig. 14c. The transition of i_{Ls1} and i_{Ls2} from pre-power balance, to the post-power balance stage is shown in



(a) Multilevel operation of CMFEC. (b) UPF Operation of CMFEC. (c) Grid line voltage disturbance rejection.

FIGURE 13. Experimental results showing voltage balance control of CMFEC. (a) Top trace: v_g (500 V/div), 2nd trace: v_{p1} (500 V/div), 3rd trace: v_{p2} (500 V/div), Bottom trace: v_{pT} (500 V/div). (b) Top trace: v_{dc1} (50 V/div), 2nd trace: v_{dc2} (50 V/div), Bottom trace: v_g (250 V/div) and i_g (20 A/div). (c) Top trace: v_{dc2} (20 V/div), 2nd trace: v_{dc1} (20 V/div), Bottom trace: v_g (200 V/div) and i_g (20 A/div). Time:- (a) 5 ms/div, (b) 4 ms/div, (c) 50 ms/div.



(a) i_{Lsn} before power balance. (b) i_{Lsn} transition when power balance is on. (c) i_{Lsn} after power balance.

FIGURE 14. Experimental results showing DAB inductor currents during power balance. (a) i_{Ls1} (5 A/div), i_{Ls2} (5 A/div). (b) Top trace: i_{Ls2} (5 A/div), i_{Ls1} (5 A/div). (c) i_{Ls1} (5 A/div), i_{Ls2} (5 A/div). Time:- (a) and (c): 10 μs/div, (b) 500 μs/div.

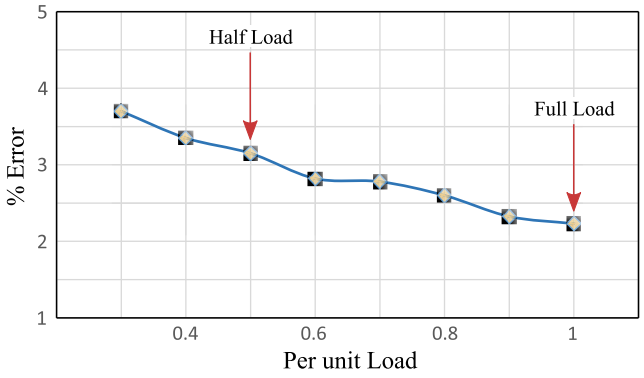
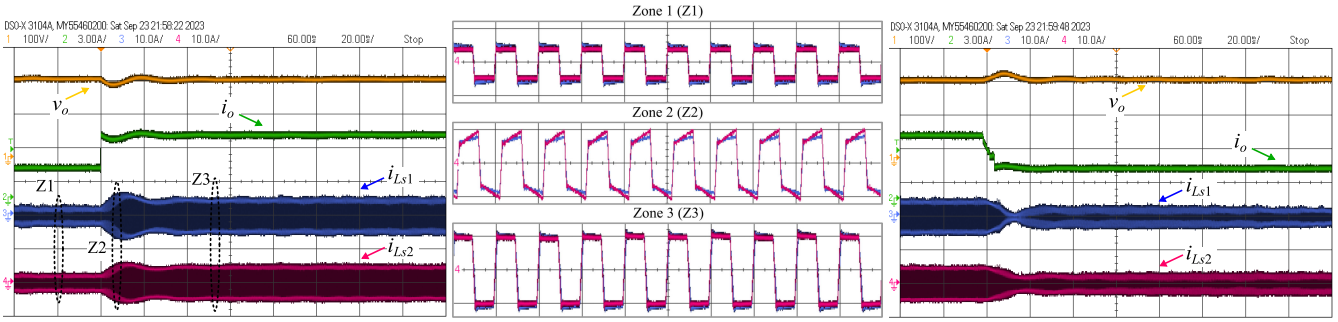


FIGURE 15. Current sharing error with change in load power.

Fig. 14b. It can be confirmed that once the power balance scheme was activated, i_{Ls1} decreases and i_{Ls2} increases to become almost equal within a few switching cycles. It was observed at this point that $i_{Ls1,rms}$ and $i_{Ls2,rms}$ were about 102.23% and 97.77% respectively of the values expected under power balance leading to a current sharing error within 2.23%. It was also observed in the digital control platform that once power balance was achieved, the duty cycle of the FEC stage for both the cells became almost equal. The experimental data were collected and plotted in Fig. 15 to show the current sharing error (in percentage) with respect to the change is load power. It can be noted that the current sharing error is below 4% for a load power variation in the range of full load to 30% of the full load.

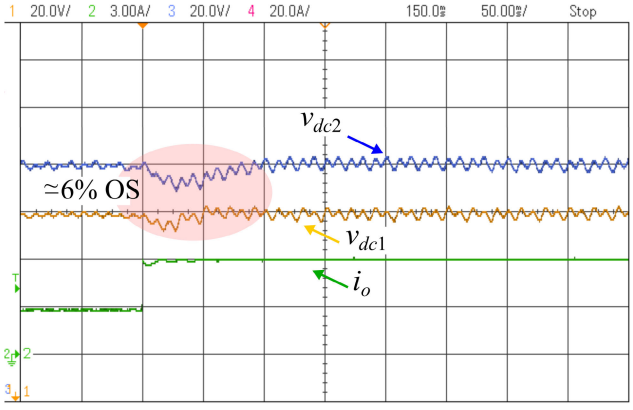
The next set of experiments were carried out to investigate the dynamic performance of the proposed control scheme during load transients. The results are shown in Fig. 16. A 50% step increase in output load current i_o was introduced as the load disturbance from half load to full load (3.1 A $\rightarrow$ 6.2 A). The corresponding results are shown in Fig. 16a. As power balance control is achieved, the output current is shared equally among L_{s1} and L_{s2}. The settling time of output voltage v_o is nearly 15 ms. The undershoot of v_o is nearly $\pm$5%. Subsequently, a step decrease in output load current i_o was given as load disturbance from (6.2 A $\rightarrow$ 3.1 A) and the corresponding results are shown in Fig. 16c. Settling time and overshoot of v_o are below 15 ms and $\pm$5% respectively. To provide better waveform clarity during these transients, the enlarged views of the zones marked as: Zone1 (Z1), Zone2 (Z2) and Zone3 (Z3) are shown in Fig. 16b. These results are shown by superimposing the oscilloscope ground reference for i_{Ls1} and i_{Ls2}. There is a slight difference during Z2 which represents the transient phase and that both currents waveforms are almost equal before and after this transient.

The results of the step load transients on MVDC voltages are shown next. To test the effectiveness of the disturbance rejection scheme, these results are shown first without the

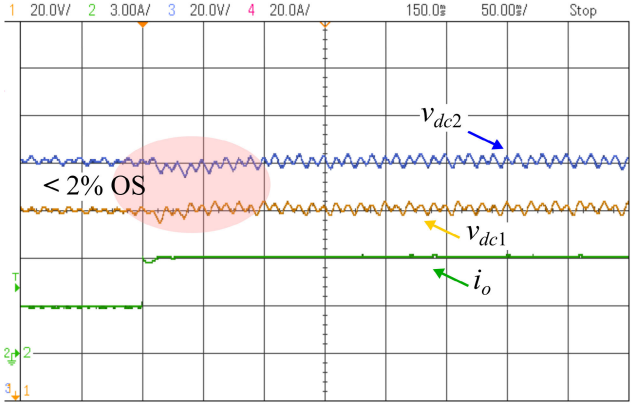


(a) Step increase in load current. (b) Zoomed view. (c) Step decrease in load current.

FIGURE 16. Experimental results during load disturbance. (a) & (c) Top trace: v_o (100 V/div), 2nd trace: i_o (3 A/div), 3rd trace: i_{Ls1} (10 A/div), Bottom trace: i_{Ls2} (10 A/div). (b) Zoomed view of i_{Ls1} and i_{Ls2} shown in (a) with their oscilloscope references superimposed. Upper trace: Zone Z1 of (a), Middle trace: Zone Z2 of (a), Bottom trace: Zone Z3 of (a). Time:- (a) & (c) 20 ms/div, (b) 50 μs/div.



(a) Without feedforward (Zoomed view).



(b) With feedforward (Zoomed view).

FIGURE 17. Effect of Feed-forward on MVDC voltages. Top Trace: v_{dc2} (20 V/div), middle Trace: v_{dc1} (20 V/div), Bottom Trace: i_o (3 A/div). Time:- 50 ms/div.

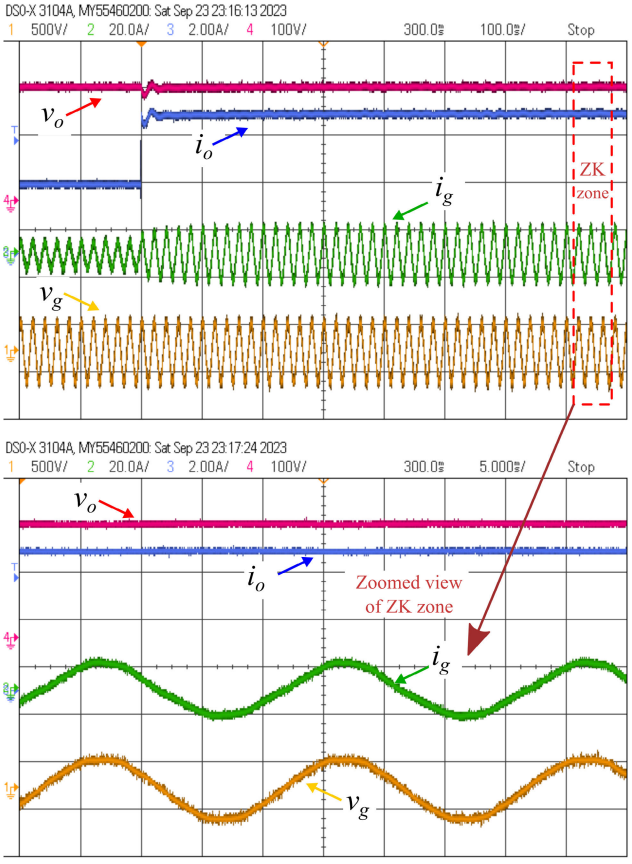
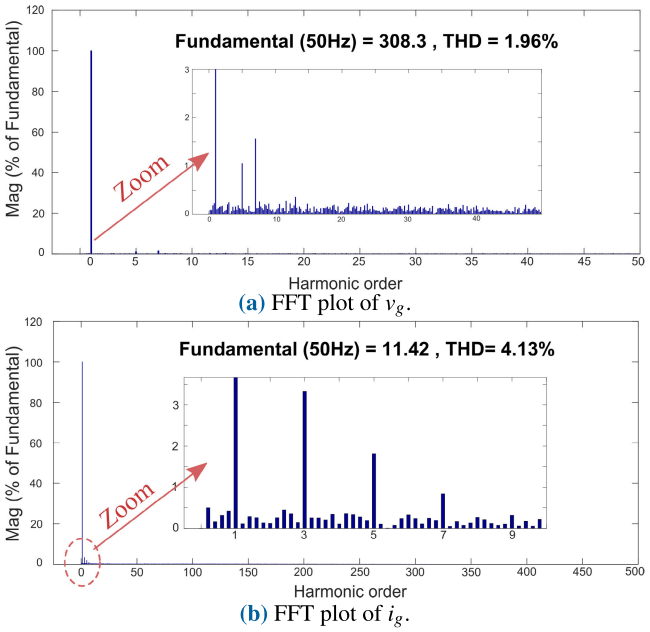


FIGURE 18. Experimental result showing v_g and i_g during load transient with zoomed view. Top trace: v_o (100 V/div), 2nd trace: i_o (2 A/div), 3rd trace: i_g (20 A/div), Bottom trace: v_g (500 V/div). Time:- (a) - 100 ms/div, zoomed view - 5 ms/div.

CMFEC stage feed-forward compensation and then with it. This was done by providing the same 50% step increase in load as done earlier. The corresponding experimental results are shown in Fig. 17. Without the feed-forward compensation the overshoot/undershoot in MVDC voltages are nearly 4-6% (Fig. 17a). However, with feed-forward compensation, significant reduction in the overshoot (≈1.5%) of MVDC voltages is achieved (Fig. 17b). Effect of step load transient on grid current dynamics is shown in Fig. 18. The settling time for i_g is nearly 3 to 4 grid cycles. Throughout these transients, UPF operation is still maintained. The FFT plot of the grid voltage and grid current are shown in Fig. 19a and Fig. 19b respectively. The THD of v_g at the site of deployment was observed to be nearly 1.9%. The THD of i_g was obtained to



(a) FFT plot of v_g.

(b) FFT plot of i_g.

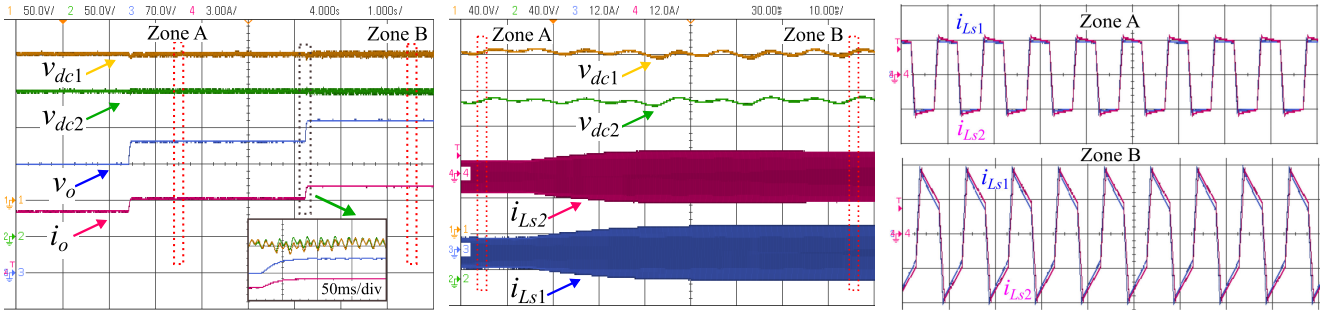
FIGURE 19. FFT Plot of grid voltage and current.

be 4.13% after voltage and power balance in the steady state, which adheres to the IEEE 519-2014 standard [41].

Subsequently, experiments were conducted to demonstrate the output current control/regulation capability of the proposed control scheme. The working of only the inner estimation based current loop was tested by deactivating the outer v_o voltage loop. The experimental result corresponding to this is shown in Fig. 20. As the current reference i_o^* was changed from (5A $\rightarrow$ 6A $\rightarrow$ 7A) in steps, it can be seen that i_o tracks the varying set points smoothly. As the load is resistive, v_o also varies from (210V $\rightarrow$ 250V $\rightarrow$ 295V), which is a total $\pm$15% voltage variation. This is shown in Fig. 20a. The MVDC voltages v_{dc1} and v_{dc2}, as evident, are still tightly regulated. This can also be seen in Fig. 20b. The two DABs operate in buck, unity gain and boost mode when v_o voltage has the values 215V, 260V and 295V respectively. Unity gain mode and boost mode are denoted as Zone A and Zone B respectively. To provide better clarity on current sharing, enlarged views of these zones are shown in Fig. 20c, by superimposing the oscilloscope reference for i_{Ls1} and i_{Ls2}. It can be noticed that the inductor currents i_{Ls1} and i_{Ls2} are still almost equally divided irrespective of the mode of operation in current mode control. This validates the output current regulation capability of this proposed scheme with balanced power sharing.

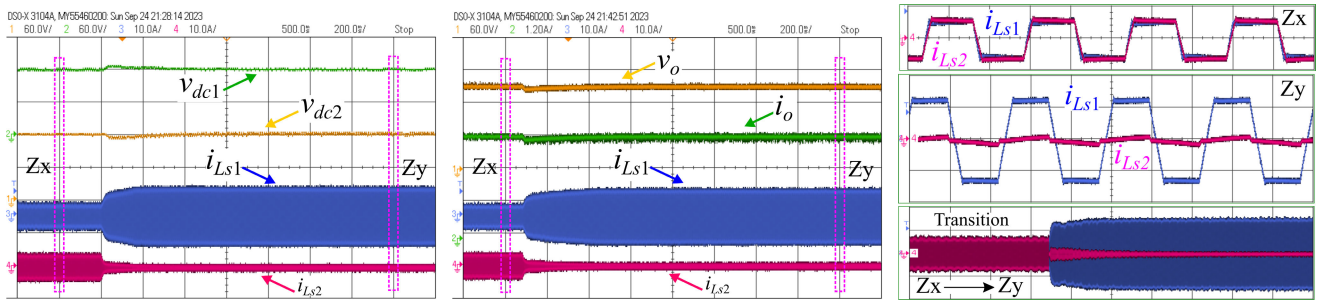
The next set of experiment was conducted to validate the controlled zero power sharing capability (phase-shedding/plug-out operation) of the proposed control strategy. For this, one SST cell current reference was suddenly made zero. The experimental results corresponding to this is shown in Fig. 21. This experiment was attempted at lower FEC modulation index due to the hardware limitation of two SST cells and the current rating of the grid interfacing inductance (L_g) used during the experiments. The low modulation index also forced the MVDC and LVDC to be operated at 125V and 160V respectively. At first, the modulation index of both FEC cells were kept nearly at 0.4. The outer v_o control loop generated the same i^*_{Ls1I} for two of the SST cells. For SST cell 2, the activation input (act_2) was made low. This forces the i_{Ls2} current reference to become zero. Hence, H_{VO} controller increases i^*_{Ls1I} accordingly to maintain v_o and load power. Now the entire active power flows in cell 1, while SST cell 2 transfers zero power in the steady state. Through out this transition, the two MVDCs are regulated equally as shown in Fig. 21a. The LVDC is still regulated, while delivering the same load power as before phase-shedding, which is shown in Fig. 21b. Zoomed views of zones Zx and Zy are provided in Fig. 21c for better clarity. It can be clearly seen that during equal power sharing i_{Ls1} and i_{Ls2} are equal corresponding to Zone X (Zx). In phase-shedding mode, i_{Ls1} current becomes twice and i_{Ls2} current goes to zero corresponding to Zone Y (Zy). During steady state, FEC2 modulation index d_2 becomes 0.8 while d_1 automatically goes to zero due to the H_{VBC} controller of CMFEC. In SST with higher number of cells the FEC modulation duty will change by a factor of $[n/(n-1)]$, which can prevent the FECs to fall in over modulation region. Hence as demonstrated, this scheme provides the provision for unequal duty ratios in FEC modules which allows the modular SST to transfer controlled equal, unequal and zero power through its cells if required, making the power sharing more flexible. This feature can be very useful for controlled shutdown of a cell during low load requirements, so that other cells can operate near to their rated condition. Throughout this lean period, the MVDC voltage in the deactivated cell remains always regulated. As a consequence, during increase in load demand, this earlier deactivated cell can be quickly reactivated to take part in power delivery as the MVDC link capacitor is already precharged. This phase addition operation of cell2 is shown in Fig. 22, where the i_{Ls2} current gets restored to its rated value from zero, in less than 50 ms. As the MVDC capacitors are already precharged it does not require additional precharge circuit during phase-addition operation helping this process smooth and fast.

Finally, the experiment was carried out to validate the DAB inductor current peak envelope monitoring capability. Peak information of DAB inductor current is essential as it is directly related to the saturation limit of the high frequency magnetics. Using the observer based estimation, the fundamental harmonic $\langle i_{Lse1}\rangle_1$ and $\langle i_{Lse2}\rangle_1$ were extracted. Subsequently, these were used to derive the peaks of i_{Ls1} and i_{Ls2}. The peak of i_{Ls1} and i_{Ls2} are denoted as i_{pke1} and i_{pke2} respectively. During 50% step increase in load, the peak current tracking of i_{Lsn} is shown in Fig. 23. It is clearly evident that estimated peak envelope very closely track the actual inductor current peak even during this load transient. This peak information can be used as an additional



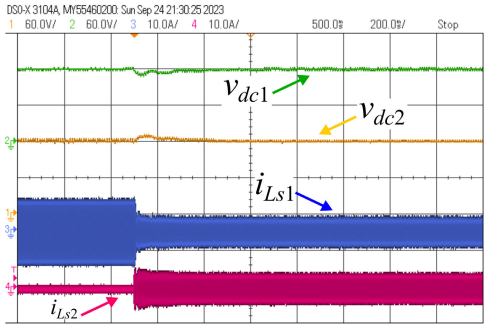
(a) step increase in i_o reference. (b) Equal sharing of inductor currents. (c) i_{Ls1} and i_{Ls2} zoomed view.

FIGURE 20. Experimental results showing output current regulation. (a) Top trace: v_{dc1} (50 V/div), 2nd trace: v_{dc2} (50 V/div), 3rd trace: v_o (70 V/div), Bottom trace: i_o (3 A/div). (b) Top trace: v_{dc1} (40 V/div), 2nd trace: v_{dc2} (40 V/div), 3rd trace: i_{Ls2} (12 A/div), Bottom trace: i_{Ls1} (12 A/div). (c) Zoomed view of superimposed i_{Ls1} and i_{Ls2} (5 A/div). Time:- (a) 1 s/div, (b) 10 ms/div, (c) 50 μs/div.

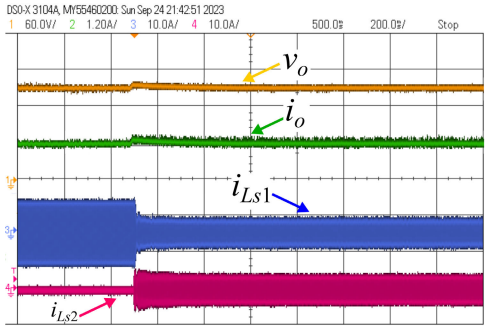


(a) MVDCs during second cell phase-shedding. (b) v_o and i_o during second cell phase-shedding. (c) i_{Ls1}, i_{Ls2}: Zoomed view and their transition.

FIGURE 21. Experimental results showing phase-shedding (plug-out) operation of cell 2. (a) Top trace: v_{dc1} (60 V/div), 2nd trace: v_{dc2} (60 V/div), 3rd trace: i_{Ls1} (10 A/div), Bottom trace: i_{Ls2} (10 A/div). (b) Top trace: v_o (60 V/div), 2nd trace: i_o (1.2 A/div), 3rd trace: i_{Ls1} (10 A/div), Bottom trace: i_{Ls2} (10 A/div). (c) Zoomed view of superimposed i_{Ls1} and i_{Ls2} (5 A/div). Time:- (a) 200 ms/div, (b) 200 ms/div, (c) Zx & Zy: 20 μs/div, Transition: 100 ms/div.



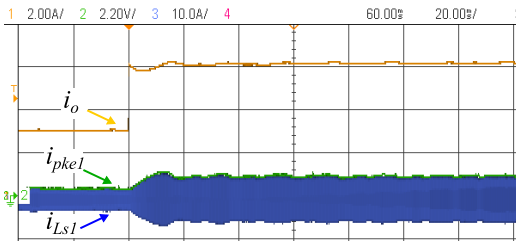
(a) MVDC voltages during phase-addition.



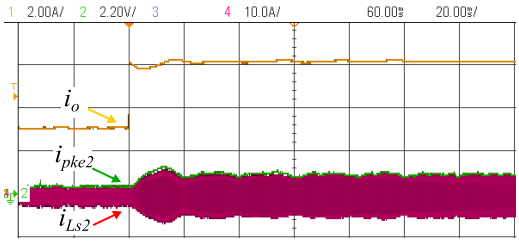
(b) v_o and i_o during phase-addition.

FIGURE 22. Experimental result showing phase-addition (plug-in) operation of cell 2. (a) Top trace: v_{dc1} (60 V/div), 2nd trace: v_{dc2} (60 V/div), 3rd trace: i_{Ls1} (10 A/div), Bottom trace: i_{Ls2} (10 A/div). (b) Top trace: v_o (60 V/div), 2nd trace: i_o (1.2 A/div), 3rd trace: i_{Ls1} (10 A/div), Bottom trace: i_{Ls2} (10 A/div). Time:- (a) 200 ms/div, (b) 200 ms/div.

marker for each DAB module to restrict it from over-current fault.



(a) Peak envelope monitoring of i_{Ls1}



(b) Peak envelope monitoring of i_{Ls2}

FIGURE 23. Top trace of (a) & (b): i_o (2 A/div). 2nd Trace of (a): i_{pke1} and 2nd Trace of (b): i_{pke2} (2.2 V/div). Bottom Trace of (a): i_{Ls1} and Bottom Trace of (b): i_{Ls2} (10 A/div). Time:- 20 ms/div.

V. CONCLUSION

A fundamental harmonic estimation based high-bandwidth current sensorless flexible power sharing control strategy of HFAC-L converter is presented in this article. This can be readily applied to modular SSTs. The salient contributions and distinguishing features of this research work are outlined in the following.

1) Estimation of inductor current fundamental harmonic active component forms the basis of this method. This variable is estimated and subsequently used for inner loop feedback of observer based power balance control through modular DAB. It also enables online monitoring of inductor peak current envelope.
2) Controlled zero power sharing (phase-shedding) while still maintaining the MVDC voltages, eliminates the need of additional MVDC link capacitor precharge circuit for subsequent phase-addition making the entire process seamless.
3) Reconfigurable for applications that require current regulation, while still maintaining power balance and MVDC voltage balance, due to direct control handle on the active component of fundamental current.
4) The current sharing error is found within $\pm 4\%$ in a load power variation range of 30% to full load without using high-bandwidth current sensors. This was achieved even after a 15% parametric variation of HF-link inductances from the rated value.

All of the above features of the proposed control scheme were validated through experiments.

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