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RESEARCH ARTICLE

Parallel AC-Link Connection of Current-Fed Dual Active Bridge Converters

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ABSTRACT This paper proposes a current-fed dual active bridge (DAB) converter, connected in parallel on the secondary-side AC-link, as a DC–DC converter with a high boost ratio and high input current capacity. Compared to conventional converters, the proposed converter can reduce the number of components without complicating power control and increase input current capacity. However, the parallel connection on the secondary-side AC-link could cause a circulating current. Therefore, this paper develops an equivalent circuit model of the proposed converter and theoretically analyzes the characteristics of the circulating current. The analysis reveals the influences caused by the circulating current on the proposed converter and shows a guideline for reducing the circulating current. Furthermore, using a prototype rated at 2 kW, the validity of the theoretical analysis is demonstrated through experiments. In the experiments, the validity of the theoretical analysis was confirmed, and it was verified that the proportion of the circulating current relative to the secondary-side converter's current was less than 8% at maximum. In addition, introducing a phase-shift control on the primary-side converters reduced the input current ripple by 38.6%. Furthermore, even under conditions where the circulating current is relatively large, the efficiency drop of the proposed converter was minimal. This indicates that the influence of the circulating current on the proposed converter is sufficiently small.

INDEX TERMS Circulating current, dual active bridge, fuel cell, high efficiency, high voltage ratio, input current ripple.

I. INTRODUCTION

Fuel cell-based power systems are increasingly used as power supplies for applications such as smart homes. As a result of easy manufacturing and cost considerations, fuel cells are often designed to operate at low voltages and high current outputs. Therefore, a DC–DC converter is typically connected to the output of the fuel cell to boost the voltage and regulate it to meet 100 V or 200 V load requirements, depending on the country. Additionally, an inverter is connected in the subsequent stage of the DC–DC converter to generate AC voltage. When the output voltage of fuel cells is assumed to be around 20 V, DC–DC converters are desired to

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have a high boost ratio and high input current capacity [\[1\],](#page-12-0) [\[2\],](#page-12-1) [\[3\],](#page-12-2) [\[4\]. A](#page-12-3)dditionally, electrical isolation between the converter input and output is recommended for safety reasons. Furthermore, since ripples in the output current can accelerate the degradation of fuel cells, converters should also maintain their input current ripple below a specified value [\[3\],](#page-12-2) [\[5\].](#page-12-4)

One such DC–DC converter that satisfies these requirements is a current-fed dual active bridge (DAB) converter [\[5\],](#page-12-4) [\[6\],](#page-12-5) [\[7\],](#page-12-6) [\[8\],](#page-12-7) [\[9\],](#page-12-8) [\[10\],](#page-12-9) [\[11\]. C](#page-12-10)urrent-fed DAB converters have been reported to effectively reduce the transformer's current and the input current ripple [\[5\],](#page-12-4) [\[7\],](#page-12-6) [\[10\]. M](#page-12-9)oreover, the current-fed DAB converter presented in reference [\[11\]](#page-12-10) successfully achieves a high boost ratio and high efficiency. On the other hand, various methods can be considered to increase the input current capacity, as shown in Table [1.](#page-1-0)

TABLE 1. Comparison of methods to increase the input current capacity of the DAB converters.

Parallel configurations are commonly adopted when trying to increase the current capacity of the converter [\[12\],](#page-12-11) [\[13\],](#page-12-12) [\[14\].](#page-12-13) However, simply paralleling them leads to doubling the number of circuit components, such as power devices [\[15\]. E](#page-12-14)specially in converters with a high boost ratio, as mentioned earlier, it is difficult to benefit from paralleling due to the low current on the high-voltage side. This reduces the advantages of paralleling and increases costs.

To enhance the input current capacity without substantially increasing the number of power devices, configurations such as the triple active bridge converter can be contemplated. These configurations share transformers in the converters, as shown in references [\[16\],](#page-12-15) [\[17\],](#page-12-16) [\[18\]. T](#page-12-17)his design parallels the low-voltage side sharing a transformer and keeps the high-voltage side single-phase. However, when magnetic components such as transformers are shared, in principle, a significant circulating current flows between the shared converters (phases). Controlling this circulating current, especially during power regulation, makes the control scheme highly complex [\[19\],](#page-13-0) [\[20\].](#page-13-1)

This paper proposes a two-parallel current-fed DAB converter, as shown in Fig. [1,](#page-1-1) where the secondary-side AC–DC converters (active bridges) are shared in the secondary AC-link connection. High-input currents can be handled effectively by paralleling the current-fed active bridges, transformers, and additional inductors. Furthermore, sharing the secondary-side active bridge allows for a reduction of up to four power devices. In the AC-link section of the proposed

FIGURE 1. Parallel AC-link connection of the current-fed dual active bridge converters.

converter, ideally, no circulating current is generated because the two ports with high output impedance are connected to the one port with low input impedance. Therefore, even when the output current ripple of the fuel cell is reduced by providing a phase shift for each phase, the circulating current is not generated between parallels. However, actual circuits are influenced by parasitic inductances, capacitances, and finite switching speeds of power devices. Due to these factors, some circulating currents could be generated. Therefore, this paper investigates these characteristics of the circulating current through theoretical analysis and experiments. Then, by demonstrating the minimal influence of circulating currents in the proposed converter, the effectiveness of the proposed converter is also shown. In addition, this paper shows a guideline for reducing the circulating current based on the theoretical and experimental results.

In this paper, Section [II](#page-1-2) explains the configuration and operational principles of the proposed converter. Section [III](#page-3-0) details the analytical methodology for the circulating currents in the proposed converter, derived from the analysis models. Section [IV](#page-7-0) delves into discussions on the analytical results of circulating-current dynamics. Lastly, Section [V](#page-9-0) validates the analytical results through experiments, emphasizing the effectiveness of the proposed converter.

II. OVERVIEW OF PROPOSED CONVERTER

This section describes the configuration and operational principles of the proposed converter in Fig. [1.](#page-1-1)

A. CONFIGURATION OF PROPOSED CONVERTER

The proposed converter is paralleled from the primary power terminals to the secondary AC-link, and in this paper, each paralleled phase is called a Cell. One Cell comprises a DC inductor, two active half-bridges, a transformer, its leakage inductor l_x [H], and an additional inductor L_x [H], where $x = a$, b. Furthermore, the two Cells connect in parallel at the AC-link of the secondary-side active bridge.

The secondary-side active bridge can be considered an AC voltage source; therefore, the input impedance seen from the AC-link is sufficiently small. On the other hand, the output impedance of each Cell is high due to inductors $(l_a + L_a)$ and $(l_b + L_b)$. Therefore, ideally, the two Cells are decoupled, and no circulating current is generated. In other words, the two Cells can be controlled independently.

B. OUTPUT VOLTAGE OF ACTIVE BRIDGES

This section explains the operational principles of the proposed converter by focusing on both the primary-side and secondary-side active bridges. For simplicity in this section, every component within the circuit is assumed to be ideal. The equivalent series impedances included in the wiring, etc., are ignored. In addition, the transient responses accompanying dead-time periods and switchings are also ignored.

The primary-side legs of Cells A and B also work as boost converters. The voltages E_a and E_b across capacitors C_{a1} , C_{a2} , C_{b1} and C_{b2} [F] can be represented as:

$$
E_{\rm a} = E_{\rm b} = \frac{E_{\rm p}}{1 - d},\tag{1}
$$

where *d* symbolizes the duty cycle of the lower switch in each leg. In this paper, the duty cycle is set to a constant value of $d = 0.5$. The amplitude of square-wave voltages v_{ap} and *v*_{bp} [V] applied to the primary winding of the transformer is expressed by:

$$
|v_{\rm ap}| = |v_{\rm bp}| = 2E_{\rm p}.\tag{2}
$$

Conversely, the amplitude of the square-wave voltage v_s [V] outputted by the secondary-side active bridge is given by:

$$
|v_{\rm s}| = E_{\rm s}.\tag{3}
$$

C. OUTPUT POWER OF PROPOSED CONVERTER

The phase-shift angles between v_{ap} and v_s and between v_{bp} and v_s are represented as δ_{as} and δ_{bs} [rad], respectively. Here, Fig. [2](#page-2-0) shows the typical operating voltage and current waveforms. In Fig. [2,](#page-2-0) δ_{ab} [rad] represents the phase-shift angle between v_{ap} and v_{bp} , where $\delta_{ab} = \delta_{as} - \delta_{bs}$ always holds.

The currents flowing through Cells A and B denoted as $i_{La}(\theta)$ and $i_{Lb}(\theta)$ [A], are the same as the inductor currents of general single-phase DAB converters. There is the relationship $i_s(\theta) = i_{La}(\theta) + i_{Lb}(\theta)$. Consequently, the output power P_{out} [W] can be derived referred to that of the single-phase DAB converter [\[21\], a](#page-13-2)s follows:

$$
Pout
$$

= $\frac{1}{2\pi} \int_0^{2\pi} v_s(\theta) i_s(\theta) d\theta$
= $\frac{2N_a E_p E_s}{\omega (l_a + L_a)} \delta_{as} \left(1 - \frac{\delta_{as}}{\pi}\right) + \frac{2N_b E_p E_s}{\omega (l_b + L_b)} \delta_{bs} \left(1 - \frac{\delta_{bs}}{\pi}\right),$ (4)

where N_a and N_b represent the turns ratios of the transformers for Cells A and B, respectively. Additionally, ω [rad/s] represents the switching angular frequency.

FIGURE 2. Typical operating waveforms of the proposed converter.

Here, the secondary-side current $i_s(\theta)$ is given by:

$$
i_{s}(\theta) = \begin{cases} (i'_{La1} - i'_{Lb2}) & \theta + i_{s}(0), \\ \text{when } 0 \le \theta < \delta_{ab}. \\ (i'_{La1} + i'_{Lb1}) & (\theta - \delta_{ab}) + i_{s}(\delta_{ab}), \\ \text{when } \delta_{ab} \le \theta < \delta_{as}. \\ (i'_{La2} + i'_{Lb2}) & (\theta - \delta_{as}) + i_{s}(\delta_{as}), \\ \text{when } \delta_{as} \le \theta < \pi, \end{cases}
$$
(5)

where i_s (0), i_s (δ_{ab}), and i_s (δ_{as}) [A] represent the initial values for their respective periods. The slopes of *iL*^a and i_{Lb} within these periods, denoted by i'_{La1} , i'_{La2} , i'_{Lb1} , and i_{Lb2}' [A/rad], are expressed in the subsequent equations:

$$
\begin{cases}\ni'_{L\text{al}} = \frac{2N_{\text{a}}E_{\text{p}} + E_{\text{s}}}{\omega (l_{\text{a}} + L_{\text{a}})}, & i'_{L\text{a}2} = \frac{2N_{\text{a}}E_{\text{p}} - E_{\text{s}}}{\omega (l_{\text{a}} + L_{\text{a}})},\\ \ni'_{L\text{b}1} = \frac{2N_{\text{b}}E_{\text{p}} + E_{\text{s}}}{\omega (l_{\text{b}} + L_{\text{b}})}, & i'_{L\text{b}2} = \frac{2N_{\text{b}}E_{\text{p}} + E_{\text{s}}}{\omega (l_{\text{b}} + L_{\text{b}})}.\end{cases}
$$
(6)

This section discussed the fundamental operation of the proposed converter under ideal conditions. However, in actual

systems, circulating currents are generated between the cells due to parasitic impedances and nonideal switching behavior. The following section delves into the characteristics of these circulating currents through a theoretical analysis.

III. ANALYTICAL MODELS FOR CIRCULATING-CURRENT EVALUATION

This paper analyzes the circulating current using the equivalent circuit model of the proposed converter, as shown in Fig. [3.](#page-3-1) This section delves into the specifics of the model.

FIGURE 3. Equivalent circuit model of the proposed converter, focusing on Node X.

A. EVALUATION STRATEGY

The model shown in Fig. [3](#page-3-1) focuses on Node X, which is the crucial connection point between each Cell and the secondary-side active bridge. The circulating current can be modeled by observing the current behavior around Node X. The variables \dot{V}_{as} and \dot{V}_{bs} [V] represent the phasors of the transformers' secondary-side voltages v_{as} and v_{bs} [V] in Cells A and B, respectively. In contrast, \tilde{V}_s [V] represents the phasor of the output (input) AC voltage v_s of the secondary-side active bridge. Furthermore, Z_a and Z_b [Ω] are the equivalent series impedances (ESIs) when considering Cells A and B as AC voltage sources. In addition, Z_s [Ω] is an ESI model of the behavior of the secondary-side active bridge. From the configuration of Fig. [3,](#page-3-1) it is found that the amplitude of the circulating current $|\vec{l}_c|$ [A] decreases as Z_s becomes smaller in relation to Z_a and Z_b .

In this analysis, the circulating-current ratio (CCR) $[\%]$ is introduced to evaluate the influence of the circulating current during power transfer. It is defined as the ratio of the circulating current $|\dot{I}_c|$ to the current $|\dot{I}_s|$ flowing through the secondary-side active bridge, as follows:

$$
CCR = \frac{|\dot{I}_c|}{|\dot{I}_s|} \times 100.
$$
 (7)

To derive $|\dot{I}_s|$ and $|\dot{I}_c|$, itis essential to model voltage sources and impedances. Firstly, \dot{V}_{as} , \dot{V}_{bs} , and \dot{V}_{s} are represented as a superposition of sinusoidal voltage sources using the Fourier series. The phasors for the *n*-th order harmonic components, denoted by $\dot{V}_{as(n)}$, $\dot{V}_{bs(n)}$, and $\dot{V}_{s(n)}$ [V], are

modeled as follows:

$$
\begin{cases}\n\dot{V}_{\text{as}(n)} = \left\{1 - (-1)^n\right\} \frac{2\sqrt{2}k_a N_a E_p}{n\pi}, \\
\dot{V}_{\text{bs}(n)} = \left\{1 - (-1)^n\right\} \frac{2\sqrt{2}k_b N_b E_p}{n\pi} \exp\left[-jn\delta_{\text{ab}}\right],\n\end{cases} (8)
$$
\n
$$
\dot{V}_{\text{s}(n)} = \left\{1 - (-1)^n\right\} \frac{\sqrt{2}E_s}{n\pi} \exp\left[-jn\delta_{\text{as}}\right],
$$

where k_a and k_b represent the coupling coefficients of the transformers in Cells A and B, respectively.

Subsequently, Z_a and Z_b represent the composite impedances derived from the inductances of the additional inductors *L*^a and *L*b, in addition to the leakage inductances *l*^a and *l*b. These are also combined with their equivalent series resistances (ESRs) r_a and r_b [Ω]. They can be simply modeled as shown in [\(9\).](#page-3-2) Although strictly speaking, the impedances *Z*^a and *Z*^b might be influenced by the switching transient of the primary-side active bridges; they are disregarded since the values of $l_a + L_a$ and $l_b + L_b$ are considerably large.

$$
\begin{cases}\nZ_{a(n)} = r_a + j n \omega (l_a + L_a), \\
Z_{b(n)} = r_b + j n \omega (l_b + L_b).\n\end{cases} (9)
$$

However, the wiring impedance between Node X and the secondary-side active bridge is minimal. Thus, the influence of the switching transient in the secondary-side active bridge cannot be neglected when focusing on Node X. This means that the secondary-side active bridge cannot be modeled as an ideal AC voltage source with an internal impedance of zero. Therefore, Z_s needs to be modeled, considering the transient response during the switching of the secondary-side active bridge. Details of the modeling method are discussed in the next section.

B. MODELING OF BEHAVIOR OF SECONDARY-SIDE ACTIVE BRIDGE

In this section, the detailed model of Z_s shown in Fig. [3.](#page-3-1) The impedance Z_s is not constant within one switching cycle; it varies depending on the operating mode of the secondary-side active bridge. Fig. [4](#page-4-0) shows the models for each operating mode of the secondary-side active bridge during a switching half-cycle. These modes in Fig. [4](#page-4-0) are modeled by focusing on the conducting path of i_s . In Fig. [4,](#page-4-0) z_{DCbus} [Ω] denotes the ESI of both the DC-link capacitor and PCB. Modes 1 to 3 correspond to the operations during the dead-time period, whereas Modes 4 and 5 represent the operations when the ON signals are applied to S_{s1} and S_{s4} . Specifically, Mode 4 represents the transient state upon turn-on switching. Basically, the operating modes progress sequentially from Mode 1 to Mode 5, with some modes potentially skipped.

Here, the impedance Z_s in Mode m ($m = 1, 2, 3, 4, 5$) is denoted as $Z_{s,m}$ [Ω], and its period is defined as Θ_m (= $\theta_m - \theta_{m-1}$) [rad]. This paper derives \dot{I}_s and \dot{I}_c considering all operating modes using $I_{s,m}$ and $I_{c,m}$ [A] specific to Mode *m*. For Mode *m*, the *n*-th order harmonic component, denoted as $I_{s(n),m}$ and $I_{c(n),m}$ [A], is represented

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FIGURE 4. Models for the operating modes of the secondary-side active bridge.

by the following:

$$
\begin{cases}\n\dot{I}_{s(n),m} = \frac{Z_{b(n)} (\dot{V}_{as(n)} - \dot{V}_{s(n)})}{Z_{a(n)} Z_{b(n)} + Z_{b(n)} Z_{s(n),m} + Z_{s(n),m} Z_{a(n)}} \\
+ \frac{Z_{a(n)} (\dot{V}_{bs(n)} - \dot{V}_{s(n)})}{Z_{a(n)} Z_{b(n)} + Z_{b(n)} Z_{s(n),m} + Z_{s(n),m} Z_{a(n)}}, \\
\dot{I}_{c(n),m} = \frac{Z_{s(n),m} (\dot{V}_{as(n)} - \dot{V}_{bs(n)})}{Z_{a(n)} Z_{b(n)} + Z_{b(n)} Z_{s(n),m} + Z_{s(n),m} Z_{a(n)}}.\n\end{cases}
$$
\n(10)

Based on [\(10\),](#page-4-1) the *n*-th order harmonic components of the instantaneous currents $i_{s(n),m}(\theta)$ and $i_{c(n),m}(\theta)$ [A] in Mode *m* are modeled as follows:

$$
\begin{cases} i_{s(n),m}(\theta) = \sqrt{2} |i_{s(n),m}| \sin \{ \theta + \arg (i_{s(n),m}) \}, \\ i_{c(n),m}(\theta) = \sqrt{2} |i_{c(n),m}| \sin \{ \theta + \arg (i_{c(n),m}) \}. \end{cases} (11)
$$

The RMS values for the currents, $|\dot{I}_s|$ and $|\dot{I}_c|$, are given by:

$$
\begin{cases}\n|\dot{I}_{s}| = \sqrt{\frac{1}{\pi} \sum_{n} \sum_{m} \int_{\theta_{m-1}}^{\theta_{m}} i_{s(n),m}^{2}(\theta) d\theta}, \\
|\dot{I}_{c}| = \sqrt{\frac{1}{\pi} \sum_{n} \sum_{m} \int_{\theta_{m-1}}^{\theta_{m}} i_{c(n),m}^{2}(\theta) d\theta}.\n\end{cases}
$$
\n(12)

However, in the operating modes shown in Fig. [4,](#page-4-0) the current path is determined by both the states of gate signals of the power devices and the current direction of *i*^s . Therefore, not all operating modes are executed within one switching cycle, and there exist modes that are skipped. To clarify these mode transitions, the flowchart is shown in Fig. [5.](#page-4-2) In Fig. [5,](#page-4-2) θ_d [rad] is the dead-time period, represented in the phase domain and converted by $\theta_d = \omega T_d$, where T_d [s] denotes the dead-time period in the time domain.

FIGURE 5. Flowchart for the transition of operating modes during a switching half-cycle.

TABLE 2. Relationship of conditions and operating modes for each transition pattern.

Pattern	Condition I	Condition II	Condition III	Modes
Α	Yes		Yes	2, 3, 5
B	No	Yes	Yes	2, 3, 5
	Nο	Yes	No	
	No	Nο		

As illustrated in Fig. [5,](#page-4-2) the transition pattern of the operating modes is contingent on whether Conditions I–III are satisfied with four possible transition patterns, from A to D, existing. Table [2](#page-4-3) shows the relationship between Conditions I–III and the operating modes for each transition

FIGURE 6. Typical voltage and current waveforms of the secondary active bridge for each transition pattern during a switching half-cycle: (a) Pattern A, (b) Pattern B, (c) Pattern C, and (d) Pattern D.

pattern. Furthermore, Fig. [6](#page-5-0) shows typical waveforms of the gate signals, voltage $v_s(\theta)$, and current $i_s(\theta)$ for the secondary-side active bridge in each transition pattern during a switching half-cycle.

In Fig. $6(a)$, Pattern A represents the transition pattern in which S_{s1} and S_{s4} turn on with soft switching. At $\theta = \theta_0$, Condition I, which determines the direction (polarity) of *i*^s , is satisfied. Then, OFF signals are applied to S_{s2} and S_{s3} , initiating the charging and discharging of the output capacitances *C*oss [F]. It is noted that *C*oss is the parasitic capacitance of the power device, referred to as the output capacitance. In other words, Mode 1 is skipped, and the operating mode starts from Mode 2. Therefore, the initial phase is defined as $\theta_0 = \theta_1$. Furthermore, Condition III, which determines that the charging and discharging of *C*oss are completed within the dead-time period, is satisfied. Thus, the operating mode transitions to Mode 3, representing the free-wheeling operation. After Mode 3, the operating mode transitions to Mode 5, where S_{s1} and S_{s4} turn on. Since Mode 4 is skipped during this transition pattern, it is set as $\theta_3 = \theta_4$. Pattern B in Fig. $6(b)$ similarly represents the transition pattern where S_{s1} and S_{s4} turn on with soft switching, as in Pattern A. However, in Pattern B, the polarity of i_s inverts during the deadtime period, leading to a commutation phenomenon. Thus, Condition I is not satisfied and the operating mode starts from Mode 1. Additionally, Condition II, which determines the presence of the commutation phenomenon during the deadtime period, is satisfied. Then, the operating mode transitions to Mode 2. The subsequent mode transitions match those of Pattern A.

Pattern C in Fig. $6(c)$ represents the transition pattern where S_{s1} and S_{s4} turn on with incomplete soft switching. This transition pattern occurs when the charging and discharging of *C*oss do not finish during the dead-time period due to the commutation phenomenon of *i*^s . As a result, Condition III is not satisfied. Thus, the operating mode in Pattern C starts from Mode 1 and transitions to Mode 2. Then, Mode 2 transitions to Mode 4, which represents the transient state (saturation region) of the power devices.

Pattern D in Fig. $6(d)$ represents the transition pattern where S_{s1} and S_{s4} turn on with hard switching. During the

dead-time period, the charging and discharging operations of $C_{\rm oss}$ for S_{s1} and S_{s4} do not occur. Consequently, the operating modes transition in the sequence of Mode 1, Mode 4, and Mode 5.

Apart from the transition above patterns, there is a case where S_{s1} and S_{s4} do not turn on with complete soft switching even if $i_s(\theta_0) \geq 0$. However, because this paper assumes that a sufficient dead-time period is set for the charging and discharging of *C*oss, modeling of such operational modes is omitted.

The subsequent sections explain the details of the impedance $Z_{s,m}$ and the period Θ_m in Mode *m*.

1) MODE 1

Mode 1 is the operating model representing the conduction behavior of the body diodes in S_{s2} and S_{s3} . Mode 1 activates when Condition I is not satisfied, as observed in Patterns B to D. In this mode, the current i_s flows through the two body diodes and the DC-bus capacitor. Therefore, in the current path, there are the equivalent on-resistances r_D [Ω] of the diodes, and the ESI *z*_{DCbus} of the DC-bus capacitor and the PCB. This results in the equivalent impedance $Z_{s(n),1}$ of the *n*-th harmonic component in Mode 1, expressed as:

$$
Z_{s(n).1} = 2r_D + z_{DCbus}.\tag{13}
$$

Additionally, the period Θ_1 of Mode 1 is given by:

$$
\Theta_1 = \begin{cases} \frac{i_s(\theta_0)}{i'_{L\text{a}1} + i'_{L\text{b}1}} & \text{for Patterns B and C,} \\ \theta_d & \text{for Pattern D.} \end{cases}
$$
(14)

Mode 1 operates during the dead-time period with $i_s < 0$ and continues until i_s reaches 0. In other words, the length of Θ_1 depends on whether or not there is a commutation point where $i_s = 0$ during the dead-time period. Condition II represents this condition.

For Patterns B and C, where Condition II is satisfied, a commutation point where $i_s = 0$ exists during the dead-time period. After this commutation phenomenon, the operating mode transitions to Mode 2. In this context, Θ_1 can be derived from the initial current value i_s (θ_0) and its slope, as shown in [\(14\).](#page-5-1)

In contrast, Pattern D does not satisfy Condition II, indicating that there is a point where $i_s = 0$ that is satisfied after finishing the dead-time period. When ON signals are applied to S_{s1} and S_{s4} , the dead-time period is finished at $\theta = \theta_0 + \theta_d$, leading to the transition from Mode 1 to Mode 4. In this case, Mode 1 continues throughout the deadtime period, where $\Theta_1 = \theta_d$.

2) MODE 2

Mode 2 models the charging and discharging behavior of the output capacitances *C*oss in the power devices. Mode 2 activates when either Condition I or II is satisfied, as observed in Patterns A to C. In Mode 2, bacause *i*^s flows only through C_{oss} , the equivalent impedance $Z_{s(n),2}$ for the *n*-th harmonic component of *i*^s can be expressed as:

$$
Z_{s(n).2} = \frac{1}{jn\omega C_{\text{oss}}}.\tag{15}
$$

Additionally, the period Θ_2 of Mode 2 is represented as:

$$
\Theta_2 = \begin{cases}\n\frac{-i_s(\theta_1) + \sqrt{-i_s^2(\theta_1) + 4(i_{Lal} + i_{Lbl}^{\prime})C_{\text{oss}}E_s}}{i_{Lal}^{\prime} + i_{Lbl}^{\prime}} \\
\text{for Patterns A and B,} \\
\theta_d - \Theta_1 \quad \text{for Pattern C.} \n\end{cases}
$$
\n(16)

Because Mode 2 represents the charging and discharging operation of C_{oss} , the length of Θ_2 is determined based on whether this operation completes within the dead-time period. This is represented by Condition III, which is satisfied in Patterns A and B. Concurrently, v_s transitions from $-E_s$ to E_s , culminating in $v_s(\theta_2) = E_s$. After the transition completes, Mode 3 starts in Patterns A and B. Assuming that the charging and discharging of *C*oss in Patterns A and B are entirely conducted by i_s , Θ_2 is expressed as [\(16\).](#page-6-0) In this analysis, *C*oss is considered constant.

Conversely, Pattern C does not satisfy Condition III, implying that the charging and discharging of *C*oss are not finished during the dead-time period. This operation halts at $\theta = \theta_0 + \theta_d$ when the ON signals are applied to S_{s1} and Ss4, and then Mode 2 transitions to Mode 4. In this case, the duration of Mode 2 is from the end of Mode 1 to the end of the dead-time period, which is $\theta_2 = \theta_0 + \theta_d$.

3) MODE 3

Mode 3 models the period during which the body diodes of S_{s1} and S_{s4} conduct. Mode 3 activates when Condition III is satisfied, as observed in Patterns A and B.

In Mode 3, as in Mode 1, *i*^s flows through the two body diodes, the DC-bus capacitor, and the PCB. Therefore, the ESI $Z_{s(n),3}$ for the *n*-th harmonic component of i_s in Mode 3 is given by:

$$
Z_{s(n),3} = 2r_D + z_{DCbus}.\tag{17}
$$

Mode 3 is an operation that exists exclusively in Patterns A and B and initiates after passing through Modes 1 and 2.

The duration continues until the end of the dead-time period when the ON signals are applied to S_{s1} and S_{s4} . Here, θ_3 is represented as $\theta_3 = \theta_0 + \theta_d$, and θ_3 is expressed as:

$$
\Theta_3 = \theta_d - \Theta_2 - \Theta_1. \tag{18}
$$

Note that because Mode 1 does not exist in Pattern A, $\Theta_1 = 0$. When the ON signals are applied to S_{s1} and S_{s4} , S_{s1} and S_{s4} turn on with soft switching since the charging and discharging of *C*oss are already completed in Mode 2. Mode 4 is skipped in this case, and Mode 3 directly transitions to Mode 5.

4) MODE 4

Mode 4 models the transient response period (saturation region) during the turn-on switching of the power devices. This mode is initiated in cases where neither Condition II nor Condition III is satisfied (Patterns C and D), and the power devices turn on with either incomplete soft or hard switching. In Mode 4, *i*^s flows through the power devices and *z*DCbus, which is in the turn-on transient state. The equivalent resistances of the power devices in the turn-on transient state are represented as $r_{on.sat}$ [Ω]. Therefore, the equivalent impedance $Z_{s(n)}$.4 for the *n*-th harmonic component of i_s can be represented as:

$$
Z_{s(n).4} = 2r_{\text{on.sat}} + z_{\text{DCbus}}.\tag{19}
$$

The power devices operate in the saturation region in the turn-on transition state. Consequently, the equivalent resistance *r*on.sat varies with the D–S voltage and the drain current and cannot be expressed as a constant resistance value. The relationship between the D–S voltage $v_{ds}(\theta)$ [V] and the current i_s flowing in the drain is averaged by Θ_4 and modeled. From the above, $r_{on,sat}$ can be modeled as follows:

$$
r_{\text{on,sat}} = \frac{1}{i_s(\theta_3) \Theta_4} \int_{\theta_3}^{\theta_4} v_{\text{ds}}(\theta) \, d\theta \simeq \frac{v_{\text{ds}}(\theta_3)}{2i_s(\theta_3)},
$$
\nwhere $v_{\text{ds}}(\theta_3) = E_s - \frac{1}{2C_{\text{oss}}}(i'_{\text{Lal}} + i'_{\text{Lbl}}) \Theta_2^2.$ (20)

For the period Θ_4 , $v_{ds}(\theta)$ is modeled to vary linearly from $v_{ds}(\theta_3)$ to 0. In addition, strictly speaking, i_s varies with θ . However, for simplification, *i*^s is modeled as a constant whose initial value i_s (θ_3) in the period Θ_4 . Additionally, v_{ds} (θ_3) is derived from the charge quantity charged and discharged in Mode 2. However, because Mode 2 is skipped in Pattern D, $v_{ds}(\theta_3) = E_s.$

Mode 4 starts when the ON signals are applied to S_{s1} and S_{s4}. Then, Mode 4 finishes at $\theta_4 = \theta|_{v_5=E_s}$, and transitions to Mode 5. Θ_4 is proportional to $v_{ds}(\theta_3)$ and is modeled as:

$$
\Theta_4 = \frac{v_{\rm ds}(\theta_3)}{V_{\rm DD}} \omega T_{\rm r},\tag{21}
$$

where V_{DD} [V] and T_{r} [s] represent the power supply voltage during switching tests and the rise time of the power device, respectively, as referred to in its datasheet.

5) MODE 5

Mode 5 models the operation during the on-period (linear region) of S_{s1} and S_{s4} . In Mode 5, as shown in Fig. [4,](#page-4-0) i_s flows through the on-resistors $r_{\text{on,lin}}$ [Ω] in the power devices and z_{DCbus} . The equivalent impedance $Z_{s(n),5}$ for the *n*-th harmonic component of *i*^s in Mode 5 can be represented as:

$$
Z_{s(n),5} = 2r_{\text{on.lin}} + z_{\text{DCbus}}.\tag{22}
$$

The period Θ_5 of Mode 5 is expressed as follows:

$$
\Theta_5 = \begin{cases}\n\pi - \theta_d & \text{for Patterns A and B,} \\
\pi - \theta_d - \Theta_4 & \text{for Patterns C and D.}\n\end{cases}
$$
\n(23)

For Patterns A and B, as Condition III is satisfied, S_{s1} and S_{s4} turn on with soft switching. Therefore, Mode 5 starts when the ON signals are applied to S_{s1} and S_{s4} at $\theta = \theta_0 + \theta_d$ and finishes upon receiving OFF signals at $\theta = \theta_0 + \pi$.

In contrast, for Patterns C and D, S_{s1} and S_{s4} either turn on with incomplete soft or hard switching. Consequently, Mode 5 starts after Mode 4 and ends when S_{s1} and S_{s4} receive the OFF signals.

IV. ANALYTICAL RESULTS OF CIRCULATING-CURRENT CHARACTERISTICS

This section clarifies the circulating-current characteristics regarding the phase-shift angle δ_{ab} between Cells A and B. In the analysis, CCR, as shown in (7) , is evaluated under the condition that only power transfer from Cell A to the secondary side is considered. From the analytical models in the previous section, it can be said that the circulating current also has frequency characteristics. Therefore, this section reveals the characteristics of the circulating current in relation to both the phase-shift angle δ_{ab} and the operating frequency *f* [Hz] of the proposed converter.

A. ANALYTICAL CONDITION

Table [3](#page-7-1) shows the circuit parameters used in the analysis. Characteristics for r_{on} , r_{D} , C_{oss} and T_{r} refer to the datasheet of the power devices (*TOSHIBA* TW027N65C) [\[22\]. H](#page-13-3)owever, for simplicity in this analysis, *C*oss is considered constant under $v_{ds} = E_s$. Other parameters are measured using the LCR meter (*HIOKI* IM3536), and the representative values at 50 kHz are shown in Table [3.](#page-7-1) Furthermore, Table [4](#page-7-2) shows the frequency characteristic models of the circuit parameters.

Here, the analysis focuses on the circulating current originating from Cell A. For this purpose, it is assumed that $\delta_{\text{as}} = \delta_{\text{ab}}$ and $\delta_{\text{bs}} = 0$ deg. Under these conditions, ideally, only Cell A transmits power to the secondary side while ensuring $P_b = 0$ W. Furthermore, the series inductances $(l_a + L_a)$ and $(l_b + L_b)$ are intentionally changed according to the following formulas so that the rated output power P_r [W] maintains constant even when the switching frequency *f* is

TABLE 3. Circuit parameters used for the analysis.

Rated output power P_r	2 kW
Input voltage $E_{\rm p}$	17, 20, 23 V
Output voltage E_s (constant)	150 V
Duty ratio in the lower arm switches d	0.5
Dead-time period Td	200 ns
Turns ratios of the transformers in Cells A and B N_a , N_b	4
Coupling coefficients k_a, k_b	0.98
Power devices in Cells A and B	IXYS
	IXTK400N15X4
	TOSHIBA
Power devices in the secondary side	TW027N65C
On-resistance of TW027N65C r_{on} @25°C	$27.0 \text{ m}\Omega$
Equivalent resistance of body diodes in TW027N65C r_D	64.3 m Ω
Output capacitances of TW027N65C $C_{\text{oss}} \otimes v_{\text{ds}} = E_{\text{ss}}$	300 pF
Turn-on time of TW027N65C T_r @ $V_{\text{DD}} = 400$ V	50 ns
$(l_{\rm a} + L_{\rm a})_{\otimes 50 \rm kHz}, (l_{\rm b} + L_{\rm b})_{\otimes 50 \rm kHz}$	33.5, 32.8 μ H
ESRs of $l_a + L_a$, $l_b + L_b r_a$, $r_b \otimes 50$ kHz	181.6 , 178.5 m Ω
$\text{Re}[z_{\text{DCbus}}]$ @50 kHz	57.0 m Ω
$Im[z_{DCbus}]$ @50 kHz	-33.6 m Ω

TABLE 4. Frequency characteristic models of the circuit parameters.

changed.

$$
l_{a} + L_{a} = \frac{50 \times 10^{3}}{f} (l_{a} + L_{a})_{\text{@50kHz}},
$$

$$
l_{b} + L_{b} = \frac{50 \times 10^{3}}{f} (l_{b} + L_{b})_{\text{@50kHz}},
$$
 (24)

where $(l_a + L_a)_{\text{@50kHz}}$ and $(l_b + L_b)_{\text{@50kHz}}$ [H] are the representative values for $(l_a + L_a)$ and $(l_b + L_b)$ at $f =$ 50 kHz, respectively, as shown in Table [3.](#page-7-1)

B. ANALYTICAL RESULTS

Fig. [7](#page-8-0) shows CCR characteristics as the switching frequency *f* and the phase-shift angle δ_{ab} vary. Fig. [7](#page-8-0) indicates that CCR decrease around the switching frequency of $f = 30$ kHz. Fig. [8](#page-8-1) shows the influences of each operating mode on CCR. CCR caused by Mode *m* is evaluated using CCR_{*m*} [%], defined in the following:

$$
CCR_{.m} = \frac{\sqrt{\frac{1}{\pi} \sum_{n} \int_{\theta_{m-1}}^{\theta_{m}} i_{c(n).m}^{2}(\theta) d\theta}}{|\dot{I}_{s}|} \times 100. \quad (25)
$$

Fig. [8](#page-8-1) shows that Modes 2 and 4 significantly influence CCR across the whole, whereas the influence of Mode 5 increases as the switching frequency decreases. In contrast, Modes 1 and 3 do not have a significant influence. Particularly at $f = 50$ and 100 kHz, Modes 2 and 4 have a significant influence. Modes 2 and 4 correspond to either the charging or discharging mode of *C*oss or the transient response during turn-on switching. In these modes, v_s transitions from $+E_s$ to −*E*^s (or vice versa). The periods of transitions of *v*^s , denoted as Θ_2 and Θ_4 , are shorter than the period Θ_5 of Mode 5. However, the impedances $Z_{s(n),2}$ and $Z_{s(n),4}$ in Modes 2 and 4 are significantly high, implying a dominant influence on CCR. From (16) and (21) , it is found that the proportion of

FIGURE 7. CCR (circulating-current ratio) characteristic regarding the switching frequency f and phase-shift angle δ_{ab} when δ_{ab} is controlled so as to satisfy $\delta_{as} = \delta_{ab}$ and $P_b = 0$ W. (a) $E_p = 17$ V. (b) $E_p = 20$ V. (c) $E_p = 23$ V.

FIGURE 8. Influences of each operating mode on CCR. (a) $E_p = 17$ V, $f = 100$ kHz. (b) $E_p = 20$ V, $f = 100$ kHz. (c) $E_p = 23$ V, $f = 100$ kHz. (d) $E_p = 17$ V, f = 50 kHz. (e) $E_p = 20$ V, f = 50 kHz. (f) $E_p = 23$ V, f = 50 kHz. (g) $E_p = 17$ V, f = 20 kHz. (h) $E_p = 20$ V, f = 20 kHz. (i) $E_p = 23$ V, $f = 20$ kHz.

Modes 2 and 4 in one switching cycle increases as*f* increases; that is, both Θ_2 and Θ_4 increase with *f*. This is corroborated by Fig. $8(a)$ -(f), which shows that CCR₂, CCR₄, and CCR at $f = 100$ kHz are higher than at $f = 50$ kHz.

In Fig. [7,](#page-8-0) although CCR increases in the area where f < 30 kHz, the underlying cause differs. This is because, as shown in Fig. [7,](#page-8-0) as (f) decreases, the influence of Mode 5 increases and becomes dominant. Around $f = 30$ kHz,

the influences of Modes 2, 4, and 5 on CCR are balanced, resulting in a local minimum of CCR with respect to *f* .

From Fig. $7(b)$ and [\(c\),](#page-8-0) it can be seen that CCR indicates a pronounced peak at $E_p = 20, 23$ V with respect to δ_{ab} . This pronounced behavior is directly associated with the soft switching operating area. As indicated in Fig. $8(b)$ and [\(c\),](#page-8-1) there is a soft-switching boundary at the marked position. At the boundary, the dominant operating mode influences

CCR transitions from Mode 4 to Mode 2. In proximity to this boundary, the current i_s during the dead-time period is nearly zero, leading to extended charging and discharging periods for *C*oss. As a result, it can be said that the value of Θ² increases, and CCR becomes maximum.

On the other hand, a similar trend cannot be observed for $E_p = 17$ V, as shown in Fig. [7.](#page-8-0) This is because, as shown in Fig. $8(a)$, all power devices operate with soft switching under $E_p = 17$ V. Consequently, although the maximum values reach approximately 6% for $E_p = 20, 23$ V as shown in Fig. [8\(d\)-\(f\),](#page-8-1) they are significantly lower for $E_p = 17$ V, remaining below 2%.

From the above analysis, it can be concluded that when the proposed converter operates in the tens of kHz range, CCR is sufficiently low. In particular, at $f = 50$ kHz, it can be observed that CCR is below 6%. Furthermore, by designing circuit parameters to operate farther from the soft-switching boundary, CCR can be reduced. Additionally, the use of power devices with a smaller *C*oss can contribute to a reduction in CCR.

V. EXPERIMENT

This section demonstrates the validity of the theoretical analysis and the effectiveness of the proposed converter using a 2 kW-rated prototype. The prototype used in the experiments is shown in Fig. [9.](#page-9-1) This prototype is developed with the circuit parameters shown in Table [3.](#page-7-1) For the experiments, the *Myway* pCUBE (MWBFP3-1008-J02) is used as the input DC power supply, and the *Myway* APL-II (MWBFP2-1040) is used as the output load with the constant voltage.

FIGURE 9. Appearance of the prototype of the proposed converter.

A. OPERATING WAVEFORMS

Fig. [10](#page-9-2) shows the voltage and current waveforms where the phase-shift angle is set as δ_{ab} = 20 deg and δ_{as} = 30 deg. In Fig. [10,](#page-9-2) the primary-side active bridges are operated with a constant duty ratio $d = 0.5$, and it can be observed

FIGURE 10. Voltage and current waveforms in the prototype $(\delta_{ab} = 20 \text{ deg}, \delta_{as} = 30 \text{ deg})$. (a) $E_p = 17 \text{ V}, P_{out} = 1.2 \text{ kW}.$ (b) $E_p = 20 \text{ V},$ $P_{\text{out}} = 1.3 \text{ kW.}$ (c) $E_{\text{p}} = 23 \text{ V}$, $P_{\text{out}} = 1.5 \text{ kW.}$

that the amplitudes of voltages v_{ap} and v_{bp} are twice that of the input voltage E_p . Additionally, the voltage v_s has an amplitude equal to the output voltage *E*^s . The apparent current distortion, caused by the circulating current, is not observed

from the waveforms of i_{La} and i_{Lb} even when the phase-shift angle δ_{ab} is set between Cells A and B.

B. VERIFICATION OF CIRCULATING CURRENT

Because i_{La} also contains i_{as} , it is difficult to directly measure the circulating current i_c directly. i_{as} is derived from the difference in the current *iL*^a of Cell A at two operating points, which are measured by an oscilloscope (*Tektronix* MSO58), and then i_c is estimated. CCR can subsequently be determined using the RMS value of the estimated current \hat{i}_c [A] as $|\dot{i}_c|$.

At any operating point, where $\delta_{ab} = x_{ab}$ [deg] and $\delta_{as} = x_{as}$ [deg], the relationship of each current is represented as:

$$
i_{\text{La}} = i_{\text{c}} + i_{\text{as}}.\tag{26}
$$

At δ_{ab} = 0 deg and δ_{as} = x_{as} , where Cells A and B are operated in-phase, the circulating current is negligible, approximating $i_c \approx 0$. Thus, it can be considered that [\(26\)](#page-10-0) becomes $i_{La}|_{\delta_{ab}=0}^{\delta_{as}=x_{as}}$ = i_{as} . In other words, through this operation for the equations, it is possible to extract only *i*as for any phase-shift angle of δ_{as} . Thus, the estimated value of the circulating current \hat{i}_c at $\delta_{ab} = x_{ab}$ can be derived by:

$$
\hat{i}_{\rm c}\Big|_{\delta_{\rm ab}=x_{\rm ab}}^{\delta_{\rm as}=x_{\rm as}} = i_{\rm La}\Big|_{\delta_{\rm ab}=x_{\rm ab}}^{\delta_{\rm as}=x_{\rm as}} - i_{\rm La}\Big|_{\delta_{\rm ab}=0}^{\delta_{\rm as}=x_{\rm as}}.\tag{27}
$$

However, consistent with the analytical conditions, δ_{as} must be set to x_{ab} when measuring $i_{La}|_{\delta_{ab}=x_{ab}}^{\delta_{as}=x_{as}}$ $\delta_{\text{ab}} = x_{\text{ab}}$ and $i_{La} \vert_{\delta_{\text{ab}} = 0}^{\delta_{\text{as}} = x_{\text{ab}}}$ $\delta_{ab}=0$. The waveforms i_c in Fig. [10](#page-9-2) are calculated in the time domain using (27) . Similarly to the theoretical results, i_c increases during the transient response of the switching.

Fig. [11](#page-10-2) shows the experimental results of CCR characteristics between Cells A and B, with the switching frequency held constant at $f = 50$ kHz. To calculate CCR, the RMS of *i*^s is derived from its waveform measured by the oscilloscope, while the RMS of i_c is derived from i_c using (27) . As shown in Fig. [11,](#page-10-2) the experimental results indicate trends similar to the analytical results in most areas of δ_{ab} , and then, the validity of the theoretical analysis can be confirmed. This indicates that, in the prototype, the transient responses related to the charging and discharging of the power devices' *C*oss significantly influence CCR. The turnon switching operation in the secondary-side active bridge also significantly influences. Furthermore, CCR is confirmed to be small, less than 8%. This clarifies that the proposed converter does not generate a substantial circulating current even when a phase-shift angle δ_{ab} is set between Cells A and B.

However, discrepancies in the trends between the analytical and experimental results are confirmed near $\delta_{ab} = 0$ deg, particularly at $E_p = 17$ V. In this area, the primary-side converters operate with hard switching. Therefore, the noise caused by hard switching can be considered to be mixing with the measured currents. As a result, the correct current waveforms cannot be measured, which can lead to discrepancies between the experimental and analytical results.

FIGURE 11. Characteristics of the circulating-current ratio of the prototype (f = 50 kHz). (a) $E_p = 17$ V. (b) $E_p = 20$ V. (c) $E_p = 23$ V.

 (c)

C. INPUT CURRENT RIPPLE RATIO

Fig. [12](#page-11-0) shows the characteristics of the input current ripple ratio α [%] with respect to the output power P_{out} under various input-voltage conditions of E_p . The input current ripple ratio α is defined as:

$$
\alpha = \frac{I_{\text{p_rip}}}{I_{\text{p_dc}}} \times 100. \tag{28}
$$

Here, I_p_{rip} [A] is the RMS value of the ripple component in the input current, and *I*p_dc [A] represents the DC component of the input current.

From Fig. [12,](#page-11-0) it can be confirmed that introducing a phase-shift angle δ_{ab} between Cells A and B reduces the input

FIGURE 12. Characteristics of the input current ripple ratio in the prototype. (a) $E_p = 17$ V. (b) $E_p = 20$ V. (c) $E_p = 23$ V.

current ripple ratio compared to the state at $\delta_{ab} = 0$ deg. The effect is more pronounced with smaller values of *E*p. Especially at $E_p = 17$ V and $P_{out} = 0.8$ kW, the current ripple is reduced by up to 38.6%. Setting $\delta_{ab} \neq 0$ causes a phase shift in the current ripples originating from the DC inductors and switching in Cells A and B. This leads to a reduction in the RMS value of the ripple components.

D. EFFICIENCY CHARACTERISTICS

Fig. [13](#page-11-1) shows the efficiency characteristics for values of δ_{ab} . At $E_p = 20$ V, the efficiency reaches 97.8% at maximum.

FIGURE 13. Efficiency characteristics of the prototype. (a) $E_p = 17$ V. (b) $E_p = 20$ V. (c) $E_p = 23$ V.

Furthermore, as evident from Fig. $13(a)-(c)$, the efficiency characteristics at δ_{ab} = 0, 5, and 10 deg are similar in each E_p . However, the efficiency with $\delta_{ab} > 15$ indicates a trend to decrease compared to that with $\delta_{ab} = 0$ deg. When δ_{ab} is increased while P_{out} is held constant, the power load on Cell A also increases, leading to an increase in the conduction loss in Cell A. Therefore, for $\delta_{ab} \geq 15$ deg, it is considered that the increased conduction loss in Cell A significantly influences the efficiency, leading to a reduction compared to the case of $\delta_{ab} = 0$ deg. On the other hand, the efficiencies at $\delta_{ab} = 5$, 10 deg barely drop with respect to the characteristic at $\delta_{ab} = 0$ deg, indicating that the power

deviation does not significantly influence it. In addition, there is almost no drop in efficiency due to circulating currents. Therefore, it is found that the proposed converter offers a degree of operational flexibility concerning the phase-shift angle δ_{ab} between Cells A and B. Thus, even if there is a variation in the components used in each cell, it can be said that compensating the transmission power from each Cell with δ_{ab} poses no issue.

This paper evaluated the proposed converter as a two-port system using a single-input power supply. However, the efficiency characteristics shown in Fig. [13](#page-11-1) suggest that the proposed converter could also serve as a three-port system with different power supplies for each Cell.

VI. CONCLUSION

This paper proposed a current-fed dual active bridge (DAB) converter, connected in parallel on the secondary-side AC-link, as a DC–DC converter with a high boost ratio and high input current capacity. Compared to conventional converters, the proposed converter can reduce the number of components without complicating power control and increase the input current capacity.

In addition, an equivalent circuit model was developed focusing on the AC-link connection point for the theoretical analysis, and the circulating current analysis method was shown. Furthermore, the operating modes of the secondary-side active bridge and the modeling based on their transition patterns were detailed. From the results of the theoretical analysis, it was found that CCR tended to increase around the operating points for the soft-switching boundary of the secondary-side active bridge, CCR (circulating-current ratio) tended to increase. Furthermore, it was revealed that the circulating current is significantly influenced by the charging and discharging operation of *C*oss in the power devices. Consequently, in the case of increasing the switching frequency of the converter, it was implied that the time proportion of the charging and discharging operation for *C*oss increased, leading to an increase in the circulating current. However, it was found that CCR in the proposed converter is relatively minimal, peaking at approximately 6% at a switching frequency of 50 kHz. Furthermore, it was revealed that CCR could be reduced by operating the converter away from the soft-switching boundary and using power devices with a smaller C_{oss} .

In the experiments with a 2 kW prototype, CCR showed a trend similar to the theoretical analysis, confirming the validity of the analytical results. However, comparison with existing modeling methods will be a future issue. Furthermore, it was confirmed that introducing the phase-shift angle δ_{ab} between Cells A and B reduced the input current ripple without a large efficiency drop. This suggests that an operation with a certain degree of phase-shift angle is feasible. From the above, it was clarified that the influence of the circulating current due to paralleling in the AC-link is small. The proposed converter not only has proven effective but also shows potential as a three-port DC–DC converter.

- [\[1\] S](#page-0-0). D. Choudhury, V. M. Bhardwaj, P. Nandikesan, S. Mohanty, M. Shaneeth, and K. P. Kamalakaran, ''Control strategy for PEM fuel cell power plant,'' in *Proc. 1st Int. Conf. Power Energy NERIST (ICPEN)*, Nirjuli, India, Dec. 2012, pp. 1–3.
- [\[2\] M](#page-0-1). Raceanu, A. Marinoiu, M. Culcer, M. Varlam, and N. Bizon, ''Preventing reactant starvation of a 5 kW PEM fuel cell stack during sudden load change,'' in *Proc. 6th Int. Conf. Electron., Comput. Artif. Intell. (ECAI)*, Bucharest, Romania, Oct. 2014, pp. 55–60.
- [\[3\] B](#page-0-2). Yuan, X. Yang, and D. Li, "A high efficiency current fed multiresonant converter for high step-up power conversion in renewable energy harvesting,'' in *Proc. IEEE Energy Convers. Congr. Expo.*, Sep. 2010, pp. 2637–2641.
- [\[4\] X](#page-0-3). Liu, H. Li, and Z. Wang, ''A fuel cell power conditioning system with low-frequency ripple-free input current using a control-oriented power pulsation decoupling strategy,'' *IEEE Trans. Power Electron.*, vol. 29, no. 1, pp. 159–169, Jan. 2014.
- [\[5\] P](#page-0-4). Xuewei and A. K. Rathore, ''Comparison of bi-directional voltage-fed and current-fed dual active bridge isolated DC/DC converters low voltage high current applications,'' in *Proc. IEEE 23rd Int. Symp. Ind. Electron. (ISIE)*, Jun. 2014, pp. 2566–2571.
- [\[6\] S](#page-0-5). Bal, A. K. Rathore, and D. Srinivasan, ''Comprehensive study and analysis of naturally commutated current-fed dual active bridge PWM DC/DC converter,'' in *Proc. IECON - 42nd Annu. Conf. IEEE Ind. Electron. Soc.*, Florence, Italy, Oct. 2016, pp. 4382–4388.
- [\[7\] Z](#page-0-6). Wang and H. Li, ''A soft switching three-phase current-fed bidirectional DC–DC converter with high efficiency over a wide input voltage range,'' *IEEE Trans. Power Electron.*, vol. 27, no. 2, pp. 669–684, Feb. 2012.
- [\[8\] T](#page-0-7).-T. Le, C. Suk, S. Kim, and S. Choi, ''A four-phase current-fed DC–DC converter for wide voltage range applications,'' in *Proc. IEEE 9th Int. Power Electron. Motion Control Conf.*, Nanjing, China, Nov. 2020, pp. 774–778.
- [\[9\] D](#page-0-8). Chen, D. Sha, and T. Sun, ''Three phase current-fed semi dual active bridge DC–DC converter with hybrid operating mode control,'' *IEEE Trans. Power Electron.*, vol. 35, no. 2, pp. 1649–1658, Feb. 2020.
- [\[10\]](#page-0-9) D. Sha, Y. Xu, J. Zhang, and Y. Yan, "Current-fed hybrid dual active bridge DC–DC converter for a fuel cell power conditioning system with reduced input current ripple,'' *IEEE Trans. Ind. Electron.*, vol. 64, no. 8, pp. 6628–6638, Aug. 2017.
- [\[11\]](#page-0-10) D. Sha, F. You, and X. Wang, "A high-efficiency current-fed semi-dualactive bridge DC–DC converter for low input voltage applications,'' *IEEE Trans. Ind. Electron.*, vol. 63, no. 4, pp. 2155–2164, Apr. 2016.
- [\[12\]](#page-0-11) L. Yifei, W. Yubin, and W. Shanshan, "Sensorless current sharing in twophase input-parallel output-parallel DC–DC converters,'' in *Proc. 18th Int. Conf. Electr. Mach. Syst. (ICEMS)*, Pattaya, Thailand, Oct. 2015, pp. 1919–1924.
- [\[13\]](#page-0-11) D. Fang, W. Xu, L. Bu, and L. Song, "Input-parallel output-parallel DC–DC converter with MPPT technique for grid connection of multiple distributed generators,'' in *Proc. IEEE 11th Conf. Ind. Electron. Appl. (ICIEA)*, Hefei, China, Jun. 2016, pp. 2329–2333.
- [\[14\]](#page-0-11) J. Shi, T. Liu, J. Cheng, and X. He, "Automatic current sharing of an inputparallel output-parallel (IPOP)-connected DC–DC converter system with chain-connected rectifiers,'' *IEEE Trans. Power Electron.*, vol. 30, no. 6, pp. 2997–3016, Jun. 2015.
- [\[15\]](#page-0-11) D. Vinnikov, A. Chub, and E. Liivik, ''Multiphase galvanically isolated impedance-source DC–DC converter for residential renewable energy applications,'' in *Proc. IEEE 26th Int. Symp. Ind. Electron. (ISIE)*, Jun. 2017, pp. 1775–1780.
- [\[16\]](#page-0-11) M. Phattanasak, R. Gavagsaz-Ghoachani, J.-P. Martin, B. Nahid-Mobarakeh, S. Pierfederici, and B. Davat, ''Control of a hybrid energy source comprising a fuel cell and two storage devices using isolated three-port bidirectional DC–DC converters,'' *IEEE Trans. Ind. Appl.*, vol. 51, no. 1, pp. 491–497, Jan. 2015.
- [\[17\]](#page-0-11) H. Tao, J. L. Duarte, and M. A. M. Hendrix, ''Three-port triple-half-bridge bidirectional converter with zero-voltage switching,'' *IEEE Trans. Power Electron.*, vol. 23, no. 2, pp. 782–792, Mar. 2008.
- [\[18\]](#page-0-11) V. Nair R., S. Gulur, R. Chattopadhyay, and S. Bhattacharya, ''Integrating photovoltaics and battery energy storage to grid using triple active bridge and voltage source converters,'' in *Proc. 46th Annu. Conf. IEEE Ind. Electron. Soc.*, Singapore, Oct. 2020, pp. 3691–3696.
- **IEEE** Access®
- [\[19\]](#page-1-3) I. Biswas, D. Kastha, and P. Bajpai, ''Small signal modeling and decoupled controller design for a triple active bridge multiport DC–DC converter,'' *IEEE Trans. Power Electron.*, vol. 36, no. 2, pp. 1856–1869, Feb. 2021.
- [\[20\]](#page-1-4) V. N. S. R. Jakka, A. Shukla, and G. D. Demetriades, ''Dual-transformerbased asymmetrical triple-port active bridge (DT-ATAB) isolated DC–DC converter,'' *IEEE Trans. Ind. Electron.*, vol. 64, no. 6, pp. 4549–4560, Jun. 2017.
- [\[21\]](#page-2-1) B. Zhao, Q. Song, W. Liu, and Y. Sun, "Overview of dual-activebridge isolated bidirectional DC–DC converter for high-frequency-link power-conversion system,'' *IEEE Trans. Power Electron.*, vol. 29, no. 8, pp. 4091–4106, Aug. 2014.
- [\[22\]](#page-7-3) TOSHIBA. (2022). *TW027N65C Data Sheet/Japanese*. Accessed: Sep. 5, 2023. [Online]. Available: https://toshiba.semicon-storage.com/ info/TW027N65C_datasheet_ja_20221214.pdf?did=143231&prod Name=TW027N65C

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