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RESEARCH ARTICLE

A 12-bit 1.1GS/s Pipelined-SAR ADC With Adaptive Inter-Stage Redundancy in 28 nm CMOS

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ABSTRACT This paper presents a 12-bit 1.1GS/s single-channel pipelined-successive approximation register (pipelined-SAR) analog-to-digital converter (ADC) with a three-stage architecture implemented in a 28nm CMOS technology. A new technique that provides adaptive inter-stage redundancy is proposed to mitigate the speed overhead of the conventional inter-stage redundancy bit. An adaptive inter-stage redundancy bit is implemented in the third stage to improve its conversion speed. In addition, the first-stage CDAC is implemented with a large-DAC and a small-DAC to address the speed bottleneck by improving the settling speed during the bit conversions, and a high speed detect-and-skip (DAS) decoder with minimum power overhead is incorporated to reduce the switching power without affecting the high-speed operation. The single-channel ADC achieves an SNDR of 60.1 dB and an SFDR of 75.3 dB at the Nyquist input operating at 1.1GS/s. With 8.5 mW power consumption at a 0.9 V power supply, it achieves a Walden FOM of 9.3 fJ/conv.-step and a Schreier FOM of 168.2 dB.

INDEX TERMS Analog-to-digital converter (ADC), successive approximation register (SAR), pipelined-SAR ADC, inter-stage redundancy, DAC switching.

I. INTRODUCTION

Recently, there has been growing interest in analog-to-digital converters (ADC) with Gigahertz sampling rate and medium-to-high resolution ($\geq$10bit) in various applications, such as wireless and wireline communication systems, and data acquisition systems in scientific instrumentation [1], [2], [3], [4], [5], [6].

Pipelined ADCs and time-interleaved (TI) ADCs are known structures for achieving a high sampling rate. For pipelined ADCs, while the pipelining scheme can achieve high sampling rate by pipelining multiple stages working simultaneously, they require a relatively large number of inter-stage residue amplifiers (RAs) that impose stringent requirements on the gain and linearity to achieve the desired precision [7], [8]. These RAs are mostly analog circuits and limit the overall energy efficiency especially in advanced CMOS processes. TI ADCs alleviate the speed bottleneck of single-channel ADCs by interleaving multiple channels that sample the input with evenly spaced phase shifts [9], [10], [11]. However, interleaving multiple channels introduces inter-channel nonidealities such as offset and gain mismatches as well as the timing mismatch, which significantly affect the accuracy of the overall ADC [12]. Sophisticated input and clock distribution networks have been proposed to minimize such mismatches [13]. In addition, background calibration techniques are usually required to suppress the inter-channel nonidealities to achieve sufficient resolution [14], [15], leading to high design complexity and large hardware overhead.

With the CMOS technology scaling, a pipelined-successive approximation register (pipelined-SAR) ADC has become an attractive candidate for high-speed applications because of its several advantages [16], [17]. On one hand, the digital SAR logic largely benefits from the advanced process in terms of speed and energy efficiency. On the other hand, the pipelining structure not only mitigates the speed limitation of SAR's one-bit-per-conversion operation

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by allocating fewer bits in one stage, but also relaxes the noise requirement of the circuits for least-significant-bits (LSBs) quantization, thus further improving the ADC performance. Three-stage pipelined-SAR ADCs have been shown capable of operating at 1GS/s with 12-bit resolution [18], [19]. In [18], [19], the 1st, 2nd and 3rd stage resolves 4-bit, 4-bit, and 6-bit, respectively, including 1-bit inter-stage redundancy implemented in both the 2nd and 3rd stages. This bit allocation balances the speed of each stage and hence optimizes the overall speed. The large-DAC(L-DAC)/small-DAC(S-DAC) approach proposed in [18] further improves the speed of the 1st stage. In addition to a large sized CDAC (L-DAC) that meets the ADC's KT/C noise requirement, it implements an additional small sized CDAC (S-DAC) with a faster settling speed for bit conversions. The bit decisions on the S-DAC are then transferred to the L-DAC to generate the residue voltage for the succeeding stages to ensure the overall resolution. Although this scheme speeds up the 1st stage conversion, the S-DAC introduces extra switching power consumption.

In this paper, we propose a three-stage pipelined-SAR ADC with reduced switching power and improved conversion speed compared to prior works with similar architecture. In this ADC, in addition to the L-DAC/S-DAC [18] that improves the 1st stage conversion speed, a high-speed detect-and-skip (DAS) encoder [20] is implemented so that the switching power of the L-DAC is considerably reduced. Moreover, an adaptive inter-stage redundancy is proposed and implemented in the 3rd stage to provide more time margin for the 6-bit conversions. The presented 12-bit single-channel ADC achieves a sampling rate of 1.1GS/s with an SNDR of 61.3 dB and 60.1 dB at low input frequency and Nyquist input, respectively. It consumes 8.5 mW when operating at 1.1GS/s, which achieves a Walden FOM (FOM_{Walden}) of 9.3 fJ/conv.-step and a Schreier FOM ($FOM_{Schreier}$) of 168.2 dB.

This paper is organized as follows. Section II explains the tolerance of inter-stage redundancy to nonidealities and the proposed adaptive inter-stage redundancy. Section III shows the architecture of the proposed pipelined-SAR ADC as well as the circuit implementation. Section IV presents the measurement results. Finally, Section V concludes this paper.

II. ADAPTIVE INTER-STAGE REDUNDANCY

A. SPEED LIMITATION

As shown in Fig. 1, in a three-stage pipelined-SAR structure, the 1st stage needs to complete the signal sampling, the 1st-stage bit conversions, and residue amplification by RA1 within one period. The 2nd stage needs to perform sampling, 2nd-stage bit conversions, and residue amplification by RA2 within one cycle. The 3rd stage needs to complete the sampling and 3rd-stage bit conversions within the same time.

As the overall speed of the pipelined-SAR ADC is limited by the slowest stage, the bit allocation is critical for achieving a high sampling rate. Since the 1st stage and 2nd stage have an amplification phase after the bit conversions while the

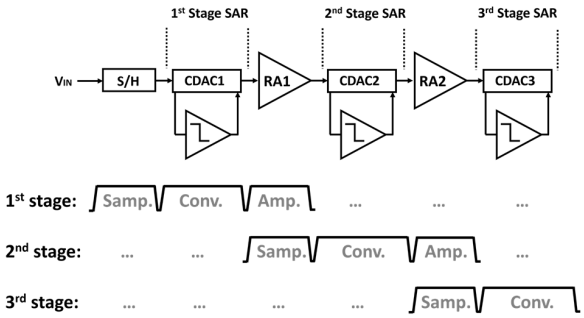

FIGURE 1. Operation principle of a three-stage pipelined-SAR ADC.

3rd stage does not, fewer bits should be allocated in the 1st stage and 2nd stage to ensure a sufficient sampling and amplification time. With a total number of 14 bit conversions in the ADC including the inter-stage redundancy bit in the 2nd stage and 3rd stage, allocating 4-bit, 4-bit, and 6-bit in the 1st, 2nd, and 3rd stage, respectively, balances the speed of each stage so that the overall speed is maximized. However, even though the 1st and 2nd stages have similar operations and the same number of bit conversions, the 1st stage is usually the speed bottleneck because of the longer settling time caused by the large CDAC size (~670fF) imposed by the KT/C noise requirement of the 12-bit ADC. This issue can be resolved by the L-DAC/S-DAC approach proposed in [18], where the S-DAC performs bit conversions and transfers the bit decisions to the L-DAC to generate a precise residue voltage for RA1. Hence, the speed of the 1st stage bit conversions is limited only by the settling time of the S-DAC and it is comparable to that of the 2nd stage as the size of the S-DAC is comparable to the size of CDAC2.

Normally, the 3rd stage does not seem to limit the overall speed because it does not require an RA amplification time after the bit conversions. However, the speed of the comparators is negatively correlated to the magnitude of its input. The averaged SAR-conversion time of each bit in the 3rd stage is longer than that of the 1st or the 2nd stage as the averaged input of the comparators in the 3rd stage is smaller due to the 6-bit conversions including one inter-stage redundancy bit. To improve the 3rd stage conversion speed, we proposed an adaptive inter-stage redundancy scheme that mitigates the speed overhead of the conventional inter-stage redundancy.

B. EFFECT OF INTER-STAGE REDUNDANCY

The inter-stage redundancy is critical in a pipelined-SAR ADC to provide tolerance to the errors caused by some of the nonidealities in the preceding stage. The nonidealities of a pipelined-SAR ADC can be roughly classified into three categories:

1) 1ST TYPE

The nonidealities in the 1st type are those that directly distort the voltage to be quantized, such as the settling error during the sampling phase, the KT/C noise of the CDAC and the

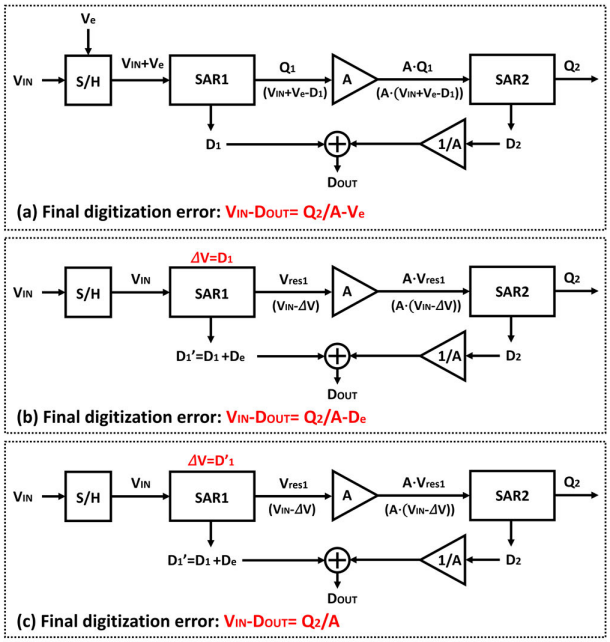

FIGURE 2. Effect of different types of nonideality in the 1st stage on the overall accuracy.

noise and nonlinearity of RAs, etc. Such nonidealities directly affect the accuracy of ADC. An example of the effect of such nonidealities is shown in Fig. 2 (a). The final digitization error (V_{IN}-D_{OUT}) is the summation of the sampling error V_e and the typical quantization error Q_2/A, where Q_2 is the quantization error of the 2nd stage SAR (SAR2) and A is the gain of the RA. These nonidealities typically dominate the noise contribution in a high-speed medium-resolution pipelined-SAR ADC.

2) 2ND TYPE

The nonideality of the 2nd type is the one that affects the quantizer to generate an incorrect digital output which differs from the CDAC switching process. In other words, the switching voltage on CDAC (i.e. the voltage change on CDAC caused by bit switching) is not equal to the voltage reconstructed by the digital output. For example, when the bit decision of one particular bit cannot be resolved in time because of metastability, the CDAC is not switched for that bit and the following bits while the digital output of those bits remains at the default value, generating an error between the switching voltage and the quantization result. An example is shown in Fig. 2 (b). The switching voltage in the 1st stage (ΔV) is equal to the voltage reconstructed by the bit decisions that have been resolved (D_1), while the 1st stage digital output (D'_1) is equal to D_1+D_e where D_e is the error of digital output caused by the unresolved bits. The residue voltage of the 1st stage V_{res1} is equal to V_{IN}-ΔV, hence the information of D_e is lost in the residue voltage. In this case, the error D_e shows up in the final digitization error regardless of the 2nd stage SAR. The metastability errors can be largely suppressed by allocating reasonable time margin for each bit in an asynchronous SAR stage so that it introduces neglectable impact on the overall SNR compared to other nonidealities.

3) 3RD TYPE

The nonidealities in the 3rd type are those that affect the quantizer to generate potential wrong bit decisions resulting in an excess residue voltage while the switching voltage on CDAC is the same as the voltage reconstructed by the digital outputs. These nonidealities include the offset/noise of the comparator, the kick-back noise from the comparator and the settling error of CDAC during the bit switching, etc. The errors caused by such nonidealities can be tolerated by the next stage if the full-scale range of the next stage is sufficient to cover the excess residue voltage. An example that shows the effect of this type of nonidealities is illustrated in Fig. 2 (c), where the 1st stage quantization result (D'_1) has an error (D_e) in addition to the correct digital code (D_1). The switching voltage (ΔV) is the same as D'_1, leading to an excess residue voltage V_{res1} that exceeds the typical quantization error (V_{IN}-D_1). When the full-scale range of the 2nd stage has enough redundancy to cover the error term $A{\cdot}D_e$, the excess residue can be quantized by the next stage's SAR quantizer with a quantization error of Q_2 and D_e does not appear in the final digitization error. Hence, the error caused by nonidealities of this type can be tolerated by the redundancy range of the next stage.

The inter-stage redundancy bit is commonly implemented to provide the redundancy range to tolerate the preceding stage's excess residue voltage caused by the nonidealities of the 3rd type. Moreover, it relaxes the CDAC settling during bit conversions and the noise requirement of the comparator design in the preceding stage, thus the speed and energy efficiency can be improved. Hence, inter-stage redundancy is necessary in this pipelined-SAR ADC to achieve the desired performance. However, while the inter-stage redundancy bit improves the speed of the SAR operation in the preceding stage, it introduces one extra bit conversion in the current stage to ensure the resolution, which results in one extra conversion step and causes speed overhead.

C. ADAPTIVE INTER-STAGE REDUNDANCY

In the ideal situation, the 2nd stage residue voltage ranges from $-0.5{\cdot}LSB_2$ to $0.5{\cdot}LSB_2$, where LSB_2 is the LSB of the 2nd stage. Therefore, with the gain of 8x provided by RA2, the input range of the 3rd stage is $8{\cdot}LSB_2$. With conventional 1-bit inter-stage redundancy, the reference voltage of the 3rd stage (V_{REF3}) is chosen as $8{\cdot}LSB_2$ so that the full-scale range of the 3rd stage is $16{\cdot}LSB_2$, which is doubled to provide $8{\cdot}LSB_2$ redundancy range that covers the excess voltage caused by the nonidealities of the 2nd stage.

To mitigate the speed overhead introduced by the extra bit conversion of the redundancy bit, an adaptive inter-stage redundancy scheme is proposed in this paper. When the magnitude of the 3rd stage input is no larger than $V_{REF3}/2$, the 3rd stage can cover such input without switching the redundancy bit. Thus, the 3rd stage only needs to perform the bit conversions of the five LSBs. On the other hand, when the 3rd

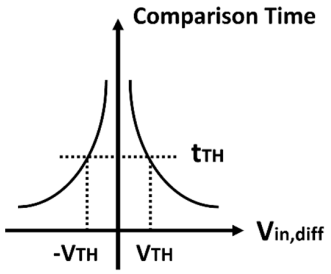

FIGURE 3. Comparator resolving time versus input voltage.

stage input exceeds $V_{REF3}/2$, the decision of the redundancy bit can be resolved quickly and is insusceptible to any small errors at the comparator's input. Hence, the comparison of the redundancy bit can be resolved during the settling phase of the RA2 amplification and the redundancy bit conversion does not affect the timing budget of the 3rd stage.

In our proposed adaptive inter-stage redundancy, the magnitude of RA2's output is sensed by the comparator's resolving time, similar to that in the proximity detector in [21]. For a conventional comparator, it is composed of a pre-amplification stage and a regeneration stage. The pre-amplification time is determined by the capacitance load and the common-mode current [22]. For the regeneration phase, the initial voltage difference grows exponentially with a time constant τ determined by the output load and the effective transconductance of the latch. Hence, the resolving time of the comparator for a given input V_{in} can be estimated as

$$t_{comp} = f\left(V_{in}\right) = t_{amp} + \tau \cdot ln\left(\frac{V_{DD}}{A \cdot V_{in}}\right) \qquad (1)$$

where $A \cdot V_{in}$ is the amplified input differential voltage that couples to the regeneration stage [23]. Without considering noise for simplicity, the monotonically decreasing relationship between the comparator's resolving time and its differential input is shown in Fig. 3.

The simplified adaptive inter-stage redundancy circuit and its timing diagram are shown in Fig. 4. When the RA2 has been enabled for some time (t_0) such that its output voltage ($RA2_{out}$) is approaching towards the final settled value, the comparator clock of the redundancy bit (CK_5) becomes active to start the comparison. A D-flip-flop clocked by a delayed version of CK_5 ($CK_{5,d}$) is used to check whether the redundancy bit decision is resolved within the timing threshold t_{TH}. When the input to the 3rd stage is larger than a certain threshold voltage V_{TH}, the comparison result (OUT_P, OUT_N) can be resolved within t_{TH}, the redundancy bit decision is made and stored by the D-flip-flop, and the redundancy bit is switched right after the RA2 amplification, as shown in Fig. 5 (a). When the input is smaller than V_{TH} such that the bit decision cannot be made during t_{TH}, the next bit (B_4) starts immediately after the RA2 amplification and the redundancy bit is not used, as shown in Fig. 5 (b). In either case, the time allocated for the redundancy bit overlaps with the RA2 amplification. Therefore, the time required for the

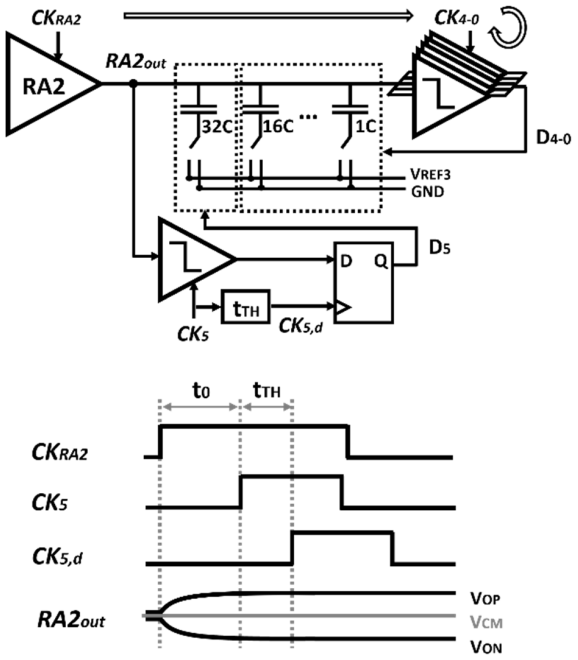

FIGURE 4. Simplified block diagram and timing diagram of the proposed adaptive inter-stage redundancy.

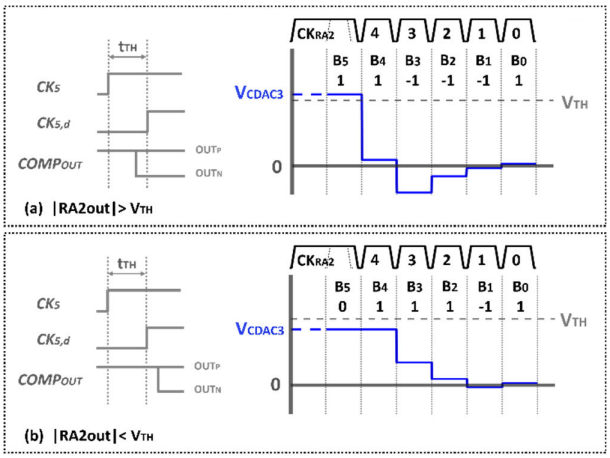

FIGURE 5. Operational example of the proposed adaptive inter-stage redundancy bit scheme. (a) $|RA2_{out}| > V_{TH}$. (b) $|RA2_{out}| < V_{TH}$.

3rd stage conversion is reduced by one bit of the comparison time and the associated SAR logic delay, resulting in an average of 95 ps (~10%) saved for the 3rd stage conversion. In addition, the switching power of CDAC3 is significantly reduced because its MSB is not switched for a large number of samples.

D. DESIGN CONSIDERATIONS FOR PVT VARIATIONS

The proper operation of the adaptive redundancy bit can be achieved by choosing the proper timing parameters t_0 and t_{TH}. Ideally, the t_{TH} should be designed such that the corresponding V_{TH} is $V_{REF3}/2$, so that the redundancy bit is only used when the rest of the bits in the 3rd stage cannot cover the RA2's output. However, the relationship between V_{TH} and t_{TH} as well as the t_{TH} itself are susceptible to PVT variations. Such variations may increase the quantization error of the

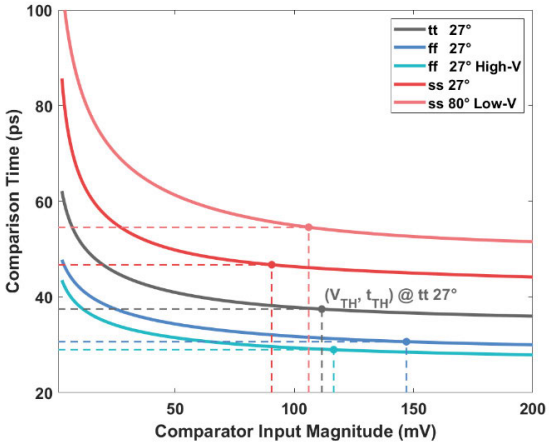

FIGURE 6. Simulated comparison time versus input magnitude and (V_{TH}, t_{TH}) at different PVT corners.

ADC, hence the value of t_{TH} needs to be carefully chosen. There are two potential issues that may be caused by the adaptive inter-stage redundancy bit with the PVT variations: (1) When the redundancy bit is not used, the 3rd stage cannot cover the output of RA2, leading to a large residue voltage that cannot be digitized; (2) When the redundancy bit is used, the bit decision is wrong due to the RA2's settling error during the redundancy bit's comparison. To avoid the above mentioned situations, two conditions must be met to ensure the robustness of the adaptive inter-stage redundancy: First, when the 3rd stage input exceeds half of the 3rd stage full-scale range, the comparison must be resolved within t_{TH} to ensure the 3rd stage will never get saturated; Second, the comparison result of the redundancy bit should not be susceptible to the RA2's settling error if it is resolved within t_{TH}.

To meet the first requirement, t_{TH} must be chosen such that V_{TH} is never larger than $V_{REF3}/2$ with PVT variations. For the second requirement, the settling error of RA2 is given by

$$V_{err}(t) = (V_{final} - V_{init}) \cdot e^{-\frac{t}{\tau}} \tag{2}$$

where V_{final} is the fully-settled output of RA2, V_{init} is the initial voltage at the beginning of the amplification, and τ is the time constant of RA2. The comparison result may flip due to the settling error when V_{final} has an opposite sign to that of the comparator's input at the start of the comparison, which can be expressed as

$$V_{final} \cdot \left(V_{final} - V_{err}(t_0)\right) < 0 \tag{3}$$

Substituting (2) into (3) yields

$$\left|V_{final}\right| < \frac{e^{-t_0/\tau}}{1 - e^{-t_0/\tau}} \cdot |V_{init}| = V_{UB} \tag{4}$$

Equation (4) shows that the settling error of RA2 may lead to wrong comparator decisions only when RA2's fully-settled output is below V_{UB}. Hence, V_{TH} must be larger than V_{UB} to ensure that the potential wrong decisions for the redundancy bit are not used. V_{TH} has been carefully simulated across different PVT corners to ensure that t_{TH} and t_0 are chosen such that:

$$\max_{PVT}(V_{TH}) < \frac{V_{REF3}}{2} \tag{5}$$

$$\min_{PVT}(V_{TH}) > V_{UB} \tag{6}$$

In this design, t_0 and t_{TH} are determined by the delay cells and combinational logic that generate CK_5 and $CK_{5,d}$. V_{REF3} is 650mV, and t_0 is chosen as 80ps such that V_{UB} is less than 20mV with PVT variations. The large voltage range between V_{UB} and $V_{REF3}/2$ provides reasonable margin to accommodate the fluctuations of V_{TH} resulting from PVT variations. Parameter t_{TH} is designed to be about 40 ps. The comparison time versus input magnitude, values of t_{TH} and its corresponding V_{TH} across different corners, temperatures (27 °C to 80 °C), and voltages (low-V of 0.81 V to high-V of 0.99 V) have been simulated and summarized in Fig. 6, where the horizontal dashed lines represent the simulated t_{TH} values and the vertical dashed lines represent the corresponding V_{TH} values for different PVT corners. With PVT variations, t_{TH} ranges from 30 ps to 55 ps and the corresponding V_{TH} ranges from 90 mV to 150 mV while still satisfying (5) and (6). Thus, calibration on t_0 and t_{TH} is not required in this ADC.

III. ADC ARCHITECTURE AND CIRCUIT IMPLEMENTATION

A. ADC ARCHITECTURE AND TIMING DIAGRAM

The block diagram and timing diagram of the proposed ADC are shown in Fig. 7. The ADC has a three-stage structure with two residue amplifiers (RA1 and RA2) in between to provide 8x voltage amplification. The three stages resolve 4b, 4b and 6b, respectively, with 1-bit inter-stage redundancy in both the 2nd and 3rd stage. Multiple comparators are used in each stage to enhance the conversion speed by eliminating the comparator reset time in the critical path. Overall, there are 14 comparators for the 14 bit conversions. Each bit structure is similar to that in [24] and it is designed in a modular way such that each bit contains its own comparator, SAR logic and CDAC drivers to reduce the design complexity. The RAs are implemented with an open-loop Gm-R structure with a Harmonic-Injecting Cross-Coupled Pair (HXCP) [19] to improve the gain and linearity.

The operation of the comparators and RAs is timed asynchronously to enhance the speed and reduce the power consumption associated with high-speed clocks. The desired pulse widths of the sampling clock (CK_S) and RA clocks (CK_{RA1}, CK_{RA2}) are generated by delay cells and combinational logic to ensure the desired pulse width. In this design, ~220ps is allocated for sampling and ~200ps is allocated for RA1 and RA2 amplification to ensure sufficient settling accuracy. To achieve a sampling rate of 1.1GS/s, ~480ps is left for the 4-bit quantization in both the 1st and 2nd stage. The CDAC1 implementation reduces the overall switching power and ensures the 1st stage and 2nd stage have similar conversion speed to meet the same timing requirement. The bit conversion of the 3rd stage needs to complete within ~700ps. The conversion of the 3rd stage's MSB (B_5) is implemented as

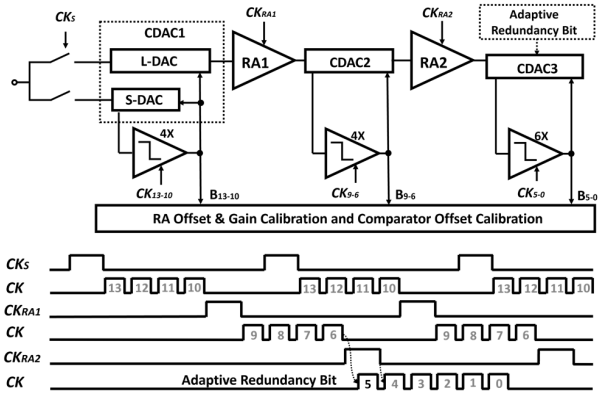

FIGURE 7. Block diagram and timing diagram of the proposed ADC.

the adaptive inter-stage redundancy bit to provide sufficient time margin for the LSBs conversions.

B. CDAC1 IMPLEMENTATION

While the L-DAC/S-DAC approach in [18] improves the conversion speed of the 1st stage, the switching of the S-DAC during bit conversions has power overhead, which increases the overall switching power of the 1st stage.

While process scaling largely improves the energy efficiency of SAR stages, it does not provide any advantage to the switching power of CDAC, given that the switching power is determined by the CDAC size and the switching frequency. Moreover, to meet the KT/C noise requirement, the CDAC size increases exponentially with the ADC resolution. The associated switching power can impact the overall power consumption of ADCs with relatively high resolution. A detect-and-skip (DAS) algorithm that utilizes a fine-ADC/coarse-ADC was proposed in SAR ADCs to significantly reduce the switching power on the large CDAC in the fine-ADC [20]. In the DAS algorithm, the coarse-ADC generates the decisions of the MSBs and these digital bits are encoded before transferring to the fine-ADC to avoid unnecessary switchings. Moreover, the encoded decisions of the MSBs are transferred simultaneously as 'aligned switching' to further reduce the switching power. However, an asynchronous signal is required to transfer the aligned switching signals to the fine-ADC, which introduces extra digital circuits and delay, suitable for low-speed SAR ADCs where the switching power accounts for a significant portion of the overall power consumption. However, for high-speed pipelined-SAR ADCs, the CDAC switching accounts for a smaller fraction of the total power consumption and there is a stringent requirement for the conversion speed, making the conventional DAS less attractive.

To reduce the overall switching power without affecting the speed and minimize power overhead in the digital logic, a CDAC1 with L-DAC/S-DAC and a high-speed DAS for the 1st MSB is implemented in this design. In addition to an L-DAC that meets the 12-bit KT/C noise requirement, an S-DAC is incorporated for faster bit conversions. The size of the S-DAC is chosen considering the tradeoff between

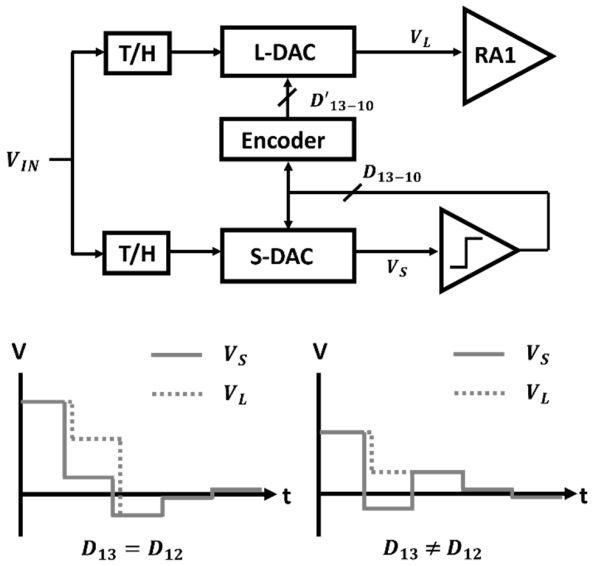

FIGURE 8. Block diagram and switching scheme of CDAC1.

speed and errors caused by mismatch and the kick-back noise from the comparators. Although these errors only need to be suppressed within 5-bit accuracy because of the inter-stage redundancy bit in the 2nd stage, they enlarge the 1st-stage residue voltage which would affect the linearity of RA1. The S-DAC is designed as 60 fF so that the mismatch and comparator kickback noise fulfill a > 6-bit accuracy [18], and the settling speed is significantly improved compared to that of using 670 fF L-DAC. The conversion time of 1-bit in the 1st stage asynchronous SAR consists of the comparison time, SAR logic delay, and CDAC switching time. Based on the post-layout simulation, the SAR logic delay is approximately 20 ps. The CDAC switching on the S-DAC takes 25 ps including the propagation delay of the buffer chain and the CDAC settling time to ensure a > 95% settling accuracy, which is about 25 ps faster than the CDAC switching on the L-DAC, thus improving the 1st-stage overall conversion time by 100 ps (∼11%). With an average of 120 ps allocated for one bit conversion, approximately 75 ps is left for the comparison with reasonable time margin to reduce the metastability rate so that it does not affect the overall SNR.

In this CDAC1, the S-DAC's bit decisions of the two MSBs are first encoded via the high-speed DAS before being transferred to the L-DAC. An operation example is shown in Fig. 8. When the S-DAC generates different bit decisions for its 1st-MSB (D_{13}) and 2nd-MSB (D_{12}), the L-DAC skips the switching of its 1st-MSB (D'_{13}) and only switches its 2nd-MSB (D'_{12}) based on D_{13} to generate the correct residue voltage. When D_{13} and D_{12} have the same value, the two MSBs of L-DAC (D'_{13} and D'_{12}) are the same as D_{13} and D_{12}. In either case, D'_{12} always follows D_{13}. Hence, the 2nd-MSB on the L-DAC can be switched immediately after resolving D_{13}. For D'_{13}, its decision is made based on two MSBs of S-DAC. Hence the 1st-MSB on the L-DAC switches after resolving both D_{13} and D_{12}. In this case, the settling time of L-DAC is maximized and the digital logic for aligned

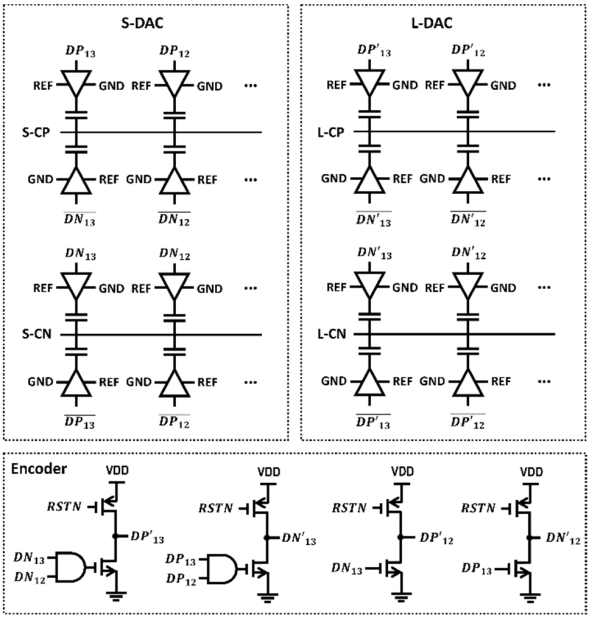

FIGURE 9. Implementation of the L-DAC/S-DAC and DAS encoder.

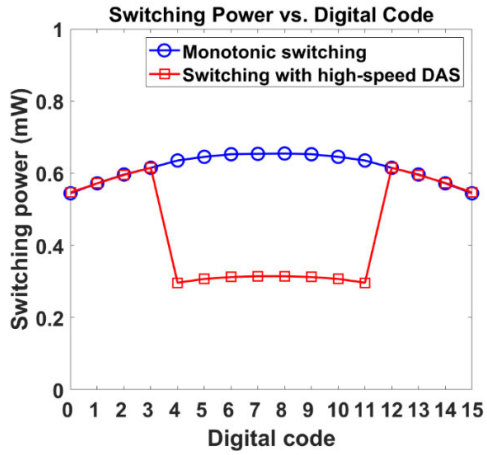

FIGURE 10. Switching power on L-DAC.

switching is not required. In this 4-bit CDAC1, the DAS is only applied to the MSB considering the trade-off between the power overhead of the DAS encoder and switching power reduction.

The implementation of the DAS encoder and the L-DAC/S-DAC is shown in Fig. 9. Both the L-DAC and S-DAC use the constant common-mode (CM) switching, where the differential summing node voltages (CP/CN) keep a constant common-mode voltage during the bit switching. DP/DN is generated by the SAR logic that controls the switch down/up operation of the S-DAC, and DP'/DN' is that of the L-DAC. The function of the encoder is summarized in TABLE 1.

The switching power comparison between the high-speed DAS scheme and the conventional monotonic switching scheme is shown in Fig. 10. Overall, the high-speed DAS saves approximately 25% (~0.16mW) of the switching

TABLE 1. Encoder function.

S-DAC		L-DAC		
D_{13}	D_{12}	DP'_{13}/ DN'_{13}	DP'_{12}/ DN'_{12}	1st MSB
0	0	0/1	0/1	Switch down
0	1	1/1	0/1	Not switched
1	0	1/1	1/0	Not switched
1	1	1/0	1/0	Switch up

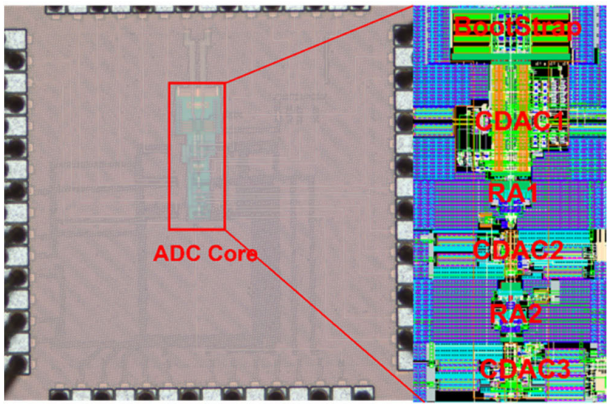

FIGURE 11. Chip photo.

power in the L-DAC when applying a full-scale sinusoidal input signal. The power consumption of the high-speed DAS is less than 0.02 mW, which is much smaller than the switching power that is saved.

C. RESIDUE AMPLIFIER DESIGN

The residue amplifier (RA) eases the noise requirements of the succeeding stages. But the RA itself introduces nonlinearities and its operation occupies the timing budget of the current stage and next stage. Moreover, the RA usually consumes a large portion of the power in the entire pipelined-SAR ADC, especially with the advanced processes. Hence, the design of RA is critical for Pipelined-SAR ADC to achieve the desired performance. In this design, the RA uses an open-loop fully-settled gm-R based structure for high speed and high energy efficiency [18]. The gm-cell is implemented in Flipped-Voltage-Follower (FVF) topology to achieve high linearity with large input range [25]. In addition to the main amplifier, a harmonic injecting cross-coupled pair (HXCP) is implemented to further improve the linearity [19]. It is shown in [19] that when the cross-coupled pair is biased in saturation region, it has an expansive I-V curve that nulls out the compressive effective transconductance of the gm cell in the main amplifier, thus suppressing the 3rd order harmonics of the RA. Moreover, the cross-coupled pair acts as a negative resistance that boosts the output impedance of the RA. Hence the gain is improved to 8x. The gain error of the open-loop RA is calibrated in foreground using the histogram-based calibration [26].

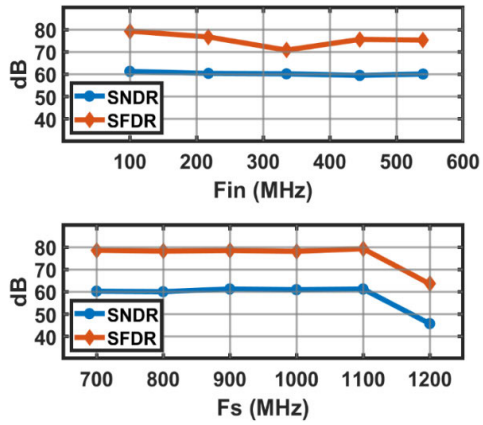

FIGURE 12. Measured SNDR/SFDR with input frequency and sampling frequency sweep.

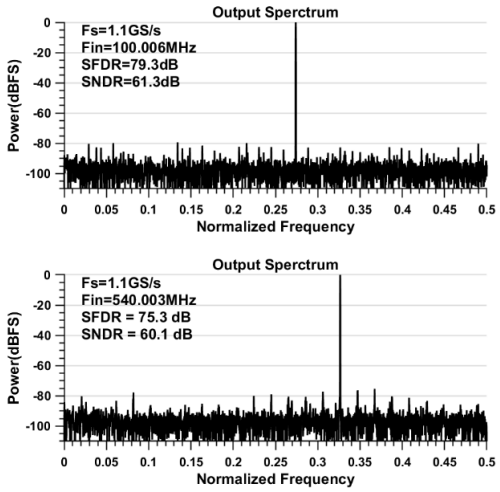

FIGURE 13. Measured output spectrum (8192 FFT points, 256x decimated).

D. COMPARATOR DESIGN

In this design, the double-tail comparator is implemented for a faster regeneration speed and smaller kick-back noise [27] compared to the strongArm latch. Moreover, the double-tail comparator does not impose a strictly defined input common-mode voltage and it provides better noise performance with a small supply voltage [23]. Note that the clock of the latch stage needs to be accurately aligned with that of the pre-amplification stage, as the latch stage needs to detect the differential voltage built up at the pre-amplifier's output nodes before they drop too low to provide sufficient gm [28]. The offset of the comparator is calibrated via the calibration voltages on the auxiliary pair in parallel with the input transistors. The calibration voltages are determined through foreground calibration and provided off-chip.

IV. MEASUREMENT RESULTS

The ADC was fabricated in a 28nm CMOS process. The chip photo is shown in Fig. 11. The measured SNDR/SFDR versus input frequency (Fin) at 1.1GS/s (top) and the SNDR/SFDR versus sampling frequency (Fs) with an input frequency of 100MHz (bottom) are shown in Fig. 12. The SNDR and

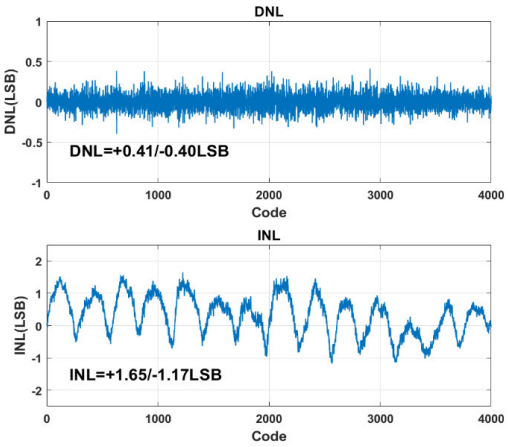

FIGURE 14. Measured DNL and INL.

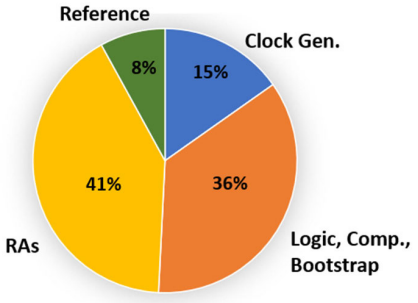

FIGURE 15. Power breakdown.

SFDR are maintained above 59 dB and 70 dB respectively when sweeping the input frequency with a sampling rate of 1.1GS/s. When sweeping the sampling rate with 100MHz input frequency, the SNDR is maintained above 60 dB and the SFDR is maintained above 78 dB up to 1.1GS/s. The FFT spectrum measured at 1.1GS/s with a low input frequency (top) and Nyquist input (bottom) is shown in Fig. 13. It achieves 61.3 dB/79.3 dB SNDR/SFDR at low input frequency and 60.1 dB/75.3 dB SNDR/SFDR at Nyquist input. The measured DNL and INL are $+0.41/-0.4$ LSB and $+1.65/-1.17$ LSB, respectively, as shown in Fig. 14.

The ADC consumes 8.5 mW at 1.1GS/s with a power supply of 0.9 V, corresponding to a Walden FOM (FOM_{Walden}) of 9.3 fJ/conv.-step and a Schreier FOM ($FOM_{Schreier}$) of 168.2 dB. The power breakdown is shown in Fig. 15. The power consumption of the reference voltages is only 0.68 mW, which is only 8% of the overall power consumption thanks to the high-speed DAS in the CDAC1 implementation.

A comparison of this ADC with previous works with similar specifications ([18], [19], [29], [30], [31]) is summarized in TABLE 2. Compared to the published state-of-the-arts, this ADC improves the sampling rate of the 12-bit single-channel ADCs while achieving comparable FOM_{Walden} and $FOM_{Schreier}$.

V. CONCLUSION

In this article, the capacitor array in the 1st stage of the pipelined SAR, CDAC1, is implemented with the

TABLE 2. Comparison table.

	This work	[31] SSCL'22 L. Fang	[30] JSSC'21 B.Hershberg	[29] JSSC'19 J. Largos	[18] JSSC'20 W. Jiang	[19] TCAS1'22 L. Fang
Process	**28nm**	28nm	16nm	28nm	28nm	28nm
Architecture	**Pipelined SAR**	Pipelined SAR	Pipeline	Pipeline	Pipelined SAR	Pipelined SAR
Resolution (bits)	**12**	12	11	12	12	12
Sample Rate (MS/s)	**1100**	1000	1000	1000	1000	1000
Supply Voltage (V)	**0.9**	0.9	0.9	0.9	1	0.9
Input Range (V_{pp})	**1.1**	1.1	1.6	1.6	1.2	1.1
SFDR @Nyq. (dB)	**75.3**	76*	75.9	73.1	74.56	73.4
SNDR @Nyq. (dB)	**60.1**	61[a]	59.5	56.6	60.02	60.7
Power (mW)	**8.5**	5.8	10.9	24.8	7.6	6.7
FoM_{Walden}@Nyq. (fj/conv-step)	**9.3**	6.3[a]	14.1	45	9.28	7.5
$FoM_{Schreier}$@Nyq. (dB)	**168.2**	168.1[a]	166.1	159.6	168.2	169.4
Active Area (mm^2)	**0.0096**	0.015	0.095	0.54	0.0091	0.007

[a]Measured with near Nyquist input (~0.6·f_{Nyq})

L-DAC/S-DAC and a high-speed DAS which improves the 1st-stage conversion speed while reducing the overall switching power. Adaptive inter-stage redundancy is presented to mitigate the speed overhead of the redundancy bit. This presented single-channel pipelined-SAR ADC is capable of operating at 1.1GS/s with 8.5 mW power consumption and it achieves a 60.1 dB SNDR at the Nyquist input. With FOM_{Walden} of 9.3 fJ/conv.-step and $FOM_{Schreier}$ of 168.2 dB, the ADC demonstrates good precision and power efficiency and validates the proposed techniques for switching power reduction and speed improvement.

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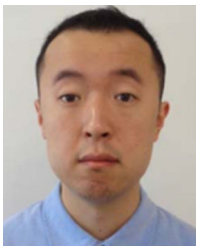

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