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RESEARCH ARTICLE

Non-Destructive Calibration Scheme for Online Monitoring Device of Metal Oxide Arrester

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ABSTRACT The reliability of online monitoring device for metal oxide arrester (MOA) is the prerequisite for ensuring the MOA normal operation. For online monitoring device, this paper proposes the non-destructive calibration scheme which can improve maintenance efficiency. The on-site calibration device consists of current source, ammeter, micro-current detector and control unit. There are two key technologies involved in the on-site calibration device, the one is the phase locked loop (PLL) for current source, the other is the high precision current detection for ammeter and micro-current detector. The proposed PLL of the reference voltage can generate low delay orthogonal signals and eliminate the second harmonic disturbances caused by the crystal oscillator error of microcontroller unit (MCU). The experimental results show the effectiveness of the proposed calibration scheme.

INDEX TERMS Arrester, on-line monitoring, non-destructive calibration, phase locked loop, current detection.

I. INTRODUCTION

The metal oxide arrester (MOA) is an important device in the power system to protect other equipments from over-voltage hazards [1], [2], [3]. The operation status of MOA directly affects the safety of the power system. Under continuous operation of MOA without time gap, the leakage current caused by bus voltage leads to aging of MOA [4], [5]. In addition, the deterioration of MOA can be caused by factors such as dampness, uneven potential distribution, surface pollution current, overvoltage, etc [6], [7]. In order to monitor the operational status of MOA, the online monitoring device is installed. The number of overvoltage actions and leakage current are recorded through the online monitoring device [8], [9].

In recent years, the current indication faults in online monitoring devices have been frequently discovered. Due to poor sealing of the online monitoring device for MOA, the current detection circuit may be affected by moisture. The corrosion of internal components in the circuit results in inaccurate current detection. The traditional maintenance of online monitoring devices for MOA is usually carried out under offline conditions. During the dismantling process, it is necessary to consider the existing safety factors and the required maintenance force. Therefore, it is meaningful to verify the online monitoring device of MOA on site.

In order to verify the online monitoring device of MOA on site, the premise is that arbitrary current based on the single-phase AC working voltage of the substation can be obtained. Due to the presence of nonlinear loads such as induction cookers, variable frequency air conditioners, uncontrolled rectifiers, etc. in the substation load, there are harmonic and DC components in the working voltage waveform [10], [11], [12]. How to successfully detect the phase of single-phase AC voltage is one of the key issues. The phase can be obtained by detecting the zero crossing point of the AC voltage. Although this method is simple to implement, its disadvantage is poor anti-interference ability. The fluctuation or distortion of AC voltage can cause zero crossing offset. And owing to the noise in the digital signal of voltage measurement, the multiple zeros appear in the judgment results [13], [14], [15]. For the single-phase power grid system, the voltage phase detection can be achieved using the phase locked loop (PLL) method based on a stationary

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coordinate system or a synchronous coordinate system. The phase discriminator of single-phase PLL based on stationary coordinate system adopts the multiplier, which outputs a second harmonic component [16]. To obtain correct frequency and phase information, the bandwidth must be very narrow, resulting in low dynamic performance and inability to achieve amplitude information. The single-phase PLL based on synchronous coordinate system constructs two orthogonal virtual reference signals based on the input signal, and then solves the amplitude and phase information of the input signal through relevant algorithms [17], [18], [19]. Due to the fact that the output signal of the Park transform in steady-state is a DC component, the bandwidth of the low-pass filter can be large. Compared with PLL based on the stationary coordinate system, this method has the advantage of good dynamic performance. However, the key is how to obtain the orthogonal virtual components required for Park transform from the input AC signal. Delaying the input signal by a quarter of fundamental period can generate the orthogonal virtual signals. Although the signal delay is simple to implement, the output signals is no longer orthogonal when the grid frequency deviates from its rated value [20], [21]. The second-order generalized integrator filters the real-time sampled power grid voltage and generates orthogonal signals in the literatures [22], [23], [24]. The orthogonal voltage vectors in the stationary coordinate system are constructed based on the finite impulse response digital filter with linear phase shift characteristic [25]. Drawing on the principle of digital phase-locked loop based on the coordinate transformation for three-phase grid connected systems, the control of single-phase phase-locked loop is achieved [22], [23], [24], [25]. The virtual orthogonal signals constructed by the single-phase PLL with good steady-state performance proposed in the literature [22], [23], [24], [25] have a delay of more than a quarter of fundamental period. The signal delay has adverse effects on the dynamic performance of PLL. In addition, as a result of the phase error between orthogonal voltage vectors, the Park transform outputs the second harmonic component which is not conducive to accurate phase detection. The low-pass filter with the low cut-off frequency can filter out the second harmonic component, but the adjustment time of the PLL will become longer.

The structure and principle of non-destructive calibration device are proposed in the section II for the online monitoring device of MOA. In the section III, The single-phase PLL method for the current source is introduced in detail. The current detection scheme for ammeter or micro-current probe is proposed in the section IV. Finally, the effectiveness of the calibration scheme was verified based on the experimental results.

II. PRINCIPLE OF ON-SITE CALIBRATION

The task of the online monitoring device for MOA is to detect the amplitude and phase of the leakage current. The on-site calibration device is used to evaluate the detection accuracy of the online monitoring device. As shown in Fig. 1, the

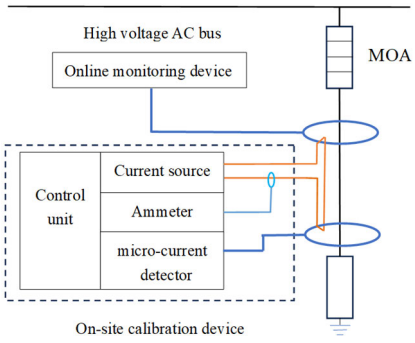

FIGURE 1. Simplified diagram of on-site calibration device for online monitoring device of MOA.

TABLE 1. Absolute error requirements for calibration passing.

Parameters	Values range	Absolute error requirements
Amplitude	1mA～20mA	Standard measurement value×0.6%+1μA
Phase angle	0～360°	2°

on-site calibration device consists of current source, ammeter, micro-current detector and control unit. The current source, ammeter and micro-current detector work independently. The control unit sends the reference signal for current source and reads the output signals of the ammeter and micro current detector.

The on-site calibration device detects the phase based on the 220V AC supply voltage. Compared to the reference, the phase angle of the high-voltage AC bus is θ. The micro current detector obtains the superimposed current of the current source and the leakage current of MOA. The mutual calibration between the current source and the ammeter is to ensure that the current source works properly. By detecting the output current of the current source, the online monitoring device can be verified for normal operation. If the results meet the absolute error requirements shown in Tab. 1, the calibration is passed. In addition, it is necessary to meet the repeatability measurement test. The relative standard deviation (RSD) of the current fundamental peak should be less than 2%. RSD can be calculated according to

$$RDS = \sqrt{\frac{\sum_{i=1}^{n} \left(B_i - \overline{B}\right)^2}{n-1}} \cdot \frac{1}{\overline{B}} \cdot 100\% \tag{1}$$

where n is the number of measurements, i is the measurement serial number, B_i is the i-th measurement result, and $\overline{B}$ is the arithmetic mean of n measurement results.

On the basis of standard DL/T1432.3-2016 formulated by State Grid of China, 0.001A, 0.002A, 0.003 A, 0.005A, 0.01A, and 0.02A should be selected as the amplitude I_m of check point current.

Before starting the calibration, it is necessary to compensate for the leakage current of MOA in its initial state. When the output signal of the micro-current detector is close to

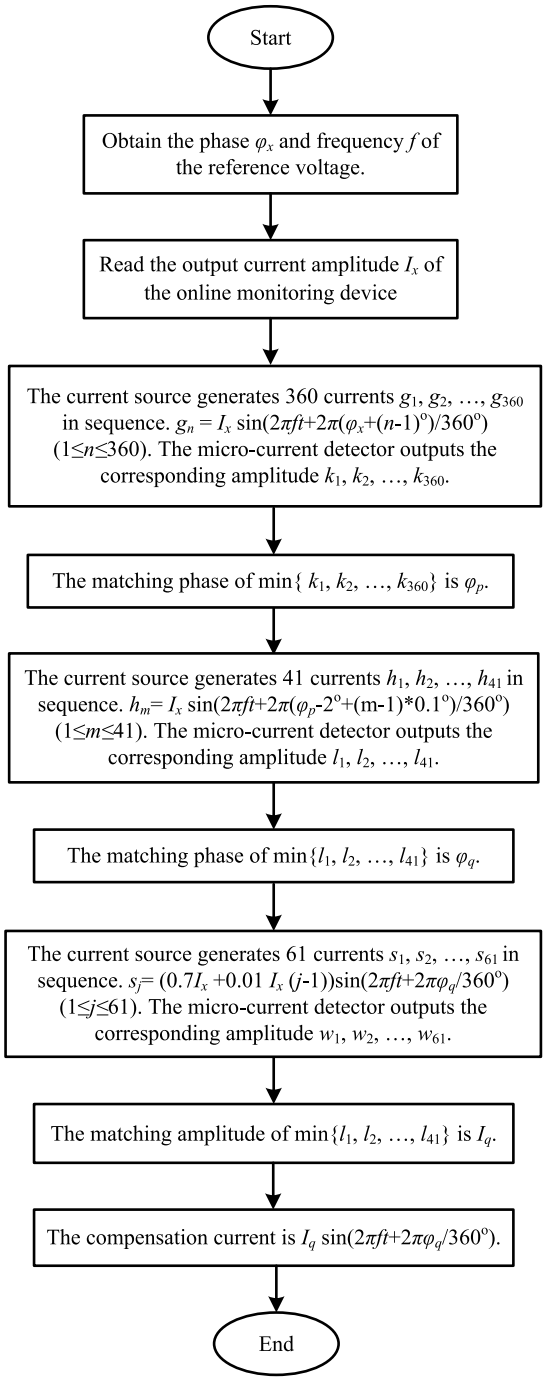

FIGURE 2. Process of determining the amplitude I_q and phase φ_q of compensation current.

zero, the compensation is considered successful. Fig. 2 shows the process of determining the amplitude I_q and phase φ_q of compensation current. The current source generates the current signal $I_q\sin(100\pi t+\varphi_q^*2\pi/360)+ I_m\sin[100\pi t+(90^\circ + \theta)\ ^*2\pi/360^\circ]$. After several fundamental periods, based on the output signals of the online monitoring device, the control unit determines whether its absolute error and measurement repeatability test meet the requirements. The calibration

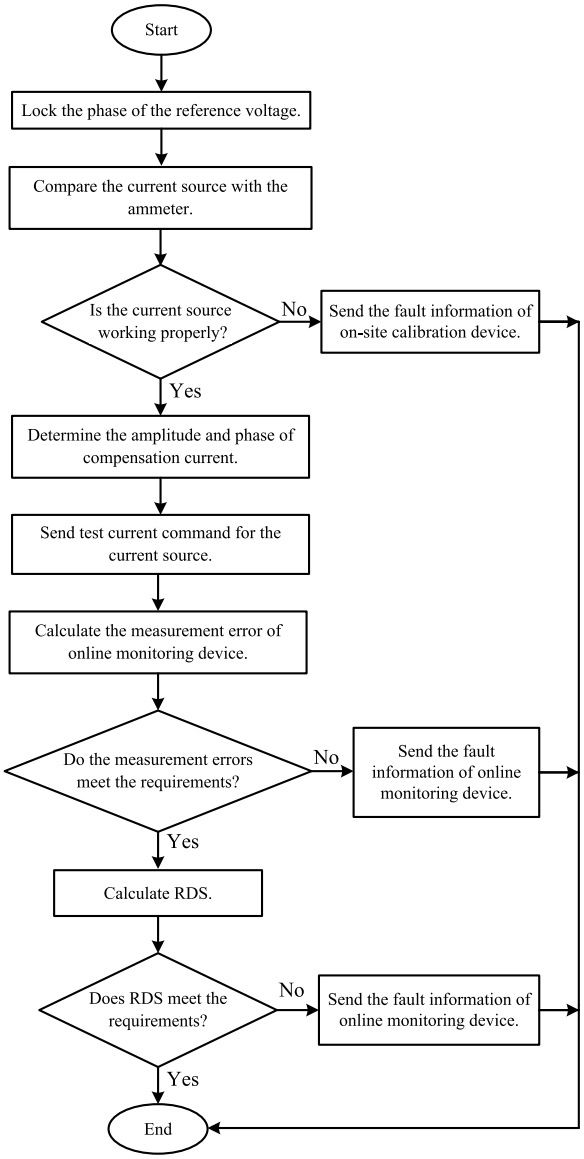

FIGURE 3. Calibration process of the on-site calibration device for each test current.

process of the on-site calibration device for each test current is shown in Fig. 3.

III. PHASE LOCKED LOOP OF THE REFERENCE VOLTAGE

The 220V AC supply voltage is selected as the reference for the phase angle calculation of high-voltage AC bus and the output current of current source. The priority of on-site calibration device is to successfully lock the reference voltage phase. As shown in Fig. 4, the reference voltage vector $\boldsymbol{U_g}$ is decomposed into two orthogonal vectors $\boldsymbol{V_\alpha}$ and $\boldsymbol{V_\beta}$ with the same amplitude in $\alpha\beta$ stationary coordinate system. Ψ is the angle between the vector $\boldsymbol{U_g}$ and α axis. V_α and V_β can be calculated as

$$\begin{bmatrix} V_\alpha \\ V_\beta \end{bmatrix} = U_g \begin{bmatrix} \cos\psi \\ \sin\psi \end{bmatrix} \tag{2}$$

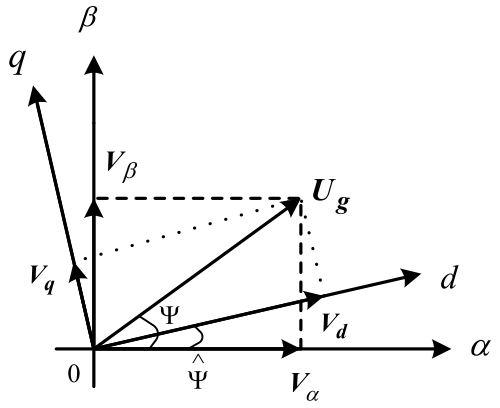

FIGURE 4. Relationship among the vectors among U_g, V_α, V_β, V_d and V_q.

By Park transformation, V_d and V_q can be expressed as

$$\begin{bmatrix} V_d \\ V_q \end{bmatrix} = \begin{bmatrix} V_\alpha & V_\beta \end{bmatrix} \begin{bmatrix} \cos\hat{\psi} & \sin\hat{\psi} \\ -\sin\hat{\psi} & \cos\hat{\psi} \end{bmatrix} = \begin{bmatrix} U_g \cos(\psi - \hat{\psi}) \\ U_g \sin(\psi - \hat{\psi}) \end{bmatrix} \tag{3}$$

where $\hat{\psi}$ is the angle between dq rotation coordinate system and $\alpha\beta$ stationary coordinate system. When the vector $\boldsymbol{U_g}$ coincides with the d axis, Ψ keeps pace with $\hat{\psi}$ and the value of V_q is zero. V_q is selected as the control variable. When the steady-state value of V_q is zero, it can be considered that the phase is successfully locked.

A. ORTHOGONAL SIGNALS GENERATION METHOD WITH LOW DELAY

The signal $U_g\cos[\omega(t\text{-}\Delta d)]$ can be obtained by delaying the reference $U_g\cos(\omega t)$ which is selected as V_α for time of Δd. Then the signal $U_g\cos[\omega(t\text{-}\Delta d)]$ is expanded as follows:

$$U_g \cos[\omega(t-\Delta d)] = U_g \cos(\omega t)\cos(\omega\Delta d) + U_g \sin(\omega t)\sin(\omega\Delta d) \tag{4}$$

According to (4), it can be inferred that

$$\frac{U_g \cos[\omega(t-\Delta d)]}{\sin(\omega\Delta d)} = \frac{U_g \cos(\omega t)\cos(\omega\Delta d)}{\sin(\omega\Delta d)} + U_g \sin(\omega t) \tag{5}$$

Based on (5), V_β can be calculated out as

$$V_\beta = U_g \sin(\omega t) = \frac{U_g \cos[\omega(t-\Delta d)]}{\sin(\omega\Delta d)} - \frac{U_g \cos(\omega t)\cos(\omega\Delta d)}{\sin(\omega\Delta d)} \tag{6}$$

The generation block diagram for V_α and V_β is shown in Fig. 5.

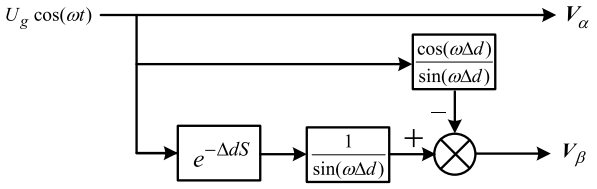

FIGURE 5. Generation block diagram for V_α and V_β.

Due to the crystal oscillator error of MCU, the delay time cannot be accurately generated. The actual V_β can be expressed as $U_g\sin(\omega t + \Delta\delta)$ deviating by angle $\Delta\delta$ from the ideal signal. Assuming that the output phase $\hat{\psi}$ has successfully followed the input phase Ψ in the initial state, the actual V_q can be derived as

$$\begin{aligned} \overline{V_q} &= -U_g \sin(\omega t)\cos(\omega t) \\ &\quad + U_g \cos(\omega t)\sin(\omega t)\cos\Delta\delta \\ &\quad + U_g \cos(\omega t)^2 \sin\Delta\delta \end{aligned} \tag{7}$$

As the value of $\Delta\delta$ is small, $\cos\Delta\delta \approx 1$ and $\sin\Delta\delta \approx 1$. (7) can be transformed into

$$\overline{V_q} = 0.5\Delta\delta U_g + 0.5\Delta\delta U_g \cos(2\omega t) \tag{8}$$

It can be seen from (8) that there is a second harmonic disturbance in the waveform of $\overline{V_q}$. The output phase $\hat{\psi}$ is inevitably affected.

B. PLL WITH SECOND HARMONIC DISTURBANCE ELIMINATION

Although the second-order harmonic disturbance can be suppressed by the low-pass filter, the dynamic performance is bound to deteriorate. The proposed method for eliminating second harmonic disturbances relies on derivative operations. $\overline{V_q}$ is processed as follows:

$$\frac{1}{4\omega^2}\overline{V_q}'' = \frac{1}{4\omega^2}\frac{d^2\overline{V_q}}{dt^2} = -0.5\Delta\delta U_g \cos(2\omega t) \tag{9}$$

Adding (8) and (9) can eliminate the second-order harmonic disturbance. According to the proposed principle, the second harmonic disturbance elimination PLL is shown in Fig. 6.

IV. CURRENT DETECTION STRATEGY

The accuracy of current detection for current source and micro-current detector is another key factor. The current detection strategy combining the analog conversion circuit with AD converter is proposed below.

In order to ensure that the online monitoring device is not damaged, the open type current transformer selected as current sensor. Fig. 7 shows the adopted analog conversion circuit. The secondary current i_s is generated by the decay of the detected primary current. By flowing through the sampling resistor r_s, i_s is converted into the voltage signal u_{s1}. u_{o2} is the voltage of analog conversion circuit output port which is connected to the input pin of AD converter. With

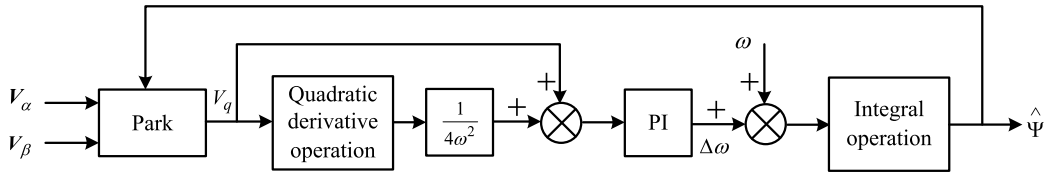

FIGURE 6. PLL with the second harmonic disturbance elimination.

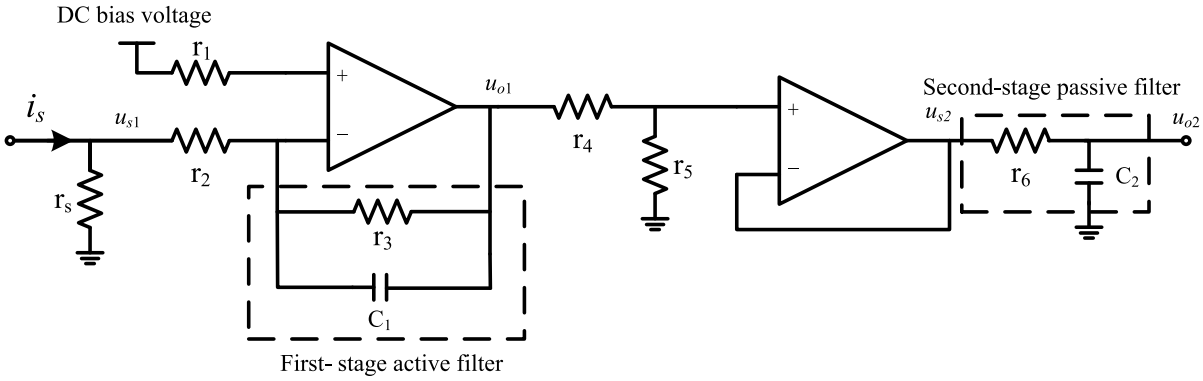

FIGURE 7. Analog conversion circuit.

the help of DC bias voltage, the output voltage range of the analog conversion circuit can match the input voltage range of AD converter. In addition, the analog conversion circuit can filter out high-frequency components in the input voltage signal u_{s1}.

Ignoring the DC bias voltage, the two stage filters in the analog conversion circuit are analyzed below. For the first-stage active filter, the relationship between -u_{o1} and u_{s1} can be expressed as

$$-\dot{U}_{o1} = \dot{U}_{s1}\frac{1}{r_2}\frac{r_3 - jr_3^2\omega C_1}{(r_3\omega C_1)^2 + 1} \tag{10}$$

According to (10), the deviation angular γ_1 and the cutoff frequency ω_{c1} can be calculated as

$$\begin{cases} \gamma_1 = \arctan(r_3\omega C_1) \\ \omega_{c1} = \dfrac{1}{2\pi r_3 C_1} \end{cases} \tag{11}$$

Based on (11), as r_3 or C_1 increases, the phase angle accuracy deteriorates and the detection range will become narrower. For the second-stage passive filter, the relationship between u_{o2} and u_{s2} can be expressed as

$$\dot{U}_{o2} = \dot{U}_{s2}\frac{1 - jr_6\omega C_2}{(r_6\omega C_2)^2 + 1} \tag{12}$$

Then the deviation angular γ_2 and the cutoff frequency ω_{c2} can be derived as

$$\begin{cases} \gamma_2 = \arctan(r_6\omega C_2) \\ \omega_{c2} = \dfrac{1}{2\pi r_6 C_2} \end{cases} \tag{13}$$

The impact of increasing r_6 or C_2 is similar to that of increasing r_3 or C_1. Ideally, the relationship between the input low-frequency current i_{s1} and the output voltage u_{o2} can be expressed as

$$\begin{aligned} u_{o2} &= -r_s\frac{r_3 r_5}{r_2(r_4 + r_5)}i_s \\ &= -r_e i_s \end{aligned} \tag{14}$$

where the equivalent sampling resistance r_e can be calculated out as

$$r_e = r_s\frac{r_3 r_5}{r_2(r_4 + r_5)} \tag{15}$$

When the measured current is zero, the digital zero drift detected by AD converter fluctuates within a specific range. If the resolution of AD converter is 12 bits and the maximum value of the input analog voltage is 3.3V, the current detection error I_e caused by digital zero drift can be calculated out as

$$I_e = \frac{3.3}{4095}\frac{\tau J}{r_e} \tag{16}$$

where τ is the range width of the digital zero drift, and J is the ratio of current transformer. According to (16), the accuracy of current detection can be improved by reducing the ratio of current transformer or increasing the equivalent sampling resistance.

When the hardware parameters are determined, reducing the range width of the digital zero drift is the only way to improve the accuracy of current detection. Tab. 2 shows the impact of the second-stage passive filter on the digital zero drift range width. When the value of r_6 or C_2 increases to a certain limit, the zero drift range width no longer narrows. Ensuring that the cutoff frequency and deviation angular are within the allowable range, the reasonable values for r_6 and C_2 are 510 Ω and 22 nF, respectively.

TABLE 2. Impact of the second-stage passive filter on the digital zero drift range width.

(a) Variation trend of the digital zero drift range width when r_6 is fixed and C_2 is changed.

r_6 (Ω)	C_2 (nF)	ω_{c2} (kHz)	Deviation angular (°)	Digital zero drift range width
510	0.33	946.141	0.003028	±21
510	2.2	141.92	0.020186	±17
510	10	31.22	0.0918	±11
510	22	14.19	0.20186	±8
510	100	3.122	0.917456	±7
510	470	0.66431	4.3043	±6
510	1000	0.31227	9.098098	±8

(b) Variation trend of the digital zero drift range width when C_2 is fixed and r_6 is changed.

r_6 (Ω)	C_2 (nF)	ω_{c2} (kHz)	Deviation angular (°)	Digital zero drift range width
10	22	723.798	0.00395799	±26
51	22	141.921	0.02018576	±18
110	22	65.79986	0.0435379	±13
510	22	14.19	0.20186	±8
1K	22	7.23798	0.39579	±7
5.1K	22	1.4192	2.01774	±8
51K	22	0.14192	19.407768	±9

V. EXPERIMENTAL RESULTS

The experimental prototype composed of on-site calibration device, online monitoring device and MOA is shown in Fig.8.

MCU for Phase locked loop is TMS320F28335 from Texas Instruments. The internal AD converter of MCU is selected for the current detection. The open type current transformer is CKT30-C from Jieli Electronic Technology Co., Ltd.

When the distortion of the reference voltage exists, the error of V_β will increase with the shortening of the delay time Δd. On the contrary, too long Δd will deteriorate the dynamic performance of PLL. The delay time Δd is one eighth of the fundamental period. The steady-state effect of the second harmonic disturbance elimination PLL is shown in Fig.9. The tracking error of the reference voltage phase is within 2°. If the setting phase signal of current source is $100\pi t+90°*2\pi/360°$, Fig.10 shows the voltage generated by the output current of the current source flowing through the sampling resistor.

The initial leakage current of MOA is 0.236mA. After injecting the compensation current, the output signal of the micro-current detector is 0.003mA. Tab.3 shows the test results of one online monitoring device passing calibration.

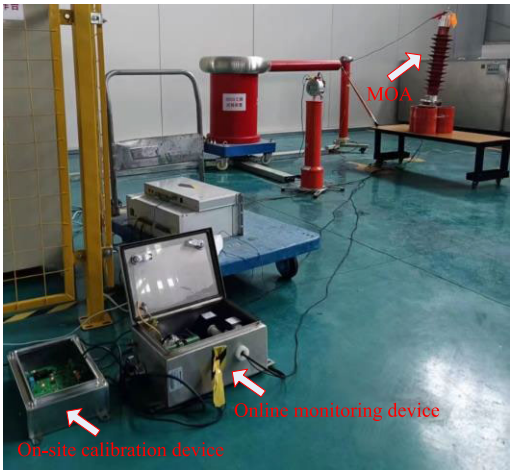

FIGURE 8. Experimental prototype.

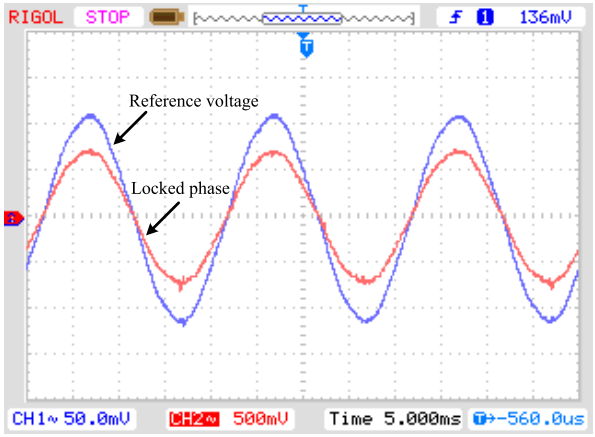

FIGURE 9. Steady-state effect of the second harmonic disturbance elimination PLL.

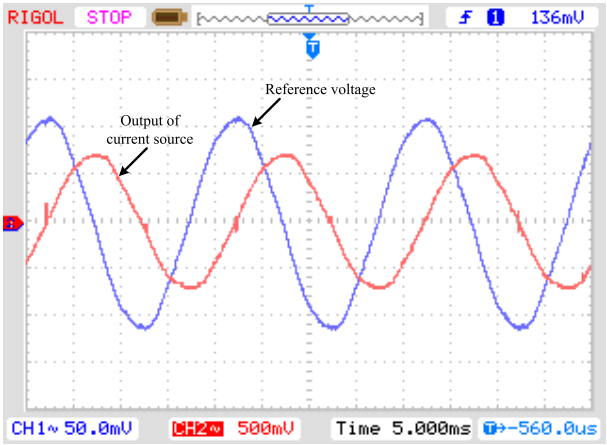

FIGURE 10. Relationship between the output of the current source and the reference voltage.

According to the results, it can be seen that the current amplitude error, phase error and RSD all meet the requirements.

TABLE 3. Test results of one online monitoring device passing calibration.

Output signal of the current source (mA)	Output signals of the online monitoring device	1st test	2nd test	3rd test	4th test	5th test	Average value	Absolute error	RSD
sin(100πt+87.14° *2π/360°)	Amplitude (mA)	0.998	0.998	0.999	0.998	0.998	0.998	0.002	0%
	Phase angle (°)	85.69	85.748	85.752	85.748	85.748	85.748	1.392	0%
2sin(100πt+87.14° *2π/360°)	Amplitude (mA)	1.998	1.997	1.996	1.997	1.998	1.997	0.003	0.1%
	Phase angle (°)	85.723	85.865	85.863	85.807	85.867	85.836	1.304	0.2%
3sin(100πt+87.14° *2π/360°)	Amplitude (mA)	2.987	2.988	2.988	2.988	2.988	2.988	0.012	0%
	Phase angle (°)	85.66	85.662	85.624	85.662	85.643	85.643	1.497	0.1%
5sin(100πt+87.14° *2π/360°)	Amplitude (mA)	4.988	4.989	4.989	4.988	4.989	4.989	0.011	0.1%
	Phase angle (°)	85.746	85.781	85.758	85.711	85.678	85.735	1.405	0.4%
10sin(100πt+87.14 °*2π/360°)	Amplitude (mA)	9.992	9.991	9.992	9.992	9.991	9.992	0.008	0.1%
	Phase angle (°)	85.718	85.775	85.816	85.73	85.821	85.77	1.37	0.8%
20sin(100πt+87.14 °*2π/360°)	Amplitude (mA)	19.999	19.998	19.997	19.999	19.997	19.998	0.002	0.1%
	Phase angle (°)	85.742	85.744	85.761	85.802	85.856	85.782	1.358	1.7%

VI. CONCLUSION

The non-destructive calibration scheme is proposed for online monitoring device of MOA in this paper. The delay time of constructing the orthogonal signals can be reduced to one eighth of the fundamental period. Using the second harmonic disturbance elimination PLL, the tracking error of the reference voltage phase is within 2°. The error of the current detection strategy for current source and micro-current detector is within the allowable range. The on-site calibration device accurately compensates for the leakage current of MOA and outputs the specified test currents to complete the calibration of the online monitoring device. Experimental results are presented to confirm the features and validity of the proposed calibration scheme.

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