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RESEARCH ARTICLE

Novel Dual Work Function Buried Channel Array Transistor Process Design for Sub-17 nm DRAM

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ABSTRACT This paper introduces the smallest dynamic random access memory (DRAM) cell, which was implemented using a new transistor structure, the dual work function - buried channel array transistor (DWF-BCAT). For the first time, a feature size of approximately 17 nm was achieved for a DRAM cell. In this study, a novel cell gate oxide process that mitigates traps in the gate oxide and gate interface, whose dimensions scale concurrently, was developed to fabricate the DWF-BCAT. By utilizing a three-step process involving in-situ steam generation (ISSG) followed by atomic layer deposition (ALD) then another cycle of ISSG (IAI) to create the dual work function gate, a significant improvement in DRAM data retention characteristics is achieved. A new barrier fabrication process called plasma nitridation treatment of oxide film (PNOF) was also developed. Oxide film barriers for two gate materials, namely tungsten and polycrystalline Si, were deposited using PNOF. Device characterization results reveal that PNOF is highly effective in reducing interfacial resistance by suppressing the inter-diffusion of gate materials, leading to improved DRAM write time characteristics. Additionally, gate oxide defects can be repaired and surface contamination can be removed by applying an HF wet strip (HFWS) process. The BCAT design and fabrication strategies applied in this study can accelerate the miniaturization of DRAMs toward the theoretical scaling limit.

INDEX TERMS Dual work function-buried channel array transistor (DWF-BCAT), IAI, PNOF, HFWS.

I. INTRODUCTION

In the current ''4th industrial revolution,'' the demand for the efficient processing and storage of extremely large datasets for applications such as the Internet of Things (IoT), Artificial Intelligence (AI), and Data Centers (DC) continues to increase. Consequently, the performance of dynamic random access memory (DRAM) cells, which are essential in storing data for computing processes, must be continuously enhanced. DRAMs are composed of arrays of unit cells typically containing a metal-oxide-semiconductor transistor and a capacitor. Bit data is determined by the state of charge of the capacitor. DRAMs necessitate periodic data resorting operations, referred to as refresh operations, to maintain the charge state of the capacitor and prevent loss of data. Therefore, maintaining a high cell capacitance is essential to ensure stable data retention. However, the continuous miniaturization of the DRAM cell footprint has unavoidably led to a decrease in cell capacitance. Further device downscaling poses challenges to the structural integrity of the device, which in turn affects device stability, power efficiency, and overall performance [1], [2], [3].

Suppressing the leakage current from the charged capacitor in DRAMs is crucial. Current DRAM cells are mainly implemented using a buried channel array transistor (BCAT) with minimum feature sizes around 20 nm [4], [5], [6], [7], [8].

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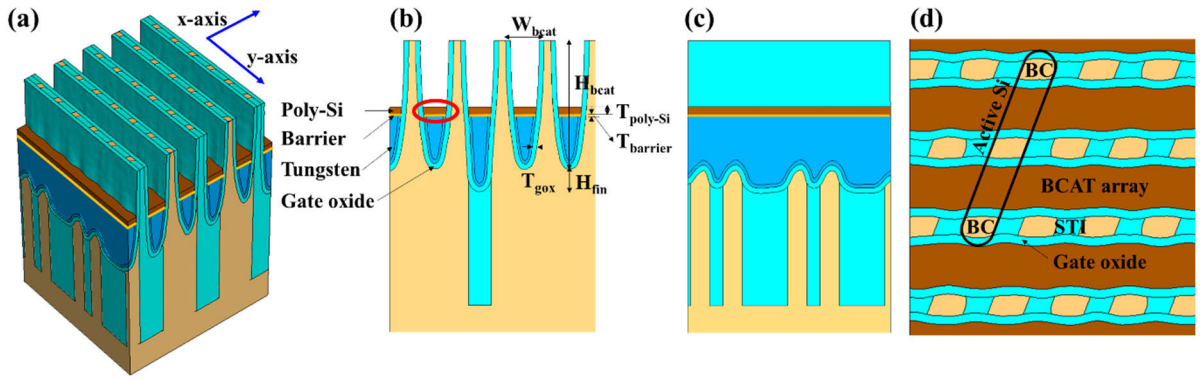

FIGURE 1. (a) 3D structure of DWF-BCAT, (b) cross-sectional view along the x-axis, (c) cross-sectional view along the y-axis, (d) top view of the 3D structure.

Gate-induced drain leakage (GIDL) current is the dominant cause of the degradation in the data retention performance of BCATs [1], [2], [3]. Therefore, suppressing GIDL can improve DRAM data retention even with a relatively low cell capacitance. In the BCAT structure, the GIDL is very sensitive to the electric field (D-field) between the metal gate electrode and the buried contact (BC) to the cell capacitor [2], [3], [6], [7]. However, the D-field strongly influences the level of the operating current. A reduction in the D-field can inhibit GIDL while simultaneously decreasing the operating current. Nevertheless, controlling the D-field still remains the best strategy for maintaining the stability of DRAMs that are being made increasingly smaller.

To reduce the D-field, herein, we propose a new BCAT structure consisting of a multi-layer gate and fabricate a 17-nm DRAM. The gate material is changed from pure W to a bi-layer composed of W and polycrystalline Si (poly-Si). The poly-Si is doped with phosphine to adjust the work function and reduce the electric field in the gate-to-drain overlap region. In the process of developing the new DRAM cell transistor, some serious challenges were expected. First, because the upper part of the gate is replaced with poly-Si and the W volume is decreased, the resistance of the word line array is predicted to increase. Therefore, a new scalable G_{ox} design and deposition scheme are introduced to increase the lateral W gate area. We examine the interface characteristics of the gate W and poly-Si and evaluate suitable barrier materials. The new process for depositing the gate poly-Si introduces defects and traps in the G_{ox} sidewall. Therefore, a cleaning step was optimized to eliminate these defects. Then, actual DRAMs whose unit cells are implement using DWF-BCAT are fabricated and characterized.

II. DEVICE STRUCTURE AND SIMULATION SETUP

A. FABRICATION

The device was fabricated using the conventional BCAT (c-BCAT) manufacturing process and following sub-18 nm feature size design rules. The fabrication process can be summarized as follows. First, the active Si area was etched to create array-type grooves. At this time, BCAT fins are formed in the active region Si and the SiO2 shallow trench isolation (STI) region. Next, the gate oxide (G_{ox}) is formed by atomic layer deposition (ALD) and in-situ steam generation (ISSG). ALD forms a uniform oxide film on the bottom and side walls. ISSG, a high-temperature (>1000°C) radical oxidation method, is used to form a second layer of high-quality oxide film. ISSG involves feeding H_2 and O_2 gas into the chamber through different nozzles. A combustion reaction then occurs on the surface of the hot wafer, and H_2 breaks O_2 to produce O^* radicals which react with Si in the active region to form SiO_2 film. After the G_{ox} is formed, a thin layer of barrier metal Ti_xN_y is deposited by ALD. Chemical vapor deposition (CVD) was used to fill the BCAT array with W. Next, the W gate was dry-etched to the appropriate height. Rapid thermal annealing (RTA) processes at more than 600 °C are carried out, and a layer is deposited to act as a barrier between the two gates. A highly P-doped poly-Si film was created over the BCAT array and then dry-etched to the appropriate height. Finally, a high-quality silicon nitride barrier was added to protect the DRAM word line.

B. DEVICE STRUCTURE

Fig. 1 (a) – (d) shows 3D, vertical, and plane top views of the DWF-BCAT. The active Si region features a $6F^2$ structure bent at 21 degrees. The word line is embedded, exhibiting a recess channel configuration or BCAT. Additionally, capacitors are connected through buried contacts (BC) [2], [3], [6], [7], [8], [9].

The area in the solid red ellipse in Fig. 1(b) shows that DWF-BCAT is a modified c-BCAT with two gates, W and poly-Si. The thickness of the poly-Si gate was optimized to minimize the cell leakage current. As discussed above, as the poly-Si thickness increases, the GIDL current decreases. But W area decreases and the resistance of word line (R_{wl}) could be increased. The vertical parameters including the BCAT height, poly-Si thickness, and fin height are defined as the distance from the active top surface to the BCAT recess bottom in the active region, the distance from poly-Si etch end to the barrier, and the distance from the BCAT recess end of the active region to the recess end of STI region, respectively.

The BCAT height, poly-Si thickness, fin height, and barrier thickness were set to 150, 25, 30 and 2 nm, respectively. Also, the lateral parameters, i.e., BCAT width and G_{ox} thickness were set to 30 and 8 nm, respectively. These parameters were chosen to minimize the leakage current while maintaining a high on-current. The P doping concentration of the n+ gate poly-Si was 5.0×10^{17} cm^{-3}, and the resulting work function was 4.15 eV. The DRAM cell dimensions are summarized in Table 1.

TABLE 1. Actual DRAM cell dimensions.

Parameter	Value	Description
W_{bcat}	30 nm	BCAT width
T_{gox}	8 nm	G_{ox} thickness
H_{bcat}	150 nm	BCAT height
H_{fin}	30 nm	FiN height
$T_{poly\text{-}Si}$	25 nm	Poly-Si thickness
$T_{barrier}$	2 nm	Barrier thickness

C. SIMULATION METHOD

Technology computer aided design (TCAD) simulations were performed. The following model device conditions were simultaneously applied: 1) band-gap narrowing; 2) Shockley-Read-Hall recombination (doping and temperature dependent, field enhancement-Hurkx); 3) nonlocal trap-assisted tunneling (TAT); 4) band to-band tunneling (Hurkx); 5) doping-dependence; 6) high field saturation; 7) avalanche breakdown; 8) Auger recombination; 9) Fermi–Dirac distribution; and 10) quantum-confinement. We also incorporated the specifications of the simulation model that were found to be effective in the case of 18, 20, and 25 nm c-BCATs.

III. RESULT AND DISCUSSION

A. SIMULATION RESULT

GIDL currents result in static power dissipation and contribute toward device breakdown [1], [2], [3], [4], [5], [6], [7]. GIDL is a band to band tunneling (BTBT) phenomenon that is caused by high electric fields in the gate-to-drain overlap region and band bending at the Si/SiO_2 interface.

The electric field, $E(x)$, can be expressed as

$$E(x) = \frac{dV(x)}{dx} = \frac{1}{q}\frac{dEc}{dx} \tag{1}$$

where $V(x)$ is the potential along the vertical direction. The conduction energy band Ec is taken as reference for potential variations in semiconductors.

From (1), it is apparent that the high gradient in the energy bands contributes to a high electric field, and a high electric field in drain region leads to high BTBT [8], [10].

$$Vox = Vgd + (\Phi ms - \frac{Qox}{Cox}) \tag{2}$$

The maximum electric field is located between storage node and the top of gate. The blue line indicates the electric field profile of DWF-BCAT. Even though the interfaces between the1st metal W gate and 2nd poly-Si gate increase the electric field locally, the maximum electric field of the DWF-BCAT is lower than that for c-BCAT, as shown in Fig. 2. From the simulation results, we could expect that the actual dual work function gate would have better GIDL characteristics and consequently, the DRAM would have a longer retention time.

B. SIDE GATE OXIDE SCALING: IAI (ISSG/ALD/ISSG)

The insertion of a poly-Si gate to achieve a gate with a dual work function reduces the word line (W) volume in the vertical direction, thereby causing an increase in R_{wl} and write time [2], [7]. To reduce the impact on R_{wl}, the side G_{ox} thickness can be decreased to enlarge the additional volume of W while maintaining a constant word line height. However, it is predicted that further reducing the G_{ox} dimensions and poor G_{ox} quality can significantly deteriorate the refresh characteristics of the G_{ox} deposited using the conventional ALD/ISSG (AI) scheme.

As shown in Fig. 3, ISSG produces distinct oxidation rates on the sidewalls and bottom of the BCAT structure, in contrast to the nearly uniform oxidation rate of the ALD method. In general, the thickness of the oxide film decreases within the BCAT device pattern as the curvature of the pattern increases. This phenomenon is attributed to the deceleration of the oxidation reaction in the bottom area due to the compressive stress from the volumetric expansion of SiO_2 during the oxidation process [11]. The thickness of the bottom G_{ox} notably influences the threshold voltage (V_{th}) of the transistor and the junction leakage, and the thickness of the sidewall G_{ox} has a major influence on GIDL. Therefore, to achieve the desired oxide thickness in the bottom region of the BCAT, the sidewall oxide film becomes excessively thick. This leads to increased R_{wl} due to the reduction in the lateral volume of W. The c-BCAT G_{ox} scheme involves the two-step AI process: oxide with exceptional step coverage is first deposited by ALD followed by the sequential curing of traps using ISSG to attain the target thickness in the bottom region. Therefore, the resulting TEM profile corresponds to the configuration depicted in Fig. 3(c) with a distinctive "④" shape. The ISSG oxide thickness saturates in the bottom region, as illustrated in Fig. 3(b) and (c). This characteristic limits the reduction in sidewall G_{ox} thickness while concurrently preserving the G_{ox} thickness in the bottom area.

Instead of ALD, starting the oxide deposition process with ISSG forms an initial oxide film where the difference in oxide thickness between the side and bottom regions is minimal, as depicted in Fig. 3(c)- ①/②. The first ISSG step is then followed by ALD. Consequently, this approach resulted in a step coverage improvement of more than 10% compared to the AI G_{ox} scheme. Finally, a 2nd ISSG step was implemented after ALD to achieve a better quality G_{ox} than that created using AI. The ISSG-ALD-ISSG (IAI) strategy ensures the requisite conditions for reducing side G_{ox} without

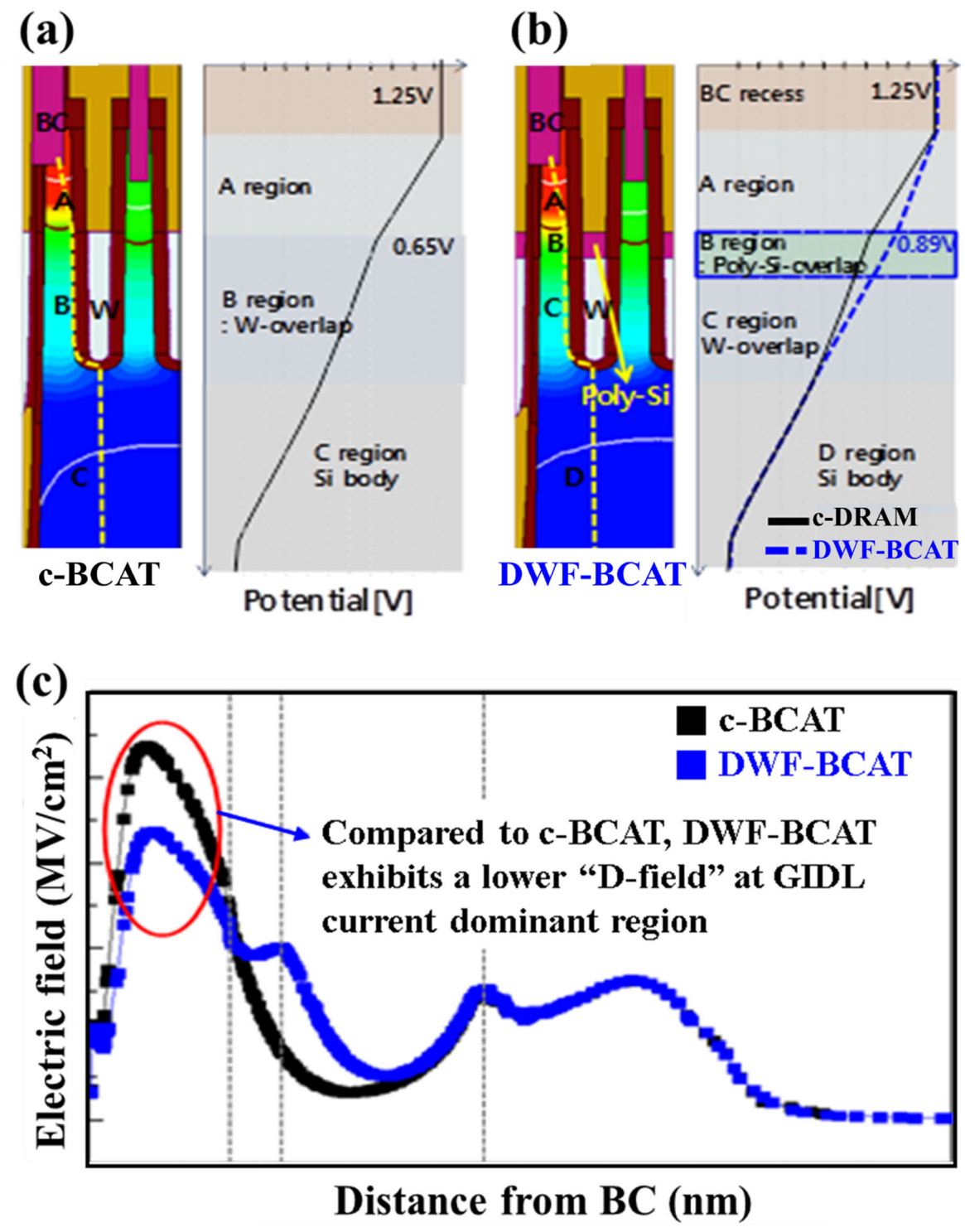

FIGURE 2. (a), (b) Vertical structure of c-BCAT and DWF-BCAT for the simulation and the potential profiles at distinct locations, respectively. (c) Comparison of the electric field profiles of c-BCAT and DWF-BCAT.

compromising film quality and diminishing the thickness of bottom G_{ox}.

Fig. 4(a) illustrates the variability in G_{ox} thickness for each process step in both the AI and IAI schemes. It is observed that IAI facilitates the scaling of the side G_{ox} thickness (-1 nm) while keeping the bottom G_{ox} constant, as shown in Fig. 4(b) and (c).

IAI enables the selective scaling of the BCAT G_{ox}, and the results are summarized in Table 2. However, a small reduction in the side G_{ox} thickness can lead to an increase

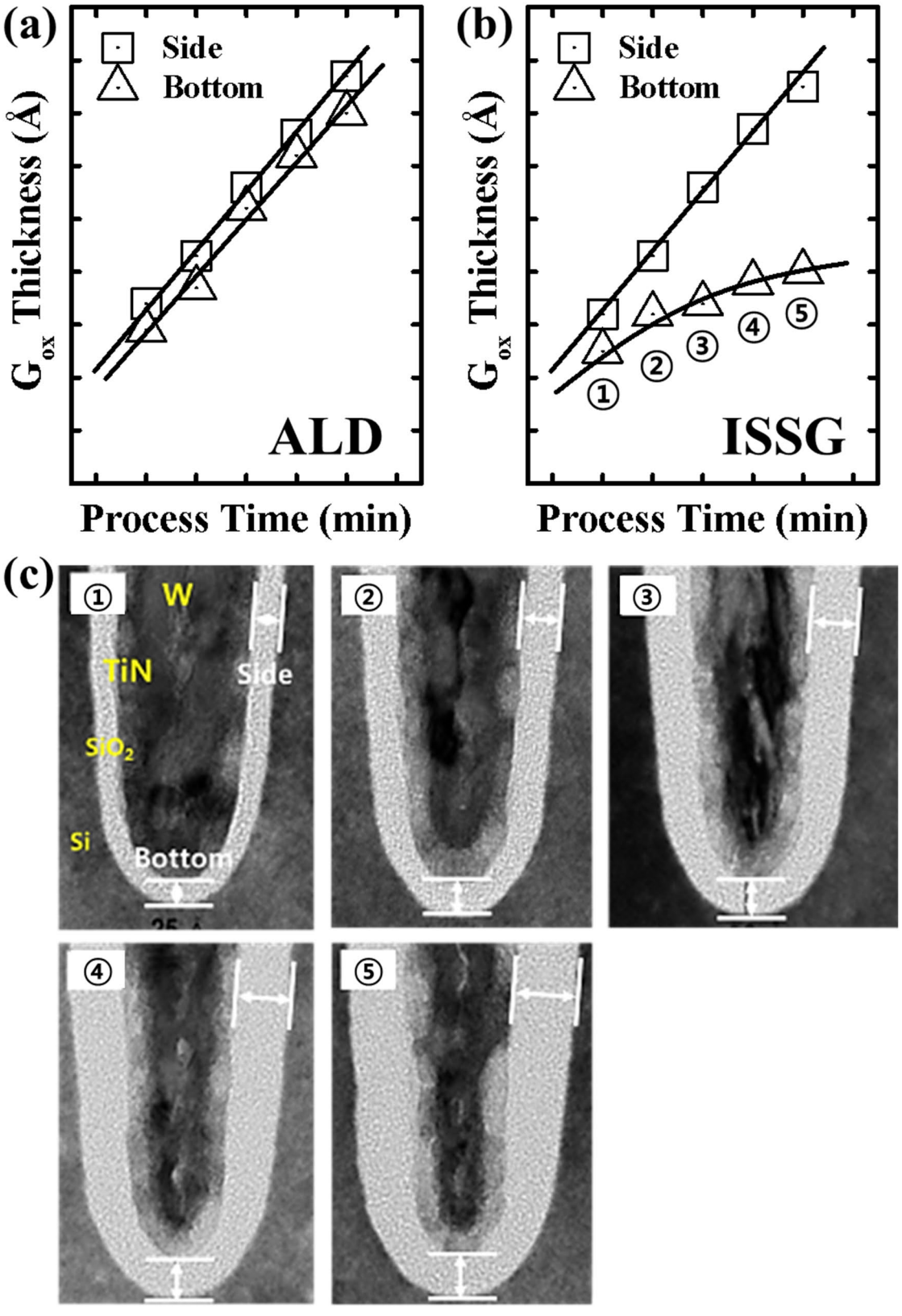

FIGURE 3. Growth behavior of the oxidation process on the BCAT pattern: (a) ALD (b) ISSG, two lines indicate the thickness of SiO_2 at the side and bottom. (C) TEM images analyzing the ISSG oxidation profile formed on the sidewalls and bottom over time: analyzing conditions ①-⑤ in Figure (b), individually.

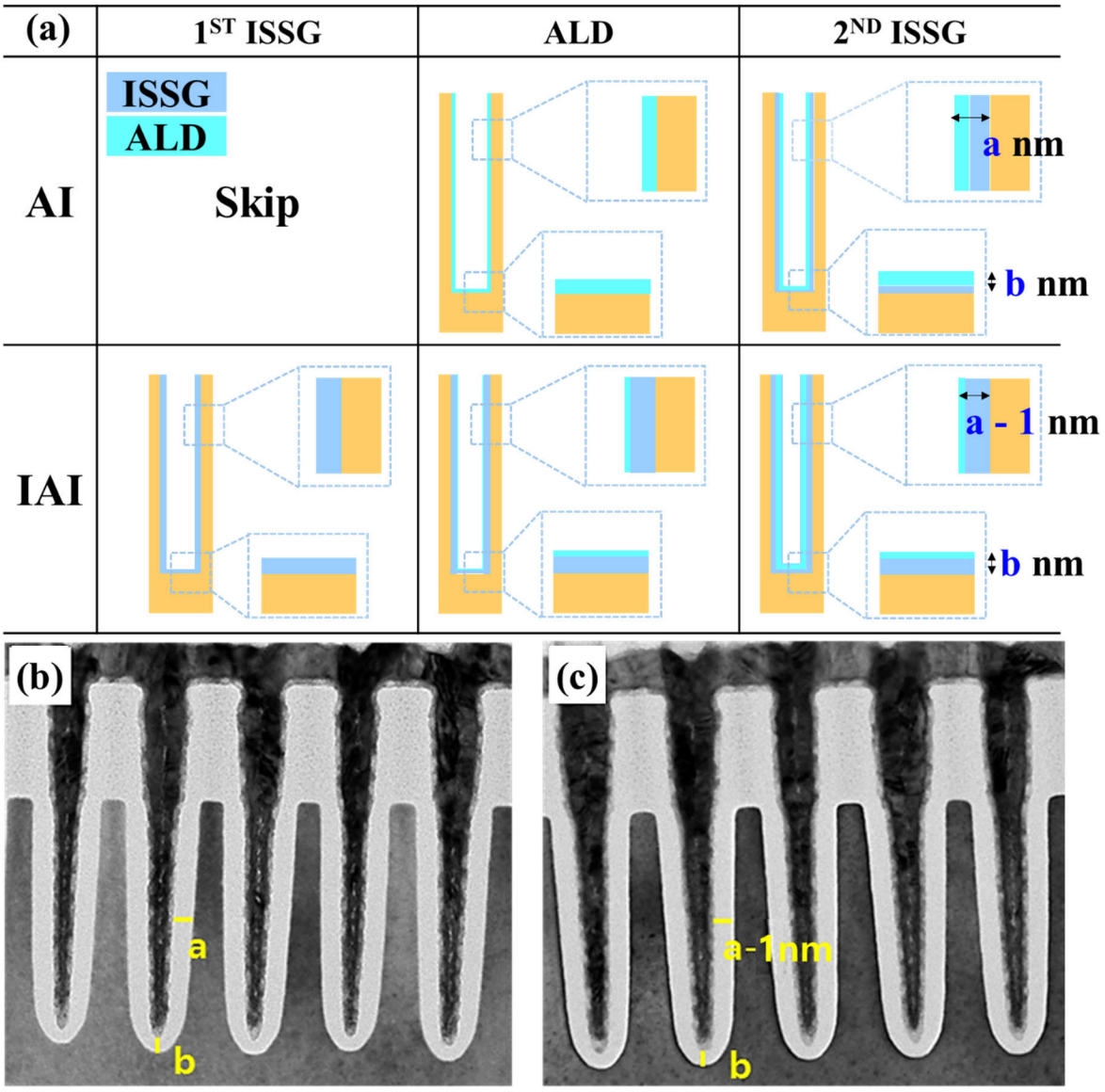

FIGURE 4. (a) G_{ox} schematic diagram of AI and IAI. The IAI scheme reduces G_{ox} thickness in the sidewalls by ~1 nm compared to the AI scheme. (b), (c) Cross-sectional TEM images of AI and IAI scheme, respectively.

TABLE 2. Actual G_{ox} thickness for each step: AI and IAI.

	(nm)	1ST ISSG	ALD	2ND ISSG	Total Thickness
AI	Side		4	~ 5	9
	Bottom		4	~ 2	6
IAI	Side	~ 6	2	< 0.1	8
	Bottom	~ 4	2	< 0.1	6

in the GIDL current. Fortunately, this unwanted effect can be addressed by adjusting the amount of high-quality oxide deposited by ISSG.

The density of the ISSG film, produced by oxidizing Si, is higher than that of ALD oxide. Therefore, the quality of the ISSG film is superior to the ALD film. This can be verified by comparing the wet etch rates. The wet etch rate of ISSG immersed in 200:1 HF solution is lower compared to ALD, as shown in Fig. 5(a).

SiO_2 film formation can be explained by the following sequential reactions where (3) is for ALD and (4) is for ISSG:

$$2Si_2Cl_3(\text{HCDs}) + \text{hot stage} \rightarrow Si + 3SiCl_4 < 700^\circ C$$
$$SiCl_4(\text{Chlorosilane Polymer}) + 2H_2O \rightarrow SiO_2 + 4HCl \uparrow \quad (3)$$

$$Si + O_2 + H_2O \rightarrow SiO_2 + H_2 \uparrow \quad > 1000^\circ C \quad (4)$$

Reactions (3) and (4) further indicate that, in terms of impurities within G_{ox}, the ISSG film is more pristine. The ALD method utilizes precursors for chemical reactions, such as Cl, which can persist in the film and potentially form traps after the reactions. Therefore, the ISSG film has fewer

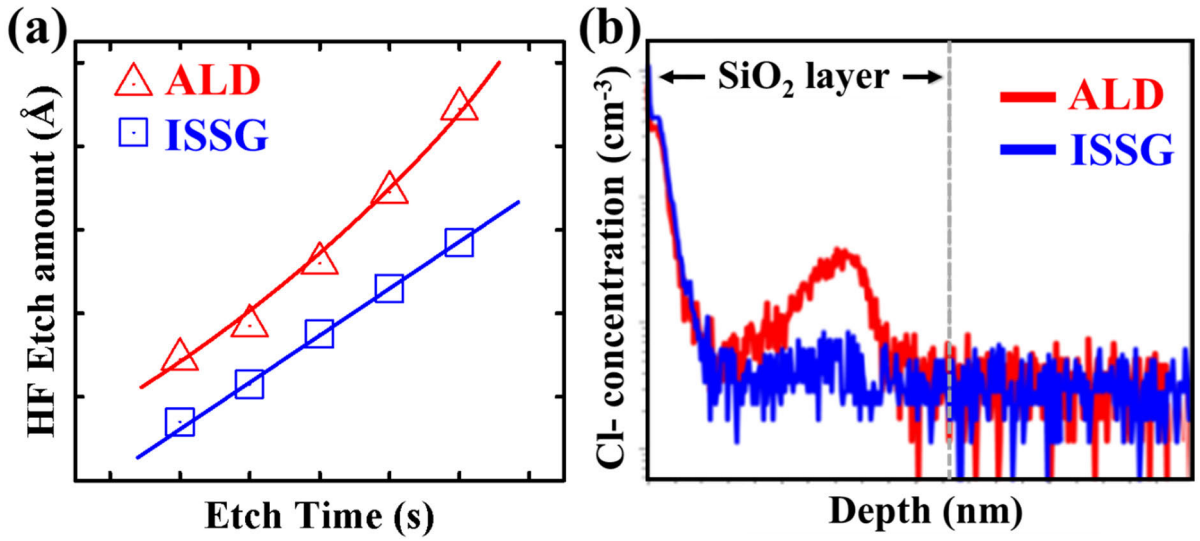

FIGURE 5. Comparison of ALD and ISSG film: (a) wet etch rate for 200:1 HF solution, (b) SIMS profile of Cl- concentration in none pattern wafer.

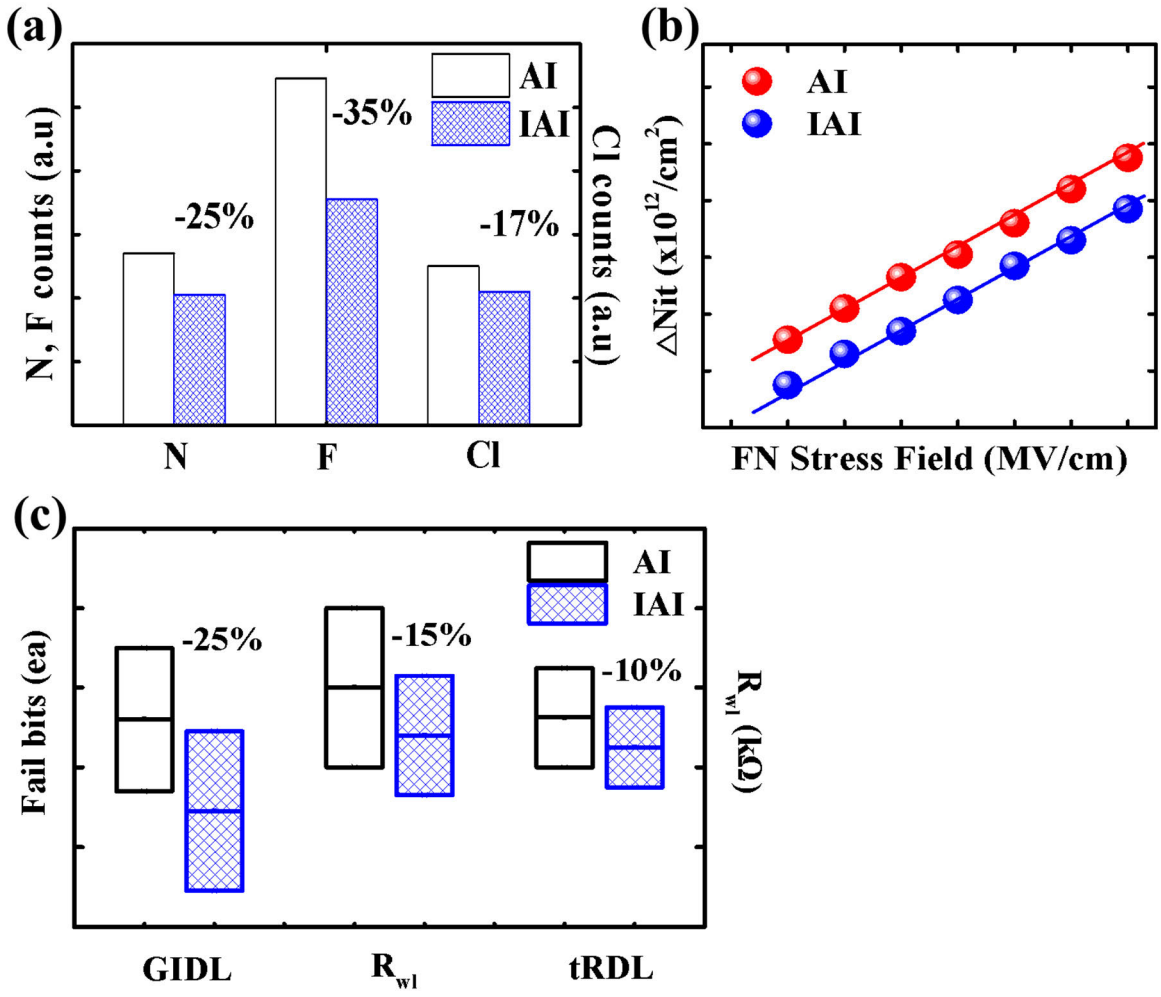

FIGURE 6. Comparison under AI and IAI conditions: (a) SIMS results for impurities including N, F, and Cl in real BCAT pattern, (b) N_{it} variation after FN stress, (c) statistical analysis results for the electrical characteristics of 2000 wafers: GIDL fail bits of IAI condition were reduced by 25 % compared to AI condition. The R_{wl} and fail bits of word line decreased by 15 % and 10 %, respectively.

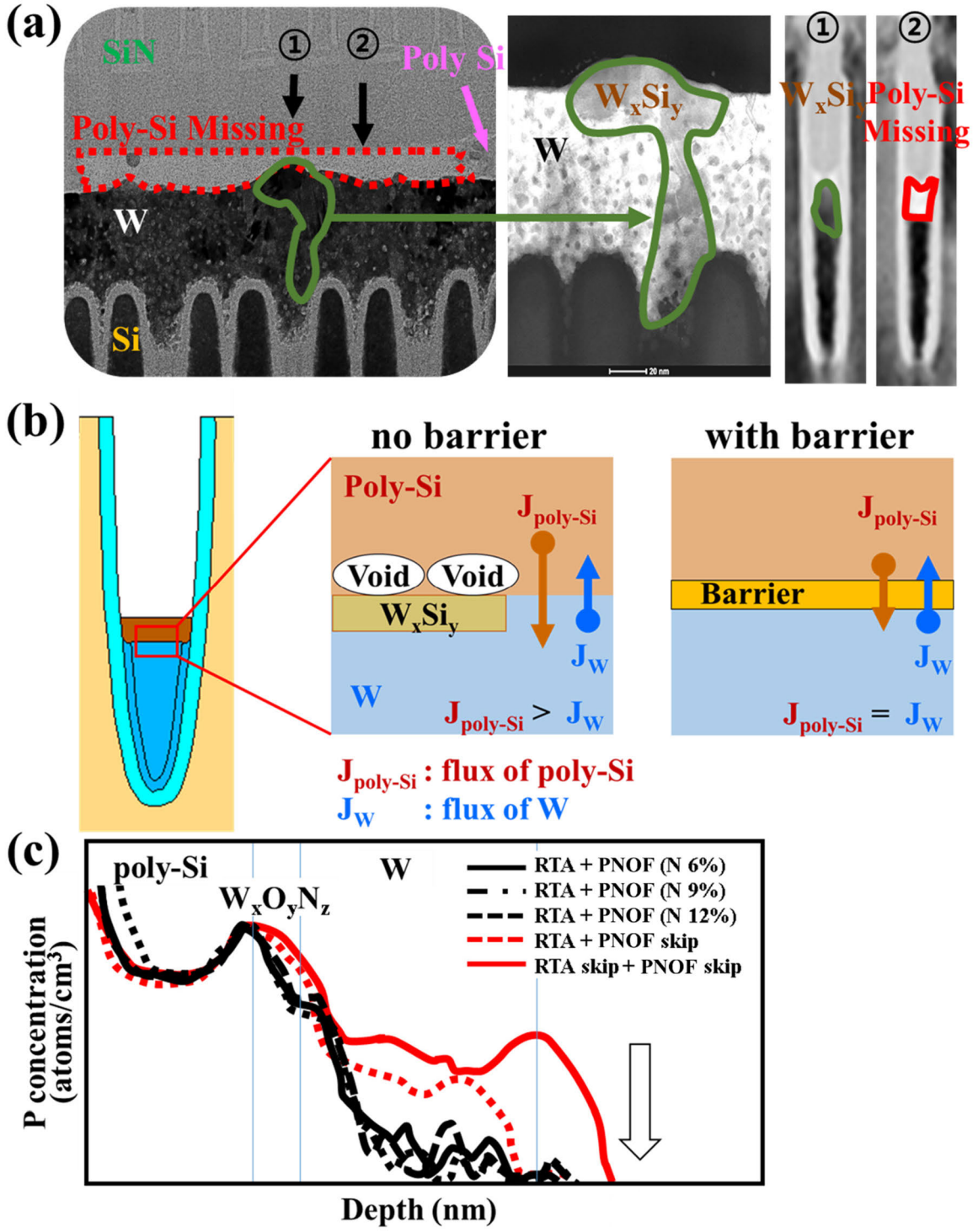

FIGURE 7. (a) TEM images of a poly-Si missing defect for x-axis and y-axis, (b) Diagram illustrating the Kirkendall effect attributed to the difference in diffusivity between W and poly-Si: Without insufficient barrier, the flux of poly-Si is high, causing it to move towards the W side, resulting in the creation of voids, (c) SIMS profiles of P diffusion with various barrier conditions after high temperature annealing. P diffusion does not occur in all cases of the PNOF barrier.

potential traps. Secondary ion mass spectrometry (SIMS) analysis on a non-patterned wafer (NPW) confirmed a significant reduction in Cl-components in the ISSG film compared to the ALD film, as presented in Fig. 5(b). And, after BCAT pattern etching, despite comprehensive cleaning procedures, residual impurities from the etching process persist on the

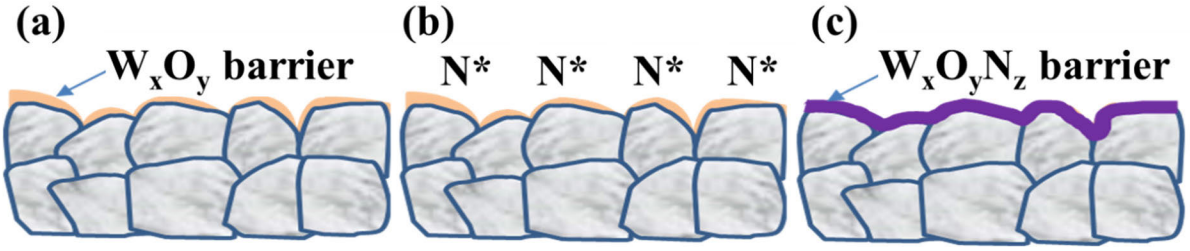

FIGURE 8. Schematic diagrams illustrating the sequence of $W_xO_yN_z$ barrier formation.

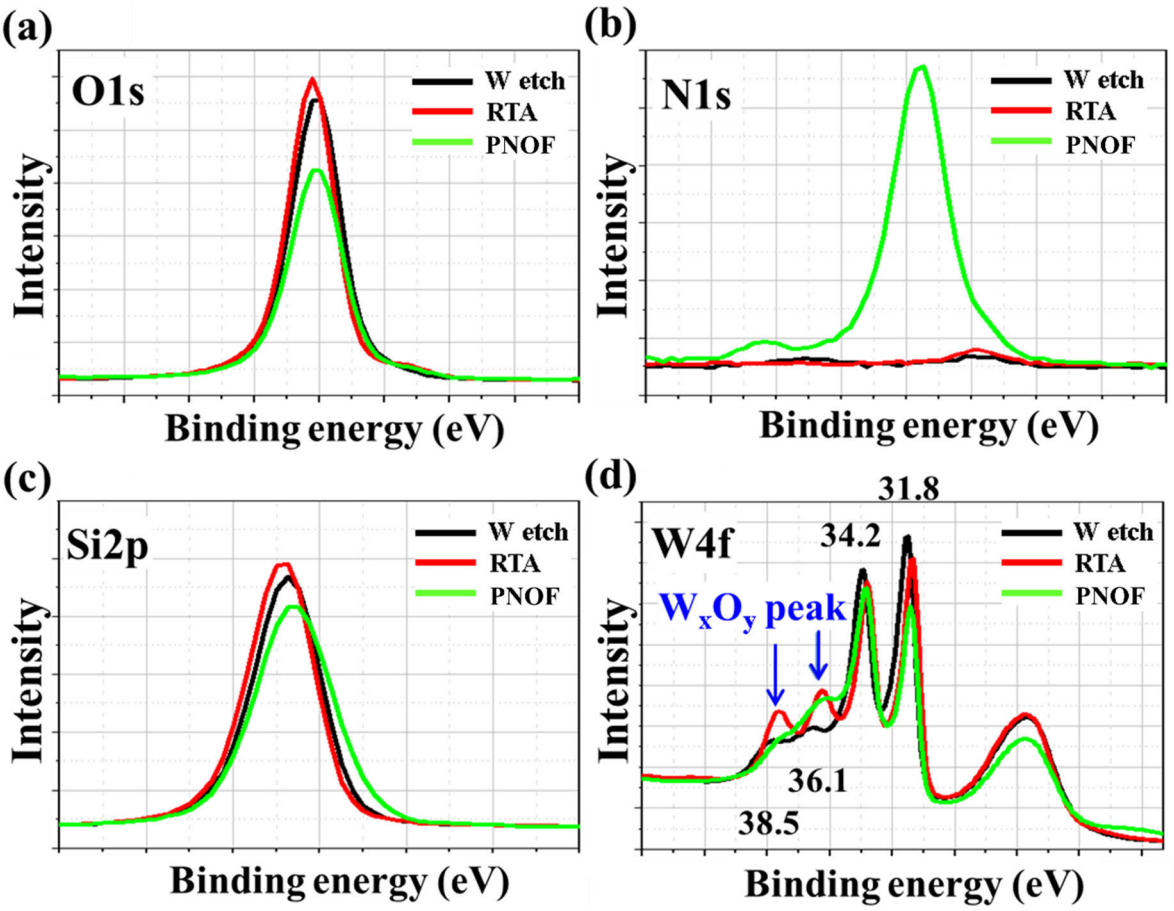

FIGURE 9. XPS spectrum analysis for the $W_xO_yN_z$ barrier layer after three consecutive processes (W etch, RTA, PNOF): (a) O1s, (b) N1s, (c) Si2p, and (b) W4f.

surface of the G_{ox}. In the IAI method, the high-temperature ISSG process is conducted first, aiding in the removal of etching impurities.

Based on the NPW experimental data, AI and IAI processing schemes were applied to fabricate BCATs and the results were compared. Initially, the impurity contents within the G_{ox} films were compared using SIMS profiles, and variations in interface trap density (N_{it}) under Fowler Nordheim (FN) stress were also examined. As expected, the IAI scheme produced lower impurity levels, including N, F, and Cl, compared to AI, consistent with the NPW results. Additionally, it was confirmed that N_{it} variation decreased after FN stress was applied to the devices made using IAI, as shown in Fig. 6(a) (b).

Applying IAI and AI schemes to fabricate 8G DDR4 DRAMs, we evaluated about 2000 wafers, and statistical data were extracted and analyzed. As shown in Fig. 6(c), the number of refresh fail bits for IAI devices was lower by 25 % compared to AI devices. This is due to the lower quantity of interfacial traps due to the decreased number of impurities in IAI devices. The R_{wl} decreased by 15 % due to the increase in the W gate area in the lateral direction.

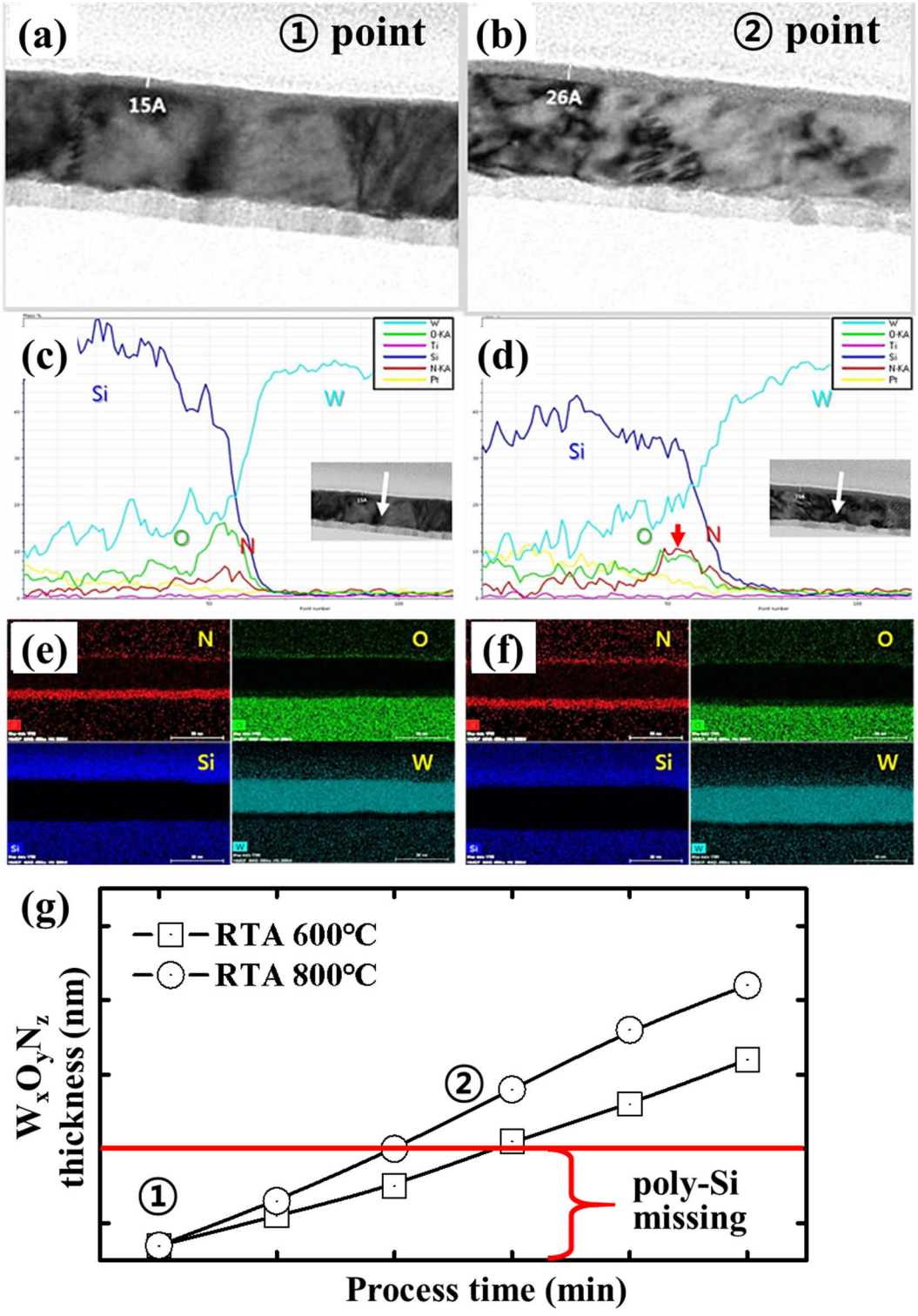

FIGURE 10. Vertical TEM images and EDX scanning results of two barriers (①, ② points in Figure (g)): (a)/(c)/(e) PNOF only and (b)/(d)/(f) combination of RTA and PNOF, (g) thickness variation due to the RTA process time and temperature conditions. Poly-Si missing defects occur below a certain thickness of $W_xO_yN_z$.

Consequently, there was a substantial 10 % reduction in the word line fail bits for IAI devices. This further confirms that the G_{ox} processing scheme developed in this study is capable of reducing traps in G_{ox} and its interface. Simultaneously,

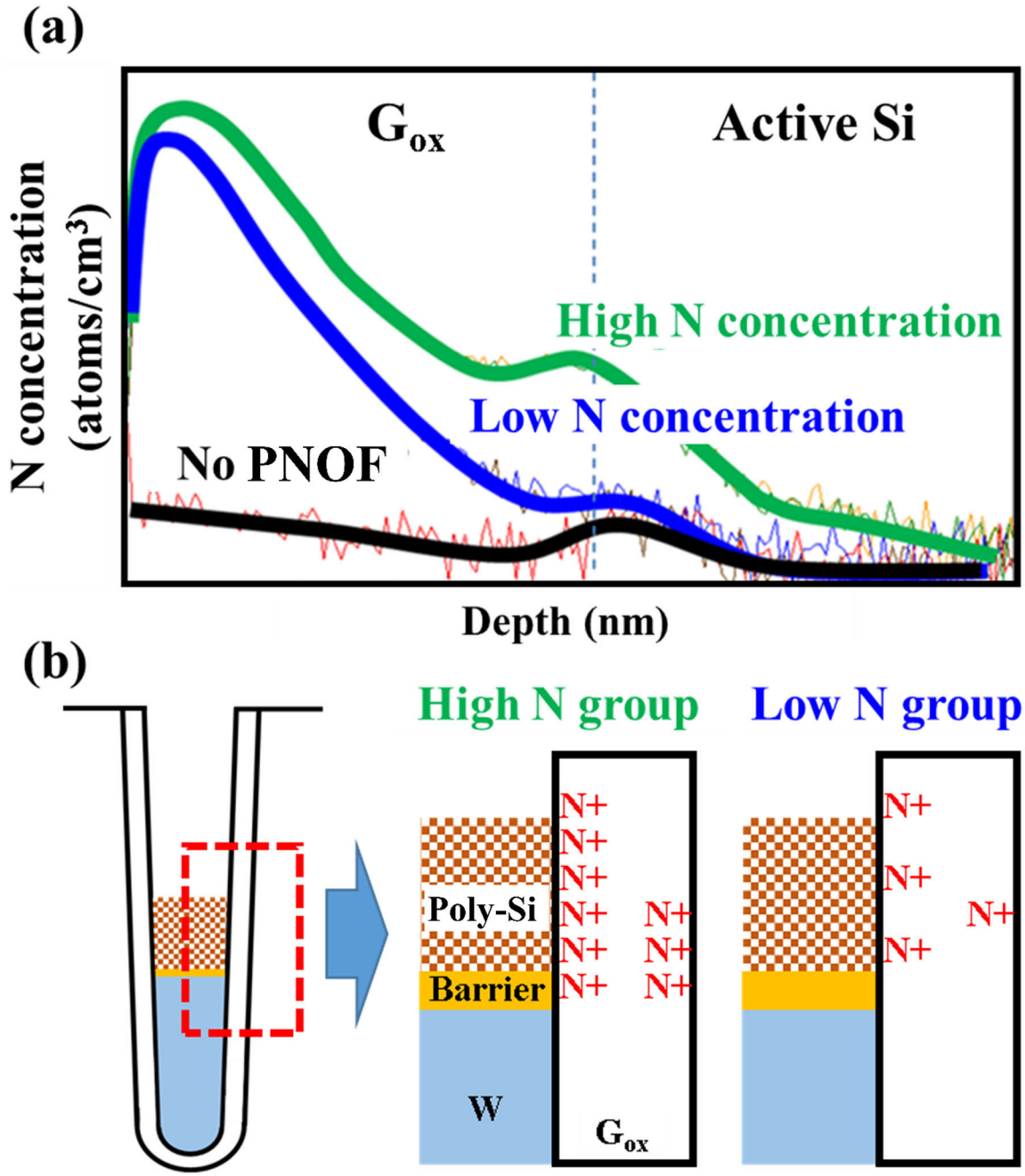

FIGURE 11. (a) SIMS analysis of increasing N concentration through PNOF process control, (b) the schematic diagram of nitrogen location into G_{ox} in case of the high/low N concentration through PNOF process, respectively.

IAI enables the feature sizes of the device to be scaled down.

C. BARRIER TECHNOLOGY: PNOF

Plasma nitridation treatment of oxide film (PNOF) was developed to create barrier layers which prevent interactions between the two gates. Therefore, PNOF can be used to enhance the performance of DWF-BCAT.

For the initial stages of this study, a separate barrier material was not inserted at the interface between gate W and poly-Si, and the poly-Si is directly deposited on the W film. Thus, only a natural oxide layer due to exposure to the atmosphere was formed in the boundary region between the two gates. From the cross-sectional TEM image in Fig. 7(a), there are missing poly-Si gates in the boundary region on the poly-Si side. Additionally, a new film was formed at the boundary region on the W side, and compositional analysis revealed this film to be tungsten silicide (W_xSi_y). In regions where no interactions occur, the thin barrier formed between the two films is identified as tungsten oxide (W_xO_y), with most layers measuring 1 nm or less in thickness. Simply, when W and poly-Si come into direct contact without a barrier material,

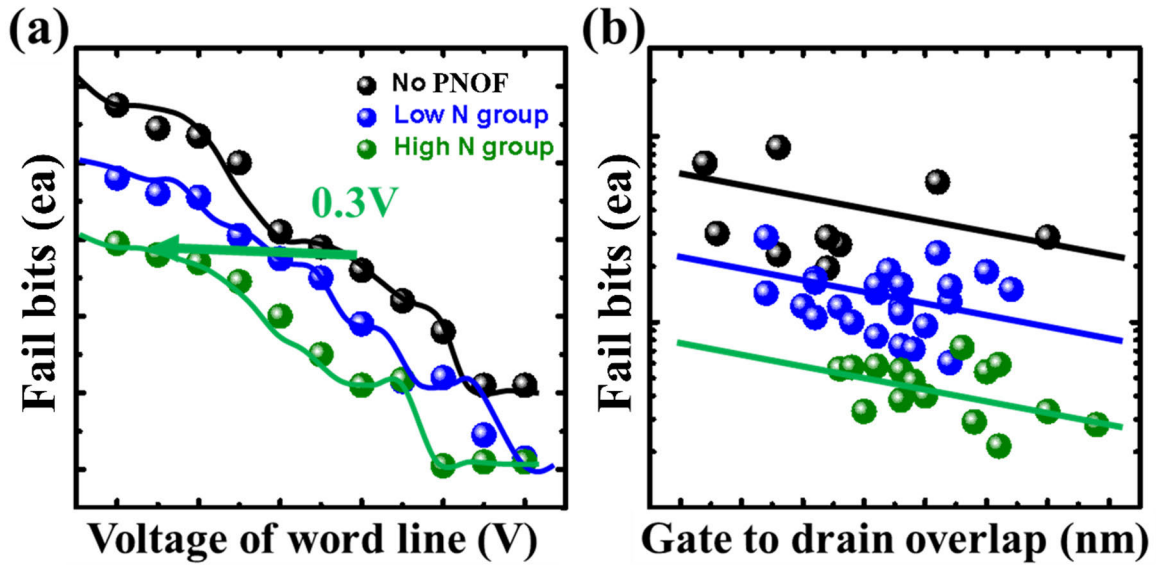

FIGURE 12. Electrical characteristics analysis results based on mass wafer: (a) gate voltage margin increases in high N concentration group, (b) analysis of word line fail bits based on three N concentrations of PNOF barrier.

a thin W_xO_y film is formed at the interface, or the W_xO_y barrier is penetrated and a W_xSi_y layer is formed. These cause significant fluctuations in R_{wl} and V_{th}.

The above is similar to the metal contact process development failure observed in traditional DRAMs. When metal and poly-Si come into direct contact, they form silicide reaction products and leave voids on the Si side. This is called the Kirkendall effect and is attributed to the difference in diffusivity between the materials, as shown in Fig. 7(b). This effect deteriorates the properties of the DRAM, including R_{wl}, V_{th}, and is detrimental for the mass production of DRAMs.

Therefore, a new PNOF barrier ($W_xO_yN_z$) was introduced and characterized [12], [13], [14]. To verify the durability of the barrier, poly-Si defect inspection and P diffusion acceleration measurements after NPW post treatment were conducted, as shown in Fig. 7(c). It was observed that there are no poly-Si vacancy defects in the wafers that utilized the PNOF barrier. Furthermore, P diffusion, where P contained in poly-Si escapes, did not occur in all cases, regardless of the N concentration during PNOF. This implies that the PNOF barrier exhibits excellent properties which prevent the formation of Kirkendall voids. The results confirm that $W_xO_yN_z$ can be used as a durable barrier material in DWF-BCAT.

In the case of the W_xO_y barrier layer, P diffusion can degrade the transistor characteristics. Additionally, if there is no nitrogen within the W_xO_y barrier, the interfacial resistance can increase [12], [13], [14]. Moreover, poly-Si vacancies may be generated after annealing in the case of W_xN_y or W_xO_y barrier layers. $W_xO_yN_z$ barrier formation can be explained by two sequential reactions:

$$W(\text{ hot stage }) + \text{Air}\,(O_2/H_2O/-OH) \rightarrow W_xO_y \quad (5)$$

$$W_xO_y + N^*(\text{PNOF, plasma }) \rightarrow W_xO_yN_z \quad (6)$$

W has a higher affinity for oxygen than N. Thermodynamically, the formation of tungsten oxide (ΔGf, $WO_3 = -842.9$ kJ/mol and ΔGf, $WO_2 = -589.7$ kJ/mol) is energetically preferred over the formation of W_2N (ΔGf, $W_2N = -22$ kJ/mol) [15]. Therefore, when exposed to the atmosphere, W readily reacts with O to form a natural oxide layer. The W_xO_y layer is partially formed on the multi-grain W surface, and discontinuous points exist in certain weak regions, such as grain boundaries, as shown in Fig. 8(a). Heat treatment, such as RTA, aids in the production of a uniform W_xO_y film. Subsequently, a continuous $W_xO_yN_z$ barrier is formed by plasma nitridation. The highly reactive N radicals generated by microwave plasma serve as catalysts to transform W_xO_y into $W_xO_yN_z$. The PNOF process is illustrated in Fig. 8.

X-ray photoelectron spectroscopy (XPS) was carried out to identify the chemical bonding states of barriers. Fig. 9(a), (b), (c), and (d) show the O1s, N1s, Si2p, and W4f XPS spectrum, respectively, for each process step (W etch $\rightarrow$ RTA $\rightarrow$ PNOF). The main binding energy of the W $4f_{7/2}$ and W $4f_{5/2}$ electrons of the W_xO_y and $W_xO_yN_z$ barriers is 31.8 and 34.2 eV, respectively, as shown in Fig. 12(d). These values are consistent with the peaks of metallic W [15]. Two additional peaks at high binding energies of 36.1 and 38.5 eV, as indicated by the blue arrows in Fig. 9(d), are observed for the W_xO_y barrier. These peaks correspond to the binding energies of $WO_2$and are attributed to oxidation during the RTA process. After the RTA, there is almost no peak in the N 1s spectrum of the W_xO_y barrier, as shown in Fig. 9(b). After the PNOF process, the intensity of the N 1s peak in the $W_xO_yN_z$ barrier dramatically increased, and the relative intensity of the peaks at 36.1 and 38.5 eV in the $W_xO_yN_z$ barrier is lower than that in the W_xO_y barrier. These XPS results are consistent with our modeling.

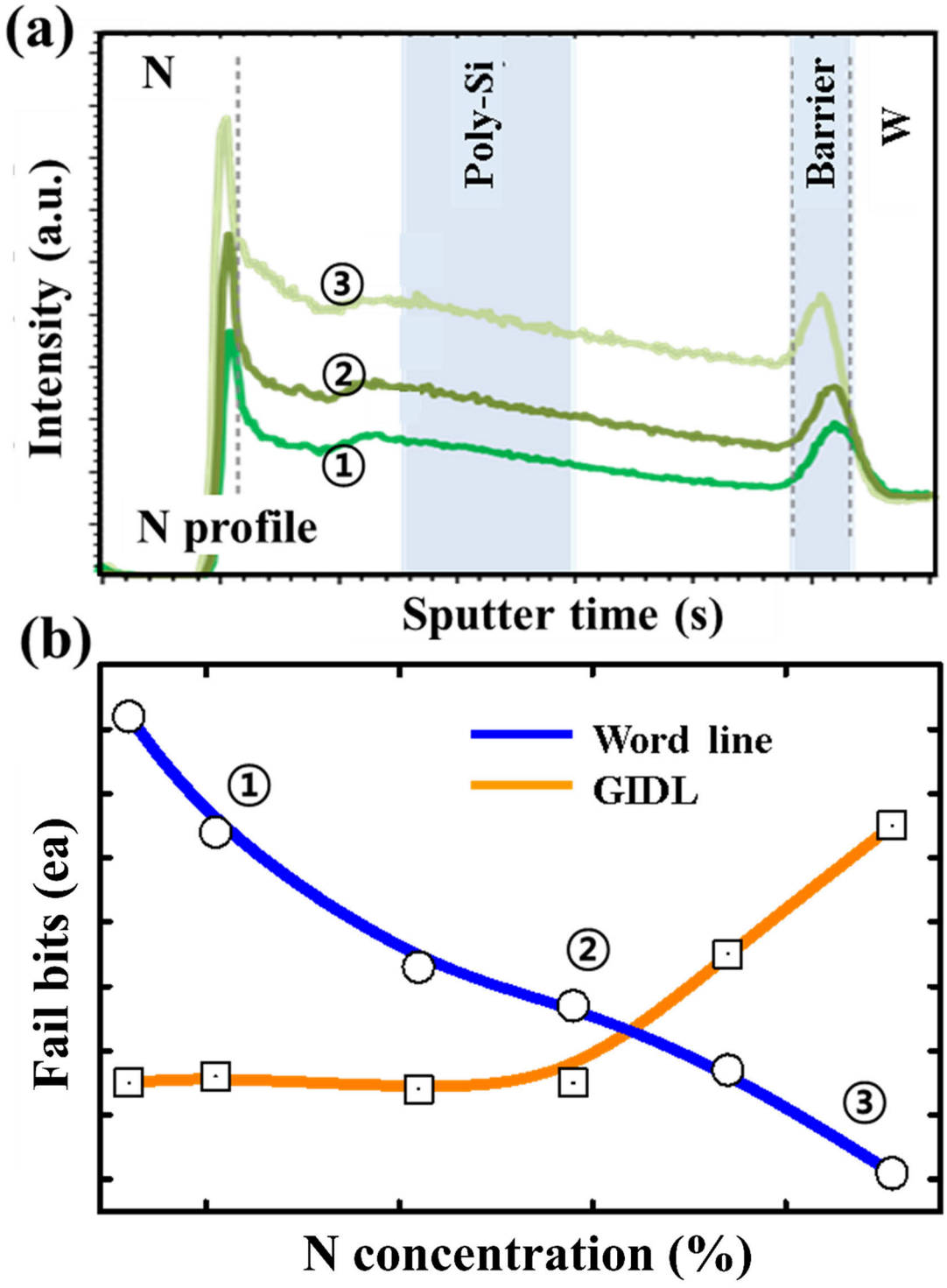

FIGURE 13. (a) N profile with increasing N concentration through PNOF process on real pattern, (b) word line and GIDL fail bit characteristics based on various N concentration in DRAM device.

To ensure that the gate films do not undergo inter-diffusion, the thickness of the $W_xO_yN_z$ layer must be optimized. The thickness of the naturally formed oxide on the W surface before and after RTA was measured, and the results are shown in Fig. 10(g). Different RTA process temperatures and annealing times were evaluated. After PNOF, the oxide thickness was measured via TEM images. As expected, the thickness of the $W_xO_yN_z$ is correlated with the RTA process temperature and annealing time. Poly-Si vacancy defects were observed for oxide thicknesses below about 2 nm,

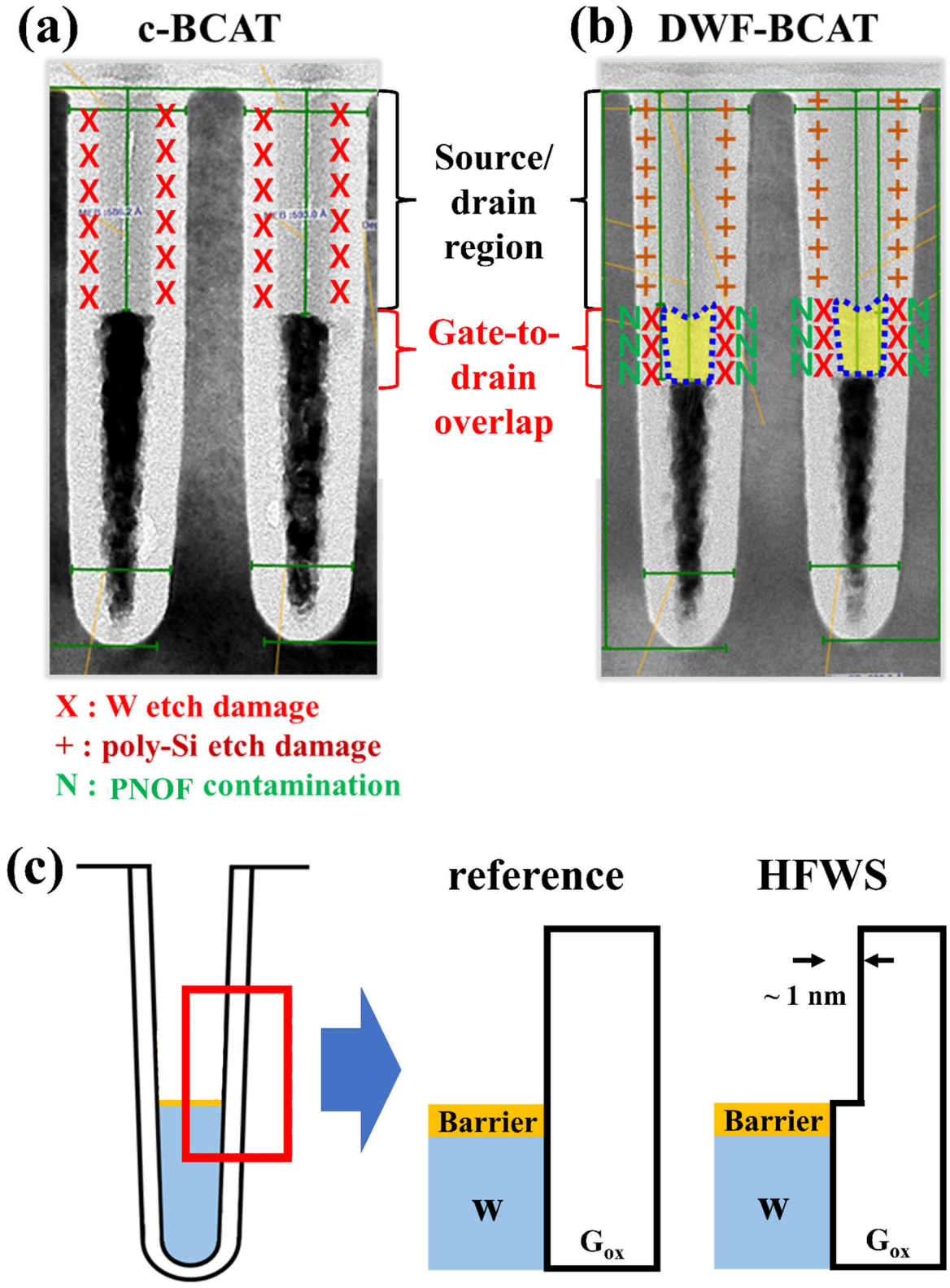

FIGURE 14. Schematic diagram of damage and contamination layer on gate-to-drain overlap region: (a) c-BCAT and (b) DWF-BCAT, (c) HFWS scheme: after the PNOF process, HFWS is carried out to remove impurities along with the G_{ox} surface.

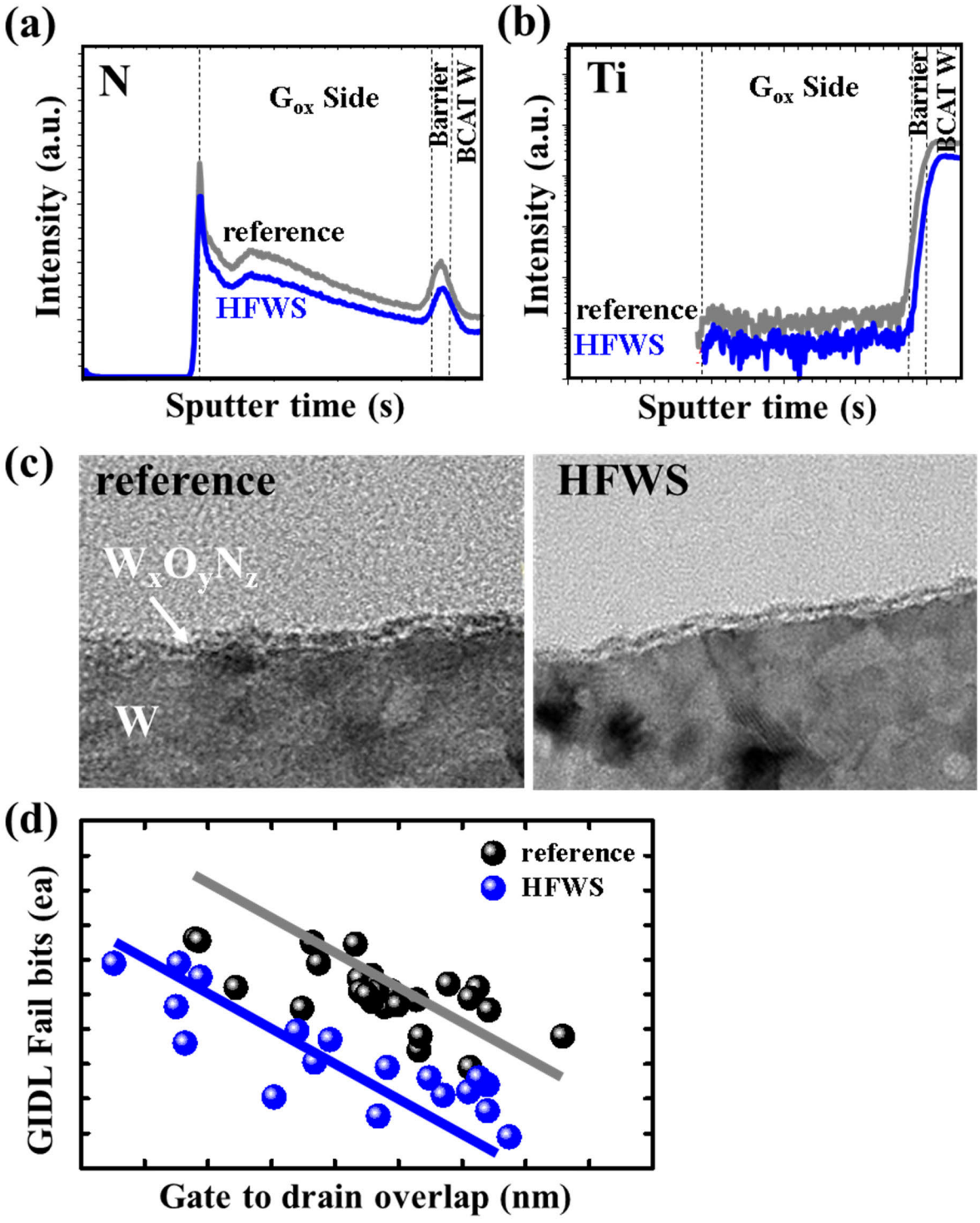

FIGURE 15. SIMS profile of reference and HFWS on real pattern: (a) Ti and (b) N into G_{ox} area, (c) barrier morphology and thickness of reference and HFWS group, (d) reduction of GIDL fail bits after HFWS due to impurities removal in G_{ox}.

as shown in Fig. 10(g). When comparing the results, two significant differences were observed, as shown in Fig. 10(g). The difference in thickness of the $W_xO_yN_z$ barrier between the two films, with and without RTA, was observed to be above 1 nm. The application of RTA and PNOF formed a barrier with a higher N content, as shown in Fig. 10(a)-(e). In other words, to obtain a stable $W_xO_yN_z$ barrier, sufficient oxidation via RTA is required to grow the W_xO_y film to a thickness above 2 nm, followed by the nitride plasma process to introduce N.

Controlling the N concentration during PNOF is critical to high-quality $W_xO_yN_z$ barrier formation. The N concentration can be regulated by adjusting the plasma density, process time, or temperature, as shown in Fig. 11(a). Low N concentrations in $W_xO_yN_z$ films produce poly-Si vacancy-type defects and P diffusion. As discussed earlier, this leads to an increase in R_{wl} and variations in the V_{th}. However, if very high N concentrations are introduced during PNOF, the G_{ox} interface characteristics are degraded because the N can also penetrate into the G_{ox} sidewall. This can decrease the barrier resistance but also increased the interfacial traps in G_{ox}, as shown in Fig. 11 (a) and (b).

NPWs were processed using different PNOF conditions and the resulting properties were compared. The N concentration was modulated by varying the plasma density and process time. Initially, the gate control characteristics for three types of PNOF conditions: no PNOF, low N concentration PNOF, and high N concentration PNOF were investigated. While sweeping the word line voltage, we examined the behavior of the tail bits where failures occurred, as revealed in Fig. 12(a). As predicted, the increase in N concentration led to a decrease in fail bits. Between the groups of wafers without PNOF application and with high N concentration PNOF, there was a significant 0.3 V difference in the gate voltage margin at the same 10 ppm fail criteria. Also, the number of word line fail bits was measured while adjusting the gate-to-drain overlap distance. On the same x-axis, it was apparent that fail bits notably decreased in the high N concentration group, as shown in Fig. 12(b). Increasing the N concentration reduces gate resistance and improves control capability.

To confirm whether the increase in N concentration has an impact on trap formation, experiments were conducted on actual BCAT devices. Similar to the NPW results, the N concentration within G_{ox} in the actual BCAT structure also varied according to the PNOF process parameters, as shown in Fig. 13(a). It can be inferred that the word line and GIDL characteristics are inversely correlated with each other based on the N concentration, and there is an optimum N concentration. As the N concentration increases, it was observed that up to the Fig. 13(b) - ② region, the GIDL values increase without a significant spike, and the word line characteristics improve linearly. Based on this data, we derived the optimal N concentration that produces devices with the best electrical characteristics and standardized the PNOF process across all devices.

D. CONTAMINATION STRIP TECHNOLOGY: HFWS

The interface between poly-Si and the G_{ox} sidewall is strategically formed as the gate-to-drain overlap region. Consequently, GIDL characteristics in this area are highly sensitive to the presence of traps, as seen in Fig. 13. The DWF-BCAT structure, unlike c-BCAT, has gates composed of two materials, W and poly-Si. Before the deposition of poly-Si on gate W, W etching and PNOF processes are conducted, exposing G_{ox} to various impurities. In addition, there may be plasma damage and etch by-products, including excess N, as shown in Fig. 14(a)(b). It is essential to identify and remove these impurities.

SIMS confirmed the presence of N and Ti residues on the G_{ox} surface, as shown in Fig. 15(a) (b). These were left behind after the W and barrier metal Ti_xN_y etch processes. N detected within G_{ox} is due to the PNOF process. These act as traps on the G_{ox} sidewalls. Therefore, after PNOF, a HF wet strip (HFWS) process was applied to remove impurities, as shown in Fig. 14(c). This process cleans the surface without etching the upper $W_xO_yN_z$ barrier, as shown in Fig. 15(c). The HFWS process parameters were optimized to ensure that only a minimal thickness of approximately 1 nm was etched from the G_{ox} sidewall. After applying HFWS, a decrease in N and Ti contaminants was observed, and electrical measurements verified the drop in GIDL current at the gate-to-drain overlap, as shown in Fig. 15(d).

IV. CONCLUSION

We successfully manufactured the world's smallest dual work function gate cell transistor. To achieve this we designed, optimized, and evaluated different processing schemes to overcome the main challenges encountered when scaling down transistors. This study involved modeling and simulation, evaluating the effect of the different processing schemes with non-patterned wafers, and finally, applying the schemes to actual DWF-BCAT devices and measuring the effect of different process parameters on the performance of the devices. Therefore, a DRAM with sub 17-nm features was fabricated and its memory retention capabilities were characterized. The DWF-BCAT design and fabrication processes developed in this study will enable further miniaturization of DRAMs, thus allowing more DRAMs to be packed in high-performance integrated circuits and processors which are crucial for meeting the intense computing applications of modern society.

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REFERENCES

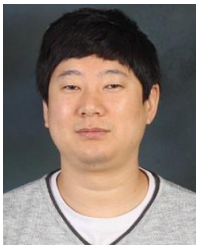
[1] A. Spessot and H. Oh, "1T-1C dynamic random access memory status, challenges, and prospects," *IEEE Trans. Electron Devices*, vol. 67, no. 4, pp. 1382–1393, Apr. 2020, doi: 10.1109/TED.2020.2963911.

[2] J. M. Park, Y. S. Hwang, S.-W. Kim, S. Y. Han, J. S. Park, J. Kim, J. W. Seo, B. S. Kim, S. H. Shin, C. H. Cho, S. W. Nam, H. S. Hong, K. P. Lee, G. Y. Jin, and E. S. Jung, "20 nm DRAM: A new beginning of another revolution," in *IEDM Tech. Dig.*, Washington, DC, USA, Dec. 2015, pp. 26.5.1–26.5.4, doi: 10.1109/IEDM.2015.7409774.

[3] K. Saino, S. Horiba, S. Uchiyama, Y. Takaishi, M. Takenaka, T. Uchida, Y. Takada, K. Koyama, H. Miyake, and C. Hu, "Impact of gate-induced drain leakage current on the tail distribution of DRAM data retention time," in *IEDM Tech. Dig.*, Dec. 2000, pp. 837–840, doi: 10.1109/IEDM.2000.904447.

[4] J. Y. Kim et al., "The breakthrough in data retention time of DRAM using recess-channel-array transistor (RCAT) for 88 nm feature size and beyond," in *Proc. Symp. VLSI Technol.*, 2003, doi: 10.1109/VLSIT.2003.1221061.

[5] J. Y. Kim et al., "S-RCAT (sphere-shaped-recess-channel-array transistor) technology for 70 nm DRAM feature size and beyond," in *Proc. Symp. VLSI Technol.*, Jun. 2005, pp. 34–35, doi: 10.1109/.2005.1469201.
[6] T. Schloesser et al., "6F^2 buried wordline DRAM cell for 40 nm and beyond," in *IEDM Tech. Dig.*, San Francisco, CA, USA, Dec. 2008, pp. 1–4, doi: 10.1109/IEDM.2008.4796820.
[7] S. Lee, G.-J. Kim, N.-H. Lee, K. Lee, B. Woo, J. Jin, J. Kim, Y. Lee, H. Kim, and S. Pae, "Reliability characterization for advanced DRAM using HK/MG + EUV process technology," in *IEDM Tech. Dig.*, San Francisco, CA, USA, Dec. 2021, pp. 6.6.1–6.6.4, doi: 10.1109/IEDM19574.2021.9720613.
[8] S. Jeong, J.-S. Lee, J. Jang, J. Kim, H. Shin, J. H. Kim, J. Song, D. Woo, J. Oh, and J. Lee, "Investigation of sub-20 nm 4th generation DRAM cell transistor's parasitic resistance and scalable methodology for sub-20 nm era," in *Proc. IEEE Int. Rel. Phys. Symp. (IRPS)*, Monterey, CA, USA, Mar. 2023, pp. 1–6, doi: 10.1109/IRPS48203.2023.10118270.
[9] D. Han, Y. Hwang, and B. Choi, "Effects of polycrystalline silicon plug defect on DRAM characteristics," *IEEE Trans. Electron Devices*, vol. 70, no. 7, pp. 3559–3562, Jul. 2023, doi: 10.1109/TED.2023.3280890.
[10] S. K. Gautam, S. Maheshwaram, S. K. Manhas, A. Kumar, S. Sherman, and S. H. Jo, "Reduction of GIDL using dual work-function metal gate in DRAM," in *Proc. IEEE 8th Int. Memory Workshop (IMW)*, Paris, France, May 2016, pp. 1–4, doi: 10.1109/IMW.2016.7495287.
[11] C. D. Krzeminski, X.-L. Han, and G. Larrieu, "Understanding of the retarded oxidation effects in silicon nanostructures," *Appl. Phys. Lett.*, vol. 100, no. 26, Jun. 2012, Art. no. 263111, doi: 10.1063/1.4729410.
[12] S. H. Mohamed and A. Anders, "Structural, optical, and electrical properties of $WO_x(N_y)$ films deposited by reactive dual magnetron sputtering," *Surf. Coatings Technol.*, vol. 201, no. 6, pp. 2977–2983, Dec. 2006, doi: 10.1016/j.surfcoat.2006.06.008.
[13] K.-C. Tsai, W.-F. Wu, J.-C. Chen, T.-J. Pan, and C.-G. Chao, "Influence of N_2O plasma treatment on microstructure and thermal stability of WN_x barriers for Cu interconnection," *J. Vac. Sci. Technol. B, Microelectron. Nanometer Struct. Process., Meas., Phenomena*, vol. 22, no. 3, pp. 993–999, May 2004, doi: 10.1116/1.1715087.
[14] K. J. Lethy, S. Potdar, V. P. M. Pillai, and V. Ganesan, "Transparent and low resistive nanostructured laser ablated tungsten oxide thin films by nitrogen doping: I. Nitrogen pressure," *J. Phys. D, Appl. Phys.*, vol. 42, no. 9, May 2009, Art. no. 095412, doi: 10.1088/0022-3727/42/9/095412.
[15] Y. G. Shen and Y. W. Mai, "Reactively sputtered WOxNy films," *J. Mater. Res.*, vol. 15, no. 11, pp. 2437–2445, Nov. 2000, doi: 10.1557/jmr.2000.0350.



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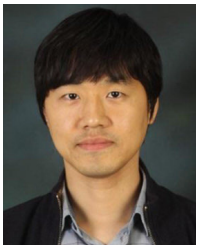

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