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RESEARCH ARTICLE

# Design of High-Robustness LDO Regulator With Floating SCR Based ESD Protection Circuit Using High Gain Buffer

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**ABSTRACT** Currently, in the semiconductor market, reliability response to Electro Static Discharge (ESD) situations is being discussed as an alternative to internal Integrated Circuit (IC) destruction. In this paper, the ESD protection circuit design integrated into the Low Drop Out (LDO) regulator presents an alternative to the reliability of the internal IC. Additionally, the LDO regulator proposed in this paper is designed to minimize output voltage changes by significantly improving gain using a high gain buffer structure. Undershoot and overshoot were effectively regulated by utilizing a high gain buffer. Under the conditions of an input voltage range of 3.3–4.5 V, a maximum load current of 400 mA, and an output voltage of 3 V, the output of the proposed LDO regulator with a high gain buffer structure kept at the undershoot and overshoot voltages of 32 mV and 36 mV, respectively. In addition, the ESD protection circuit used so far was designed with only a single diode, but the proposed ESD protection circuit is a new structure designed based on Silicon Controlled Rectifier (SCR). The proposed ESD protection circuit has an incomparable area efficiency compared to diodes.

**INDEX TERMS** LDO regulator, high reliability, ESD protection circuit, SCR, LDO regulator in integrated with ESD protection circuit.

## I. INTRODUCTION

Wearable and mobile application market is continuously growing, driven by technological advancements and the escalating demands of users. Systems employing various applications to enhance everyday convenience demand performance that can operate efficiently and persistently, even within constrained battery capacities. Due to the diverse voltage and current conditions these applications use, power supply units encounter conditions with transient load changes. These power units must effectively address such abrupt fluctuations. Moreover, given the significant requirement for standby current, mobile applications necessitate voltage stability concerning the load current.

As shown in Fig. 1, LDO regulators play a key role in smartphone, tablet PC, and various mobile devices. These devices must operate under a variety of voltage and current conditions due to the diverse user requirements and application complexity. Additionally, many mobile devices are equipped with dozens or more LDO regulators to respond to momentarily changing load conditions, ensuring the overall stability and performance of the device. However, activating numerous LDO regulators can shorten battery life. Therefore, to extend battery life, the LDO regulator should consume only low quiescent current, regardless of the presence or absence of load current.

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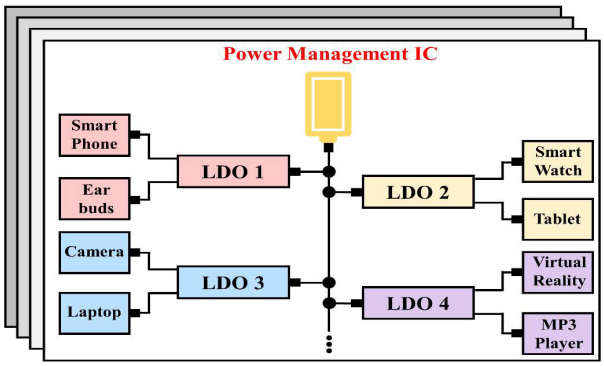


**FIGURE 1.** Power management integrated circuit.

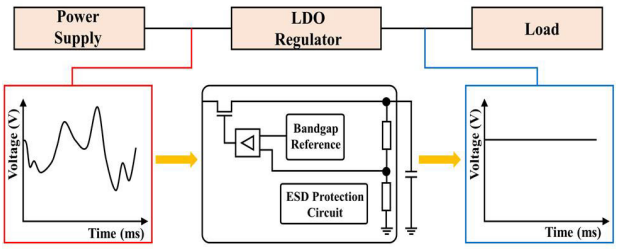


**FIGURE 2.** Voltage regulation using LDO regulator.

As shown in Fig. 2, LDO regulator is typically placed after the switching regulator to reduce the noise from the switching supply and provide a stable power supply. LDO regulators can maintain stable performance of the overall system by effectively controlling rapidly fluctuating output voltages in response to rapidly changing load conditions. Additionally, since the LDO regulator is located at the end block of the power supply, undershoot and overshoot control is required [1], [2], [3], [4], [5]. The primary objective of this study is to propose an efficient method for controlling under-shoots and over-shoots that occur during load current variations in LDO regulators. Conventional LDO regulators have a problem in that a significant amount of parasitic capacitance exists at the gate of the pass transistor. While resizing the pass transistor is vital for enhancing stability, it's equally important to ensure adequate current supply in response to load current changes. In this process, transient response output load current arise due to large under-shoots and over-shoots caused by the charging and discharging responses of the considerable parasitic capacitance. The optimized LDO regulator has improved transient response characteristics and can sustain full load currents of 100 to 200 mA. The proposed LDO regulator has been improved to reliably handle load current ranges up to 400 mA [6], [7], [8], [9], [10].

As process technology advances, IC continues to be miniaturized and integrated, reducing the device's junction depth and oxide film thickness. These changes have further limited the scope of ESD design, especially in low-voltage ICs used in mobile devices. Low-voltage IC used in these mobile

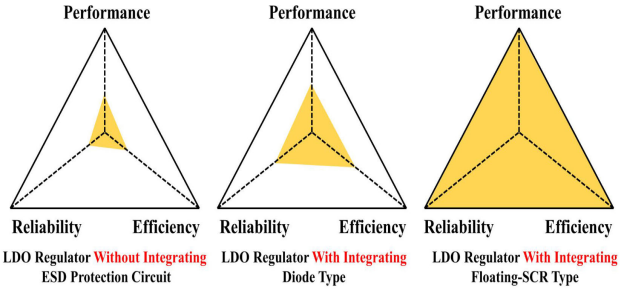


**FIGURE 3.** Differences in characteristics of the LDO regulator depending on the presence or absence of an ESD protection circuit.

applications are key components that have a critical impact on the energy efficiency, response speed, and run time of mobile devices. However, if such IC is not adequately protected against ESD, there's an elevated risk of circuit malfunctions or damage, adversely impacting the overall lifespan and reliability of the mobile device. In the semiconductor industry, ESD is a major issue directly related to the reliability and stability of IC. Particularly, when an ESD event occurs, not only the affected IC but also all interconnected IC is at risk of compromised performance and stability. Therefore, ESD is recognized as an important problem that cannot be avoided, and in modern Power Management Integrated Circuit (PMIC) design, the integration of ESD protection circuit is viewed not as an option but a mandatory requirement.

As shown in Fig. 3, the reliability of the IC significantly depends on whether or not an ESD protection circuit is integrated. ESD is a phenomenon in which electric charges move very quickly (on the order of nanoseconds). Especially in today's highly integrated and miniaturized mobile devices, ESD protection is considered essential and has a significant impact on the overall lifespan and performance of the device. One of the main objectives of this study is to verify the effectiveness and reliability of electrostatic discharge technology along with extending the battery life of these mobile devices. First, the proposed LDO regulator exhibited excellent transient response characteristics and very low bias current characteristics even under high load current conditions. Second, the proposed LDO regulator is proven to meet the ESD requirements of low-voltage integrated circuits by integrating a SCR based ESD protection circuit to prevent IC damage due to static electricity [20], [21], [22], [23].

## II. PROPOSED LDO REGULATOR

### A. THE PROPOSED LDO REGULATOR WITH HIGH GAIN BUFFER

Mobile devices with a high degree of integration generally use low-voltage mobile applications. As a result, an LDO regulator that handles a high current load must have a function that effectively regulates overshoot and undershoot, which impact circuit performance and result in the failure to maintain the required output voltage based on the current load.

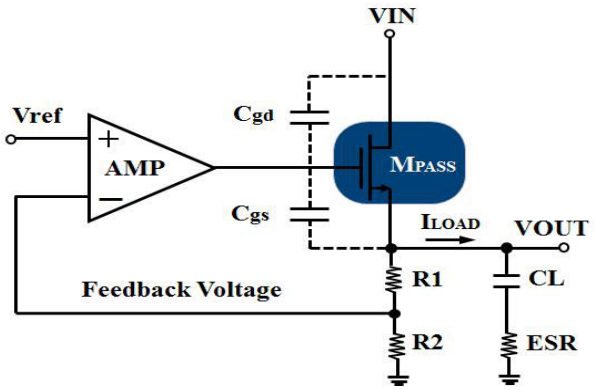


**FIGURE 4.** Conventional LDO regulator.

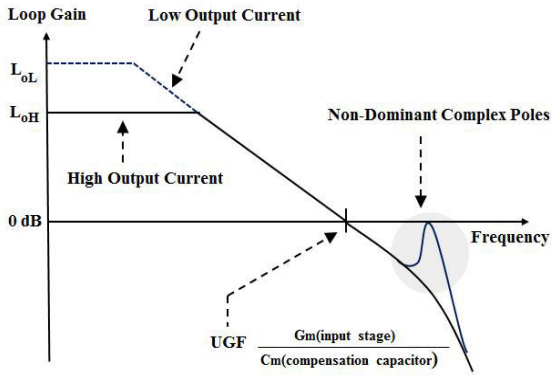


**FIGURE 5.** Loop gain according to the load.

As shown in Fig. 5, the conventional LDO regulator (circuit shown in Fig. 4) exhibits transient response characteristics as a function of load current. When the output voltage fluctuates owing to the instantaneously changing load current at the output stage, conventional LDO regulators produce more overshoot/undershoot due to the charging and discharging time of the huge parasitic capacitance of the pass transistor. By enhancing the gain and adjusting the unit gain bandwidth (UGBW), the proposed LDO regulator minimized the change in output voltage according to the load current. In a conventional LDO regulator, the overshoot and undershoot caused by load current are proportional to the overall gain of the system.

The effect of reducing the output resistance is referred to as a buffer. In the conventional buffer structure, the output resistance is expressed as $1/G_m$. To decrease the output resistance, the size of the input Metal-Oxide-Semiconductor Field-Effect Transistor (MOSFET) must be increased in the conventional buffer structure. However, since the output resistance impacts the entire system of the LDO regulator, it can only be reduced to a limited extent. The proposed LDO regulator, as shown in Fig. 6, reduces the size of the output resistance compared to the conventional buffer structure through a high gain buffer structure. The high gain buffer structure operates differently depending on undershoot and overshoot situations. The input

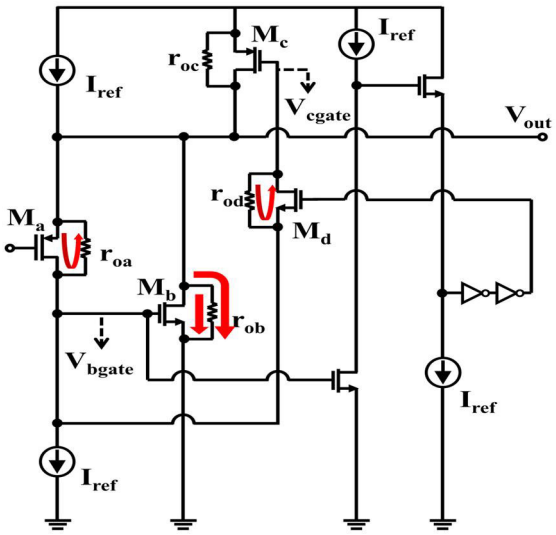


**FIGURE 6.** High gain buffer in undershoot situations.

voltage of the high gain buffer structure according to the undershoot situation is sensed as a lower voltage, and operates to lower the output voltage accordingly. Therefore, in this situation, the supply current stage of the high gain buffer structure is designed not to operate. The input voltage of the high gain buffer structure according to the overshoot situation is sensed as a higher, and operates to increase the output voltage accordingly. Therefore, in this situation, the discharge current stage of the high gain buffer structure is designed not to operate. The high gain buffer structure supplies current in a switch mode during an overshoot situation. This is because if it is designed to supply current at all times, the problem of a significant increase in quiescent current occurs. Therefore, it is designed to effectively supply and discharge current depending on overshoot and undershoot situations. If $\Delta V_{out}$ occurs due to a change in the output voltage of the high gain buffer structure owing to an undershoot situation, a current is generated according to the change in $M_a$. Since the drain terminal of $M_a$ and the gate terminal of $M_b$ are connected, the amount of current change in $M_a$ can be expressed as $r_{oa}$. Because of this, only the current path at $r_{oa}$ is created even if the output voltage changes. The voltage at (1) is formed due to the current flow in $M_a$, and the voltage at $V_{b_{gate}}$ is formed by (2). Since $\Delta V_{out}$ $(1 + G_{ma} \times r_{oa})$ is equal to the $V_{b_{gate}}$ voltage, the amount of current change in $M_b$ can also be determined. (3) represents the amount of current change in $M_b$ according to the output voltage change. As the output voltage changes, the change in current can be observed through the current generated in $M_b$ and $r_{ob}$, and this value is expressed as (4). Therefore, as shown in (5), the output resistance was formed smaller than that of the conventional buffer structure.

$$V_{M_a} = G_{ma} \times \Delta V_{out} \times r_{oa} \tag{1}$$

$$V_{b_{gate}} = \Delta V_{out} + \Delta V_{out} \times G_{ma} \times r_{oa} \tag{2}$$

$$\Delta I_{b_{gate}} = \Delta V_{out}\,(1 + G_{ma} \times r_{oa}) \times G_{mb} \tag{3}$$

$$\Delta I = \Delta V_{out}\,(1 + G_{ma} \times r_{oa}) \times G_{mb} + \frac{\Delta V_{out}}{r_{ob}} \tag{4}$$

$$R_{out} = \frac{1}{\left((1 + G_{ma} \times r_{oa}) \times G_{mb} + \frac{1}{r_{ob}}\right)} \tag{5}$$

Conversely, in an overshoot situation, when $\Delta V_{out}$ occurs due to a change in the output voltage of the high-gain buffer structure, the $M_c$ current is generated according to the change in $M_a$. Unlike the undershoot situation, the change in gate voltage of $M_c$ due to the current change in $M_d$ is expressed as (7). As the output voltage changes, the change in current can be observed through the current generated in $M_c$, $r_{oc}$, and $r_{ob}$, and this value is expressed as (8). As a result, as shown in (9), depending on the overshoot situation, the output resistance was formed to be smaller than that of the conventional buffer structure.

$$V_{bgate} = \Delta V_{out}\,(1 + G_{ma} r_{oa}) \tag{6}$$

$$V_{cgate} = \{(1+G_{ma} r_{oa})\,\Delta V_{out} + G_{md} r_{od}\,(1+G_{ma} r_{oa})\,\Delta V_{out}\} \tag{7}$$

$$\Delta I = G_{mc}\,(1+G_{ma} r_{oa})\,(1+G_{md} r_{od})\,\Delta V_{out} + G_{mb}\,(1 + G_{ma} r_{oa})\,\Delta V_{out} + \frac{\Delta V_{out}}{r_{ob}} + \frac{\Delta V_{out}}{r_{oc}} \tag{8}$$

$$R_{out} = \frac{1}{\frac{1}{r_{ob}} + \frac{1}{r_{oc}} + G_{mb}\,(1+G_{ma} r_{oa}) + G_{mc}\,(1+G_{ma} r_{oa})\,(1+G_{md} r_{od})} \tag{9}$$

As is well known, the overshoot and undershoot due to load current occurring in a conventional LDO regulator are proportional to the overall gain of the system, as shown in Fig 5, indicating high gain of the system under no-load conditions. However, depending on the size of the load current, $A_v$ becomes $G_m \times R_{out}$, so unlike the proposed LDO regulator, Rout according to the load current remains $r_o \left| \left(R_{f1} + R_{f2}\right) = r_o \right.$. Therefore, the gain due to system stability decreases and the offset voltage increases, which directly affects overshoot and undershoot. Therefore, in order to improve the stability of the system according to the load current of the conventional LDO regulator, stable power supply will be possible by increasing the loop gain and reducing the bandwidth trade-off. For this purpose, the proposed LDO regulator was designed in three stages to further increase the gain and provide sufficient compensation. Accordingly, it was designed to improve the peak value of undershoot/overshoot voltage caused by instantaneous and rapidly changing load current. In other words, to enhance the transient response of the output voltage, a high gain buffer structure and a pole-split compensation capacitor, which can compensate by adjusting the UGBW according to the load current, was applied to the proposed LDO regulator. As a result, the proposed 3-stage gain level LDO regulator not only maintains high gain and stability against load current fluctuations but also provides additional current to the output terminal. The voltage at the output stage is designed to turn on/off according to changes in the undershoot/overshoot voltage of the LDO regulator, allowing for an additional current pass. While the input voltage of the error amplifier in the conventional LDO regulators is at the cathode terminal, the proposed LDO regulator applies the feedback voltage of the anode terminal of the error amplifier to amplify the gain. Consequently, the error amplifier of the suggested LDO regulator is positioned to perform normal feedback by inverting the output generated in the next stage. Thus, it has a higher gain value than the error amplifier of conventional LDO regulators. Additionally, the R1 and R2 resistors of the error amplifier of the proposed LDO regulator are fixed resistors at the output stage, so the Y-axis gain can be changed without any problem by adding a resistor to reduce the $G_m$ of the input MOSFET.

Fig. 7 shows a schematic of a circuit designed in three stages to increase the gain in the proposed LDO regulator. The compensation capacitor applied in the proposed LDO regulator is connected between the output terminal and the drain terminal of the amplifier's input MOSFET, and between the drain terminal of the amplifier's input MOSFET and the output terminal of the second amplifier, compensating for it. Stability is ensured by maintaining high loop gain. Compensation capacitors are available in two sizes: 25pF and 280fF. Therefore, when the load current fluctuates, the proposed LDO regulator restores the output voltage through the feedback loop generated by the amplifier. Additionally, the output section of the proposed LDO regulator has been configured with a high gain buffer structure at the amplifier's output, simultaneously creating an additional current path. In the output voltage stage of the proposed LDO regulator, additional current is supplied to maintain an effective output voltage change. Conversely, an increase in the amplifier's output voltage means that an overshoot voltage has occurred due to the change in load current. Thus, an additional current discharge path can be created to achieve an effective output voltage change. Therefore, the proposed LDO regulator can maintain a more constant output voltage by including a discharge function and an additional current supply function [11], [12], [13], [14], [15], [16], [17], [18], [19].

### B. PROPOSED ESD PROTECTION CIRCUIT

Fig. 8 shows the ESD design window. ESD protection circuit has a defined ESD design window based on the applied voltage of the IC being protected, and must be designed for this window. This ESD design window represents the range between the power supply voltage and the gate oxide breakdown voltage of the IC being protected. An ideal ESD protection circuit should have the following characteristics. The trigger voltage (Vt1) should be set lower than the gate oxide breakdown voltage of the IC being protected. If the trigger voltage surpasses this breakdown voltage, the IC can suffer catastrophic damage because of oxide breakdown, leading to malfunctions. The holding voltage (Vh) should

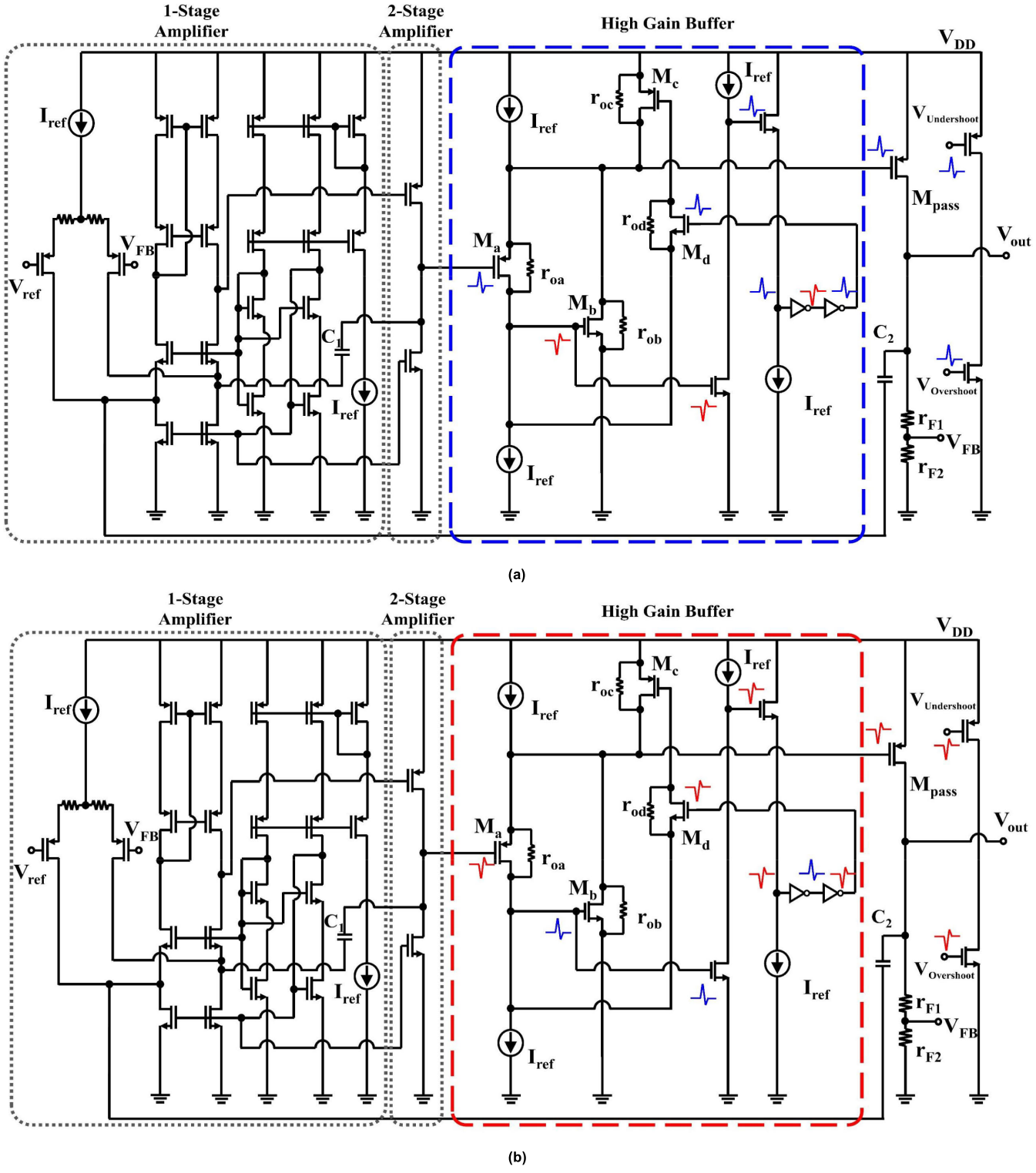


**FIGURE 7.** Schematic of (a) Overshoot and (b) Undershoot situations of the proposed LDO regulator.

be higher than the IC's supply voltage. If the maintenance voltage is lower than the supply voltage of the IC to be protected, the voltage that should be supplied to the internal IC is supplied to the ESD protection circuit, causing continuous current discharge. As a result, undesired current discharges, increasing power consumption. Moreover, this leads to issues

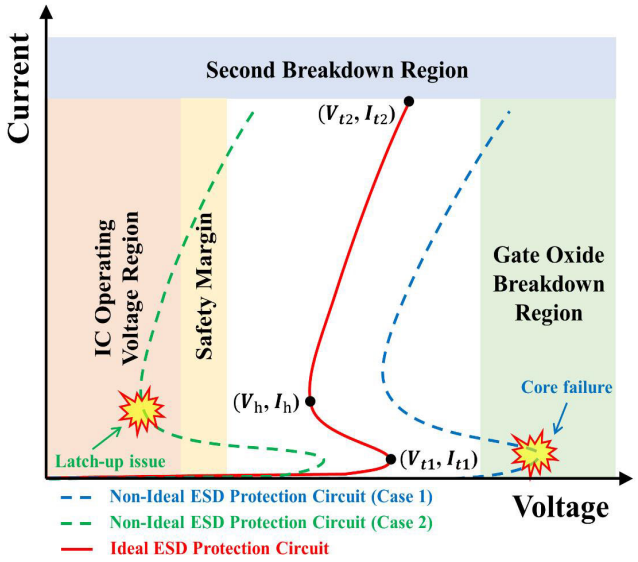


**FIGURE 8.** ESD design window of ESD protection device and main parameters.

such as input signal distortion and propagation delay, interfering with the normal operation of the IC. Therefore, the proposed ESD protection circuit ensures stable operation within the standard ESD design window and is optimized for 5 V class application.

Fig. 9(a) shows the structure and internal circuit diagram of Low Voltage Trigger SCR (LVTSCR). LVTSCR is a structure that adds a grounded gate NMOS (GGNMOS) to the conventional SCR. Due to this, the avalanche breakdown that previously occurred between the N-well and P-well now takes place between the N+ bridge region and the P-well. This results in a significant reduction in the trigger voltage by lowering the breakdown voltage. Fig. 9(b) shows the structure and internal circuit diagram of Low Ron SCR (LRSCR). LRSCR is a structure that adds P-well and P+ implant region to the left side of the LVTSCR structure shown in Fig. 9(a). The added P+ implant region is connected to the anode, turning on an additional parasitic PNP bipolar transistor. Due to this structure, the LRSCR included the characteristic of significantly lowering the trigger voltage of the LVTSCR, and the on-resistance component is reduced owing to the operation of the added parasitic PNP bipolar transistor (QPNP2). Fig. 9(c) shows the cross-sectional view and internal circuit of a new ESD protection circuit. The proposed ESD protection circuit is based on the floating SCR structure. This proposed circuit has added the N-Well, N+ implant region, and N+ bridge region to the right side. Additionally, a N+ floating region has been added. A feature of this structure is that the added N+ injection region is connected to the anode to turn on an additional parasitic NPN bipolar transistor. The proposed ESD protection circuit operates as follows. Due to the ESD surge from the anode region, the potential of the left and right N-well regions increases. When the threshold between the reverse-biased N+ bridge region and the P-well region is reached, avalanche breakdown occurs and electron-hole pairs are generated. The generated holes flow to the P+ cathode region, raising the potential of the P-well region. When a forward junction is formed between the P-well and the N+ cathode region, two parallel-connected parasitic NPN bipolar transistors (QNPN2, QNPN3) turn on. Additionally, the current passing through the parasitic NPN bipolar transistors turns on the parasitic PNP bipolar transistor (QPNP3). Thus, the three parasitic bipolar transistors (QNPN2, QNPN3, and QPNP3) create a SCR positive feedback loop and discharge a substantial amount of ESD surge. As a result, the proposed protection circuit operates with a parasitic NPN bipolar transistor (QNPN3) with a shorter discharge path and higher current gain in addition to the parasitic NPN bipolar transistor (QNPN2). The operation of the added parasitic NPN bipolar transistor (QNPN3) leads to a decrease in the on-resistance. Furthermore, the added floating region extends the base length of the parasitic PNP bipolar transistor (QPNP3), reducing the current gain ($\beta$) and increasing the holding voltage, making it optimized for proposed LDO regulator [24], [25], [26], [27], [28], [29], [30].

Fig. 10 shows the LDO block in conjunction with the proposed ESD clamp. The ESD clamp is connected to the VDD-VSS and VOUT-VSS of the proposed LDO regulator. Considering the operating voltage of the proposed LDO regulator, it was optimized for the 5V ESD design window. When an ESD surge is supplied to VDD or VOUT, the ESD clamp activates to allow for safe discharging. The ESD clamp is designed considering the operating voltage of the LDO regulator, and it is triggered before gate oxide breakdown and junction breakdown of the LDO internal circuit occur to discharge the ESD surge to the VSS, thereby ensuring normal operation of the proposed high gain buffer LDO regulator.

## III. SIMULATION RESULT

Fig. 11 shows the simulation result of the high gain buffer that affects the output terminal of the proposed LDO regulator. In an undershoot condition, where the output voltage is reduced, the output voltage can be more effectively controlled if a supply current is formed. Conversely, in an overshoot condition, where the output voltage rises, the output voltage can be effectively controlled if a discharge current is formed.

Fig.12 shows the phase margin result according to the presence or absence of a high gain buffer of the proposed LDO regulator. The conventional LDO regulator typically exhibited a phase margin and gain of 55 dB and 26°, respectively. However, the proposed LDO regulator has phase margin and gain of 91 dB and 57°, respectively. Consequently, it was found that the gain was boosted and the phase margin stability was enhanced simultaneously depending on the presence or absence of the designed high gain buffer structure in the proposed LDO regulator.

Fig. 13 shows the variation of the phase margin according to the presence or absence of the compensation capacitor in the proposed LDO regulator. The stability compensation of

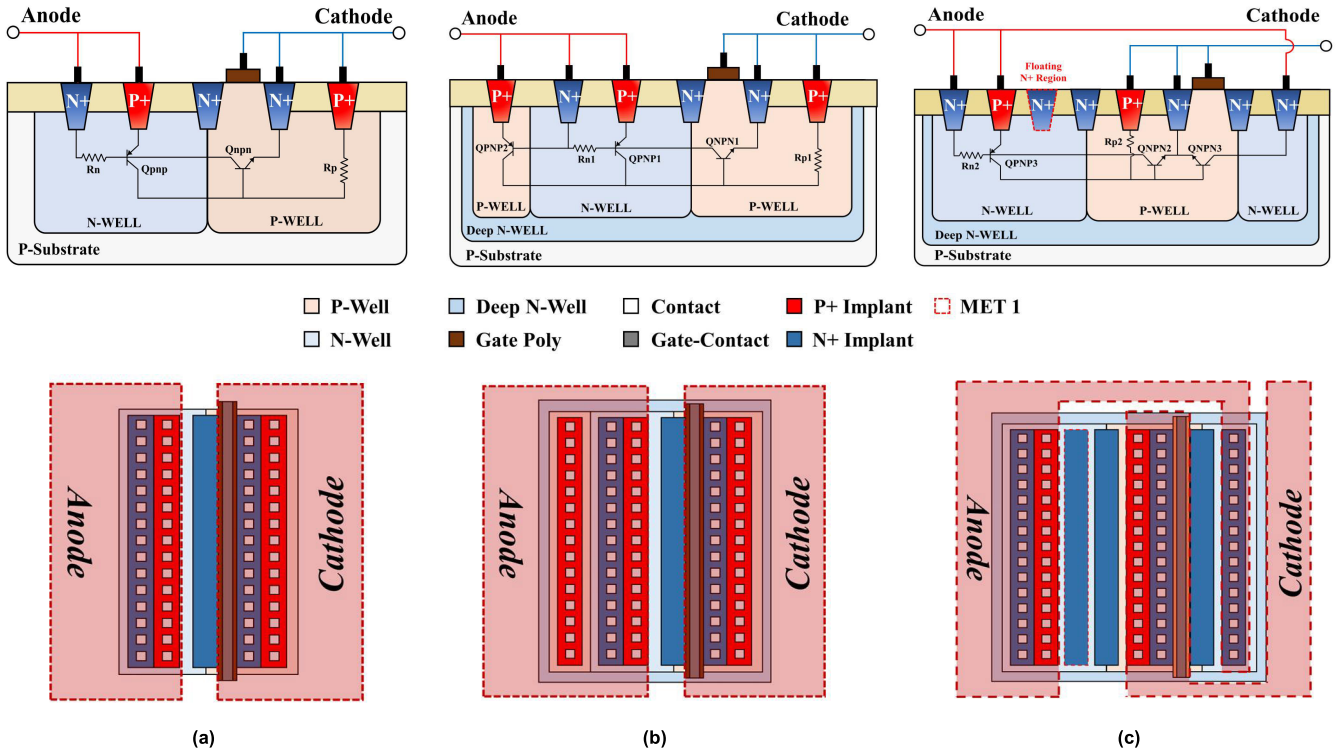


**FIGURE 9.** Cross-section and layout of the typical (a) LVTSCR, (b) LRSCR, (C) New-LRSCR (NLRSCR).

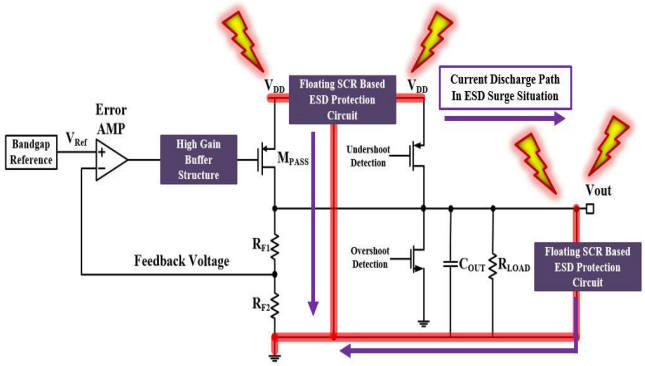


**FIGURE 10.** ESD current discharge path of LDO regulator when ESD occur.

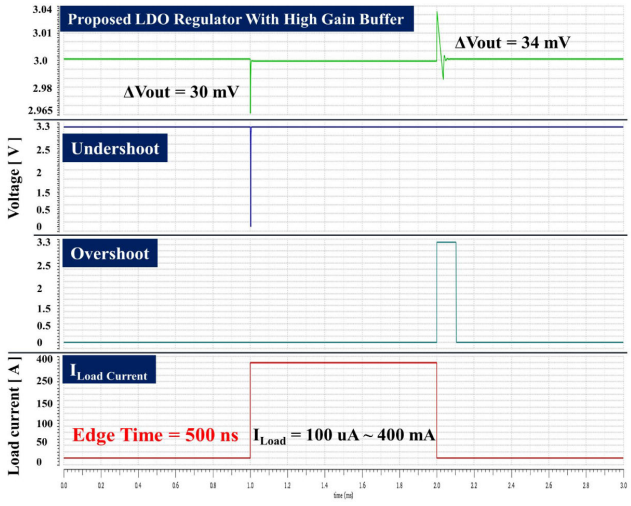


**FIGURE 11.** Load transient simulation result of the proposed LDO regulator.

the proposed LDO regulator was performed by pole splitting due to the compensation cap. The system stability of the LDO regulator was induced by dividing the poles of the two poles, which could easily overlap, using a compensation capacitor. When a 100mA load current was applied, the proposed LDO regulator shifted the pole to a high frequency range using the compensation capacitor, and as a result, the stability for high loop gain was compensated. If the load current is not large, the degree of compensation of the compensation capacitor may not be meaningful. However, a larger compensation of the compensation capacitor is predicted because the proposed LDO regulator is designed to endure large load currents.

Fig. 14 shows the variation in the phase margin according to the load current applied to the proposed LDO regulator. The LDO regulator requires stability; thus, its stability must be verified under every load condition. The regulator is designed to endure large load currents. The proposed LDO regulator is designed to endure large load currents. The simulation about the AC stability of the proposed LDO regulator was performed under the load current conditions of 0, 100, 300, and 400 mA. The phase margin obtained by simulation maintained 57° at 0 mA, 86° at 100 mA, 86° at 300 mA, and 85° at 400 mA. This result confirmed that the proposed LDO regulator operated stably under light and heavy load conditions.

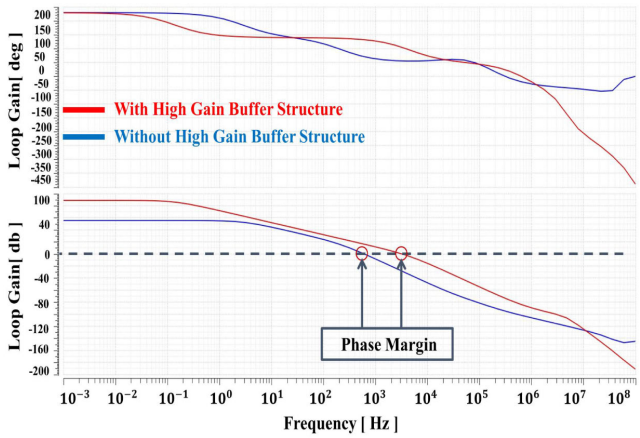


**FIGURE 12.** Phase margin of the proposed LDO regulator.

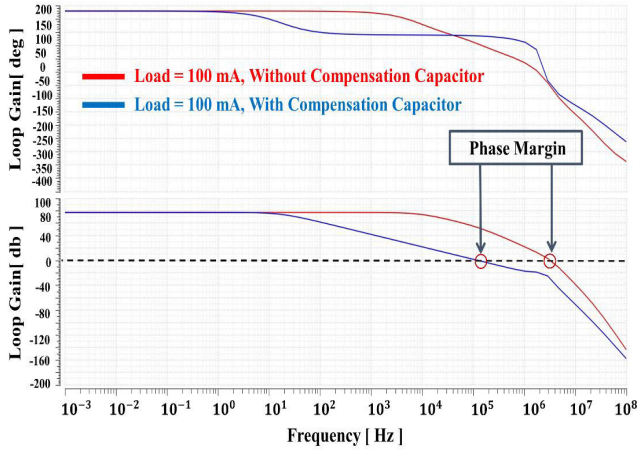


**FIGURE 13.** Phase margin according to the presence or absence of a compensation capacitor of the proposed LDO regulator.

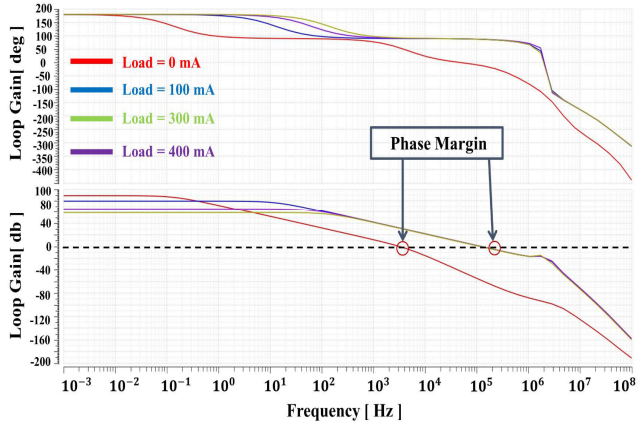


**FIGURE 14.** Phase margin according to the load of the proposed LDO regulator.

## IV. MEASUREMENT RESULT

### A. LAYOUT OF THE PROPOSED LDO REGULATOR

Fig. 15 shows a photograph of the actual chip and layout of the proposed LDO regulator. The proposed LDO regulator has dimensions of 450 × 372 um. Furthermore, the ESD protection circuit was applied to the VOUT-VSS and VDD-VSS.

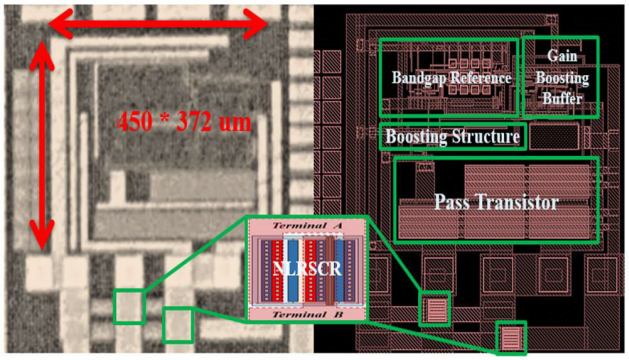


**FIGURE 15.** Layout of the proposed LDO regulator.

### B. LOAD TRANSIENT RESPONSE

The primary function of the LDO regulator is to deliver a stable output voltage, independent of variations in load current. However, in mobile applications, the output voltage can be influenced by the load level. Furthermore, the load transient response is characterized by maintaining a constant output voltage despite swift load fluctuations at the output terminal. The proposed LDO regulator minimized the fluctuations of the output voltage according to the load current by maximizing the gain and controlling the UGBW. It can be confirmed through measurement that the overshoot and undershoot formed by the load current generated in the LDO regulator with a high gain buffer structure is proportional to the total gain of the system. The measurement results of the proposed LDO regulator are shown after performing the ESD zapping test. ESD zapping testing is an important process for evaluating the durability and reliability of devices and products because ESD causes fatal damage to electronic devices and products. This test was conducted to mimic ESD based on the standard ESD modelling, the Human Body Model (HBM). During testing, the LDO regulator was subjected to a total of three times positive ESD stresses at 1-second intervals at sequential voltage levels of 2 KV, 4 KV, 6 KV, and 8 KV. As a result, there was no difference in the performance of the LDO regulator before and after the ESD zapping test, confirming that it can reliably respond to the ESD stress of HBM 8 KV. Therefore, the proposed LDO regulator has high durability and reliability.

Fig. 16 shows the output voltage change under undershoot and overshoot conditions when the load current suddenly changes to 200 mA, as 18 mV and 9 mV, respectively. As shown in Fig. 17, the transient response characteristics of a LDO regulator in non-integrated with ESD protection circuit. It can be seen that a LDO regulator without an ESD protection circuit cannot maintain a stable voltage due to the destruction of internal elements due to ESD surges. Due to the ESD phenomenon, the output voltage of the LDO regulator dropped to 1.8 V, a decrease of 1.2 V. As a result, it can be seen that normal regulation operation has become difficult due to damage to the internal elements. Fig. 18 shows the output voltage according to load current changes under undershoot and overshoot conditions. Fig. 19(a) shows the output voltage

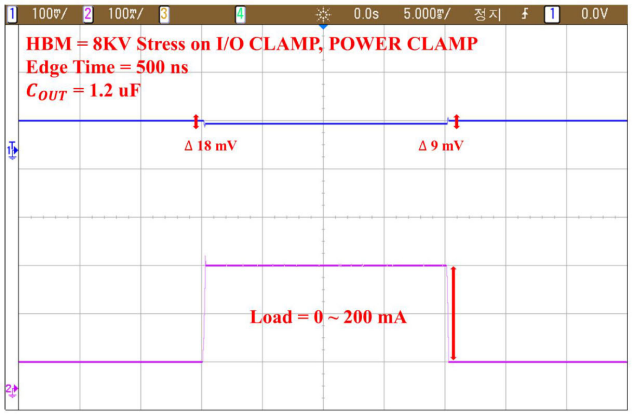


**FIGURE 16.** Load transient response measurement result of the proposed LDO regulator in integrated with ESD protection circuit.

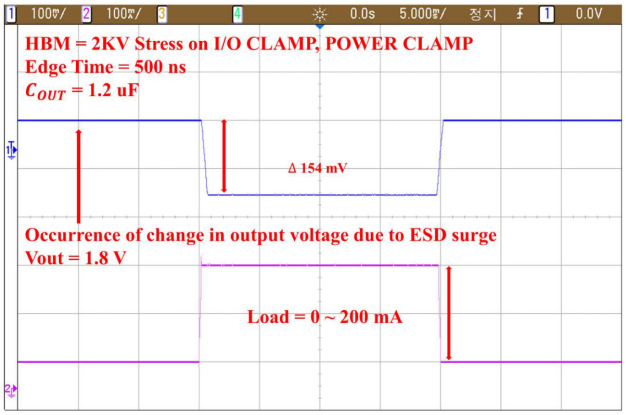


**FIGURE 17.** Load transient response measurement result of the proposed LDO regulator in non-integrated with ESD protection circuit.

change under undershoot and overshoot conditions as 26 mV and 24 mV, respectively, when the load current momentarily changes to 300 mA. Additionally, Fig. 19(b) shows that the improved output voltage of 32 mV and 36 mV is maintained under undershoot and overshoot conditions, respectively, when the load current changes rapidly to 400 mA. In a typical LDO regulator, a large peak voltage change occurs when a large load current changes, but the proposed LDO regulator showed that the peak voltage change at a large load current can be effectively improved by using a high gain buffer structure. As a result, the proposed LDO regulator's high gain buffer structure forms a system that can additionally turn the current on and off along the conventional current path and establish a system that can adeptly regulate the power voltage. Additionally, the integrated ESD protection circuit in the proposed LDO regulator effectively discharges ESD surges even under significant ESD conditions of HBM = 8 KV, and it was verified that this does not affect the output voltage of the LDO regulator based on load current variations.

### C. LOAD REGULATION

Fig. 20(a) shows the load regulation measurement results of the proposed LDO regulator. Load regulation refers to the amount of change in output voltage as the load current continues to increase. It was verified that the LDO regulator in non-integrated with ESD protection circuit was unable to discharge an ESD surge of HBM = 2 KV and therefore failed to perform normal regulation operation. However, when the ESD protection circuit was integrated, normal regulation was confirmed by discharging the ESD surge of HBM = 8 KV. As a result, the proposed LDO regulator was validated to have an output voltage change of 7.42 mV at a load current of 0 to 400 mA.

### D. LINE REGULATION

Fig. 20(b) shows the line regulation measurement results of the proposed LDO regulator. Line regulation allude to the amount of change in output voltage when the input voltage changes. It was proved that the LDO regulator in non-integrated with ESD protection circuit was unable to discharge the ESD surge of HBM = 2 KV and thus did not perform normal regulation operation. However, when the ESD protection circuit was integrated, normal regulation was affirmed by discharging the ESD surge of HBM = 8 KV. As a result, the proposed LDO regulator was validated to have an output voltage change of 4.38 mV at an input voltage of 3.3 V to 4.5 V.

### E. QUIESCENT CURRENT

The quiescent current denotes the minimum input current that a LDO regulator needs to sustain a constant output voltage. Due to limited battery capacity, large amounts of current continuously consumed within the system can adversely impact battery longevity. Especially since the PMIC system consists of dozens of circuits, current consumption can be an important issue. As such, an excessively high quiescent current can undermine the battery's efficient usage. Fig. 21(a) shows the quiescent current of the proposed LDO regulator. If the ESD protection circuit is not integrated, the proposed LDO regulator not only fails to operate normally due to internal element destruction due to HBM = 2 KV ESD surge, but also increases the quiescent current. In contrast, the proposed LDO regulator in integrated with ESD protection circuit was confirmed to operate normally by discharging the ESD surge of HBM = 8 KV. As a result, over the input voltage range of the LDO regulator, the quiescent current was observed to be a maximum of 41 $\mu$A and a minimum of 38 $\mu$A.

### F. TEMPERATURE CHARACTERISTICS

Temperature characteristics are directly related to reliability. If the proposed LDO regulator reacts sensitively to temperature fluctuations between −40 °C and 140 °C, situations may arise where it's unable to stably control the output voltage. Hence, temperature characteristics are vital for ensuring high reliability. Fig. 21(b) shows the temperature characteristics of the proposed LDO regulator. For thermal reliability testing, the wafer was heated using a Hot Chuck Controller, and the temperature characteristics of the LDO regulator was measured. it was noted that the LDO regulator in non-integrated with ESD protection circuit failed to provide normal temperature characteristics even under minor ESD conditions of

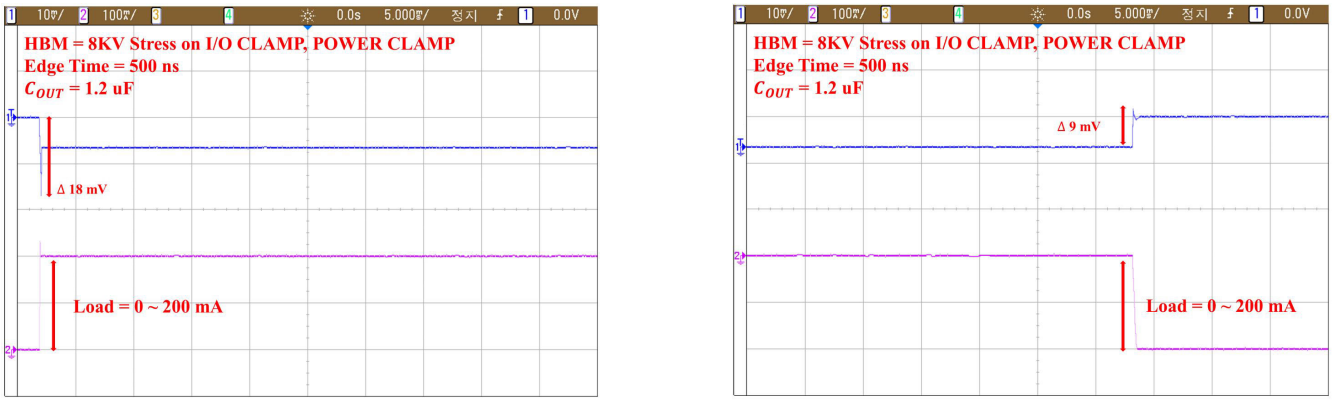


**FIGURE 18.** In (a) Undershoot condition, (b) Overshoot condition, load transient response measurement result of the proposed LDO regulator.

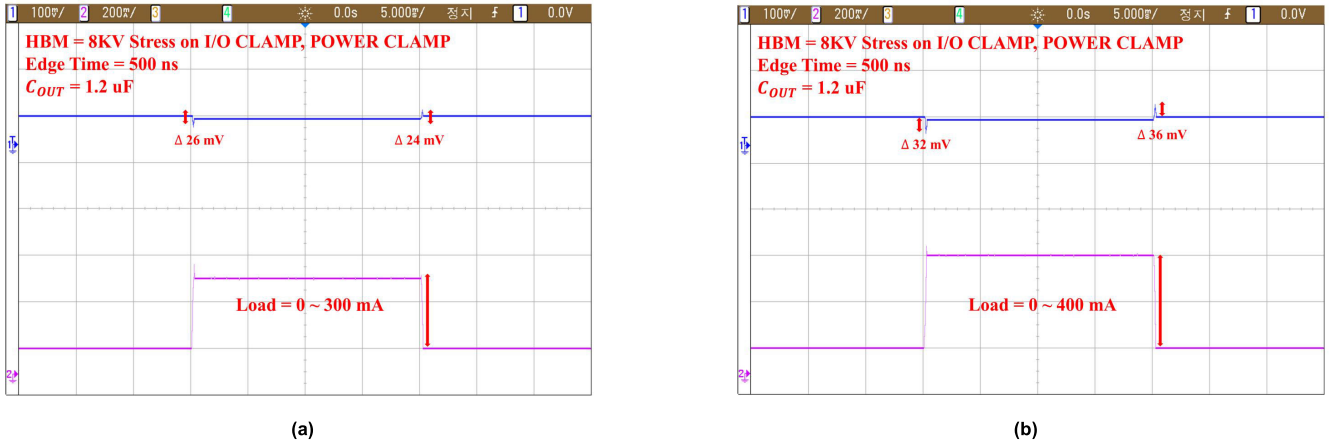


**FIGURE 19.** Load transient response of the proposed LDO regulator (a)$I_{Load}$ = 300 *mA*, (b) $I_{Load}$ = 400 *mA*.

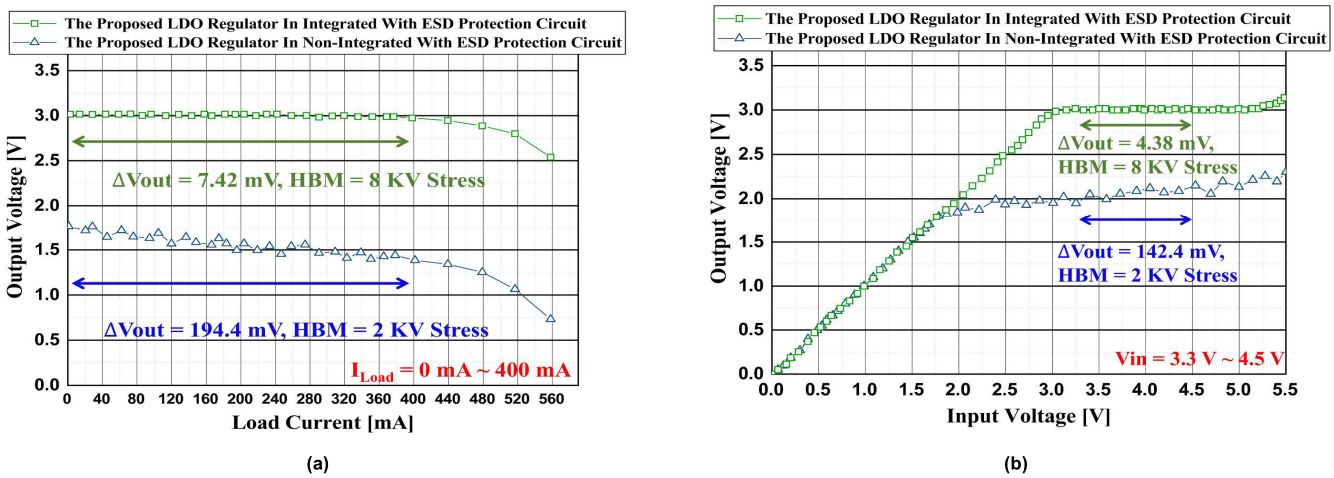


**FIGURE 20.** Measurement result of the proposed LDO regulator (a) Load regulation, (b) Line regulation.

HBM = 2 KV. Conversely, the LDO regulator in integrated with the proposed ESD protection circuit maintained stable output voltage according to temperature characteristics even under substantial ESD conditions of HBM = 8 KV. Therefore, The amount of change in output voltage of 2.68 mV was observed over the temperature range of −40 °C to 140 °C. As a result, confirm that the proposed LDO regulator ensures stable output voltage control and reliability according to temperature changes.

### G. ESD CHARACTERISTICS EVALUATION

Fig. 22 shows the results of measuring I-V characteristics using TLP, through which the electrical characteristics of the proposed ESD protection circuit are compared and verified

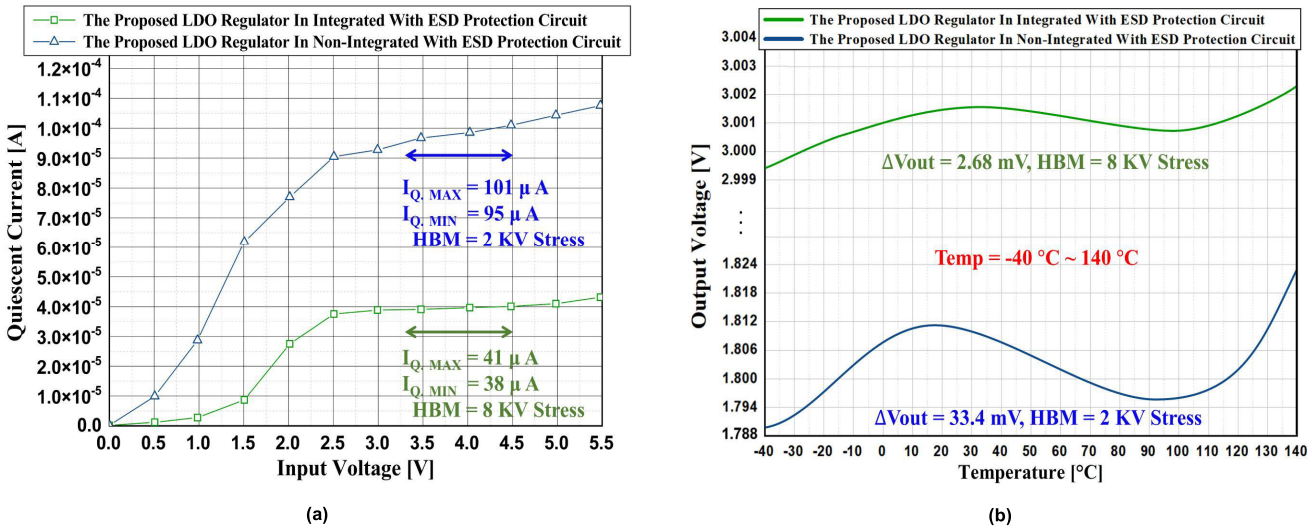


**FIGURE 21.** Measurement result of the proposed LDO regulator (a) Quiescent current, (b) Temperature characteristics.

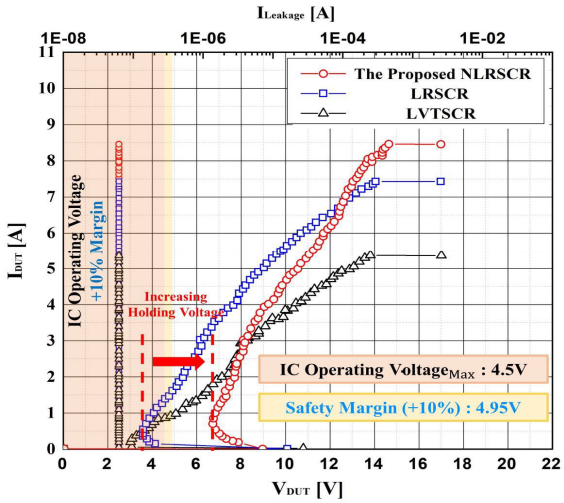


**FIGURE 22.** TLP I–V curves of the LVTSCR, LRSCR and the proposed NLRSCR ESD protection circuit.

against LVTSCR, LRSCR. For integration into the proposed LDO regulator, the holding voltage of the ESD design window must exceed 4.95 V (maximum operating voltage of the proposed LDO regulator + 10% margin). The holding voltage of LVTSCR is 2.94 V and that of LRSCR is 3.7 V, which may encroach upon the operating region of the internal IC, leading to issues such as latch-up. However, the holding voltage of the proposed ESD protection circuit is 6.76 V, providing latch-up immunity characteristics. Additionally, upon comparing the trigger voltages, the trigger voltages for LVTSCR and LRSCR are 10.8 V and 9.88 V, respectively, and the proposed ESD protection circuit stands at 8.95 V, which is lower than that of the conventional ESD protection circuit. Therefore, the proposed ESD protection circuit is suitable for integration into the targeted proposed LDO regulator, ensuring stable operation and enhanced reliability.

The reason ESD protection circuit is essential in IC circuits is due to reliability. In the semiconductor market, reliability is not only a concern at the individual device level but also a critical aspect at the broader IC level. If reliability issues related to ESD are not resolved in IC, frequent malfunctions due to ESD will occur in all electronic devices. This is a concern both in terms of cost and the future of the semiconductor market. Therefore, ESD protection circuit needs the ability to protect internal circuits in both minor and severe ESD conditions, while also being able to discharge large currents in a small area. Diodes, with their simple structure and ease of design, serve as ESD protection circuit, but have the disadvantage of large size. Fig. 23(a) and (b) compare the areas of various ESD protection circuit in ESD situations of HBM 2 KV and HBM 8 KV, respectively. Total Size (1) represents the area of a diode operating stably, Total Size (2) represents the area of a diode operating uncertainly, and Total Size (3) represents the area of the proposed ESD protection circuit. In Fig. 23(a), The area of Total Size (1) compared to Total Size (2) decreased by 66%, and the area of Total Size (2) compared to Total Size (3) decreased by 90%. In Fig. 23(b), the area of Total Size (1) compared to Total Size (2) decreased by 66%, and the area of Total Size (2) compared to Total Size (3) decreased by 91%.

As a result, it can be seen that the ESD protection circuit to be integrated into the LDO regulator, where minimizing chip size is important, is designed to have an effectively small area. Since the chip size is incomparably smaller than that of a diode, it was confirmed that it cannot be replaced in terms of area efficiency. The proposed ESD protection circuit secures HBM 8 KV robustness characteristics with much less area compared to conventional diodes. To respond ESD phenomena in LDO regulators, the proposed ESD protection circuit utilizes I/O clamps and power clamps to prevent ESD current from entering the internal circuit and discharges the ESD current through the VSS pin, protecting circuit stably. Such a design increases the efficiency of ESD protection circuit while simultaneously minimizing chip size, thus enhancing space and cost efficiency.

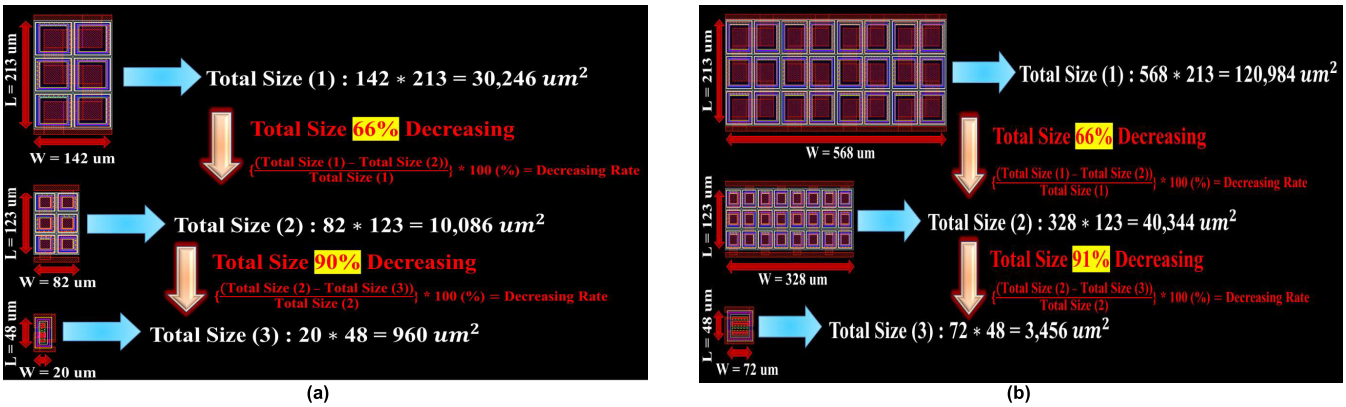


**FIGURE 23.** Comparison of the size of the proposed ESD protection circuit and diode in (a) HBM 2 KV, (b) HBM 8 KV.

**TABLE 1.** Performance comparison and summary with proposed LDO regulator.

| | This work | [1] | [2] | [3] | [4] | [5] | [6] | [7] | [8] | [9] |
|---|---|---|---|---|---|---|---|---|---|---|
| Technology ($\mu$m) | 0.18 | 0.18 | 0.13 | 0.35 | 0.065 | 0.065 | 0.13 | 0.13 | 0.065 | 0.18 |
| Supply Voltage(V) | 3.3-4.5 | 1.2-1.8 | 1.2-1.5 | 2.3-3.3 | 0.75-1.2 | 0.75-1.2 | 1.2-1.5 | 1.05-2 | 0.95-1.2 | 3.3 |
| Output Voltage (V) | 3 | 1 | 1 | 1.2-2.5 | 0.5 | 0.55 | 1 | 0.7-1.3 | 0.8 | 3 |
| Load Current: $I_{MAX}$ (mA) | 400 | 100 | 100 | 1 | 50 | 50 | 50 | 300 | 100 | 350 |
| Quiescent Current (µA) | 43 | 0.6-6.9 | 6.2 | 0.25 | 16.2 | 15.9-487 | 42 | 14 | 14 | 29 |
| Load Transient ($I_{LOAD}$ Rising) (mV) | 32 | 388 | 234 | 160 | 103 | 51 | 140 | 56 | 230 | 30 |
| Load Transient ($I_{LOAD}$ Falling) (mV) | 36 | 200 | 170 | 93 | 100 | 42 | 80 | 24 | 133 | 33 |
| Load Regulation (mV) | 8 | 1 | - | 1.8 | 20 | 9 | 0.5 | 1.8 | 9 | 11 |
| Line Regulation (mV) | 5.8 | 9 | - | 0.561 | 13.2 | 4.8 | 0.45 | 0.88 | 14.4 | 9 |
| COUT (µF) | 1.2 | 0-0.0001 | 0-1 | 0-0.001 | 0-0.0001 | 0.01 | 0-0.0004 | 1 | 0-0.0001 | 100E-6 |
| FoM(1) (V) | 1.94E-12 | 2.68E-12 | 1.45E-11 | 3.04E-12 | 3.34E-12 | 4.97E-11 | 1.18E-11 | 2.61E-12 | 7.08E-12 | 1.37E-12 |
| FoM(2) (V) | 6.29E-14 | 8.68E-14 | 2.45E-13 | 3.72E-13 | 1.41E-14 | 2.10E-13 | 1.99E-13 | 4.41E-14 | 2.99E-14 | 4.43E-14 |
| Year | 2024 | 2022 | 2022 | 2017 | 2014 | 2014 | 2018 | 2017 | 2019 | 2022 |

$FoM(1) = \frac{\Delta t_{edge} \times \Delta V_{out} \times I_q}{\Delta I_{load}}$, $FoM(2) = \frac{\Delta t_{edge} \times \Delta V_{out} \times I_q}{\Delta I_{load} \times Technology^2(\mu m)}$ [1]

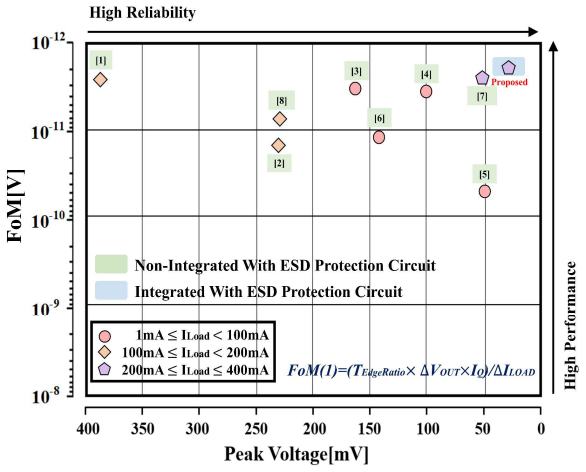


**FIGURE 24.** Comparative analysis of reliability and performance between the proposed LDO regulator and conventional LDO regulators.

Fig. 24 shows the peak voltage and figure of merit (FoM) of the proposed LDO regulator constructed with a high gain buffer structure. FoM is an important metric to measure the performance of a LDO regulator from a balanced perspective, considering both reliability and performance. Comparative analysis considering the FoM values demonstrates that the proposed LDO regulator not only outperforms conventional regulators but also provides high ESD protection, ensuring high reliability even in potential ESD events. As a result, the design of the proposed LDO regulator with the configuration of high gain buffer structure and integration of ESD protection circuit has very good potential in terms of performance, reliability, efficiency and cost in power electronics field. Additionally, as shown in Table 1, the proposed LDO regulator can be compared with conventional LDO regulators. The high gain buffer output resistance of the proposed LDO regulator was designed to be effectively lowered. It is designed to have a much lower output resistance than a conventional buffer in an undershoot situation and at the same time lower the output resistance even more in an overshoot situation at the gate node of the pass transistor to effectively improve current driving ability. As a result, it can be confirmed that the proposed LDO regulator effectively controls the peak voltage value according to the load current.

## V. CONCLUSION

This study aimed to contribute to the extension of battery life by applying a bias to the high gain buffer structure to maintain a constant output voltage by handling the peak voltage of the output voltage generated in the LDO used in highly integrated and miniaturized mobile devices. This study also aimed to evaluate the performance of the proposed LDO regulator using electro-static discharge technology. Furthermore, protection against ESD phenomena in actually used IC is closely related to reliability. If the operating region of the IC is invaded by ESD surge, the appropriate IC voltage that must be supplied cannot be provided to each system. Because high reliability is indispensable in IC design, the ESD protection circuit was set up in the I/O and Power clamps of the proposed LDO regulator to provide high reliability. The LDO regulator incorporating the ESD protection circuit fabricated with the chip used in this study was verified to maintain a constant output voltage in the ESD condition. The proposed high gain buffer LDO regulator was found to maintain small peak voltages of 32 mV and 36 mV in the undershoot and overshoot conditions in mobile applications sensitive to load current. Moreover, the current of the output terminal could be simultaneously increased or decreased according to the load change using the high gain buffer structure that was additionally installed. As a result, the proposed LDO regulator demonstrated that the high gain buffer structure, which is a new control path, kept a constant output voltage even when a relatively high load current of 400 mA was rapidly applied. Furthermore, the proposed LDO regulator circuit with an ESD protection circuit of the NLRSCR structure provided high reliability by maintaining low peak voltages irrespective of the load current. Previously, LDO regulators were classified as IC, and ESD protection circuit was classified separately as single-element configurations. The reason ESD protection circuit is essential in IC circuits is for reliability. Additionally, the reason why LDO regulators are essential in circuit design is because they can provide stable voltage. Therefore, in electronic devices that are actually used, IC and ESD protection circuit must be designed as an integrated system to ensure the reliability of electronic devices and IC routinely used in the semiconductor market. In this paper, an ESD protection circuit was built into the LDO regulator to not only provide a stable voltage but also achieve high reliability in ESD situations. Consequently, the proposed LDO regulator was proven to be suitable for smooth operation of mobile applications requiring sensitive voltage control. In addition, as we are directly faced with reliability and stability issues associated with IC damage and failure due to ESD, the NLRSCR ESD protection circuit was applied to the proposed LDO regulator, thereby achieving excellent robustness and high reliability over 8 kV for HBM.

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