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RESEARCH ARTICLE

Load and Generation Converters Control Strategy to Enhance the Constant Power Load Stability Margin in a DC Microgrid

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ABSTRACT Integrating Constant Power Loads (CPL) in a DC microgrid generates a virtual negative impedance that may lead to system instability. CPL deteriorates the system damping, which is more severe for the DC power system with large line impedances. This paper proposes a novel and simple virtual negative resistance-based control loop for the DC-DC converters connected at both source and load ends to enhance the CPL stability margin in a DC microgrid. The proposed control scheme includes a simple pole-zero criterion to evaluate the virtual negative resistance. Further, small-signal and extended large-signal models of the bidirectional DC-DC converters are developed to calculate stabilizer parameters and assess system stability with CPL. These models effectively calculate optimal stabilizer parameter values using simple root locus analysis. A comparative stability analysis is conducted to illustrate the system's resilience in the face of changes in parameter values and considerable enhancement of the stability margin. The eigenvalue analysis and time domain simulations are performed with the proposed control strategy at the source and load side converters without affecting the load side voltage profile to demonstrate its effectiveness.

INDEX TERMS Constant power loads, DC microgrid, negative resistance control, stability, virtual negative impedance droop.

I. INTRODUCTION

In the recent past considerable efforts have been implemented for harnessing renewable energy sources (RES) to establish a sustainable and cost-effective means to enhance last-mile connectivity and reduce the stress on grid transmission. The RES are direct current (DC) in nature and connected to the grid through power electronics converters (PEC). In order to enhance efficiency, flexibility and controllability, DC microgrids (DCMGs) are more effective [1]. Apart from diversified distributed sources, DCMGs consist of different types of loads. These diversified components in a system demand efficient control strategies for a smooth and stable operation [2], [3]. Especially, DCMG with the integration of constant power loads (CPLs) has a major concern of the system stability due to the negative impedance characteristics of CPL. CPL introduces negative impedance into the system which in-turn to reduce the system damping and hence stability. It is essential to assess the CPL stability of the DC microgrid [4].

In [5], the fundamental voltage, current and power loop modelling is discussed for inverters at DC sources. It focused on power-sharing among the DGs in islanded mode, but the stability criterion must be verified properly. The authors in [6] deal with the parallel operation of DGs using droop control techniques without sufficient stability margin. Moreover, in [7], the droop control method is proposed for sharing the power among the inverter-based generators. The stability criterion for AC microgrid with CPL is given in [8]. For these problems, physical dampers are introduced to increase

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the system damping capability. This is a passive damping method where a large capacitor or resistor is deployed [9]. In [10], a two-layer control structure has been proposed for regulation of DC microgrids. It has a complex cascaded structure and estimation based analysis. In [11], a T-S fuzzy model approach has been used to investigate the large signal stability of the DC microgrid with various loads. In this paper small signal model of DC microgrid is not consider. The damping effect in DCMGs is realized in Aircraft, ships and space shuttles. Research is happening in these domains, but finding the solution for the stabilization and sharing of loads, especially the CPL loads needs to be more comprehensive. The instability caused by CPL is discussed in [12]. The paper [9] discusses the stability criterion used for the DCMGs analysis. The primary stabilization techniques with CPL using small signal stability criterion have been developed in [13], [14], [15], [16], [17], [18], [19], and [20]. Almost all methods have been implemented at the source side converter, except [16], where sufficient stability criteria for the DCMGs are discussed. This criterion can be used to design efficient controllers for AC and DC microgrids. Controlling at the source side may limit the flexibility of the microgrid because the control system only has access to the sources, such as RESs, and cannot directly control the loads. In [16], the author has proposed a controller for the load-side converter. Similarly, a robust passivity-based control (PBC) strategy has been proposed to solve the instability problem in the DC microgrid caused by the CPLs [21]. Large signal stabilization techniques are used in [22] and [23] to implement an adaptive Adaptive PBC for DC-DC buck converters that feed paralleled CPL and R loads. In these PBC methods, adaptive covariance matrices, which demand the proper tuning, are used. The secondary stabilization techniques are used in [24]. Tertiary control techniques are developed in [25] and [26]. A large signal stability analysis of an AC microgrid using a distributed control algorithm is given in [27]. In this paper, CPL impacts are ignored. Recently, Machine Learning algorithms have also been proposed for stabilization [28] of CPLs in microgrids.

In recent past, various non-linear control methods are proposed for stabilising DC microgrids having CPLs. Most controllers are implemented on source-side converters and have complicated parameter calculations. A simplified solution to the stability problem in the DC microgrid system caused by CPL is a challenging and recent demand due to an increase in converter-based sources and loads (like CPL). The main objectives of this work include demonstrating a simplex method for assessing and improving the stability and developing a controller that can be implemented for DC-DC converters connected at source and load ends.

A. CONTRIBUTIONS

Source-side control limits the system's flexibility and responsiveness to changes in load conditions. It also reduces the control over load voltage regulation. Since the source-side controllers are centralized, adapting to dynamic load variations or incorporating new loads may be challenging. Source-side controllers are less efficient and demand robust communication infrastructure to regulate the power flow and stability. In contrast, a load-side control enables effective load management and voltage regulation in a DC microgrid. The load-side converter can actively respond to changes in load demand, allowing for load shedding or load restoration as needed. This flexibility in load management improves the overall system efficiency and ensures stable operation. Load side control facilitates to accommodate more renewable energy sources in a DCMG. Also, it is easy to actively manage the power flow between the distributed RESs, energy storage systems, and loads. Therefore, this paper proposes a flexible control strategy that can effectively be implemented on source and/or load-side DC-DC converters.

The major contributions of this paper can be given as:

- Mathematical models (Small-signal and large signal) for CPL and a novel virtual resistance-based control loop to evaluate the stability of DC microgrid.
- Load side as well as source side control strategies to enhance the CPL stability margin of the microgrid
- State space model for extraction of stable modes under different droop values
- Real-time simulations for controlling boost converters at the source side and buck converters at the load side to ensure the voltage regulation and CPL stability of DCMG

The suggested loop maintains the droop characteristics established at the source side to facilitate power sharing among sources without any interference. The stabilization strategy we propose can seamlessly integrate into both the load-side and source-side converters, ensuring minimal impact on terminal voltage reduction, in contrast to conventional droop control techniques. The proposed control strategy is flexible enough to implement on source or load-side converters. It maintains the droop characteristics established at the source side to facilitate power sharing among sources without any interference. The stabilization strategy we propose can seamlessly integrate into both the load-side and source-side converters, ensuring minimal impact on terminal voltage reduction, in contrast to conventional droop control techniques.

The remaining paper is organized as follows: Section II deals with the modelling of components in DC microgrid. Stability criterion are discussed in Section III. In Section IV, evaluation of controlling parameters and proposed virtual negative inductance control strategies are described. The numerical simulations based on proposed control strategy are conducted in Section V to validate its effectiveness for CPL stabilization in a DC microgrid. Final conclusions and future scopes are given in Section V.

II. MODELLING OF DC MICROGRID SYSTEM

The effective mathematical modelling of individual microgrid components (loads, converters, sources, etc.) is essential for analysing system behaviour in real-time operating

scenarios. There are two types of modelling: small signal and large signal. Small-signal modelling is where the models are linearised around an operating point for stability and control analysis. In contrast, the large signal modelling is non-linear and includes an exact model of the individual components.

A. SMALL SIGNAL MODEL OF CPL

Although many types of load can exist in a DCMG system, some loads are tightly controlled by PECs and draw constant power irrespective of the system voltage. These constant power loads (CPL) introduce negative impedance in the system, which may impact the stability margin of the DCMG system. In this paper, the stability of CPL in a DCMG is considered. Mathematical model of the CPL can be given as

$$P_{CPL} = V_{load} \times I_{load} = Constant \tag{1}$$

where

V_{load} = CPL load terminal voltage
I_{load} = CPL load current
P_{CPL} = power drawn by CPL

The straight line passing through the operating point (V_{load},I_{load}) is given below,

$$slope = \frac{\partial V_{load}}{\partial I_{load}} = R_{CPL} = -\frac{V_{load}^2}{P_{CPL}} \tag{2}$$

$$V = slope * I + C \tag{3}$$

At the operating point eq (3) can be written as

$$I = \frac{V}{R_{CPL}} + \frac{2P_{CPL}}{V_{load}} \tag{4}$$

The equivalent circuit of eq (4) can be drawn as in Fig. 1 (a). This linear (small-signal) model of CPL can be used for stability analysis and developing an effective control strategy. A non-linear model of the CPL is derived in the following subsection.

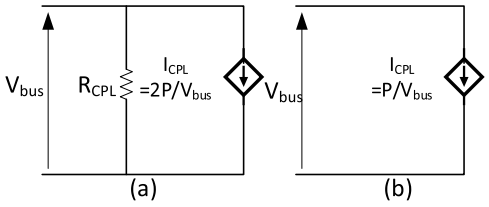

FIGURE 1. (a) Small signal model of CPL (b) Large signal model of CPL.

B. LARGE SIGNAL MODEL OF CPL

Naturally, the CPL has rectangular hyperbola characteristics with negative slop. So, the dynamic model of CPL must be able to track it. Hence, the CPL's non-linear (large-signal) model is modelled as a dynamic current carrying load given by the equation (5). The equivalent circuit of large signal model is represented in Fig. 1(b)

$$I_{CPL} = \frac{P_{CPL}}{V_{load}} \tag{5}$$

C. CONVERTERS MODELLING

In a DCMG, bi-directional boost converters or bidirectional buck converters are used to integrate RES and loads. A simple mathematical model for these converters can be derived as follows.

1) BI-DIRECTIONAL BOOST CONVERTER

A simplest bi-directional boost converter circuit (Fig. 2) consists of input DC voltage sources, two switches operated as per the duty ratio D, a set of resistance R_{in} and inductance L_{in}, and a capacitor C_{in} across the converter terminal. Using fundamental laws Kirchhoff's current (KCL) and voltage (KVL), dynamic model of the converters can be written as -The dynamic equations are given as,

$$L_{in}\frac{di_L}{dt} = V_{dc} - R_{in}i_L - (1-D)V_o \tag{6}$$

$$C_{in}\frac{dV_o}{dt} = (1-D)i_L - i_o \tag{7}$$

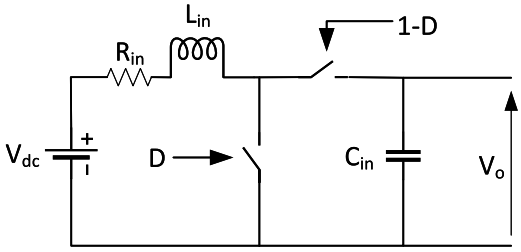

FIGURE 2. Bi-directional boost converter.

Writing the parameters for small disturbance around the steady state values

$$i_L = i_L + \hat{i}_L$$
$$V_o = V_o + \hat{V}_o$$
$$V_{dc} = V_{dc} + \hat{V}_{dc}$$
$$D = D + \hat{d}$$
$$i_o = i_o + \hat{i}_o$$

The dynamic equations (6) and (7) are transformed as

$$L_{in}\frac{d(i_L+\hat{i}_L)}{dt} = (V_{dc}+\hat{V}_{dc}) - R_{in}(i_L+\hat{i}_L) - (1-(D+\hat{d}))(V_o+\hat{V}_o) \tag{8}$$

$$C_{in}\frac{d(V_o+\hat{V}_o)}{dt} = (1-(D+\hat{d}))(i_L+\hat{i}_L) - (i_o+\hat{i}_o) \tag{9}$$

After simplifying the above equations

$$L_{in}\frac{d\hat{i}_L}{dt} = (\hat{V}_{dc}) - R_{in}(\hat{i}_L) - (1-D)\hat{V}_o + \hat{d}V_o \tag{10}$$

$$C_{in}\frac{d(\hat{V}_o)}{dt} = (1-D)\hat{i}_L + \hat{d}(i_L) - (\hat{i}_o) \tag{11}$$

The above equations are transformed to Laplace domain as shown in eqs.(12) and (13), receptively.

$$sL_{in}\hat{i}_L(s) = (\hat{V}_{dc}(s)) - R_{in}(\hat{i}_L(s)) - (1-D)\hat{V}_o(s) + \hat{d}(s)V_o \tag{12}$$

$$sC_{in}(\hat{V}_o(s)) = (1-D)\hat{i}_L(s) + \hat{d}(s)(i_L) - (\hat{i}_o(s)) \tag{13}$$

2) MODELLING OF CONTROLLER FOR DC-DC CONVERTERS

A dual loop controller is required to regulate the DC-DC converter output voltage. A general controlling structure of the dual loop controller is illustrated in Fig. 3, and its large signal model is expressed in eq (14).

$$D = K_{pi}[K_{pv}(V_o^* - V_o) + K_{iv}\int(V_o^* - V_o)dt - i_L] + K_{ii}\int[K_{pv}(V_o^* - V_o) + K_{iv}\int(V_o^* - V_o)dt - i_L]dt \tag{14}$$

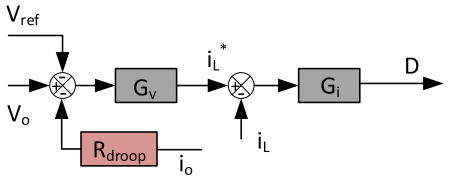

FIGURE 3. Control structure of converters.

where,

G_v = PI voltage controller
G_i = PI current controller
$V_o^* = V_{ref}$ = Reference output voltage
K_{pv} = Proportional gain of voltage controller
K_{pi} = Proportional gain of current controller
K_{iv} = Integral gain of voltage controller
K_{ii} = Integral gain of current controller
i_L = Actual inductor current in converter
V_o = Actual output voltage of controller
i_o = Actual output current of controller
i_L^* = Reference inductor current
R_{droop} = Droop between output voltage and output current of converter
D = PWM Duty cycle

On linearizing the dynamic equations of converter and the duty cycle eq. (14) the small signal model of converter is shown in Fig. 4. Any converter can be modelled in small-signal as shown in Fig. 4 with appropriate transfer functions in them. The converter can be replaced as a source connected with an impedance as shown in Fig. 5. Further, the modelling details can be found in [4]. The $Z_o(s)$ can be derived as in eq.(15)

$$Z_o(s) = -\frac{\hat{V}_o(s)}{\hat{i}_o(s)}$$

$$Z_o(s) = \frac{Z_{out}(1 + G_iG_{id}) - A_{io}G_iG_{vd} + R_{droop}G_vG_iG_{vd}}{1 + G_iG_{id} + G_vG_iG_{vd}} \tag{15}$$

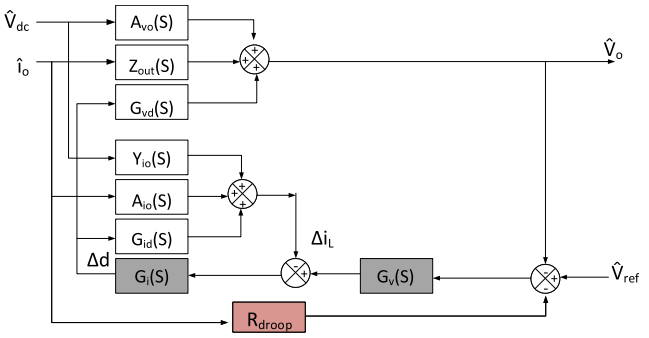

FIGURE 4. Small signal model of converter.

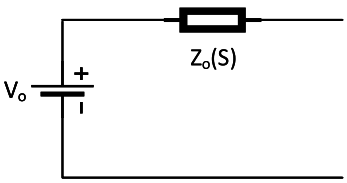

FIGURE 5. Converter equivalent model.

In Fig.4, the transfer functions of small signal model can be found as

$$A_{vo} = \frac{\hat{V}_o(s)}{\hat{V}_{dc}(s)}\bigg|_{\hat{d}(s),\hat{i}_o(s)=0} \tag{16}$$

The $A_{vo}(s)$ is derived as

$$\begin{aligned} sL_{in}\hat{i}_L(s) &= \hat{V}_{dc}(s) - R_{in}\hat{i}_L(s) \\ &\quad - (1-D)\hat{V}_o(s) \\ sC_{in}\hat{V}_o(s) &= (1-D)\hat{i}_L(s) \\ (sL_{in}R_{in})\hat{i}_L(s) &= \hat{V}_{dc}(s) - (1-D)\hat{V}_o(s) \\ [\frac{s^2L_{in}C_{in} + sC_{in}R_{in}}{(1-D)}]V_o(s) &= V_{dc} - (1-D)V_o(s) \\ A_{vo} = \frac{\hat{V}_o(s)}{\hat{V}_{dc}(s)}\bigg|_{\hat{d}(s),\hat{i}_o(s)=0} &= \frac{1-D}{s^2L_{in}C_{in} + sC_{in}R_{in} + (1-D)^2} \end{aligned} \tag{17}$$

Let,

$$Den^r = s^2L_{in}C_{in} + sC_{in}R_{in} + (1-D)^2$$

Similarly, other transfer functions are derived as

$$Z_{out}(s) = -\frac{\hat{V}_o(s)}{\hat{i}_o(s)}\bigg|_{\hat{v}_{dc}(s),\hat{d}(s)=0} = \frac{L_{in}s + R_{in}}{Den^r}$$

$$G_{vd}(s) = \frac{\hat{V}_o(s)}{\hat{d}(s)}\bigg|_{\hat{v}_{dc}(s),\hat{i}_o(s)=0} = \frac{-L_{in}I_Ls - R_{in}I_L + V_{dc}}{Den^r}$$

$$Y_{io}(s) = \frac{\hat{i}_L(s)}{\hat{V}_{dc}(s)}\bigg|_{\hat{i}_o(s),\hat{d}(s)=0} = \frac{C_{in}s}{Den^r}$$

$$A_{io}(s) = -\frac{\hat{i}_L(s)}{\hat{i}_o(s)}\bigg|_{\hat{v}_{dc}(s),\hat{d}(s)=0} = \frac{-(1-D)}{Den^r}$$
$$G_{id}(s) = \frac{\hat{i}_L(s)}{\hat{d}(s)}\bigg|_{\hat{v}_{dc}(s),\hat{i}_o(s)=0} = \frac{C_{in}V_o s + I_L(1-D)}{Den^r}$$

The output impedance of boost converter can be calculated from equation (15) with transfer functions derived above.

3) BI-DIRECTIONAL BUCK CONVERTER

The bi-directional buck converter circuit is shown in Fig. 6. Like boost converter, dynamic model of buck converter can be expressed as in eq.(18) and (19) respectively.

$$L_{in}\frac{di_L}{dt} = DV_{in} - i_L R_{in} - V_o \tag{18}$$
$$C_{in}\frac{dV_o}{dt} = i_L - i_o \tag{19}$$

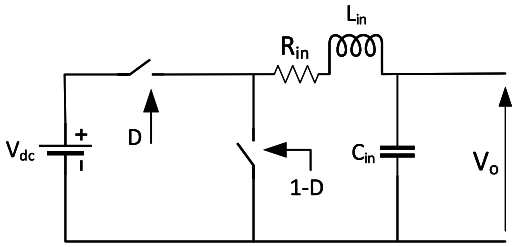

FIGURE 6. Bi-directional buck converter.

Similar to the analysis done for bi-directional boost converter the transfer functions for the controller (Fig. 4) can be derived as

$$A_{Vo}(s) = \frac{\hat{V}_o(s)}{\hat{V}_{dc}(s)}\bigg|_{\hat{d}(s),\hat{i}_o(s)=0} = \frac{D}{L_{in}C_{in}s^2 + R_{in}C_{in}s + 1}$$
$$Z_{out}(s) = -\frac{\hat{V}_o(s)}{\hat{i}_o(s)}\bigg|_{\hat{v}_{dc}(s),\hat{d}(s)=0} = \frac{R_{in} + L_{in}s}{L_{in}C_{in}s^2 + R_{in}C_{in}s + 1}$$
$$G_{vd}(s) = \frac{\hat{V}_o(s)}{\hat{d}(s)}\bigg|_{\hat{v}_{dc}(s),\hat{i}_o(s)=0} = \frac{V_{dc}}{L_{in}C_{in}s^2 + R_{in}C_{in}s + 1}$$
$$Y_{io}(s) = \frac{\hat{i}_L(s)}{\hat{V}_{dc}(s)}\bigg|_{\hat{i}_o(s),\hat{d}(s)=0} = \frac{DC_{in}s}{L_{in}C_{in}s^2 + R_{in}C_{in}s + 1}$$
$$A_{io}(s) = -\frac{\hat{i}_L(s)}{\hat{i}_o(s)}\bigg|_{\hat{v}_{dc}(s),\hat{d}(s)=0} = \frac{-1}{L_{in}C_{in}s^2 + R_{in}C_{in}s + 1}$$
$$G_{id}(s) = \frac{\hat{i}_L(s)}{\hat{d}(s)}\bigg|_{\hat{v}_{dc}(s),\hat{i}_o(s)=0} = \frac{V_{dc}C_{in}s}{L_{in}C_{in}s^2 + R_{in}C_{in}s + 1}$$

The output impedance of the buck converter from eq (15) with transfer functions mentioned above.

III. STABILITY CRITERION AND CALCULATION OF NEGATIVE IMPEDANCE

The concept of the proposed virtual negative resistance loop for the stabilization of CPL in a DCMG has been described in this section. First, based on the small signal model of DCMG components, the stability of converters is analyzed. As it is shown in the previous section, eq. (2), CPL introduces negative impedance into the system, which reduces the damping in the system. It results in voltage oscillations and sometimes voltage instability in a DCMG. A DCMG is considered stable if its components operate well within the stability limits. In other words, the operation of individual converters in a DCMG must be stable. To design the controller parameters, a stability criterion-based approach is proposed for the DCMG's PECs.

A. BI-DIRECTIONAL BOOST CONVERTER STABILITY CRITERION

In the recent research [29], it was seen that the destabilizing impact of CPL is profound when voltage regulation is insufficient or a smaller DC link capacitor is used. The dynamic model of the converters considered in the DCMG is derived in eqs (6) and (7). The converter output current is dependent to the load connected across its terminal. Let the load current is i_o due the terminal load $R = R_{CPL} \parallel R_{dc}$ where, R_{CPL} = CPL resistance and R_{dc} = Resistive load. This load current can be written as

$$i_o = V_o/R \tag{20}$$

Converter transfer function can be rewritten with substitution of i_o and expressed as

$$L_{in}\frac{di_L}{dt} = V_{dc} - R_{in}i_L - (1-D)V_o$$
$$C_{in}\frac{dV_o}{dt} = (1-D)i_L - \frac{V_o}{R}$$

Further, the small signal model given in eqs. (12)-(13) are transformed as

$$sL_{in}\hat{i}_L(s) = \hat{V}_{dc}(s) - R_{in}\hat{i}_L(s) - (1-D)\hat{V}_o(s) + \hat{d}(s)V_o \tag{21}$$
$$sC_{in}\hat{V}_o(s) = (1-D)\hat{i}_L(s) + \hat{d}(s)(i_L) - \frac{\hat{V}_o(s)}{R} \tag{22}$$

From eq (21), the transfer function $\frac{\hat{V}_o(s)}{\hat{d}(s)}$ is derived as shown below

$$i_L(s) = \frac{(sC_{in} + \frac{1}{R})\hat{V}_o(s) + \hat{d}(s)i_L}{1-D} \tag{23}$$

From eq (23) and (21)

$$\frac{\hat{V}_o(s)}{\hat{d}(s)} = \frac{(1-D)V_o - (R_{in} + sL_{in})i_L}{L_{in}C_{in}s^2 + s(\frac{L_{in}}{R} + R_{in}C_{in}) + (D-1)^2 + \frac{R_{in}}{R}} \tag{24}$$

In order to have a stable system, roots of the denominator in eq (24) should be on the left side of $j\omega$ axis.

$$s = -(\frac{L_{in}}{R} + R_{in}C_{in}) \pm \sqrt{(\frac{L_{in}}{R} + R_{in}C_{in})^2 - 4L_{in}C_{in}[(1-D)^2 + \frac{R_{in}}{R}]}$$
$$2L_{in}C_{in} \tag{25}$$

The real part of roots should be negative. The above analysis is done assuming the PI controllers are very fast. Then L_{in}, C_{in}, R_{in} is always positive so,

$$\frac{1}{R} > 0$$
$$\frac{R_{dc} - \frac{V^2}{P_{CPL}}}{R_{dc}.(-\frac{V^2}{P_{CPL}})} > 0$$
$$R_{dc} < \frac{V^2}{P_{CPL}} \tag{26}$$

P_{CPL} is the CPL power, V is the terminal voltage of the CPL load. If eq (26) is satisfied then the boost converter is stable.

B. BI-DIRECTIONAL BUCK CONVERTER STABILITY CRITERION

Similar to the analysis of bi-directional boost converter, transfer function for the buck converter can be derived and holds the stability criterian given in eq (26).

C. SOURCE SIDE CONTROLLING STABILITY CRITERION

A typical microgrid controlling through the sources' side converters is depicted in Fig.7. The small signal model of this DCMG (Fig. 7) with converters and loads is shown in Fig. 8.

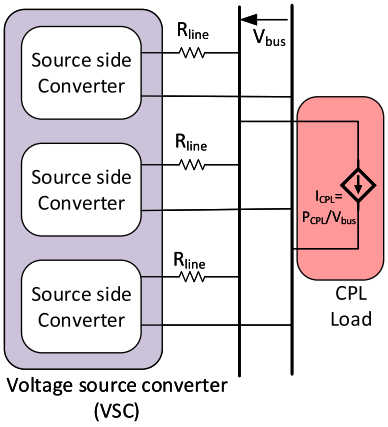

FIGURE 7. Source side controlled DC microgrid.

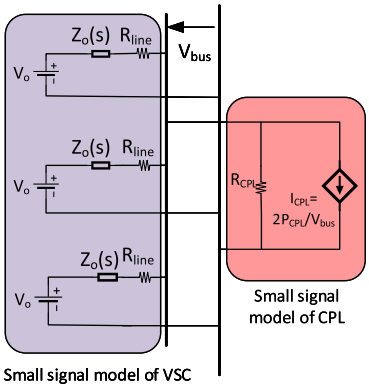

FIGURE 8. Small signal model of grid.

It can be further simplified using the Thevenin equivalent across the bus for analyzing the grid stability. The proposed simplest equivalent circuit of the DCMG, shown in Fig. 9, is very useful for obtaining the controller's parameters. Mathematical details of the equivalent circuit are given in eq. (27). DC bus voltage in DCMG (V_{bus}) can be written as,

$$V_{bus} = \frac{R_{CPL}V_o}{\frac{Z_o+R_{line}}{3} + R_{CPL}} - I_{CPL}\frac{(R_{CPL}(\frac{Z_o+R_{line}}{3}))}{R_{CPL} + \frac{Z_o+R_{line}}{3}}$$
$$V_{bus} = \frac{V_o - I_{CPL}(\frac{Z_o+R_{line}}{3})}{\frac{\frac{Z_o+R_{line}}{3}}{R_{CPL}} + 1} \tag{27}$$

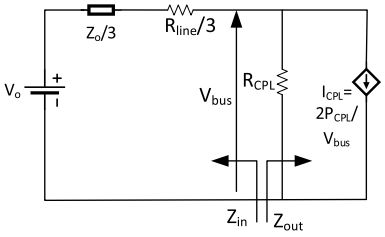

FIGURE 9. Equivalent model of microgrid.

Let in the equivalent circuit;

$Z_{in} = \frac{Z_o+R_{line}}{3}$

$Z_{out} = R_{CPL}$

T_m = Minor loop gain $= Z_{in}/Z_{out}$

$$\frac{1}{T_m + 1} = \frac{1}{\frac{\frac{Z_o+R_{line}}{3}}{R_{CPL}} + 1} \tag{28}$$

The eq (27) consists of two transfer functions $\frac{V_{bus}}{V_o}$ and $\frac{V_{bus}}{I_{CPL}}$. Denominators of both the transfer functions are T_m+1. So the poles and zeroes of the $\frac{1}{T_m+1}$ should be to the left of the '$j\omega$' axis to have a stable system.

D. LOAD SIDE CONVERTER STABILITY CRITERION

A control strategy can be employed to the PEC connected at the load end, as shown in Fig. 10. It is important to

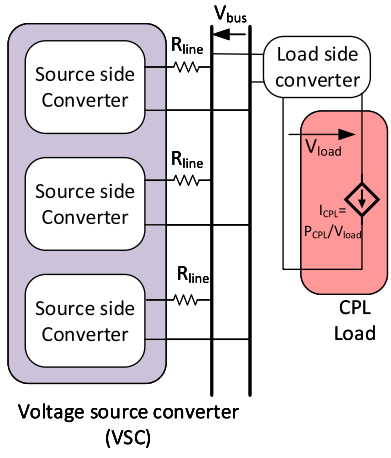

FIGURE 10. Load side control microgrid.

note that the source-side converters are bi-directional boost converters, whereas the load-side converter is a bi-directional buck converter. The small signal equivalent and its Thevenin equivalent circuit are depicted in Fig. 11 and 12, respectively. This equivalent circuit is designed after referring the loads connected across the converter output to the source side, just like a transformer having a turns ratio $(1 : D)$.

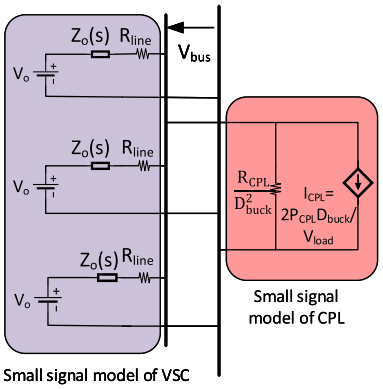

FIGURE 11. Small signal model of microgrid.

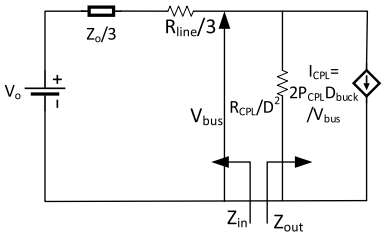

FIGURE 12. Equivalent model of microgrid.

From Fig 12,

$$Z_{in} = \frac{Z_o + R_{line}}{3}$$
$$Z_{out} = \frac{R_{CPL}}{D^2_{buck}}$$
$$T_m = Z_{in}/Z_{out}$$
$$\frac{1}{T_m + 1} = \frac{1}{\frac{\frac{Z_o + R_{line}}{3}}{\frac{R_{CPL}}{D^2_{buck}}} + 1} \tag{29}$$

Like the stabilization criterion used in bi-directional boost converter, $\frac{1}{T_m+1}$ should have the roots left to the $j\omega$ axis.

IV. PROPOSED CONTROL STRATEGY AND STABILITY ANALYSIS

This section proposes a novel negative resistance method to stabilize the instability caused by the CPL loads on the grid. The converter control structure discussed above (Fig. 3) is modified with the proposed negative resistance loop as shown in the can be seen in Fig. 13. The small-signal loop of the proposed control structure with the converter is shown

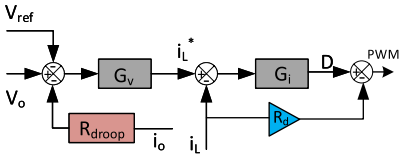

FIGURE 13. Proposed control loop structure for converters.

TABLE 1. Source side converter parameters.

Variable	Description	value
V_dc	Source voltage	48
V_ref	Bus reference voltage	200 V
L_{in}	Converter Inductance	2 mH
C_{in}	Converter Capacitance	2200 μF
R_{in}	Converter resistance in series with inductance	0.04 ohms
R_{line}	line resistance	0.08 ohms
F_{sw}	switching frequency	10 KHz
R_{droop}	voltage current droop of converter	0.4
Kpv	Proportional gain of PI voltage controller	0.1061
Kiv	Integral gain of PI based voltage controller	50
Kiv	Proportional gain of PI based current controller	18.8495
Kii	Integral gain of PI based current controller	376.991

in Fig. 14. This small signal model is used for finding the $Z_o(s)$ for each converter discussed in sections III-C and III-D, respectively, with the proposed negative resistance loop. The Fig. 13 is the control structure used for real-time simulation. The following parts discuss the stability margin of MG without the proposed loop using $\frac{1}{1+T_m}$ from section III and the stability margin of the MG with the proposed loop at the source side or load side using $\frac{1}{1+T_m}$ with $Z_o(s)$ calculated from the enhanced small-signal model (Fig. 14).

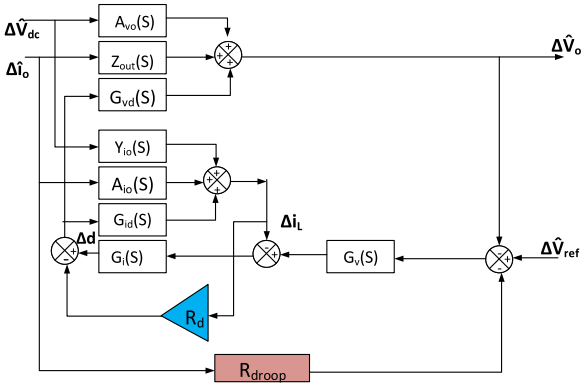

FIGURE 14. Small signal model with the modified control loop.

The Pole-Zero plots are found by varying the 'R_d' in the derived transfer functions. The proposed control strategy selects an optimal value of R_d using these pole-zero plots for the system stability. Detailed stability analysis is given in the following sub-sections.

A. SOURCE SIDE CONTROL

1) BI-DIRECTIONAL BOOST CONVERTER AS VSC

A voltage source converter (VSC) consisting of the bi-directional boost converter is used to connect the 48V DC

source with a common DC bus of the DCMG operating at 200V DC (Fig. 7). The source side converter and microgrid parameters are given in Table 1. The trial and error method is used to find the gains of the proportional-integral (PI) based controllers. The system stability is analyzed using the eq. $\frac{1}{T_m+1}$ derived from eq (28).

a: STABILITY MARGIN

The stability margin of the system is assessed using a pole-zero plot of the function $\frac{1}{T_m+1}$. The CPL load in the DCMG is increased slowly from 1KW to 20 KW. At around 10kW, the system poles are moved to the right of $j\omega$ axis. It is shown in Fig (15). So, the system is stable for the CPL less than 10 KW. Any CPL load greater or equal to 10 KW in the microgrid shown in Fig. 7 with a bi-directional boost converter as VSC becomes unstable.

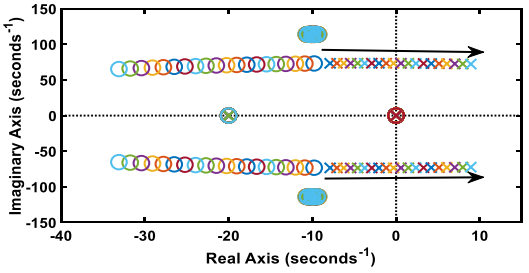

FIGURE 15. Stability margin with source side bi direction boost converter.

b: STABILITY MARGIN WITH PROPOSED CONTROL STRATEGY

The proposed negative impedance loop with R_d is now performed to enhance the CPL stability limits up to 15 kW. By varying the R_d value from -1 to -12 in steps of 1, the pole-zero plot of $\frac{1}{T_m+1}$ is drawn to show the movement of poles (eigenvalues) towards the stable region (left of the $j\omega$ axis). This DCMG stability assessment is depicted in Fig. 16. The R_d is chosen to be -10.5 so that stability margin of the grid is increased from 10KW to 15KW of CPL. The stability margin increased by 50%

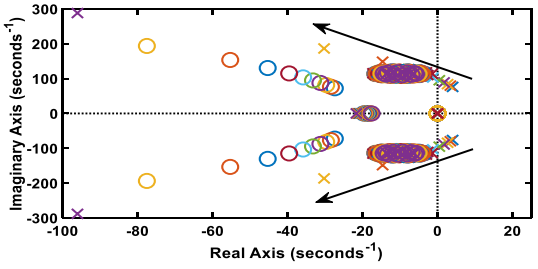

FIGURE 16. Root locus when R_d is varied from -1 to -12.

c: REDUNDANCY TO DROOP CHANGE

At $R_d = -10.5$, the droop of converters is changed from 0.05 to 0.2 in steps of 0.05. The pole-zero plot of the grid is shown in Fig. 17. It can be seen that the stability of the DCMG

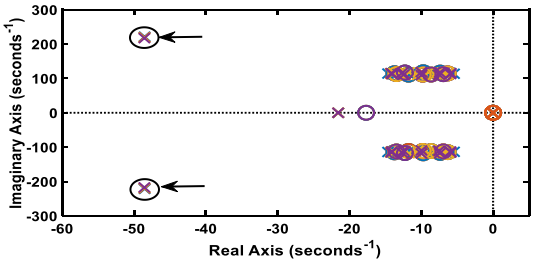

FIGURE 17. Root locus when R_{droop} is varied from 0.05 to 0.2.

is not much affected by the droop values. Hence, the proposed control strategy is almost independent of droop value R_{droop}.

2) BI-DIRECTIONAL BUCK CONVERTER AS VSC

In this subsection, the bi-directional buck converter is considered as VSC with input source voltage 200V. It has to maintain 150 V DC at output terminal. Stability of the system having source side VSC's (Fig. 7) is analyzed according to eq. $\frac{1}{T_m+1}$ in next subsections. The parameters of the source side converter and microgrid are shown in Table 1. Thease parameters can be found in [4] and it can be validated mathematically using the approach given in [30].

a: STABILITY MARGIN

The stability margin of the system is calculated using pole zero plot of $\frac{1}{T_m+1}$, where CPL load is increased from 1KW to 20 KW. At, around 10kW the system poles are moved towards right of jω axis as shown in Fig. 18. So, system is stable till the CPL is less than 10 KW. Any CPL load greater than 10 KW leads to system instability.

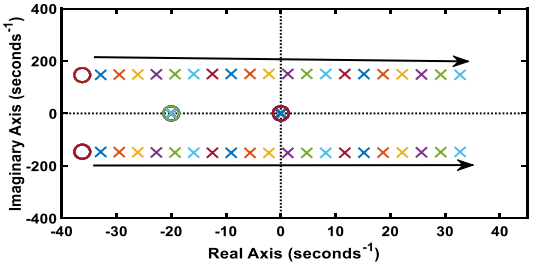

FIGURE 18. Stability margin with bidirectional buck converter.

b: STABILITY MARGIN WITH PROPOSED CONTROL STRATEGY

The CPL in the grid is maintained at 15KW so that the microgrid is in an unstable state. The proposed control strategy with $R_d = -10.5$ can enhance the CPL stability margin up to 15 kW. The pole zero plot of $\frac{1}{T_m+1}$ with different R_d values is shown in Fig. 19. The stability margin increased by 50%

c: REDUNDANCY TO DROOP CHANGE

At R_d of -10.5, impact of droop values is negligible in presence of the proposed control strategy.

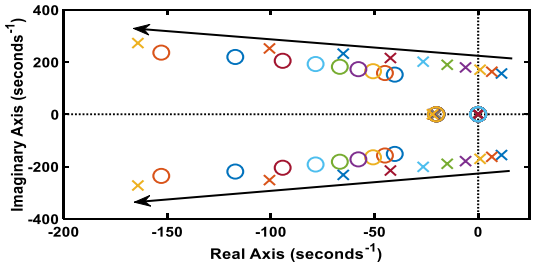

FIGURE 19. Root locus when R_d is varied from −1 to −12.

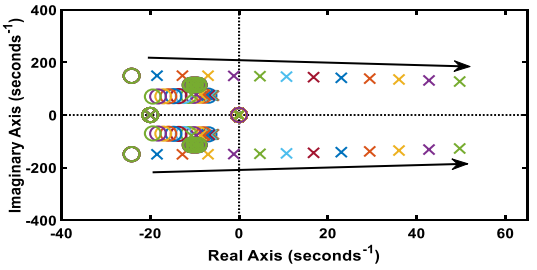

FIGURE 20. Stability margin.

B. LOAD SIDE CONTROL

The network shown in Fig. 10 consist of a bi-directional boost converter at the source side and a bi-directional buck converter at the load-side. If the controlling needs to be done at the load-side, the system dynamics are always decided by the slower response component in the network. So, the load-side converter dynamics should be slower than the source-side converter. The parameters associated to source and load side converters are given in Table 2, and 3, respectively. Stability of the system is analyzed using eq. (29).

TABLE 2. Source side converter parameters for load side control.

Variable	Description	Value
Kpv	Proportional gain of PI voltage controller	0.1061
Kiv	Integral gain of PI voltage controller	50
Kpi	Proportional gain of PI current controller	12.5663
Kii	Integral gain of PI current controller	251.3274
Fsw	Switching frequency	15 KHz
Rdroop	Voltage current droop of converter	0.05

TABLE 3. Load side converter parameters.

Variable	Description	value
Vdc	Bus Voltage	200 V
Vref	load terminal reference voltage	150 V
Rdroop	voltage current droop of Converter	0

1) STABILITY MARGIN

The CPL is varied from 1KW to 8KW in steps of 1KW the pole zero plot of the $\frac{1}{1+T_m}$ is shown in Fig.20. As, the CPL increases on the grid shown in Fig. 10 stability decreases and poles are moving to right of jω axis. The stability margin of system is about 4KW. For any CPL load greater-than or equal to 4 KW make system unstable as the poles of $\frac{1}{T_m+1}$ lie on the right of jω axis.

2) NEGATIVE INDUCTANCE DROOP METHOD

At load side there is no droop but for stabilization a negative inductance droop is incorporated as shown in small signal model of converter at load side in Fig. 21 and the controlling structure of load side converter is shown in Fig. 22. Due to negative droop inductance a differential term sL_{droop} to reduce its effects a filter is used along with it so the total

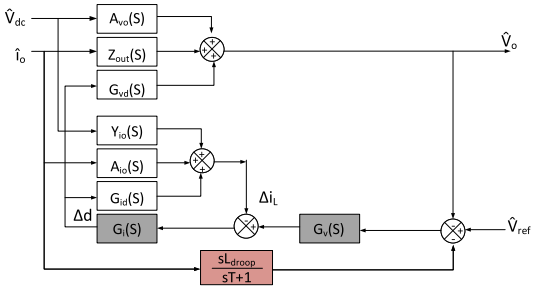

FIGURE 21. Negative inductance droop small signal model.

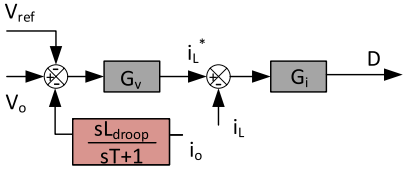

FIGURE 22. Negative inductance droop control structure.

droop is given as $\frac{sL_{droop}}{sT+1}$ appropriate filter design should be used to counter the differential gain produced to the noise in the system. where;

T = Time constant of the filter = 1m sec

L_{droop} = inductance droop The CPL is maintained at 8KW and the L_{droop} is changed from −1mH to −0.025H, the poles of system $\frac{1}{T_m+1}$ moves to left as shown in Fig. 23. The L_{droop} is chosen to be −0.025H to have stability margin of system up-to 8KW of CPL.

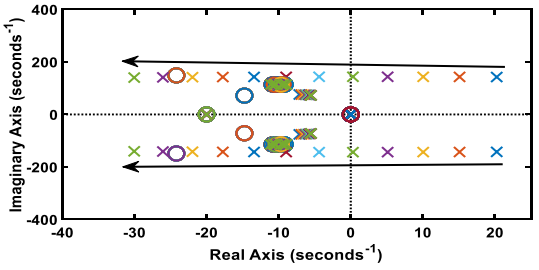

FIGURE 23. Root locus when L_{droop} is varied from −1mH to −0.025H.

3) PROPOSED CONTROL STRATEGY

The proposed control strategy is incorporated at load side. The CPL on the grid is maintained at 8KW so that instability

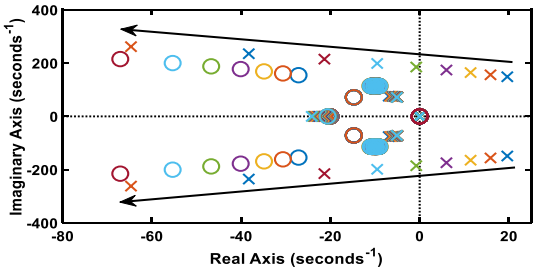

FIGURE 24. Root locus when R_d is varied from −1 to −10.

is created on the grid. The R_d is varied from −1 to −10, the poles lying on the right side of jω axis is moves to the left of jω axis as shown in Fig. 24. The R_d is chosen to be −12.5 to have system stability margin till 8KW of CPL. The stability margin increased by 100%.

V. SIMULATIONS

MATLAB simulations for the source and load-side control are done in this section. The simulations are done using the exact models of converters and the large signal model of CPL.

A. SOURCE SIDE CONTROLLING

The parameters of the grid are chosen from Table 1 for simulation with the source side controlling strategy.

1) BI-DIRECTIONAL BOOST CONVERTER

The real-time simulation of the DCMG (Fig 7) with a bi-directional boost converter is performed to show the voltage stability (Fig. 25). There is no load on the grid until 1 sec. At t=1sec, 10KW of CPL is added to the grid. At the same time, the proposed stabilization loop with $R_d = -10.5$ is activated. At t=1.5sec, an additional 3KW of CPL is added, and further, at t=2sec, an additional 2KW of CPL is added to the grid. The Fig. 25 shows that the system is stable with any load under 15KW. At 2.5sec, the source side droop is changed from 0.05 to 0.1; at 3sec, the source side droop is changed from 0.1 to 0.2, the system is still stable, but due to increased droop, the bus voltage decreased.

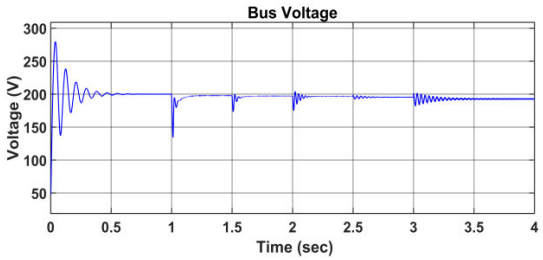

FIGURE 25. Bi-directional boost converter real-time simulation.

2) BI-DIRECTIONAL BUCK CONVERTER

The simulation is done with same parameters of bi-directional boost converter above except here V_{dc} is chosen to be 200V and V_{ref} is chosen to be 150V. The real-time simulation of the grid (Fig. 7) with bi-directional buck converter shown in Fig. 26. The sequence of simulation is same as bi-directional boost converter shown in section V-A1.

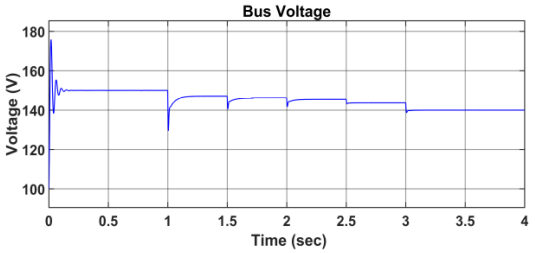

FIGURE 26. Bi-directional buck converter real-time simulation.

B. LOAD SIDE CONTROLLING

The microgrid under analysis for this section is shown in Fig. 10. The parameters are discussed in section IV-B

1) CONVENTIONAL NEGATIVE VIRTUAL INDUCTANCE METHOD

The control structure at load-side controller is chosen to be same as shown in Fig. 22. The parameters used for simulation are discussed in the section IV-B2. The real-time simulation with negative droop control with L_{droop} chosen to be −0.025mH is shown in Fig. 27. At time t=0sec, there is no load on the grid. At t=1sec, a CPL of 4KW is added into the grid and at t=2sec, the negative inductance droop loop is activated. At 3sec, an additional CPL of 2KW is added, and at 4sec, another additional CPL of 2KW is added. The overall system is stabilized with load-side controlling. The bus voltage gets damped to 200V with negative droop control at the load side while maintaining the voltage profile across the load terminals at 150V. So, there is no performance degradation of load due to a change in terminal voltage profile.

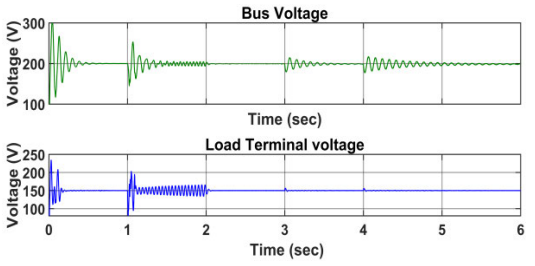

FIGURE 27. Negative inductance droop control at load side.

2) PROPOSED CONTROL STRATEGY METHOD

Here, the simulation is done through the proposed control loop with R_d chosen to be −12.5 at the load side converter. The simulation sequence is the same as above, but the proposed control loop is used at 2 seconds instead of a negative inductance droop. The real-time simulation with the

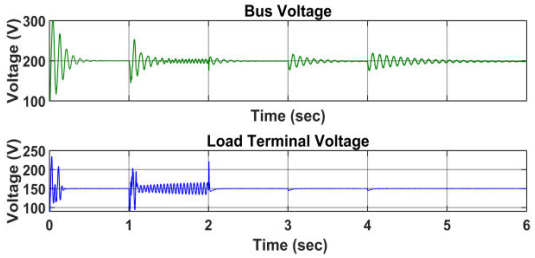

FIGURE 28. Proposed control strategy at load side.

proposed control method at load side converter is shown in Fig. 28.

3) RESULT DISCUSSION AND FUTURE SCOPE

The load-side control strategy to enhance the CPL stability margin is simple and easy to implement in a DCMG. Additionally, load-side control offers decentralized control and flexibility, where individual loads or load groups can independently control and stabilize the bus voltage without changing the load performance. In the result, it was found that Droop has negligible impact on the system. Due to load-side converter control, the availability of the source-side controllers is increased to incorporate advanced power-sharing and economic load dispatch algorithms. The proposed approach can be extended for coordinated distributed control for economic power-sharing in CPL-dominated DCMG.

VI. CONCLUSION

This paper proposes a novel virtual negative resistance-based control loop for the load-side and source-side converters to enhance the CPL stability margin of a DCMG. The pole-zero-based stabilization criterion is developed and tested with small-signal models of DCMG that have both source-side and load-side control techniques. The effectiveness of the proposed control loop is demonstrated with a typical DCMG, and the results are compared with the existing virtual negative impedance droop method. Sometimes, the existing virtual inductance droop method gives faster control at the cost of complex implementation and filter design. However, the proposed stabilization strategy doesn't require any filter design and is easy to implement with comparable faster stability control.

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