IEEE Access
Multidisciplinary ⋮ Rapid Review ⋮ Open Access Journal

Received 28 January 2024, accepted 18 February 2024, date of publication 26 February 2024, date of current version 4 March 2024.

Digital Object Identifier 10.1109/ACCESS.2024.3370035

RESEARCH ARTICLE

A Novel Hybrid RF-DC Converter Using CMOS n-Well Process

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This work was supported by the Deanship of Research Oversight and Coordination at the King Fahd University of Petroleum & Minerals (KFUPM) under Project SB201018.

ABSTRACT The use of RF harvesting as a power source for low-power systems, such as wearables, wireless sensor nodes, and Internet of Things, has gained attention. The primary obstacle to develop an effective RF-DC system has been the RF rectifier. The method most frequently employed in the design of RF-DC converters is called Cross-Coupled Differential Drive (CCDD). To enhance the DC output voltage, multistage systems are typically employed. In these designs, DC output will reach saturation as the number of stages rises. This is because the NMOS threshold voltage will rise if the bulk of the NMOS is connected to the lowest potential. An alternative is to employ the twin-well CMOS process, which is more expensive than the regular n-well process. A novel CMOS RF-DC converter is presented in this brief. The design is hybrid in the sense the first stage is designed using a standard CCDD, while the second and subsequent stages are designed exclusively with PMOS transistors. This allows the use of the n-well process during fabrication. With CADENCE Virtuoso in 0.18μm TSMC CMOS technology, the suggested design's functionality is verified. The design is functional and achieves 45% efficiency and a power dynamic range of 23dB for power conversion efficiency (PCE) >20%, according to simulation findings.

INDEX TERMS Energy harvesting, efficiency, dynamic range, rectifier, body effect, twin-well.

I. INTRODUCTION

An increasingly promising option for creating self-powered nodes for Internet of Things applications is energy harvesting technology. Despite the fact that wireless energy in free space has the lowest energy density, researchers are nonetheless interested in RF energy harvesting because of its possible viability. Fig. 1 depicts a system block diagram for the RF energy harvesting system [1]. To obtain the necessary DC voltage, an RF-to-DC converter is utilized in conjunction with antennas to gather ambient radio frequency energy outside. The most crucial component of an RF energy harvesting system is the RF-to-DC rectifier whose efficiency is key for the function of the energy harvester.

The fundamental components of every RF-DC converter are MOS rectifiers. In CMOS technology, there are two well-known topologies: CCDD and Dickson rectifiers [1], [2], [3], [4], [5], [6], [7], [8], [9], [10], [11], [12], [13], [14]. As seen in Fig. 2a, the majority of designs documented in the literature employ the CCDD technique, with the NMOS transistor source coupled to the bulk in the second and subsequent stages. The fabrication of such designs is accomplished by the expensive twin-well process instead of to the n-well approach. On the other hand, NMOS transistors' threshold

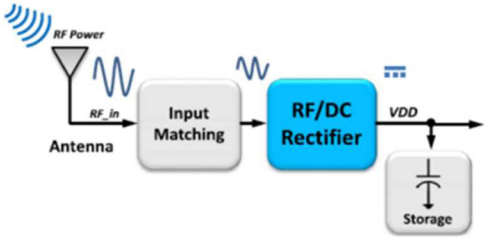

FIGURE 1. Block diagram of the RF harvesting system.

The associate editor coordinating the review of this manuscript and approving it for publication was Harikrishnan Ramiah.

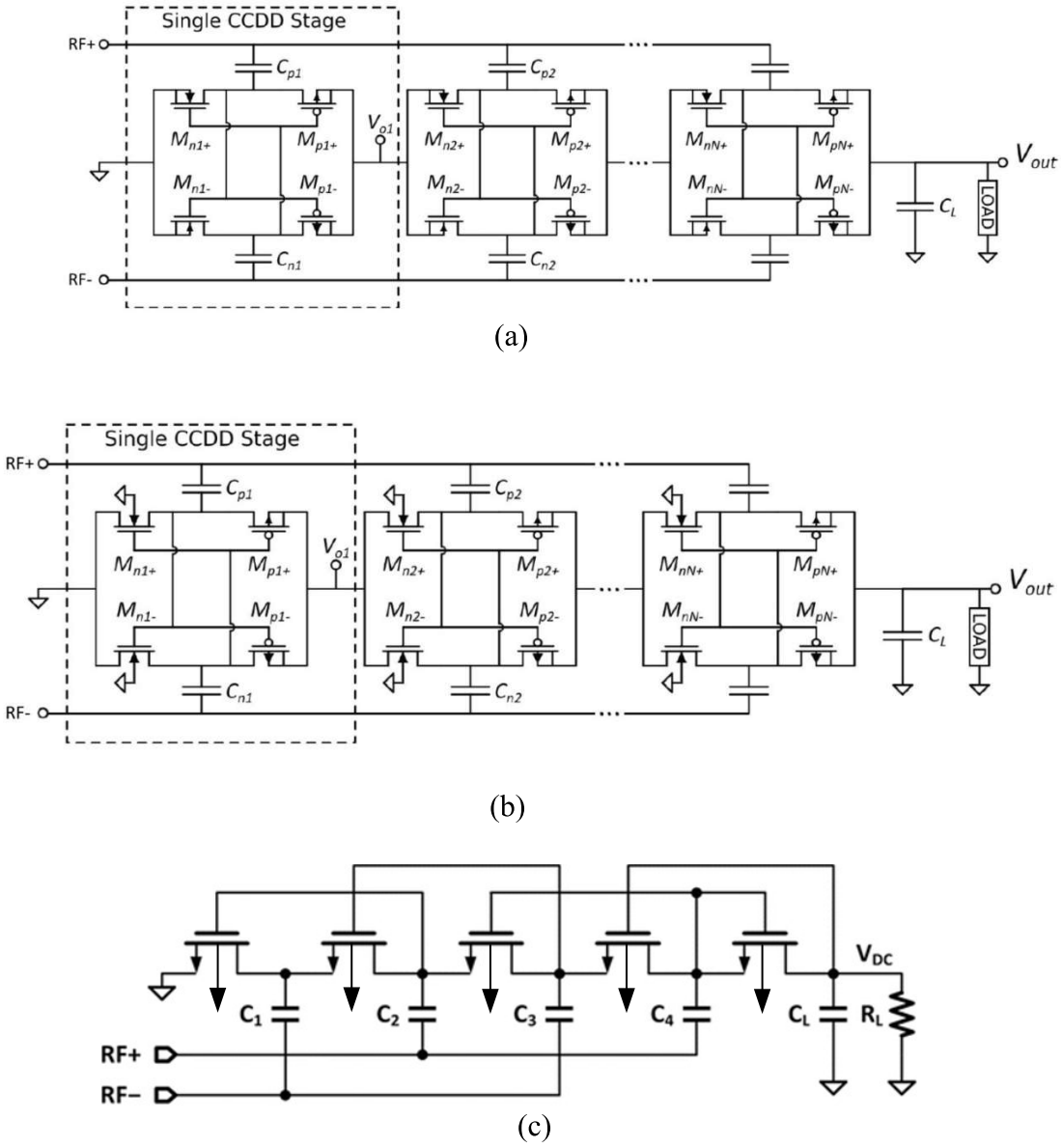

FIGURE 2. CMOS Rectifiers (a) CCDD rectifier with $V_{BS} = 0$ (b) CCDD with grounded bulk (c) Dickson rectifier with grounded bulk.

voltage will rise as the number of stages grow if the bulk is connected to ground, as indicated in Fig. 2b and 2c. This is because an increase in source potential will drive the NMOS in the off state. As a result, the flying capacitor will not charge and the DC output voltage will reach saturation. It is clear from the preceding that the twin-well technique must be employed when cascading stages in order to prevent saturation of the DC output voltage. This is the issue that needs to be resolved in order to use the n-well method in the suggested design.

This paper introduces a new hybrid design that can be fabricated using the n-well process technology. Transistors with NMOS and PMOS configurations make up the standard CCDD first stage. In order to ensure that the input RF signal is caught using the NMOS lower threshold voltage as a normal CCDD rectifier, this stage is required. The consequent stages are designed using PMOS only and connected in a different configuration (gates are cross coupled). This design will cause the DC output to increase as the number of stages increases without saturation. The rest of the paper is organized as follows: The proposed design is presented in section II. Section III reports the simulation results. The paper conclusion is presented in section IV.

II. PROPOSED DESIGN

Fig.3 depicts the suggested RF-DC converter. The first stage is formed utilizing the well-known CCDD to capture the low RF signal. The second and subsequent stages are

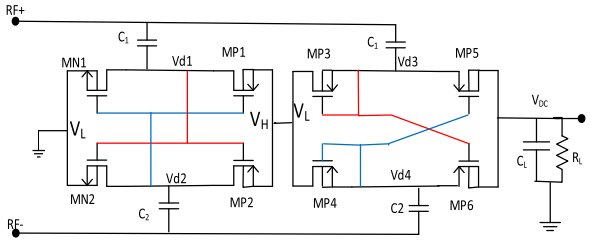

FIGURE 3. Circuit diagram for the hybrid stage.

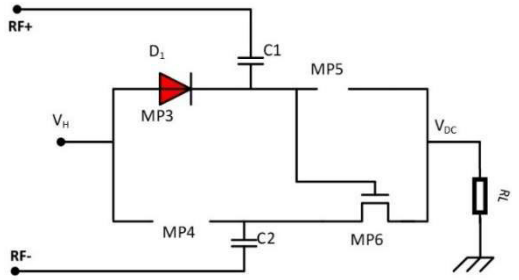

FIGURE 4. Circuit diagram for the PMOS stage.

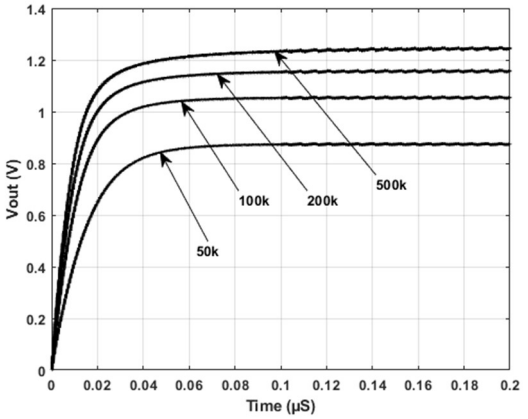

FIGURE 5. Plots of the DC output voltage for different loads.

cross-coupled in gates and are solely developed with PMOS. Therefore, it will be possible to build this rectifier design using an n-well technique. The advantages include smaller silicon area and cheaper cost. Furthermore, as the number of stages increases, a larger DC output voltage is obtained.

The rectifier operates as follows: the first stage is a standard CCDD; transistors MN1 and MP2 will be ON during the negative half of the cycle, causing C_1 to charge to $V_a - V_{DS1}$, and C_2 to pump the charge to the output. In the cycle's positive half, the opposite will occur. Referring to Fig. 3, the first stage's (CCDD) output voltage is provided by:

$$V_H \approx V_L + \left(2V_a - V_{drp}\right) \tag{1}$$

Each stage converts the peak voltage of its input signal into a DC increment with some loss V_{drp}. Here, V_a is the peak amplitude of the RF signal. This is caused by the turn-on voltage dead zone, the transistors' limited saturation voltage,

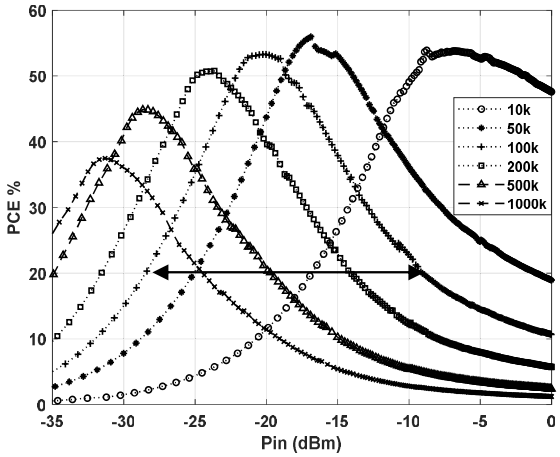

FIGURE 6. Plot of efficiency vs the input power for different Loads.

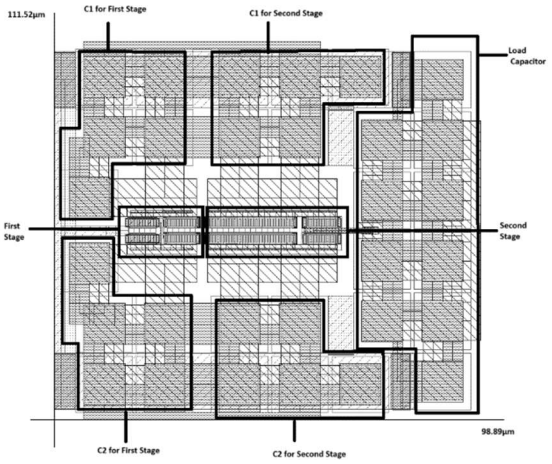

FIGURE 7. Layout of the rectifier.

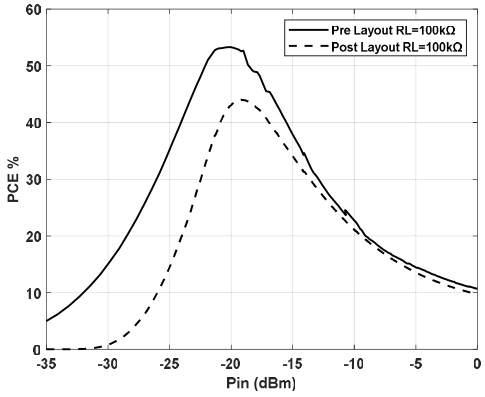

FIGURE 8. Plots of the PCE for the pre-layout and post-layout of the proposed design.

and the incomplete refreshing of the capacitor voltage, which decreases as a result of losses from reverse current and load current.

Fig. 4 shows the circuit operation for one half of a cycle of the second PMOS stage, where MP3 is diode connected and is therefore replaced by D_1 when it is ON.

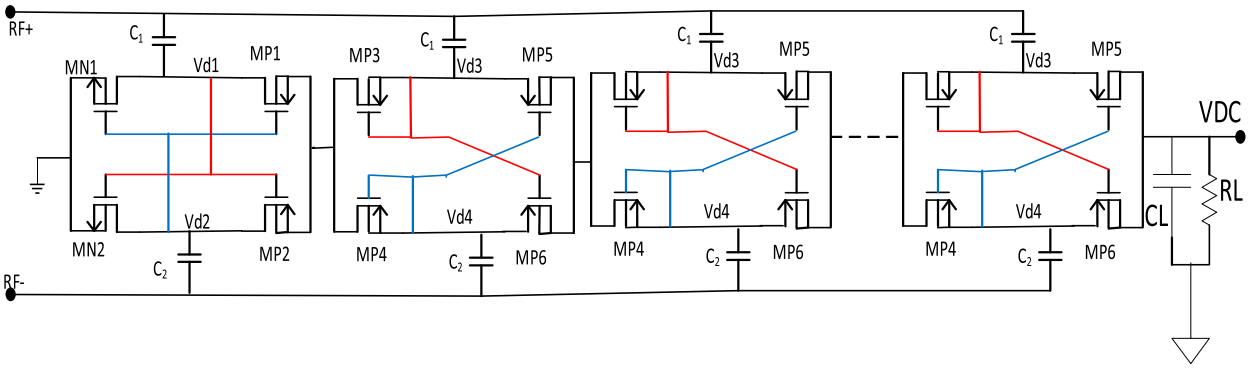

FIGURE 9. Connection for cascading stages.

The capacitor C_1 will charge through D_1 during the negative half of the cycle, and the voltage across C_1 is determined by:

$$V_{C1} = V_a + V_H - V_{D1} \tag{2}$$

where V_H represents the DC output of the preceding stage. In this case the DC output of the CCDD, and V_{D1} is the diode voltage drop, which represents V_{THP}. The load will receive a pumping action from the charge in C_2. The DC output voltage is obtained by combining equations (1) and (2) as:

$$V_{DC} \approx \left(2V_a + V_{CCDD} - |V_{THP}| - V_{drp}\right) \tag{3}$$

where V_{drp} is the drop in MP6 and $V_{CCDD} = V_H$ is the CCDD DC output voltage.

It is easy to show that the DC output voltage for the N^{th} stage is given by:

$$V_{DC,N} \approx V_{CCDD} + (N-1)\left(2V_a - |V_{THP}| - V_{drp}\right) \tag{4}$$

The rectifier's performance is dependent on the number of stages and is influenced by both its input and output impedances, as stated by [13].

$$Z_{in} \approx \left(N * C_{stage}\right) \left\| \left(\frac{R_{in-satge}}{N}\right)\right. \tag{5}$$

$$Z_{out} \approx N * R_{out-satge} \tag{6}$$

The number of stages will affect the maximum power transfer condition, therefore the peak PCE for a particular load will be displayed later.

III. SIMULATION RESULTS

The suggested design is verified using the Cadence Virtuoso environment and implemented in 0.18μm TSMC CMOS manufacturing technology. With the exception of MP3 and MP4, which have aspect ratios of 60μm/0.18μm and the flying capacitors $C_1 = C_2 = C_b = 1$pF and $C_L = 2$pF, all transistors have an aspect ratio of 20μm/0.18μm. The RF signal has a frequency of 920MHz and a peak amplitude of 0.5V. Fig. 3's hybrid architecture is simulated under various loads. Fig. 5 displays plots of the DC output voltages. The

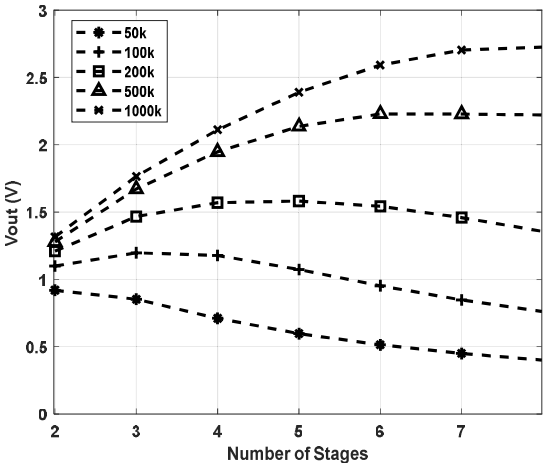

FIGURE 10. Plot of the DC output voltage vs the number of stages for different loads.

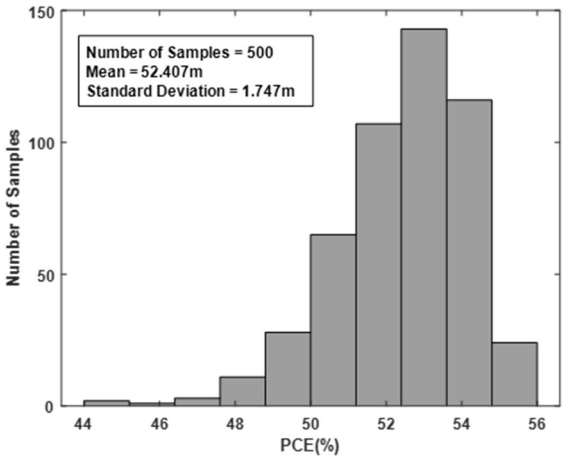

FIGURE 11. Plot of Monte-Carlo simulation result when the input power is −15dBm.

chart makes it rather evident that an increase in load will result in a rise in output voltage.

Fig. 6 displays efficiency plots under various loads. The plot indicates that, at $R_L = 100$kΩ, the power dynamic range for PCE >20% is 23dB, the highest of earlier rectifiers.

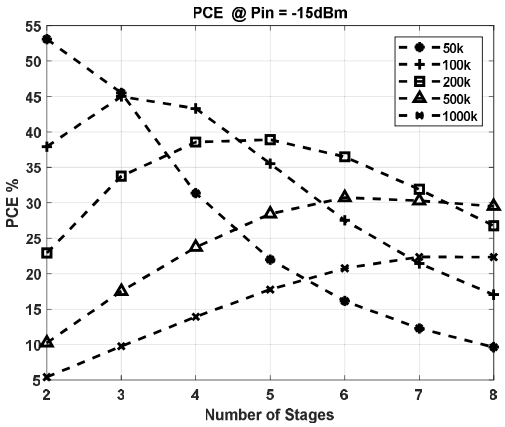

FIGURE 12. The efficiency as function of the number of stages.

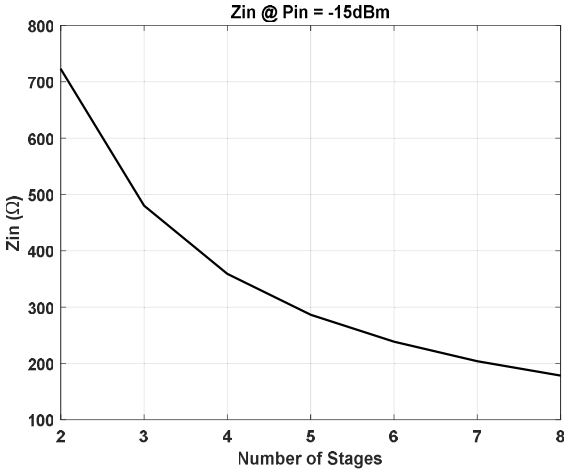

FIGURE 13. The input resistance as a function of the number of stages.

The layout of the circuit in Fig.3 excluding R_L is shown in Fig.7 and the total area is $0.011mm^2$.

Fig. 8 displays plots of the efficiency for the pre- and post-layout simulations ($R_L = 100k\Omega$). The parasitic capacitance will, as predicted, have an impact on the design's performance.

Fig.9 illustrates how to cascade the stages without adding any capacitors in between to obtain a greater DC output voltage.

Fig.10 displays the DC output voltages as a function of the number of stages for various loads with an input power fixed at −15dBm. The DC output voltage will peak at a specific load and input power, as is to be expected.

The Monte-Carlo analysis was used to assess the sensitivity of the circuit in Fig.3 to process change. A plot of the efficiency variation at −15dBm and $R_L = 100k\Omega$ is displayed in Fig. 11.

Plots demonstrating the efficiency as a function of the number of stages, with the input power set to −15dBm, are displayed for various loads in Fig. 12. The number of stages and the load will affect the peak efficiency. As indicated by equation (6), the graphic unequivocally demonstrates that the output resistance increases with the number of stages. Because of this, the number of stages will affect the maximum power transfer condition and, in turn, the peak PCE for a given load.

Fig.13 depicts the rectifier's simulated input resistance as a function of the number of stages at −15dBm. The graph makes it clear that, as implied by equation (5), the input resistance drops with the number of stages.

The proposed design is compared to the previous arts and is summarized in Table 1. It is clear from the table that the proposed design is superior to prior arts in almost all aspects.

TABLE 1. Summary of comparison.

	This work	[1]	[2]	[6]	[7]	[8]	[10]	[12]	[14]
Technology (nm)	180	180	180	180	180	180	130	180	130
Process for multistage	N-Well	Twin Well	Twin Well	Twin Well	Twin Well	Twin Well	Twin Well	Twin Well	Twin Well
Topology	Hybrid	CCDD	CCDD	CCDD	CCDD	Dual Path	-	CCDD	CCDD
Frequency (MHz)	920	953	953	1000	914	902	896	953	900
Load R_L (kΩ)	100	30	2	100	30	200	1000	10	100
PCE (%)	45	61	61.8	63	43.1	33	43	-73.6	47.91
Input (dBm)	-15	-5.5	6.4	-14.8	-16	-8	-11	14.3	-14
Max VDC (V)	1.2	NA	3.5	1	1	2.23	-	0.5	-
Number of Stages	3	3	3	1	1	`1	4	1	3
power dynamic range for PCE>20% (dBm)	23	15	12	-	16	13	8.5	17	22.8
Area (mm^2)	.011*	-	.029	.0084	-	.105	.53	.0004**	.18

*The area for hybrid stage (Fig.3).
**The area for active elements only.

IV. CONCLUSION

An innovative RF-DC converter using a hybrid n-well technology is created. The initial stage of the design is CCDD, and the subsequent stages are designed with PMOS transistors that have gates cross-coupled. Compared to earlier arts, the suggested design obtains the maximum power dynamic range for PCE >20 and has a respectable efficiency. We strongly believe there is an opportunity to boost productivity and make this hybrid design very attractive in all aspects.

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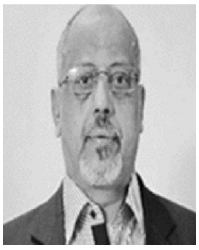

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