

Received 8 February 2024, accepted 18 February 2024, date of publication 23 February 2024, date of current version 1 March 2024. Digital Object Identifier 10.1109/ACCESS.2024.3369171

RESEARCH ARTICLE

Preparation and Performance Analysis of Thin-Film Artificial Intelligence Transistors Based on Integration of Storage and Computing

PEILONG XU^{1,2} AND INCHEOL SHIN¹⁰, (Member, IEEE)

¹Department of Artificial Intelligence Convergence, Pukyong National University, Nam-gu, Busan 48513, Republic of Korea ²State Key Laboratory of Bio-Fiber and Eco-Textile, Qingdao University, Qingdao 266071, China

Corresponding author: Incheol Shin (icshin@pknu.ac.kr)

This work was supported in part by the Pukyong National University Research Fund under Grant CD20211002; and in part by the Ministry of Trade, Industry and Energy, South Korea, under the "Regional Innovation Cluster Development Program (Research and Development) supervised by the Korea Institute for Advancement of Technology (KIAT) under Grant P0025861.

ABSTRACT In this study, a thin-film artificial intelligence transistor device based on the integration of memory and computing was designed and assessed. For this device, skyrmions were used to construct an integrated memory and computing architecture that combined content-addressable memory functions and logic operational functions. First, a dual memory cell under vertical current control was designed; based on this, a current-driven skyrmion track memory was constructed. Then, the logic gate components of the skyrmion track were constructed as the operation module. Subsequently, simulates were conducted on the device, and the results showed that when Db = 0 mJ/m² and 3 mJ/m², Wb = 0 nm, and the position of the temporal lateral displacement curve was highest. When Wb = 18 nm, the position of the skyrmion reflected a positive proportional relationship with driving-current density. Finally, in the skyrmion moving simulate, the upper part of the system stably displayed NOR operational functions, and the lower end stably displayed NAND operational functions. This research lays the foundation for designing a fifth-generation AI processor in which storage and computing are integrated.

INDEX TERMS Storage and computing integration, artificial intelligence, transistors, skyrmion.

I. INTRODUCTION

In recent decades, Moore's Law has been an important manifestation of the sustained development of the microelectronics industry. However, as the characteristic size of traditional metal oxide semiconductor transistors gradually approaches their physical limits in computational environments, the continued applicability of Moore's law is no longer assumed. How to further reduce component volume while maintaining or even improving existing computing performance has become the most important challenge in

The associate editor coordinating the review of this manuscript and approving it for publication was Sneh Saurabh $^{(D)}$.

the development of microelectronics technology [1], [2], [3]. Magnetic tunneling junction (MTJ) plays a crucial role in improving the sensor sensitivity and storage density of devices such as hard drives. The operation of MTJ relies on spin dependent tunneling, which is a phenomenon where electrons have different probabilities of tunneling through insulating barriers based on their spin orientation. Magnetic tunnel junctions greatly improve the sensitivity of sensors and the storage density of hard drives. In addition to their use in hard drive production, they can also be effectively applied in environments such as magnetic field sensors [4], [5], [6]. The Skyrmion track logic gate device integrates storage and computing, providing a platform for advanced computing architecture. The advantage here lies in the potential for efficient and parallel computing due to the simultaneous processing and storage capabilities of skyrmions. In addition, skyrmions can be used as building blocks for spin electronic devices. These devices utilize the spin properties of electrons to store, process, and transmit information. The use of skyrmions in spin electronic devices can enhance their functionality, reduce power consumption, and potentially achieve new computing modes [7], [8], [9]. When considering nonlinear electronic spin structures, the unique topological structure of skyrmions is particularly noteworthy. Artificial intelligence largely relies on the processing and analysis of large amounts of data. Integrated storage and computing technology provides an efficient way to store and retrieve large datasets, enabling faster access and processing.

With the development of computer technology, research on artificial intelligence transistors is becoming increasingly in-depth and extensive. Pan J's team used electrical nanotechnology to analyze the electrical effects of transistors integrated with artificial intelligence. They transferred information from current devices to new transistor technologies for reuse and achieved defect region classification of up to 99% and 5% on nanoscale field-effect transistors [10]. Noh J's team conducted experiments on gallium oxide ferroelectric field-effect transistors using sapphire as a substrate to evaluate the synaptic behavior of the material in high-temperature environments. The results show that in high-temperature environments, the learning accuracy of the display chip reaches 94% [11]. Cao's team proposed a solute thin film transistor based on dielectric layer conduction, and made appropriate modifications to the excitatory synaptic response in the transistor. The research results indicate that in the application field of image recognition, the recognition rate of artificial synapses can reach 92% [12]. Hao's team has prepared a semiconductor based photonic protrusion transistor through a solution process. This type of transistor can simulate basic synaptic behavior and exhibit excellent performance at ultra-low operating voltages [13]. Wan H's team proposed an artificial sensory memory system based on multisensory input sensors and synaptic signal processing. The memory system converts physical signals into presynaptic action points, with transistor synaptic plasticity characteristics, and uses five actual inputs as stimulus signals. The research results indicate that the system has application potential [14].

In recent years, research on storage and computing integration has also been extensive. To achieve this integration, Leitersdorf O's team proposed a carry save shift memory algorithm based on new partitioning and shift techniques, which effectively reduces operational area overhead [15]. Kwon YC's team has designed a storage and computing engine based on non-traditional architecture to reduce off chip loan requirements for integrated storage and computing chips. In the initial stage of off chip coarsening, the engine provides four times higher bandwidth than traditional



FIGURE 1. The research architecture.

systems through group level parallelism, meeting the bandwidth requirements of computation [16]. Sakr C's team has proposed a signal processing method to enhance the balance between energy and accuracy in integrated storage and computing architectures. The research results indicate that compared with other methods, the proposed method reduces energy consumption by an order of magnitude [17]. Liu Fu's team designed a computing system using crossbar memory, which compresses the weights on the crossbar through a novel time scheduling method to achieve hardware bit line decoupling. The research results indicate that their method is effective [18]. Despite extensive research from the perspectives of field effects and energy structures, there has been relatively little research on memory and computational integrated transistors using electromagnetic structures. From previous research, it can be seen that many studies are still in a state of improving existing computing storage systems and have not invested in the development of new architectures. At the same time, there is a lack of overall evaluation of storage integration when improving the performance of the system. At the same time, recent research has shown insufficient consideration for equipment energy consumption issues. Therefore, this study focuses mainly on magnetic skyrmions and designs a current driven memory and computational integrated transistor. The research architecture is shown in Figure 1.

II. DESIGN OF ARTIFICIAL INTELLIGENCE TRANSISTORS AND PREPARATION FOR INTEGRATED STIRAGE AND COMPUTING

A. DESIGN OF CURRENT-DRIVEN SKYRMION TRACK MEMORY

With the increasing growth rate and processing requirements of modern network data, traditional computing systems are gradually approaching saturation in performance, unable to



FIGURE 2. Hierarchy of storage units.

meet computing and storage needs, and there is a necessary need for higher performance computing and storage. Therefore, it is necessary to study the design method. In the architecture of research construction, artificial intelligence is reflected in the form of algorithmic tools, whose main function is to optimize the transmission process of skyrmions and achieve efficient transmission.

When researching the design and preparation of integrated artificial intelligence transistors for storage and computing, integrated transistors can be divided into two main modules: memory devices and logic computing devices. Memory devices can themselves be divided into two parts: storage unit and memory. Because the ferromagnetic film can be generated and eliminated reversibly when the spin-polarized current is locally connected to the ferromagnetic film, the method used for building a stack structure on the ferromagnetic layer was adopted in the current work to design the storage cell. The storage unit structure consists of a thermal potential layer, a pinned layer, a tunneling layer, a free layer, and a stack of heavy-metal layers [19], [20]. The free and pinned layers have vertical magnetic anisotropy. The hierarchical structure of the storage unit is shown in Figure 2.

As illustrated in Figure 2, the vertically flowing unidirectional-current stack structure enters the free layer, and transfers the torque effect through spin, generating a skyrmion in the ferromagnetic uniform state. In addition, the temperature of the free layer can also be increased through the Joule thermal effect to realize the reversible operation, erase the skyrmion, restore the ferromagnetic uniformity, and achieve the effect of writing data information. When the free layer is in the ferromagnetic uniform state, the magnetic tunnel is in the low-resistance state, which can be recorded as "0" at this time. When the free layer is in the skyrmion state, the magnetic tunnel is in the high-resistance state, which can be recorded as "1" at this time. This switching achieves the effect of data information storage. The LLG equation with spin moment term and disturbance field in the magnetized state of the free layer is shown in Formula (1).

$$\frac{\partial m}{\partial t} = -\gamma m \times \left(H_{eff} + H_T\right) + \alpha \left(M \times \frac{\partial m}{\partial t}\right) + \Gamma_{ST} \quad (1)$$

In Formula (1), *m* represents the unit magnetization vector on the free layer, *t* represents the time, γ represents the gyromagnetic ratio, α represents the damping coefficient, H_{eff} represents the effective field, H_T represents the thermal disturbance field, and Γ_{ST} represents the spin transfer torque term. The saturation magnetization is shown in Formula (2).

$$M_s(T) = M_s(0) \cdot \left(1 - BT^{1.5}\right)$$
(2)

In Formula (2), T represents temperature and B represents the Bloch constant. The relationship between magnetic anisotropy and saturation magnetization can be further expressed, as shown in Formula (3).

$$\frac{K_u(T)}{K_u(0)} = \left[\frac{M_s(T)}{M_s(0)}\right]^2 \tag{3}$$

In the one-dimensional thermal diffusion model, as the current enters the magnetic tunnel junction and causes heating, the temperature change in the free layer can be determined using Formula (4).

$$T = T_{RT} + aP\left[1 - \exp\left(-\frac{t}{\tau}\right)\right] \tag{4}$$

In Formula (4), T_{RT} represents the indoor temperature, τ represents the thermal characteristic time constant, and *a* can be calculated using Formula (5).

$$a = \frac{d_{TB}}{2k_{TB}A} \tag{5}$$

In Formula (5), d_{TB} represents the thickness of the thermal barrier layer, k_{TB} represents the thermal conductivity of the thermal barrier layer, and *A* represents the area of the magnetic tunnel junction from a planar perspective. *P* can be calculated using Formula (6).

$$P = I^2 R \tag{6}$$



FIGURE 3. Motion track of skyrmion.

In Formula (6), I represents the specification of the writing current. After the current is stopped, the free layer can cool down, and the temperature change can be calculated using Formula (7).

$$T = T_{RT} + (T_0 - T_{RT}) \cdot \exp\left(-\frac{t}{\tau}\right)$$
(7)

The main constraint of formula (7) is that the current is constant, and the skyrmion needs to be in a stationary state at the beginning. In Formula (7), T_0 represents the temperature at which the current is stopped. Because the skyrmion is driven by the influence of spin track torque caused by current, a magnetic skyrmion track memory based on current drive was researched and designed, and this was used in combination with the memory cell. Although there have been examples of the application of skyrmions in track memory, the Hall effect of the skyrmion presents a problem for designers of such applications. When moving along the direction of the nanowire, the skyrmion is affected by the Magnus force, resulting in a certain deviation from the predetermined trajectory. The specific motion trajectory is shown in Figure 3.

Figure 3 shows the transverse displacement phenomenon caused by the Magnus force when the skyrmion moves in the direction of the nanowire. The term "nanowire" refers to a narrow wire-like structure that serves as a track along which the skyrmion moves. It provides a confined pathway for the skyrmion motion within the memory device. The Magnus force is a physical phenomenon that arises due to the interaction between the spin of the electrons carrying the current and the magnetic moments in the skyrmion [21]. It is an inherent property of the skyrmion and is not influenced by external factors. The Magnus force acts perpendicular to both the direction of the skyrmion's velocity and its spin, resulting in a sideways force. This force causes the skyrmion to deviate from its original path, leading to the transverse displacement phenomenon depicted in Figure 3. In summary, the Magnus force is an intrinsic property of the skyrmion and arises due to the interaction between the skyrmion's spin and the moving electrons' spins. It causes the skyrmion to deviate from its intended trajectory as it moves along the nanowire track. This phenomenon often occurs in the initial stage of movement. After traversing for a certain distance, the skyrmion exhibits a stable forward motion near the boundary. This is because, at this time, the skyrmion is simultaneously affected by the



FIGURE 4. Stress diagram of skyrmion.

Magnus force and the boundary repulsion force. The two forces interact and cancel each other out; consequently, the skyrmion orbit is reshaped. When the boundary repulsion force and Magnus force are no longer able to effectively interact with each other due to the excessive current, this leads to a collision between the skyrmion and the boundary, and annihilation eventually results. In this study, a boundary zone was set to suppress the Hall effect of the skyrmion. It was necessary to locate this boundary zone on the side of the nanowire perpendicular to the magnetic anisotropy, while facing the anisotropy. At the same time, the magnetization direction of the boundary region is opposite to that of the boundary region of the skyrmion. This gives the field a stronger boundary repulsion force, which can then be balanced with the Magnus force under a strong current to inhibit the Hall effect. By such means, the forward movement of the skyrmion can be maintained under an appropriate level of current, so that the track memory has a higher stability. The stress diagram of the skyrmion is shown in Figure 4.

The Landau–Lifshitz–Gilbert (LLG) equation can now be used to simulate the process simulation of current-driven motion, as shown in Formula (8).

$$\frac{\partial m}{\partial t} = -\gamma m \cdot H_{eff} + \alpha \left(m + \frac{\partial m}{\partial t} \right) + \Gamma_{ST} \qquad (8)$$

In Formula (8), *m* represents the unit magnetization vector of the free layer, *t* represents the time, γ represents the gyromagnetic ratio, α represents the damping coefficient, and H_{eff} represents the effective field.



FIGURE 5. Free-layer skyrmion control.



COMBINED-CURRENT-AND-VOLTAGE SKYRMION CIRCUIT LOGIC GATE DEVICES

To achieve integration of storage and computing, a reconfigurable logic gate device was designed, using skyrmions as the main data carrier. The device combines the motion laws affecting skyrmions under current control to achieve logic operation based on nanowire transmission. This period mainly consists of three parts, namely, the device input end, transmission channel, and device output end. The input end of the device is dominated by the magnetic tunnel junction structure, which controls the skyrmion in the free layer through current pulse.

As illustrated in Figure 5, when the input voltage is below the critical point of the topological stability energy barrier, a skyrmion is not generated in the free layer, and the input is recorded as "0". When the input voltage is above the critical point of the topological stability energy barrier, a skyrmion is generated, and the input is recorded as "1". The skyrmion formed at the input end moves under the influence of the spin torque formed by the current entering the heavy-metal level. The movement tracks occurring in different transmission channel structures are often different. The output terminal is a kind of magnetic tunnel junction, which can detect the skyrmion in the free layer. There are different types of magnetic tunnel junction at the output terminal, and these can be divided into four types: parallel state, quasi-antiparallel state, antiparallel state and quasi-parallel state. The parallel state is the state without a skyrmion in which the resistance state is the low-resistance state and the binary datum is "0". The quasi-antiparallel state is the state without a skyrmion in which the resistance state is the high-resistance state and the binary datum is "1". The antiparallel state is the state without a skyrmion in which the resistance state is the high-resistance state, and the binary datum is "1". The quasi-parallel state is the state without a skyrmion in which the resistance state is the low-resistance state and the binary datum is "0".

The realization of the skyrmion logic gate device depends on a holistic detection structure. When implementing the "AND" logic in the logic gate, the transmission orbit is mainly connected by two nanowires, with different input magnetic tunnels located on the left, and the output magnetic tunnel junction located in the bottom-right corner. Here, the output layer of the output magnetic tunnel junction needs to



FIGURE 6. AND operation structure.

maintain an upward magnetization direction. If the output terminal detects a skyrmion, "0" is output, otherwise "1" is output. The specific device structure obtained is shown in Figure 6.

When the input data of the two input terminals A and B output "0" at the same time, there is no skyrmion in the transmission track, and the final output Y is "0". At this time, in the absence of the skyrmion, the system is in a low-resistance state, as expressed as Formula (9).

$$\begin{cases} A = 0 (V_{in} < V_c) \\ B = 0 (V_{in} < V_c) \end{cases}, y = 0$$
(9)

When the input datum of input A in the two input terminals is "0", and the input datum of input B is "1", the transmission track also cannot detect the skyrmion and is in a low-resistance state, as expressed in Formula (10).

$$\begin{cases} A = 0 (V_{in} < V_c) \\ B = 1 (V_{in} > V_c) \end{cases}, y = 0$$
(10)

When the input datum of input A in the two input terminals is "1", and the input datum of input B is "0", the transmission track cannot detect the skyrmion, but it is in a high-impedance state, as expressed in Formula (11).

$$\begin{cases} A = 1 (V_{in} > V_c) \\ B = 0 (V_{in} < V_c) \end{cases}, y = 0$$
(11)

When the input datum of input A in the two input terminals is "1" and the input datum of input B is "0", the transmission track can detect the skyrmion, and it is in a high-impedance state, as expressed in Formula (12).

$$\begin{cases}
A = 1 (V_{in} > V_c) \\
B = 1 (V_{in} > V_c)
\end{cases}, y = 1$$
(12)

When implementing the "OR" logic in the logic gate, it is necessary to adjust the track position and structure and transfer the output end to the upper right, as shown in Figure 7.

Given the characteristic of magnetic skyrmions being driven by nanoscale currents, the distance between the input and output contacts is set to 50 nanometers. In Figure 7, both the lower-left and upper-left corners of the skyrmion are affected by the Hall effect in the current drive process, and

Parameter	Parameter Code	Parameter Code	
Simulation grid unit size	\	$1 \times 0.2 \times 1 \text{ nm}^3$	
Spin Hall angle	$ heta_{S\!H}$	0.08	
Damping coefficient	α	0.3	
Exchange constant	A_{ex}	$1.5 \times 10^{-11} \text{ J/m}$	
DM interaction constant	D	$3.0 \times 10^{-3} \text{ J/m}^2$	
Magnetic anisotropy constant	K_u	$0.8 \times 10^{6} \text{ J/m}^{3}$	
Saturated magnetization	M_{s}	$5.8 \times 10^5 \text{ A/m}$	

TABLE 1. Simulation parameters.



FIGURE 7. OR operation structure.

they reach the output terminal in the upper-right corner. When there are two moving skyrmions in the transmission track at the same time, the skyrmion at the top can be at the output end at the top right, while the skyrmion at the bottom is blocked by a deliberately set gap after collision with the skyrmion at the top, and finally stops at the lower position. To ensure collision between the two skyrmions at the junction, a gap is artificially set at the upper boundary to adjust the movement track of the bottom skyrmion. At this time, as long as one output is "1", then the output terminal can successfully detect the skyrmion and then output "1". When the input data of input terminal A and input terminal B in the two input terminals are both "0", the transmission track cannot detect the skyrmion and is in the low-resistance state, as expressed in Formula (13).

$$\begin{cases} A = 0 (V_{in} < V_c) \\ B = 0 (V_{in} < V_c) \end{cases}, y = 0$$
(13)

When the input datum of input A in the two input terminals is "0" and the input datum of input B is "1", the transmission track can detect the skyrmion and is in the high-impedance state, as expressed in Formula (14).

$$\begin{cases} A = 0 (V_{in} < V_c) \\ B = 1 (V_{in} > V_c) \end{cases}, y = 1$$
(14)

When the input datum of input A in the two input terminals is "0" and the input datum of input B is "1", the transmission track can detect the skyrmion and is in the high-impedance state, as expressed in Formula (15).

$$\begin{cases} A = 1 (V_{in} > V_c) \\ B = 0 (V_{in} < V_c) \end{cases}, y = 1$$
(15)

When the input datum of input A in the two input terminals is "1" and the input datum of input B is "0", the transmission track can detect the skyrmion and is in the high impedance state, as shown in Formula (16).

$$\begin{cases} A = 1 (V_{in} > V_c) \\ B = 1 (V_{in} > V_c) \end{cases}, y = 1$$
(16)

Implementation of logical 'N' can be achieved by switching the output direction of the magnetic tunnel junction pinning layer at the output end. At this time, there is one input terminal and one output terminal. When the input terminal is "0", then $V_{in} < V_c$, the skyrmion can be detected, and the system presents a high-resistance state. When the input terminal is 1, then $V_{in} > V_c$, no skyrmion can be detected, and the system presents a low-resistance state.

III. SIMULATION ANALYSIS OF ARTIFICIAL INTELLIGENCE TRANSISTOR FOR INTEGRATED STORAGE AND COMPUTING

The micromagnetics software OOMMF was used to conduct micromagnetics simulation experiments. The simulation structure of the components adopted the memory-andlogic-operation component structure of the material system described above, with a double-layer film nanowire structure of heavy metal and ferromagnetic layers. The ferromagnetic layer was perpendicular to the magnetization zone; its size was 400 nm \times 40 nm \times 1 nm, including the boundary zone of in-plane magnetization. The specific simulation parameters are shown in Table 1.

The study calibrated the simulation before conducting the simulation, as shown in Table 2

From the calibration results, it can be seen that the effectiveness of the operation is verifiable. The simulation obtained the state of change formed by the transverse and longitudinal displacements of the lattice under different DM interaction constants in the boundary region over time, as shown in Figure 8.

It can be seen in Figure 8 that, under the parameter Db = 0 mJ/m2, different boundary zone widths show different temporal displacement trends of the skyrmion. When Wb = 0 nm, the position of the temporal lateral displacement curve

IEEEAccess

Time (seconds)	Middle region width (in nanometers)	Lateral displacement position	Longitudinal displacement position	Validity of logical operations
t=0	0	Upper end	Lower end	/
t=1	18	Lower end	Upper end	Confirm
t=2	0	Upper end	Lower end	Confirm
t=3	18	Lower end	Upper end	Confirm
t=4	0	Upper end	Lower end	Confirm

TABLE 2. Simulated calibration.



FIGURE 8. States of change formed by the lateral and longitudinal displacements of the lattice over time.

was highest; when Wb = 18 nm, the position of the temporal lateral displacement curve was lowest. The narrower the width of the boundary zone, the more significant the temporal variation of lateral displacement. At the same time, all curves showed a trend of lateral displacement slowing down over time. In terms of longitudinal displacement, when Wb = 0 nm, the position of the temporal longitudinal displacement curve was lowest; when Wb = 18 nm, the position of the temporal longitudinal displacement curve was highest. The wider the boundary zone, the more significant the temporal



FIGURE 9. Relationships between Magnus force, boundary force, and boundary zone width.

variation of longitudinal displacement. In addition, all curves showed a trend of stable growth over time. Under the parameter Db = 3 mJ/m2, different boundary zone widths showed different trends of temporal displacement of the skyrmion. When Wb = 0 nm, the position of the temporal lateral displacement curve was highest; when Wb = 18 nm, the position of the temporal lateral displacement curve was lowest. The narrower the width of the boundary zone, the more significant the temporal variation of lateral displacement. At the same time, all curves showed a trend of lateral displacement slowing down over time. In terms of longitudinal displacement, when Wb = 0 nm, the position of the temporal longitudinal displacement curve was lowest; when Wb = 18 nm, the position of the temporal longitudinal displacement curve was highest. The wider the boundary zone, the greater the temporal variation of longitudinal displacement. At the same time, all curves showed a trend of stable growth over time.

The relationship between Magnus force, boundary force, and boundary zone width is shown in Figure 9.

It can be seen in Figure 9 that when Db = 0 mJ/m2, the Magnus force curve showed a stable growth trend with increasing boundary zone width, which was relatively fast in the early stage and relatively slow in the later stage. When Db = 3 mJ/m2, the Magnus force curve first showed a stable growth trend with increasing boundary zone width, but then decreased in the later stage, with the turning point located at Wb = 8 nm. In terms of boundary forces, when Db = 0 mJ/m2, the boundary force curve showed a stable growth trend with increasing boundary zone width, which was relatively fast in the early stage and relatively slow in the later stage. When Db = 3 mJ/m2, the boundary zone width, which was relatively fast in the early stage and relatively slow in the later stage. When Db = 3 mJ/m2, the boundary force curve first showed a stable growth trend with increasing boundary zone width, but then decreased in the later stage, with the turning point located at Wb = 12 nm.

With respect to the calculation of effective field, the relationship between effective field components and coordinates is shown in Figure 10.

It can be seen in Figure 10 that the absolute value of the effective field component is relatively large near the boundary zone. This is caused by the gradient of the magnetic moment vector in space, resulting in a significant change in magnetic moment orientation near the boundary, leading to an increase in the effective field component. When Db = 0 mJ/m2, the effective field component monotonically increased with the width of the boundary zone. When Db = 3 mJ/m2, the absolute value of the effective field component reached its maximum at Wb = 10 nm.

Next, the performance of skyrmion logic gates was assessed. The operation efficiency of the skyrmion logic gate mainly depended on the transmission efficiency of the skyrmion between the input and output. The motion of a skyrmion is influenced by multiple factors, including both the magnitude of the driving current and the influence of the boundary. These factors may all lead to non monotonic changes in the effective magnetic field. Especially when the interaction force increases, the motion of the skyrmions is more susceptible to interference and exhibits non monotonicity.

Therefore simulated the speed of the skyrmion, and the specific results are shown in Figure 11.

Figure 11a shows the relationship between the moving speed of the skyrmion and the density of the driving current. A compromise between operation time and power consumption was evident. There was also a positive proportional relationship between the moving speed of the skyrmion and the density of the driving current. At the same time, as illustrated in Figure 11b, the speed of the skyrmion was affected by the magnetic parameters of the ferromagnetic layer. In its

IEEEAccess



components and coordinates $(D_b = 0 \text{mJ/m}^2)$

components and coordinates ($D_b=3mJ/m^2$)







FIGURE 12. Effectiveness simulating of skyrmion logic operation.

stable state, the velocity of the skyrmion increased with decreases in the magnetic anisotropy constant, and also with increases in the DM interaction constant. In addition, the diameter of the skyrmion decreased with increases in the magnetic anisotropy constant, and also with decreases in the DM interaction constant, as illustrated in Figure 11c, The

relationship between the moving speed of the skyrmion and the driving current density can be explained by the underlying physics of skyrmion dynamics and current-induced spin torques. In magnetic systems, skyrmions are topologically stable spin textures characterized by a swirling spin configuration. They can be manipulated and moved by applying spin-polarized currents. The motion of skyrmions is governed by the interplay of various forces, including the Magnus force and the spin transfer torque. When a current is passed through a material, it exerts a spin transfer torque on the localized magnetic moments, including those forming the skyrmion. The spin transfer torque arises due to the interaction between the electron spins in the current and the local magnetic moments. This torque can exert a force on the skyrmion, causing it to move. The driving current density determines the strength of the spin transfer torque applied to the skyrmion. Higher current densities result in a stronger torque, leading to a higher driving force on the skyrmion. Consequently, the skyrmion moves faster with increasing current density. The speed of the skyrmion is crucial for the operation of logic gates based on skyrmions. Logic gates utilize the presence or absence of a skyrmion to represent binary information (e.g., 0 or 1). The speed at which the skyrmion can move determines the response time of the logic gates. Faster skyrmion motion allows for quicker information processing and gate operations. Therefore, the direct proportionality between the moving speed of the skyrmion and the driving current density is essential for achieving faster logic gate operations. By increasing the current density, the skyrmion can be driven more quickly, enabling faster switching and computational processes in skyrmion-based logic gates.

Finally, the effectiveness of skyrmion logic operation under different input conditions was simulated, as shown in Figure 12.

As can be seen in Figure 12, when the input end produced a skyrmion, the skyrmion was affected by the Hall effect to reach the upper output end. When two skyrmions were generated at the input end, they would collide in the connection area in the middle. One would then reach the upper input end and the other would reach the lower input end. As a result, the upper end was mainly used for performing NOR operations, while the lower end was mainly used for performing NAND operations, and we confirmed the effectiveness of the of our research design pattern.

IV. CONCLUSION

In this study, a transistor structure with integrated memory and logic operation was designed using skyrmions as a main tool. The structure was composed of two main modules: a current-driven skyrmion track memory; and skyrmion logic gate components. Simulation methods were then used for device simulating, and the results showed that when Db =0 mJ/m2 and Db = 3 mJ/m2, the position of the temporal lateral displacement curve was highest at Wb = 0 nm, while the position of the temporal lateral displacement curve was lowest at Wb = 18 nm. The results for longitudinal displacement were exactly the opposite. In addition, when Db = 0 mJ/m2, the effective field component monotonically increased with the width of the boundary zone, and when Db = 3 mJ/m2, the absolute value of the effective field component reached its maximum at Wb = 10 nm. In the performance simulation of logic gates, the moving speed of the skyrmion was in direct proportion to the driving-current density. The speed of the skyrmion increased with decreases in the magnetic anisotropy constant and increases in the DM interaction constant. At the same time, in the effectiveness simulation, the skyrmion demonstrated its effectiveness under different generation conditions of the logic gate. Its upper end was mainly used for execution of the NOR operation, and its lower end was mainly used for execution of the NAND operation. From these findings, we conclude that the research and design of our integrated- storage-and-computing architecture was effective, and that this design may provide an optional solution for new miniaturized computing systems.

REFERENCES

- B. Dieny et al., "Opportunities and challenges for spintronics in the microelectronics industry," *Nat. Electron.*, vol. 3, pp. 446–459, Aug. 2020.
- [2] Y. Zhang, Y. Zhu, S. Zheng, L. Zhang, X. Shi, and J. He, "Ink formulation, scalable applications and challenging perspectives of screen printing for emerging printed microelectronics," *J. Energy Chem.*, vol. 63, pp. 498–513, Dec. 2021.
- [3] S. U. Khalid, H. Babar, H. M. Ali, M. M. Janjua, and M. A. Ali, "Heat pipes: Progress in thermal performance enhancement for microelectronics," *J. Therm. Anal. Calorim*, pp. 2227–2243, 2021.
- [4] J. F. Sierra, J. Fabian, R. K. Kawakami, S. Roche, and S. O. Valenzuela, "Van der Waals heterostructures for spintronics and opto-spintronics," *Nat. Nanotechnol.*, vol. 16, no. 8, pp. 856–868, 2021.
- [5] Q. L. He, T. L. Hughes, N. P. Armitage, Y. Tokura, and K. L. Wang, "Topological spintronics and magnetoelectronics," *Nat. Mater.*, vol. 21, no. 1, pp. 15–23, Jan. 2022.
- [6] Z. Guo, J. Yin, Y. Bai, D. Zhu, K. Shi, G. Wang, K. Cao, and W. Zhao, "Spintronics for energy- efficient computing: An overview and outlook," *Proc. IEEE*, vol. 109, no. 8, pp. 1398–1417, Aug. 2021.
- [7] H. Li, P. Xu, D. Liu, J. He, H. Zu, J. Song, J. Zhang, F. Tian, M. Yun, and F. Wang, "Low-voltage and fast-response SnO₂ nanotubes/perovskite heterostructure photodetector," *Nanotechnology*, vol. 32, no. 37, 2021, Art. no. 375202.
- [8] J. He, P. Xu, R. Zhou, H. Li, H. Zu, J. Zhang, Y. Qin, X. Liu, and F. Wang, "Combustion synthesized electrospun InZnO nanowires for ultraviolet photodetectors," *Adv. Electron. Mater.*, vol. 8, no. 4, Apr. 2022, Art. no. 2100997.
- [9] S. Gao, H. D. Rosales, F. A. G. Albarracín, V. Tsurkan, G. Kaur, T. Fennell, P. Steffens, M. Boehm, P. Čermák, A. Schneidewind, E. Ressouche, D. C. Cabra, C. Rüegg, and O. Zaharko, "Fractional antiferromagnetic skyrmion lattice induced by anisotropic couplings," *Nature*, vol. 586, no. 7827, pp. 37–41, 2020.
- [10] K. M. Song, J.-S. Jeong, B. Pan, X. Zhang, J. Xia, S. Cha, T.-E. Park, K. Kim, S. Finizio, J. Raabe, J. Chang, Y. Zhou, W. Zhao, W. Kang, H. Ju, and S. Woo, "Skyrmion-based artificial synapses for neuromorphic computing," *Nat. Electron.*, vol. 3, no. 3, pp. 148–155, Mar. 2020.
- [11] D. Wolf, S. Schneider, U. K. Rößler, A. Kovács, M. Schmidt, R. E. Dunin-Borkowski, B. Büchner, B. Rellinghaus, and A. Lubk, "Unveiling the three-dimensional magnetic texture of skyrmion tubes," *Nature Nanotechnol.*, vol. 17, no. 3, pp. 250–255, Mar. 2022.
- [12] J. Pan, K. L. Low, J. Ghosh, S. Jayavelu, M. M. Ferdaus, S. Y. Lim, E. Zamburg, Y. Li, B. Tang, X. Wang, J. F. Leong, S. Ramasamy, T. Buonassisi, C.-K. Tham, and A. V.-Y. Thean, "Transfer learning-based artificial intelligence-integrated physical modeling to enable failure analysis for 3 nanometer and smaller silicon-based CMOS transistors," ACS Appl. Nano Mater., vol. 4, no. 7, pp. 6903–6915, 2021.

IEEEAccess

- [13] J. Noh, H. Bae, J. Li, Y. Luo, Y. Qu, T. J. Park, M. Si, X. Chen, A. R. Charnas, W. Chung, X. Peng, S. Ramanathan, S. Yu, and P. D. Ye, "First experimental demonstration of robust HZO/β-Ga₂O₃ ferroelectric field-effect transistors as synaptic devices for artificial intelligence applications in a high-temperature environment," *IEEE Trans. Electron Devices*, vol. 68, no. 5, pp. 2515–2521, May 2021.
- [14] S. Xin, Y. Chang, R. Zhou, H. Cong, L. Zheng, Y. Wang, Y. Qin, P. Xu, X. Liu, and F. Wang, "Ultraviolet-driven metal oxide semiconductor synapses with improved long-term potentiation," *J. Mater. Chem. C*, vol. 11, no. 2, pp. 722–729, 2023.
- [15] Y. Cao, T. Zhao, C. Zhao, Y. Liu, P. Song, H. Gao, and C. Z. Zhao, "Advanced artificial synaptic thin-film transistor based on doped potassium ions for neuromorphic computing via third-generation neural network," *J. Mater. Chem. C*, vol. 10, no. 8, pp. 3196–3206, Feb. 2022.
- [16] D. Hao, J. Zhang, S. Dai, J. Zhang, and J. Huang, "Perovskite/organic semiconductor-based photonic synaptic transistor for artificial visual system," ACS Appl. Mater. Interfaces, vol. 12, no. 35, pp. 39487–39495, 2020.
- [17] O. Leitersdorf, R. Ronen, and S. Kvatinsky, "MultPIM: Fast stateful multiplication for processing-in-memory," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 69, no. 3, pp. 1647–1651, Mar. 2022.
- [18] C. Sakr and N. R. Shanbhag, "Signal processing methods to enhance the energy efficiency of in-memory computing architectures," *IEEE Trans. Signal Process.*, vol. 69, pp. 6462–6472, 2021.
- [19] Y.-C. Kwon et al., "25.4 a 20nm 6GB function-in-memory dram, based on HBM2 with a 1.2TFLOPS programmable computing unit using bank-level parallelism, for machine learning applications," in *Proc. IEEE Int. Solid-State Circuits Conf. (ISSCC)*, vol. 64, San Francisco, CA, USA, Feb. 2021, pp. 350–352.
- [20] P. Xu, Q. Yuan, W. Ji, Y. Zhao, R. Yu, Y. Su, and N. Huo, "Study on electrochemical properties of carbon submicron fibers loaded with cobaltferro alloy and compounds," *Crystals*, vol. 13, no. 2, p. 282, Feb. 2023.
- [21] F. Liu, W. Zhao, Z. Wang, Y. Zhao, T. Yang, Y. Chen, and L. Jiang, "IVQ: In-memory acceleration of DNN inference exploiting varied quantization," *IEEE Trans. Comput.-Aided Design Integr. Circuits Syst.*, vol. 41, no. 12, pp. 5313–5326, Dec. 2022.



PEILONG XU was born in Qingdao, Shandong, China, in 1977. He received the M.S. degree from the School of Software, Tongji University, Shanghai, in 2007. He is currently pursuing the Ph.D. degree in computer engineering with Pukyong National University. In 2008, he was with the State Key Laboratory, Qingdao University. His research interests include the experimental and performance analysis of artificial intelligence transistor electrical materials and the characterization of material properties.



INCHEOL SHIN (Member, IEEE) was born in Incheon, Republic of Korea, in 1977. He received the Ph.D. degree from the Department of Computer Engineering, University of Florida. He is currently a Professor with the Department of Artificial Intelligence Convergence, Pukyong National University. His research interests include artificial intelligence software and hardware integration, algorithm optimization, computer engineering, and computer security.

...