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RESEARCH ARTICLE

A Dual-Wordline 6T SRAM Computing-In-Memory Macro Featuring Full Signed Multi-Bit Computation for Lightweight Networks

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ABSTRACT In this paper, we present an analog-mixed-signal 6T SRAM computing-in-memory (CIM) macro. The macro uses dual-wordline 6T bitcells to reduce power consumption and write-disturb issues. The macro also proposes an analog computation logic circuit for high precision, energy efficient charge-domain computation. The bitcell structure combined with the analog computation logic circuit allows direct input of signed activations and weights to the chip for full signed computation. The proposed macro consists of four CIM blocks, each with four 32 × 8 compute blocks, a pulse generator, an analog computation logic circuit and a SAR-ADC. Fabricated in a 55 nm process, our CIM macro test chip achieves an energy efficiency of 7.3 TOPS/W. A comprehensive computing test that encompasses the entire range of inputs and weights has been conducted. The results show that the CIM macro test chip can achieve a precision of 79.51% in a 1-FE error range of 71.88%. The target application of the proposed CIM macro is lightweight neural networks, this is demonstrated by mapping a pre-trained network into the macro and achieving a recognition accuracy of 92.28% on the CIFAR-10 dataset. The design surpasses existing designs in comprehensive consideration of energy efficiency, technology and bit width.

INDEX TERMS Computing-in-memory, SRAM, dual-wordline, neural network, charge-domain, multiply-and-accumulate.

I. INTRODUCTION

Over the last few years, SRAM-based CIM designs have demonstrated their advantage in significantly improving energy efficiency through reducing data movement, showing potential application in deep learning (DL) based edge computing devices [1], [2], [3], [4], [5], [6], [7], [8]. Recent works show CIMs being implemented across a wide variety of technologies and covering more novel application scenarios [9]. This indicates a transformation in the research direction of CIM, from solely pursuing energy efficiency to pursuing a balance between performance and functionality. Recent works [10], [11], [12], strengthen the relationship between algorithm and CIM structure, thereby making CIM designs more domain specific to enhance performance for practical scenarios.

Analog-mixed-signal SRAM-based CIM designs have unique advantages compared to other CIM categories, such as high computation parallelism, significant shorter access time, industrial maturity and relatively low energy cost when performing signed bit and floating-point computing operations [13]. However, analog-mixed-signal CIMs face

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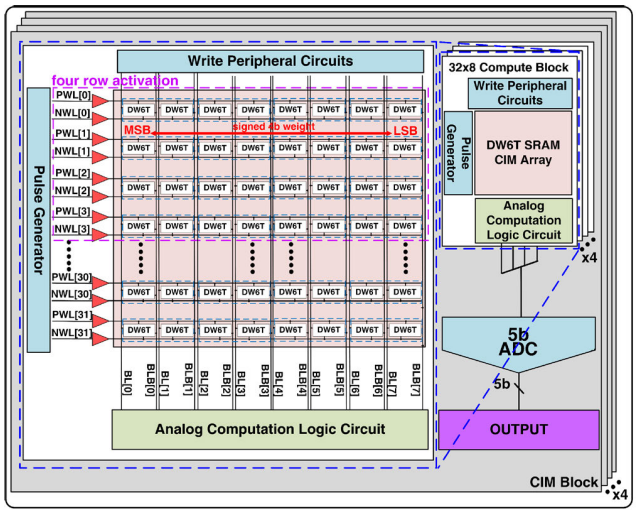


FIGURE 1. Structure of proposed DW6T SRAM based CIM.

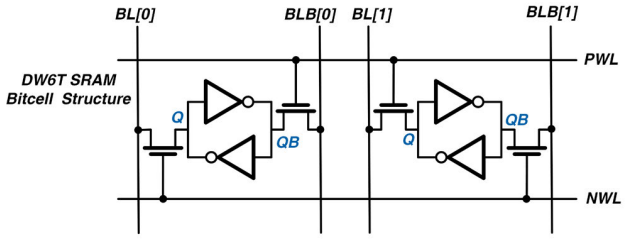
challenges including high ADC overhead and decreased precision caused by non-idealities. Apart from using design techniques to overcome these problems, a meaningful topic is to broaden the functions of analog-mixed-signal CIMs and find suitable fields of application to leverage the advantages of high computation speed without being affected by the disadvantages of certain accuracy lost. Analog-mixed-signal SRAM-based CIMs have become the preferred design for simple image and speech recognition tasks when moderate precision is required. The value of analog-mixed-signal integrates sensing, storage and computing functions on a single chip. In this situation, signals are sampled in the analog domain [14] and computation speed is required to keep up with the sensor sampling speed. Another field which shows their advantage is sparse lightweight networks [15], [16], a main category under neural networks. In contrast to digital SRAM-based CIMs, which trade more area and computing time for higher precision [17], [18], [19], [20], analog-mixed-signal SRAM-based CIMs perform small kernel convolution computations in a single cycle, significantly reducing computation time at the cost of minor recognition rate lost [21], [22], [23]. The lightweight network's high parallelism and energy efficiency computing requirements when using small convolution kernels, as well as its high tolerance for computational accuracy, perfectly match the characteristics of analog in-memory computing. However, application for analog-mixed-signal SRAM-based CIM designs on lightweight networks still need more research. The computing method and circuit structure that can perform the most efficient computation in the context of lightweight networks requires further discussion. Additionally, how to meet the needs of specific applications, such as full signed multi-bit computation, also deserves further research.

In this work, we introduce an analog-mixed-signal multi-bit CIM based on a 4kb Dual-Wordline 6T SRAM (DW6T SRAM) macro fabricated in 55 nm process. It supports full signed multi-bit computation for better recognition accuracy. The overall structure is shown in Fig. 1. The CIM macro is composed of four 1kb CIM blocks, with each CIM block containing four 32 × 8 compute blocks to perform accumulation of 16 multiplication results. The DW6T SRAM cells, which are modified from compact 6T foundry bitcells with no area increase, store the signed 4b weights for calculation. Utilization of the dual-wordline structure reduces power consumption and write-disturb issue [24] during the computation process. The inputs for calculation are given in the timing domain, produced by an on-chip simple and robust pulse generator. The 3b input is indicated by the length of the pulse and the symbol determines which wordline should be activated. An analog computation logic circuit accumulates the multiplication results on capacitors in the charge-domain, which are subsequently sampled by a SAR-ADC to generate signed 4b outputs. The CIM macro computes 128 multiply-and-accumulate (MAC) operations in parallel, achieving a total energy efficiency of 7.3 TOPS/W, using 16 signed 3b inputs and 64 signed 4b weights. The CIM macro is tested using computation operations under various scenarios for a direct result of the computation accuracy. Power consumption and energy efficiency results are also obtained in this process. Then a lightweight network is mapped onto the macro to perform recognition tests using the CIFAR-10 dataset. The analog-mixed-signal SRAM-based CIM macro, featuring a full signed computation method, exceeding energy efficiency and high precision, acts as a design worthy of reference in similar sparse lightweight network scenarios.

II. COMPUTING-IN-MEMORY ARCHITECTURE AND WORKING MECHANISM

A. COMPUTING-IN-MEMORY ARCHITECTURE

Fig. 2 presents the schematic and layout of the DW6T SRAM cells. As shown, 2 bitcells store one signed bit, while a row of 8 bitcells store a signed 4b weight. The SRAM bitcells are modified from compact foundry bitcells, with a modification that enables the transmission transistor to QB of the left bitcell to share the same wordline with the transmission transistor to Q of the right bitcell, while the other two transmission transistors share another wordline. Signed weight storage can be achieved by utilizing convolutional SRAM write-in method to store the values displayed in the first table in Fig. 2. During the computation phase, a charge accumulation capacitor is shared by the two bitlines of a single SRAM bitcell for the purpose of positive or negative result accumulation. The activation of positive wordline (PWL) or negative wordline (NWL) is determined by the input's symbol, whereas the charge current applied to the charge accumulation capacitor will be determined by the value of Q or QB. Due to this mechanism, two distinct storage methods can be used to store the value '0'. Depending on the activated wordline and stored weight, either the same amount of charge or no charge will be accumulated on both the positive and negative capacitors



Left Bitcell		Right Bitcell		Represent Value
Q	QB	Q	QB	
1	0	1	0	1
0	1	0	1	-1
0	1	1	0	0
1	0	0	1	0

	Left Bitcell		Right Bitcell	
	Q	QB	Q	QB
Charge Accumulation	Positive Cap		Negative Cap	

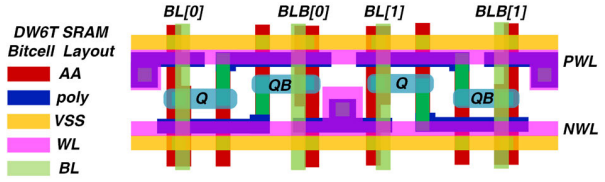


FIGURE 2. DW6T SRAM schematic and layout. Table shows method for storing signed bit in bitcells and the correspondence between storage node and capacitor during computation process.

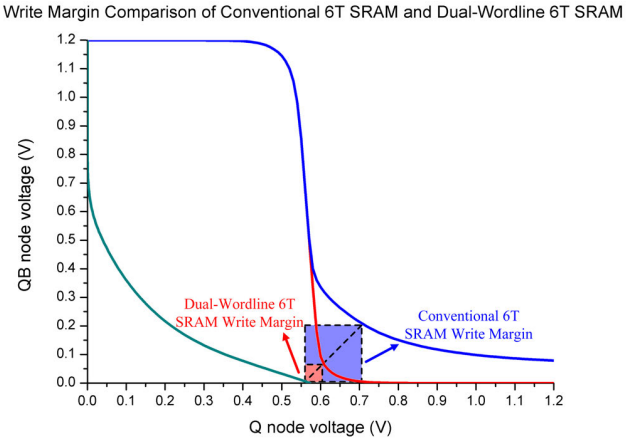


FIGURE 3. Write margin comparison of conventional 6T SRAM and dual-wordline 6T SRAM.

under both methods. Either way, they will neutralize when positive and negative results accumulate.

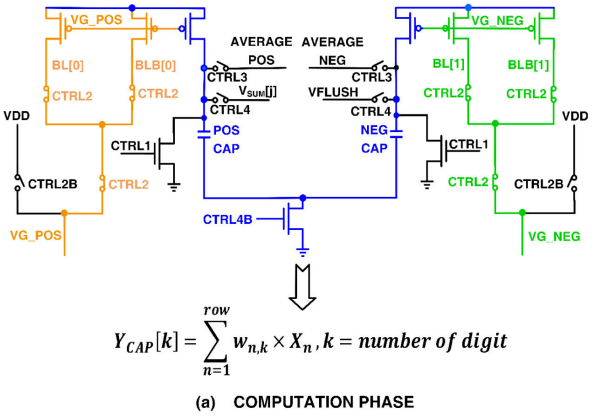
Utilizing the dual-wordline 6T SRAM structure reduces write-disturb issue during the computation process. We plot the ''butterfly curve'' of the conventional 6T SRAM and proposed dual-wordline 6T SRAM in Fig. 3 to compare their write margins. As shown, the write margin of the dual-wordline 6T SRAM is smaller, reducing the likelihood of cells getting overwritten during computation [25]. In dual-wordline 6T SRAM, the flip voltage for '1' to '0' when using 0.9 V and 1.2 V wordline voltage are 20 mV and 250 mV, respectively. In the analog computation logic circuit, the discharge current generated by the bitcells is converted into a charge current for the charge accumulation capacitors through current mirrors. As a result, when activating 1-4 rows simultaneously, the bitline voltages maintain at a stable level far above the flip voltage from '1' to '0', solving the write-disturb issue. Similarly, the state of the cell doesn't flip from '0' to '1'even when bitline voltage is 1.2 V.

B. FULL SIGNED MULTI-BIT COMPUTATION SCHEME

To accomplish the design objective of performing precise, energy efficient full-signed multi-bit computation, our proposed design is innovative in activation input method and result accumulation method. Dual wordlines are used to distinguish the signed digit, while the pulse width varies to signify the magnitude of activation. This activation input method harnesses the benefits of both pulse width modulation and multiple signal control to enhance accuracy. This makes our method stand out from existing single measure methodologies such as: wordline pulse count or pulse width modulation [4], [6], [18], analog input voltage on wordline [26], and multiple input wordlines or signals [1], [27]. Our approach for result accumulation also corresponds with our objective. Charge sharing between charge accumulation capacitors realizes multi-bit computation and ''capacitor stacking'' offers fast speed power saving accumulation between positive and negative results. This is different from [2] and [4] in that they achieve multi-bit computation through charge averaging, and from [28] and [29] in that they achieve multi-bit computation through charge redistribution. The entire signed multi-bit computation scheme is executed using the analog computation logic circuit, and its workflow is divided into four phases, controlled by signals CTRL1-CTRL4. The four phases are introduced in detail below.

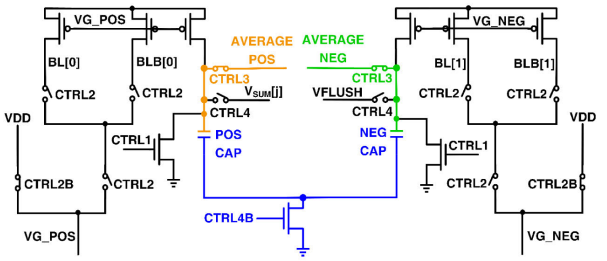
The first phase is the clear phase, and CTRL1 is activated. The charge accumulation capacitors, namely the positive capacitor (POS CAP) and the negative capacitor (NEG CAP) are cleared to prepare for the new cycle of computing.

The computation phase, which is controlled by CTRL2, is the second phase and is depicted in Fig. 4(a). As described in the previous section, activation inputs are given row-wise, in the form of a pulse. The length of the pulses corresponds to the data, while the selection of PWL and NWL varies depending on the symbol. The POS CAP and NEG CAP are charged based on the amount drained by the weights using a current mirror. The current mirror enhances the linearity of analog compute results by stabilizing the voltage on the bitlines throughout the computation phase. Modulating the transistor size of the current mirrors allows for the retention of small capacitor sizes, consequently reducing power consumption. In practical application, four rows are activated



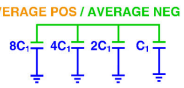
$$Y_{CAP}[k] = \sum_{n=1}^{row} w_{n,k} \times X_n, k = number\ of\ digit$$

(a) COMPUTATION PHASE

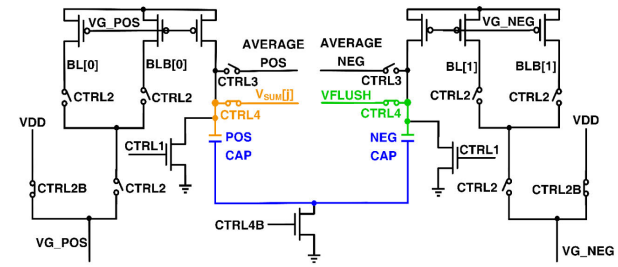


$$Y_{CAP\,TOTAL} = \frac{1}{2^{digit}-1} \sum_{i=1}^{digit} 2^{digit-i} Y_{CAP}[k]$$

$$= \frac{1}{15}(8Y_{CAP}[3] + 4Y_{CAP}[2] + 2Y_{CAP}[1] + Y_{CAP}[0])$$



(b) AVERAGING PHASE



$$V_{SUM}[j] = V_{POS} + (VFLUSH - V_{NEG})$$

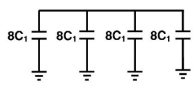
$$= VFLUSH + (V_{POS} - V_{NEG})$$

(c) POS-NEG ACCUMULATION

$$\frac{1}{N}\sum_{j=1}^{N} V_{SUM}[j]$$

$$= \frac{1}{4}(V_{SUM}[0] + V_{SUM}[1] + V_{SUM}[2]$$

$$+ V_{SUM}[4]) = \sum_{i=1}^{16} w_i \times X_i$$



(d) ADC SAMPLING

FIGURE 4. Signed multi-bit computation scheme, showing the workflow of the analog computation logic circuit. (a) Computation phase. (b) Averaging process. (c) Mechanism of how the positive and negative results accumulate. (d) ADC sampling process, the values on the positive capacitors are averaged and sampled.

simultaneously to accumulate 4 multiplication results in a computation unit. Charging of the capacitors finishes within

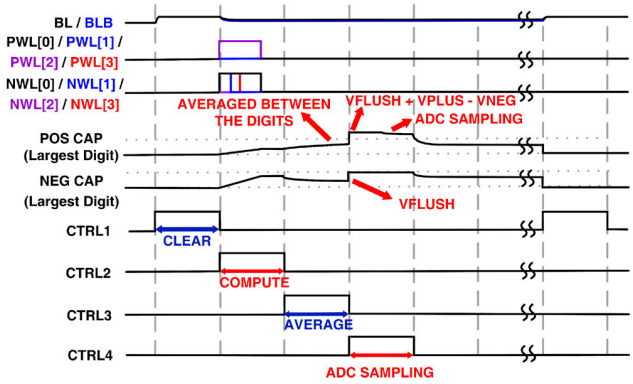


FIGURE 5. Waveform of the signed multi-bit computation scheme. Signals CTRL1-CTRL4 control the different phases of the scheme.

computation phase with CTRL2 having the same duration as the maximum input pulse.

The third phase is the averaging phase, where the positive and negative results of different digits are summed up separately, shown in Fig. 4(b). Signal CTRL3 controls the transistors for charge accumulation capacitor connection. The charge accumulation capacitors of 8 adjacent columns which form a 4b signed weight are geometric, with the biggest capacitance being 8 times the size of the smallest. During the averaging phase, bigger capacitance has a greater impact on the final averaged voltage, reflecting digit difference.

The fourth phase is when the positive and negative results accumulate, followed by ADC sampling, as illustrated in Fig. 4(c) and Fig. 4(d). This is controlled by CTRL4. During POS-NEG accumulation, the connection between ground and the bottom plates of POS CAP and NEG CAP is disconnected, whereas the connection between the two bottom plates remains. In this way, the POS CAP is "stacked" on top of NEG CAP. The voltage of NEG CAP top plate is then pulled up by VFLUSH, and since the electrons of the node connecting the two bottom plates are fixed, the voltage of this node increases by an equal amount as the voltage of NEG CAP top plate has been pulled up. Furthermore, due to the equal capacitance of POS CAP and NEG CAP, the voltage of POS CAP top plate (V_{SUM}[j]) increases the same amount as VFLUSH has pulled up minus the difference of the 2 capacitors, achieving the accumulation of positive and negative results, as shown in (1).

$$V_{SUM}[j] = VFLUSH + (V_{POS} - V_{NEG}) \quad (1)$$

This POS-NEG accumulate process is only performed by the analog computation logic circuit of the largest digit (with $8C_1$ POS CAP / NEG CAP) for faster accumulation and reduced error caused by switches. Four of these results (V_{SUM}[j]) are then averaged for accumulation, and sent to a SAR-ADC for ADC sampling which outputs 5b digital results. Due to this distinct calculation method, bigger ADC output corresponds to bigger positive calculation results, smaller ADC output corresponds to bigger negative calculation results and

TABLE 1. Impact of activating multiple wordlines on analog result precision.

Wordlines Activated	Stored Value	Bitline Voltage (mV)	Discharge Current (μA)
1	0	690	9.62
1	1	1200	0
2	0,0	638	18.6
2	0,1	693	9.58
2	1,1	1200	0
3	0,0,0	596	27.22
3	0,0,1	638	18.72
3	0,1,1	693	9.67
3	1,1,1	1200	0
4	0,0,0,0	565	35.26
4	0,0,0,1	598	27.09
4	0,0,1,1	638	18.61
4	0,1,1,1	694	9.67
4	1,1,1,1	1200	0

"2b'10000" represents the result of 0. The reference voltage of the ADC is adjustable according to the maximum and minimum accumulated calculation results. For instance, when the CIM macro is mapped as the last fully connected layer and calculation results are relatively low, reference voltage can be lowered for better distinction and enhance recognition rate. Our CIM comprises four CIM blocks of the circuits above, sharing the same inputs and different weights, a typical scenario in CNN layers of deep learning networks. The waveform timing diagram for the full signed multi-bit computation process is shown in Fig. 5 for overall examination. Changes of voltage on the charge accumulation capacitors during different phases are given as an example. During circuit design, the size and position of the transistors and capacitors are adjusted according to post-simulation results to reduce non-ideality issues caused by parasitics.

Activation of multiple wordline has an impact on bitcell storage stability and analog result precision. As analyzed in Section II-A, the dual-wordline bitcell structure solves write-disturb problems during computation. Table 1 lists the change in bitline voltage and discharge current corresponding to the difference in activated wordline number and stored value. Results are acquired through simulation using a column of 32 bitcells under tt corner. Through calculation, the average integral nonlinearity (INL) of the discharge current is 0.05 least significant bit (LSB). Considering the small value, the impact on precision is limited when only 4 rows are activated simultaneously, making it acceptable for applications in targeted lightweight network scenarios.

III. STATISTIC ANALYSIS

Fig. 6 illustrates the setup of our test environment, using our CIM macro for tests on accuracy, performance and recognition. The PC uses software tools Vivado and Vitis to program the FPGA board, and it analyzes the calculation results of the CIM macro. The FPGA is for data transfer between the PC and the CIM macro and mode control of the CIM macro. The CIM macro chip is packaged in the COB matter on the test PCB board. A power management circuit is also on the test PCB board to satisfy the different power supply needs of the CIM macro, which includes digital power, analog power, test circuit power, etc. The power analyzer is used to acquire power efficiency results throughout the performance test.

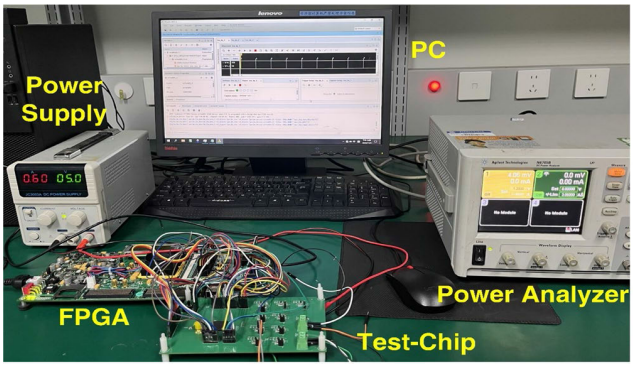
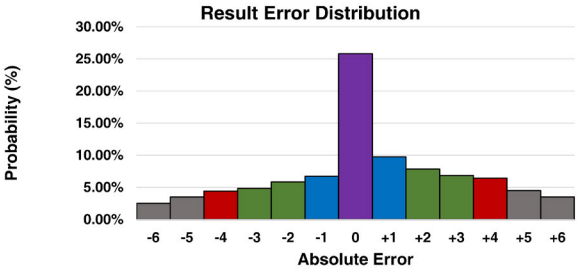


FIGURE 6. Test environment setup for the DW6T CIM macro.



Accuracy Analysis

Error Range	0	-1~+1	-3~+3	-4~+4
$1-FE$	100%	90.65%	78.13%	71.88%
Probability	25.79%	43.25%	68.65%	79.51%

$$Fiducial\ Error\ (FE) = \frac{\Delta_{Error\ Range}}{ADC\ Range} \times 100\% = \frac{\Delta_{Error\ Range}}{32} \times 100\%$$

FIGURE 7. Measured accuracy analysis and result error distribution.

A. COMPUTATION ACCURACY AND PERFORMANCE TEST

The computation accuracy test analyzes the results of 500 computation operations under various computing scenarios, covering the entire computation range. Fiducial Error (FE) is commonly used to express maximum errors coming from limited instrument resolution or quantization during analog-to-digital conversion [30].

$$Fiducial\ Error\ (FE) = \frac{\Delta_{Error\ Range}}{ADC\ Range} \times 100\% \quad (2)$$

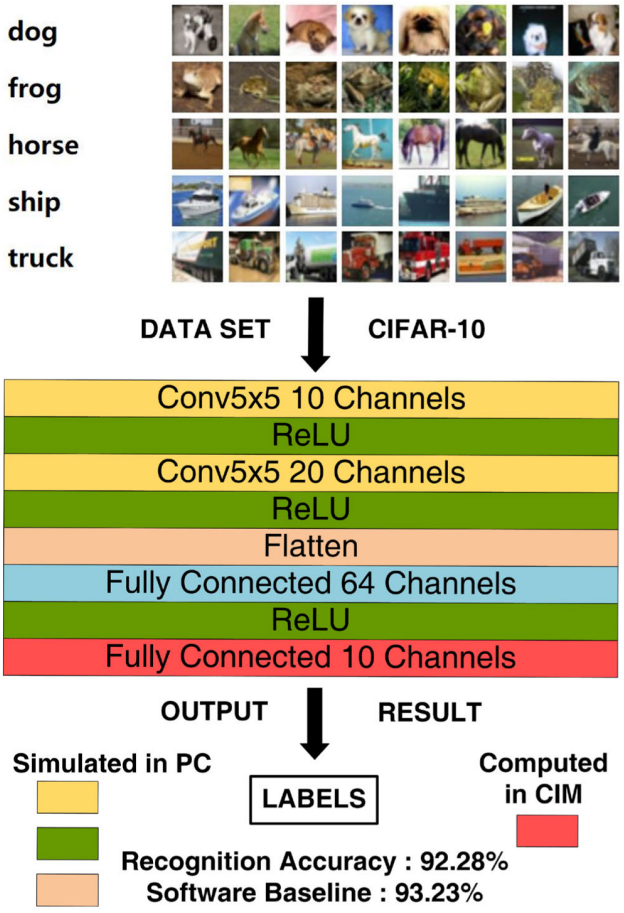


FIGURE 8. CIFAR-10 recognition network schematic.

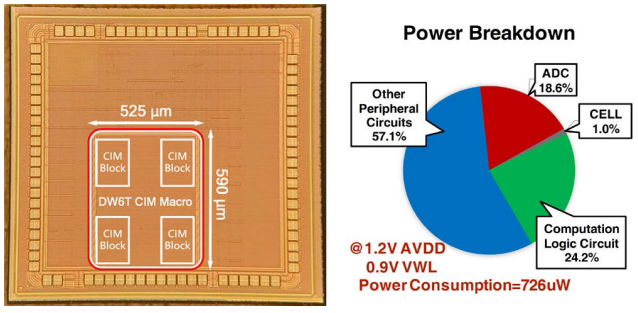


FIGURE 9. Chip micrograph and power breakdown.

By analyzing the value and probability of 1-FE, the influence of the computation result error distribution on the final recognition rate can be intuitively expressed. Using this method, accuracy analyzation reveals that more than 25% of the results have a 1-FE value of 100% (exactly correct), while 79.51% of the results have a 1-FE value of 71.88% (within a ±4 range of the theoretic result). Fig. 7 presents the result error distribution and FE calculation method. Absolute error is the difference between the output result by the CIM macro chip and the ideal result of the weights and inputs imported. Although the same ideal result can be produced by different sets of inputs and weights, when setting digital '1' as LSB, the

TABLE 2. Area statistic comparison.

	[3]	[18]	[12]	[34]	This Work
Type	Digital	Digital	Analog /Mixed	Analog /Mixed	Analog /Mixed
Technology (nm)	28	28	65	28	55
Bitcell Area (um^2)	/	0.7215	2.79	0.257	[a]1.05
[b]Function Area (mm^2)	[c]2.9118	[d]1.7000	1.6632	0.3234	0.0760
[e]Scaled Function Area (mm^2)	9.1501	5.3422	1.2529	1.0162	0.0760
Scaled Function Area Efficiency (GOPS/ mm^2)	8.22	37.44	74.50	122.89	70.12
Die Area(mm^2)	8.97	5.04	/	/	2.02
Scaled Die Area(mm^2)	28.19	15.84	/	/	2.02
Scaled System Area Efficiency (GOPS/ mm^2)	2.67	12.63	/	/	2.64

[a]The area of 2 bitcells are calculated; [b]Function Area = Bitcell Area + Additional CIM Circuits Area; [c]Area of 16 BSOCIMs; [d]Statistics of 5 T-PIM cores using 4bit inputs; [e]Scaled Area = Area × 1.8^$\log_2(55^2$ / technology^2) [31].

average INL of the digital output data can still be calculated with the provided data in the distribution graph, which results in 2.1 LSB, a satisfying result for digital-to-digital whole chip INL [31]. The data provided in the accuracy analysis table can also be used to simulate the performance of our CIM on various neural networks and calculation algorithms. This is done by adding a random offset during accumulation of each 16 multiplication results, with the probability and size of the offset determined by referring to the accuracy analysis table.

B. CIFAR-10 RECOGNITION TEST

The CIM macro is tested in an application scenario using the CIFAR-10 dataset. We use a pre-trained lightweight network as presented in Fig. 8 for implementation. It consists of 2 convolutional layers, 3 ReLU layers, 1 flattening layer and 2 fully connected layers with a total of 26.498K features. Limited CIM macro size still remains as a common challenge in the CIM field, so many CIM designs are tested by only mapping 1 or 2 layers [20], [32], [33]. Mapping entire networks into CIM hardware still requires continuous research for the CIM community. In this work, the last fully connected layer is mapped onto the macro, while the other layers operate on the PC and FPGA. The CIM macro calculates recognition results and outputs them directly to the PC, where they can be compared to the results computed by software. Through testing, the CIM macro achieves a recognition accuracy of 92.28% using the CIFAR-10 dataset compared to baseline accuracy of 93.23%.

C. AREA STATISTIC ANALYSIS

The chip micrograph of the CIM is shown in Fig. 9 left. The die area of the chip is 2.02 mm^2, with the CIM macro

TABLE 3. Comparison to prior CIM macros.

	JSSC'22 [1]	JSSC'21 [2]	JSSC'20 [6]		JSSC'22 [15]	JSSC'23 [18]	ISSCC'23 [19]	This Work
Technology (nm)	28	7	55		65	28	4	55
Cell Structure	6T SRAM	8T SRAM	6T SRAM		8T SRAM	8T SRAM	6T SRAM	DW6T SRAM
Array Size	64kb	4kb	4kb		16kb	219kb	54kb	4kb
Input Bits	4	4	7	8	5	1	4 (±3)	4 (±3)
Weight Bits	4	4	1	8	1	2	5 (±4)	5 (±4)
ADC Output Precision (analog) Full Output Precision (digital)	5 (analog)	4 (analog)	4 (analog)		5 (analog)	[c]24b (digital)	24 (digital)	5 (±4) (analog)
Energy Efficiency (TOPS/W) (sparsity)	29.2	351	5.7	0.6	15.8	161.08 (90%)	87.4 (87.5%)	[d]7.3 (70%)
[a]Energy Efficiency @55nm	7.57	5.69	5.7	0.6	22.07	41.74	0.46	7.3
[b]FoM	121.1	91.0	39.9	38.4	110.4	83.5	29.5	146.0

[a]Energy Efficiency scaled, assuming $Energy \propto (Technology)^2$ [4]; [b]FoM = Input Bits × Weight Bits × Energy Efficiency (scaled to 55nm); [c]24b has an 24b storage, for storage under different computation conditions; [d]Each Nb × Nb is considered as 2 operations.

occupying 0.30975 mm^2 of that space. The macro's function area is 0.076012 mm^2, which includes the bitcell area and the area of additional CIM circuits. These additional CIM circuits include ADC, capacitors, row circuitry, etc. Table 2 compares our CIM macro to those of works that employ similar technologies, providing a more detailed analysis of area statistics. According to comparison, our proposed CIM macro has a small bitcell area, this is because it is modified from foundry compact bitcells. Compared to other works, the area efficiency of our work is moderate, showing decent trade-off between area, function, energy efficiency and accuracy.

D. ENERGY EFFICIENCY TEST AND STATISTIC COMPARISON

The power breakdown of the CIM is shown in Fig. 9 right. In addition to the CIM macro, the chip contains test circuits and temporary storage SRAMs for testing convenience. Tested power consumption is 726μW at 1.2 V main analog power for CIM and 0.9 V wordline activation voltage. This is an average power of the CIM macro working under different computation scenarios with an average input sparsity of 70%. The power breakdown shows that the SAR-ADC and analog computation logic circuit consume about half of total power, which is a common distribution in charge-domain analog-mixed-signal SRAM based CIMs.

We compare this work with state-of-the-art SRAM CIM macros in Table 3. The CIM macro we present achieves 7.3 TOPS/W under 1.2 V main power and 200 MHz clock frequency, it reaches the highest figure of merit (FoM) value of 146 when technology and input/weight precision is added to consideration. Compared to [1], our CIM macro exceeds similar bitwise CIMs, even with more complicated full signed computation. Compared to [2], statistics show the advantages of structure improvement compared to advanced technology process. Compared to [17], [18], [19], and [20], the advantage of analog-mixed-signal SRAM-based CIM designs over digital CIM designs when performing signed multi-bit computing operations is revealed, even with a smaller input sparsity.

IV. CONCLUSION

This paper presents a dual-wordline 6T SRAM-based analog-mixed-signal computing-in-memory macro designed for energy efficient signed multi-bit computing in sparse lightweight networks. Thanks to the DW6T bitcell structure and exquisite computation scheme, the CIM macro outputs precise results with low power and short time cycle. A test-chip is fabricated using 55nm CMOS technology. It is tested using comprehensive computing operations achieving a precision of 79.51% in a 1-FE error range of 71.88%, and an energy efficiency of 7.3 TOPS/W at ±4/±3 weight/input precision. The CIM macro is tested in an application scenario by mapping a lightweight network into the macro and preforming CIFAR-10 recognition task. Compared with other state-of-the-art CIM macros, our proposed work reaches the highest FoM value of 146 when comprehensively considering energy efficiency, technology and input/weight bit width. The CIM macro is a design with high energy efficiency and accuracy, making it worthy of reference for future analog-mixed-signal SRAM-based CIMs aiming for sparse lightweight network applications.

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