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RESEARCH ARTICLE

Impedance Model Based Coordination Control of Secondary Ripple in DC Microgrid

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ABSTRACT The connection of single-phase AC loads to a DC microgrid not only large secondary currents flowing into energy storage units with droop control cause, but also lead to secondary voltage ripples appeared on the DC bus, which seriously affects the normal operation of DC microgrids. In this paper, the secondary currents and voltages can be suppressed simultaneously by means of reconstructing the output impedances of energy storage converter and active capacitor converter. The main characteristics, impedance model, control strategies, and system stability in terms of secondary ripples are comprehensively investigated. Particularly, it is shown that the output impedance of the energy storage converter with droop control is relatively small and the input impedance DC loads buck converter are relatively large, so the secondary currents mainly flow into energy storage units and DC bus capacitor. Based on this, the output impedance of the energy storage converter and active capacitor converter are reconstructed relatively larger and smaller respectively, so the secondary currents mainly flowing into the active capacitor. Therefore, the secondary ripple currents flowing into energy storage units and the secondary ripple voltages appeared on the DC bus can be suppressed. Finally, the proposed methods are varied through simulations results.

INDEX TERMS DC microgrids, secondary ripple, virtual impedance, coordination control.

I. INTRODUCTION

DC microgrids are generally composed of distributed power sources, energy storage batteries, and load units. Compared to AC microgrids, DC microgrids have advantages such as high efficiency, easy control, and high reliability [1]. Besides, in DC microgrids, only active power balance needs to be considered. The reactive power balance and phase synchronization can be neglected. Therefore, DC microgrids has become the development trend of future distribution networks [2].

However, AC loads usually connected to the DC microgrid through single-phase inverters. Based on the instantaneous balance theory, the input power includes double line frequency components inherently [3]. The double line frequency power will be coupled with other units through the DC bus, which not only lead to large secondary currents ripples for the energy storage units with droop control [4], [5], [6], but also cause large secondary DC bus voltage ripples through bus capacitor. The secondary ripple currents not only increase the current stress and conduction loss of the switch tube, but also causes continuous charging and discharging of energy storage units, seriously affecting the lifespan of power electronic devices and batteries [7]. The secondary voltage ripple is relatively large compared to high-frequency ripples

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currents [5], [8], which reduces the power supply quality for other units connect to the DC bus, specially affect the MPPT accuracy for the PV modular connected to the DC bus through DC/DC converter [9]. Therefore, the objective of this paper is to suppress the secondary current ripples flowing into the units with small output impedance and suppress the secondary voltage ripples appeared on the DC bus simultaneously.

In order to suppress the secondary current or voltage ripples, two methods are usually adopted: hardware solutions [10], [11], [12], [13], [14], [15], [16] and control solutions [17], [18], [19], [20], [21], [22]. Large output capacitance of the energy storage converter is used to allow the secondary current ripple to flow into the output capacitor instead of battery in [10] and [11]. This method is easy, but the volume of the capacitor is too large, which is limited for high power density applications. Ripple power compensation circuit is added to the DC bus to suppress the secondary voltage ripples in [12] and [13]. These methods always have higher power density. However, complex calculations are needed to obtain the compensation value of the secondary ripple power [12], and the control delay may have a significant impact on compensation accuracy [13]. Besides, H-bridge rectifier with ripple power decoupling function to reduce the secondary voltage ripple is proposed in [15] and [16]. The complex calculation is not needed, but this method is only adaptive to the single unit with AC/DC conversion, it cannot be applied to the DC microgrids with multiple units directly.

In terms control solutions, there is no additional component, only control strategy needs to be improved. Third harmonic injection is proposed to eliminate the second ripple current in [17], but additional fourth harmonic will be introduced in DC microgrid. Virtual impedance methods by introducing resonant filter and notch filter are proposed to change the output impedance of single-phase H-bridge rectifier to suppress the secondary current ripples flowing into the output DC side [18], [19], [20]. Although the secondary current flowing into DC side unit is reduced, the excessive secondary voltage ripple will appear on the middle DC bus. Second ripple current suppressing control in DC microgrid is proposed in [21] and [22]. The equivalent output impedance of the energy storage converter is increased at secondary line frequency. These methods can effectively suppress the secondary current ripple in energy storage units, but the secondary voltage ripples on the DC bus cannot be suppressed, so other additional units connected to DC microgrid will be affected. Overall, the battery secondary current ripple and DC bus voltage ripple in DC microgrids cannot be reduced simultaneously with existing methods.

In this paper, the secondary ripple current flowing into the energy storage units and secondary ripple voltage on the DC bus can be suppressed simultaneously by the proposed impedance model based coordinated control strategy. The contribution of this paper mainly includes three parts. Firstly, virtual impedance was introduced through resonant and notch filters to improve the output impedance of the energy storage unit converter at secondary line frequency, making its output impedance nearly equal to the input impedance of the DC load converter at that frequency, though which the secondary ripple current flown into energy storage converter is reduced effectively. Secondly, an active capacitor is further introduced, and the secondary ripple power can be absorbed by reducing the output impedance of the active capacitor, so the secondary ripple voltage of the DC bus can be suppressed. Thirdly, the system impedance model of the DC microgrid was presented, and the system stability is analyzed.

The paper is organized as follows. Section II presents the origin of the secondary ripples in DC microgrids. Small signal impedance model of key converters in DC microgrids are established in Section III. The proposed impedance-based coordination control strategy for secondary ripple suppression is presented in Section IV. System stability and key parameter impact is analyzed in Section V. Section VI presents the simulation results. Section VII concludes this paper.

II. ORIGIN OF THE SECONDARY RIPPLES IN DC MICROGRIDS

A. STRUCTURE OF THE DC MICROGRID

A typical DC microgrid system structure is shown in Fig. 1, which includes photovoltaic (PV), DC load, active capacitor, single-phase inverter load, and energy storage battery.

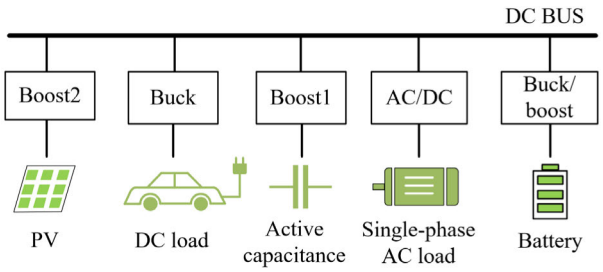

FIGURE 1. Structure of a typical DC microgrid.

In the DC microgrid, the PV unit and the active capacitor unit adopts Boost converter, and the DC load unit adopts Buck converter. The single-phase AC load unit adopts single-phase AC/DC converter, and the energy storage unit adopts bidirectional Buck/boost converter. The specific topology is shown in Fig. 2.

In Fig. 2, S_1-S_{10} are switching tubes, u_{bus1} and i_{ac} are input voltage and input current of the active capacitor converter. u_{ac} and i_{ac} are capacitor voltage and inductance current of the active capacitor converter. C_{ac} and L_{ac} are capacitor and inductor of the active capacitor converter. u_{PV} and i_{PV} are PV output voltage and current respectively, and C_{PV1} and C_{PV2} are PV side capacitor and DC bus side capacitor respectively. L_{PV} is the inductor of PV converter. u_{bus2} and i_e are input voltage and input current of load converter, and u_e and i_{Le} are capacitor voltage and inductor current of load converter. C_e

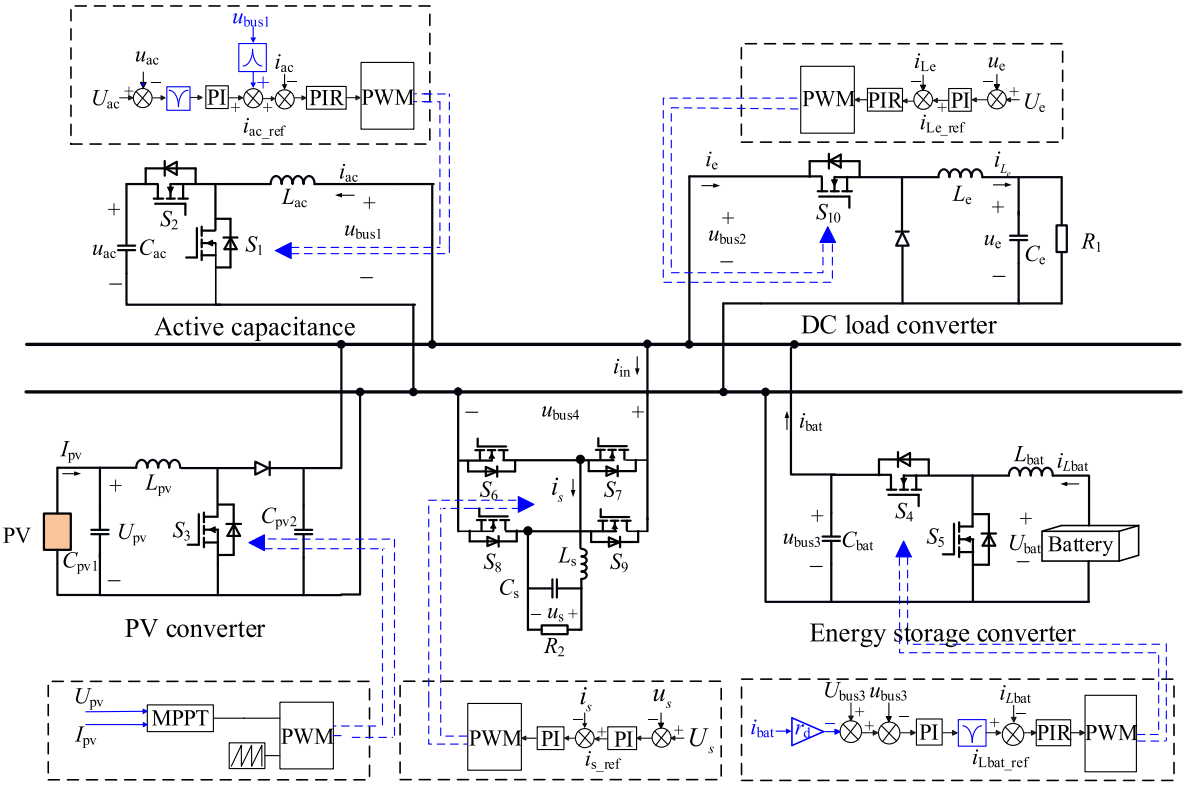

FIGURE 2. Topology and control strategy of key converters in the DC microgrid.

and L_e are capacitor and inductor of load converter. u_{bus3} and i_{bat} are the output voltage and output current of the energy storage Buck/boost converter. i_{Lbat} is the inductor current, and U_{bat} is the battery voltage. C_{bat} and L_{bat} are the DC bus capacitor and the Buck/boost converter inductor. u_{bus4} and i_{in} are input voltage and input current of the single-phase inverter load. u_s and i_s are capacitor voltage and inductor current of the single-phase inverter. C_s and L_s are capacitor and inductor of the single-phase inverter.

Voltage and current dual loop control is adopted for the active capacitor boost converter. The voltage outer loop adopts PI controller, and the current inner loop adopts PIR controller. U_{ac} is the reference of the capacitor voltage on the output side of the active capacitor converter. MPPT control is adopted by the PV Boost converter, and U_{PV} and I_{PV} are the input of the MPPT unit. Voltage and current dual loop control is adopted by the Buck converter. The voltage outer loop adopts PI controller, and the current inner loop adopts PIR controller. U_e is the reference value of DC load voltage. The control scheme of a bidirectional Buck/boost converter consists of three loops: the voltage outer loop, the inductor current inner loop, and the droop loop. In microgrids, there is usually more than one energy storage, so droop control with droop coefficient r_d is used. U_{bus3} is the voltage reference under no-load conditions. A PI controller is used to the voltage outer loop, and a PIR controller is used to the current inner loop. The single inverter converter adopts dual loop control of voltage and current. The voltage outer loop adopts a PI controller, and the current inner loop adopts a PI controller. U_s is the reference of the AC load voltage, usually a sine wave signal with an amplitude of 311V and a frequency of 50Hz.

B. CHARACTERISTIC OF SECONDARY RIPPLES IN DC MICROGRIDS

The AC load voltage and current is assumed as

$$u_s = \sqrt{2}U_s \sin \omega t \tag{1}$$

$$i_s = \sqrt{2}I_s \sin(\omega t - \theta) \tag{2}$$

where the U_s and I_s represents the RMS values of voltage and current, respectively. ω is the angular frequency and θ is the phase angle between u_s and of i_s.

The instantaneous power delivered by single-phase inverter can be calculated as the summation of (3) and (4).

$$\bar{P}_{AC\_0} = U_{ac\_L} I_{ac\_L} \cos\theta \tag{3}$$

$$\tilde{P}_{AC\_2} = -U_{ac\_L} I_{ac\_L} \cos(2\omega t - \theta) \tag{4}$$

where $\bar{P}_{AC\_0}$ and $\tilde{P}_{AC\_2}$ is the DC component and secondary component of the instantaneous power of the single-phase inverter load respectively.

Considering the power balance of between input and output, the instantaneous power absorbed by the DC bus capacitor equal to the output power of the PV unit and energy storage unit minus the input power of AC load and DC load.

S_{bus} can be expressed as:

$$\begin{aligned} S_{bus} &= \bar{S}_{bus} + \tilde{S}_{bus} = C_{\text{bus}} \frac{du_{\text{bus}}}{dt} u_{\text{bus}} \\ &= P_{PV} + P_{bat} - P_{DC} - P_{AC\_L} \\ &= P_{PV} + P_{bat} - P_{DC} - \bar{P}_{AC\_0} - \tilde{P}_{AC\_2} \end{aligned} \tag{5}$$

where $\bar{S}_{bus}$ and $\tilde{S}_{bus}$ are the DC and secondary components of the instantaneous power absorbed by the DC bus capacitor, C_{bus} is the DC bus capacitor, and P_{PV} and P_{bat} are the output power of the PV and energy storage battery respectively. P_{DC} is the input power of DC loads.

It can be seen from (5) that the secondary component of the instantaneous power delivered by single-phase AC load should be delivered to the DC bus capacitor and other units through the interface converters. The secondary component of the instantaneous power usually distributed among the units based on the impedance of each unit, and the smaller the impedance, the larger the current. Therefore, the secondary component of the instantaneous power flowing into energy storage unit will cause large secondary current ripple, and the remaining secondary components power flowing into DC bus capacitor will lead to secondary voltage ripple appeared on the DC bus.

III. SMALL SIGNAL IMPEDANCE MODELING OF THE KEY CONVERTERS IN DC MICROGRIDS

A. OUTPUT IMPEDANCE MODEL OF THE ENERGY STORAGE CONVERTER

The linearized circuit equations of the Buck/boost converter around an operation point are as follows:

$$s L_{\text{bat}} \hat{i}_{L_{\text{bat}}} = -(1 - \text{D}_3)\hat{u}_{\text{bus3}} + U_{\text{bus3}} \hat{d}_3 \tag{6}$$

$$s C_{\text{bat}} \hat{u}_{\text{bus3}} = (1 - \text{D}_3)\hat{i}_{L_{\text{bat}}} - I_{L_{\text{bat}}} \hat{d}_3 - \hat{i}_{\text{bat}} \tag{7}$$

where the superscript symbol represents an AC small signal. The duty cycle of S_4 is D_3, and S_4 and S_5 are complement. Combining (6) and (7), the state variable $\hat{i}_{L_{\text{bat}}}$ and $\hat{u}_{\text{bus3}}$ can be expressed as follows:

$$\begin{aligned} &\hat{i}_{L_{\text{bat}}} \\ &= \underbrace{\frac{1 - \text{D}_3}{s^2 L_{\text{bat}} C_{\text{bat}} + (1 - \text{D}_3)^2} \hat{i}_{\text{bat}}}_{G_{\text{ii}_0}(\text{s})} + \underbrace{\frac{s C_{\text{bat}} U_{\text{bus3}} + I_{\text{bat}}}{s^2 L_{\text{bat}} C_{\text{bat}} + (1 - \text{D}_3)^2} \hat{d}_3}_{G_{\text{id}}(\text{s})} \end{aligned} \tag{8}$$

$$\begin{aligned} &\hat{u}_{\text{bus3}} \\ &= \underbrace{\frac{U_{\text{bat}} - s L_{\text{bat}} I_{L_{\text{bat}}}}{s U_{\text{bus3}} C_{\text{bat}} + I_{\text{bat}}} \hat{i}_{L_{\text{bat}}}}_{G_{\text{ui}}(\text{s})} - \underbrace{\frac{U_{\text{bus3}}}{s U_{\text{bus3}} C_{\text{bat}} + I_{\text{bat}}} \hat{i}_{\text{bat}}}_{Z_0(\text{s})} \end{aligned} \tag{9}$$

where U_{bat} equals (1-D_3) U_{bus3}, and I_{bat} equals (1)-D_3) I_{Lbat}. The power stage of the Buck/boost converter can be described by the transfer functions $G_{\text{ii}0}(\text{s})$, $G_{\text{id}}(\text{s})$, $G_{\text{ui}}(\text{s})$, and $Z_0(\text{s})$. The control block diagram of the energy storage Buck/boost converter is shows as Fig. 3.

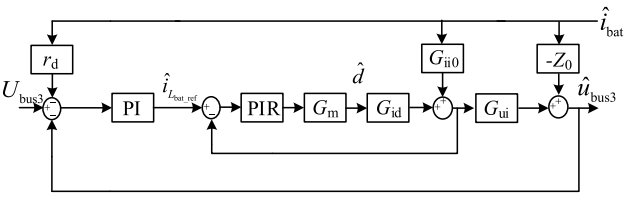

FIGURE 3. Dule loop control block diagram of the energy storage converter.

According to Fig.3, the output impedance $Z_{\text{oc}}(\text{s})$ of the Buck/boost converter without considering droop control and voltage outer loop can be obtained as (10)

$$Z_{\text{oc}}(\text{s}) = -\left.\frac{\hat{u}_{\text{bus3}}}{\hat{i}_{\text{bat}}}\right|_{\hat{i}_{L_{\text{bat\_ref}}}=0} = -[Z_0(\text{s}) + \frac{G_{\text{ii}_0}(\text{s}) G_{\text{ui}}(\text{s})}{1 + T_{\text{i\_bat}}(\text{s})}] \tag{10}$$

where the $T_{\text{i\_Bat}}$ (s) is the open loop transfer function of the current inner loop.

$$T_{\text{i\_bat}}(\text{s}) = G_{\text{i}}(\text{s}) G_{\text{m}}(\text{s}) G_{\text{id}}(\text{s}) \tag{11}$$

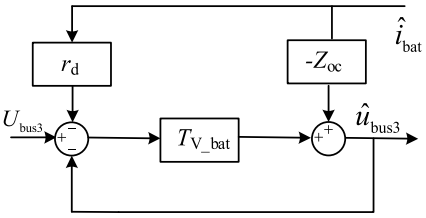

FIGURE 4. Equivalent control block diagram of the energy storage converter.

The equivalent control block diagram of the energy storage converter can be obtained, as shown in Fig. 4, where the $T_{\text{v\_bat}}$ (s) is the open-loop transfer function of the voltage outer loop.

$$T_{\text{v\_bat}}(\text{s}) = G_{\text{u}}(\text{s}) T_{\text{iop\_bat}}(\text{s}) G_{\text{ui}}(\text{s}) \tag{12}$$

$$T_{\text{iop\_bat}}(\text{s}) = \frac{T_{\text{i\_bat}}(\text{s})}{1 + T_{\text{i\_bat}}(\text{s})} \tag{13}$$

The closed-loop output impedance of $Z_{\text{out\_bat}}(\text{s})$ is as follows:

$$Z_{\text{out\_bat}}(\text{s}) = -\left.\frac{\hat{u}_{\text{bus3}}}{\hat{i}_{\text{bat}}}\right|_{\hat{U}_{\text{bus3=0}}} = \frac{Z_{\text{oc}}(\text{s}) + r_{\text{d}} T_{\text{v\_bat}}(\text{s})}{1 + T_{\text{v\_bat}}(\text{s})} \tag{14}$$

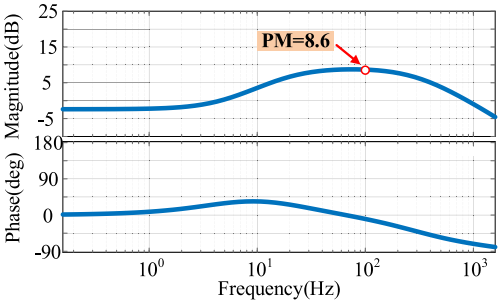

FIGURE 5. Output impedance bode diagram of energy storage converter.

Substituting the relevant parameters of the energy storage converter as shown in Table 1, the closed-loop output impedance Bode diagram of the energy storage converter is shown in Fig. 5.

TABLE 1. Parameters of energy storage buck/boost converter.

Parameter	Symbol	Value
Bus voltage	U_{bus3} /V	380
Energy storage voltage	U_{bat}/V	200
Droop coefficient	r_d/V/A	0.76
Inductance	L_{bat}/mH	0.5
Capacitance	C_{bat}/μF	220
Current regulator	K_{ip}	0.01
Current regulator	K_{ii}	50
Current regulator	K_{ir}	1.3
Voltage regulator	K_{vp}	0.7
Voltage regulator	K_{vi}	100

It can be seen that $|Z_{out\_bat}(s)|$ is about 8.6dB (2.69) at 100Hz, which means that the relatively small secondary ripple power will also generate relatively large secondary ripple current flowing into the energy storage battery.

B. INPUT IMPEDANCE MODEL OF THE DC LOAD BUCK CONVERTER

The linearized circuit equations of the Buck converter around an operation point are as follows:

$$sL_e\hat{i}_{L_e} = D_2\hat{u}_{bus2} + U_{bus2}\hat{d}_2 - \hat{u}_e \tag{15}$$

$$sC_e\hat{u}_e = \hat{i}_{L_e} - \frac{1}{R_1}\hat{u}_e \tag{16}$$

where the duty cycle of S_{10} is D_2, combined with (15) and (16), the state variable $\hat{u}_e$, $\hat{i}_{L_e}$ and $\hat{i}_e$ can be represented as follows:

$$\hat{i}_{L_e} = \underbrace{\frac{sC_eR_1D_2+D_2}{s^2L_eC_eR_1+sL_e+R_1}}_{G_{iu_b}(s)}\hat{u}_{bus2} + \underbrace{\frac{sC_eR_1U_{bus2}+U_{bus2}}{s^2L_eC_eR_1+sL_e+R_1}}_{G_{id}(s)}\hat{d}_2 \tag{17}$$

$$\hat{u}_e = \underbrace{\frac{R_1}{sC_eR_1+1}}_{G_{ui}(s)}\hat{i}_{L_e} \tag{18}$$

$$\hat{i}_{L_e} = \frac{1}{D_2}\hat{i}_e \tag{19}$$

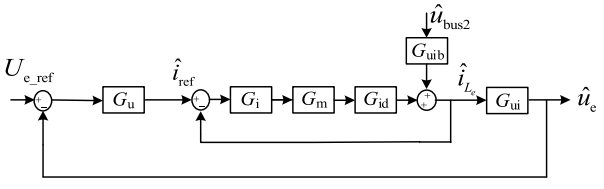

FIGURE 6. Control block diagram of the Buck converter.

The power stage of the Buck converter can be described by the transfer functions $G_{iub}(s)$, $G_{id}(s)$, and $G_{ui}(s)$. The control block diagram of the Buck converter is shown as Fig. 6.

Combining the main circuit and control transfer functions, the closed-loop input impedance of the Buck converter $Z_{in\_buck}(s)$ is obtained as follows:

$$Z_{in\_buck}(s) = \frac{\hat{u}_{bus2}}{\hat{i}_e}\bigg|_{\hat{u}_{e\_ref}=0} = \frac{1+G_{ui}(s)G_v(s)T_{i\_e}(s)+T_{i\_e}(s)}{G_{iu_b}(s)D_2} \tag{20}$$

where the $T_{i\_e}(s)$ is the open loop transfer function of the current inner loop.

$$T_{i\_e}(s) = G_i(s)G_m(s)G_{id}(s) \tag{21}$$

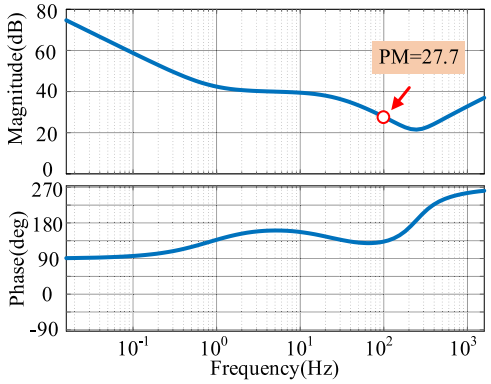

FIGURE 7. DC load converter input impedance bode diagram.

Substituting the relevant parameters of the Buck converter shown in Table 2, the closed-loop input impedance Bode diagram of the Buck converter is shown in Fig. 7.

TABLE 2. Parameters of dc load buck converter.

Parameter	Symbol	Value
Bus voltage	U_{bus2} /V	380
DC load voltage	U_e/V	200
Inductance	L_e/mH	2
Capacitance	C_e/μF	600
Current regulator	K_{ip}	0.008
Current regulator	K_{ii}	0
Current regulator	K_{ir}	1.1
Voltage regulator	K_{vp}	0.5
Voltage regulator	K_{vi}	5

It can be seen that $|Z_{in\_buck}(s)|$ is about 27.7dB (24.3) at 100Hz, which is relatively large. It means that the secondary ripple power on the DC bus has little impact on this converter.

C. INPUT IMPEDANCE MODEL OF THE SINGLE-PHASE INVERTER

The linearized circuit equations of the Single-phase inverter around an operation point are as follows:

$$sL_s\hat{i}_s = (2D-1)\hat{u}_{bus4} + 2U_{bus4}\hat{d} - \hat{u}_s \tag{22}$$

$$sC_s\hat{u}_s = \hat{i}_s - \frac{1}{R}\hat{u}_s \tag{23}$$

where duty cycle of S_7 and S_8 is D, combined with (22) and (23), the state variable $\hat{u}_s$, $\hat{i}_s$ and $\hat{i}_{in}$ can be

represented as follows:

$$\hat{i}_s = \underbrace{\frac{sC_sR_2(2D-1)+(2D-1)}{s^2L_sC_sR_2+sL_s+R_2}}_{G_{iu_b}(s)}\hat{u}_{bus4} + \underbrace{\frac{sC_sR_2U_{bus3}+U_{bus4}}{s^2L_sC_sR_2+sL_s+R_2}}_{G_{id}(s)}\hat{d} \quad (24)$$

$$\hat{u}_s = \underbrace{\frac{R_2}{sC_sR_2+1}}_{G_{ui}(s)}\hat{i}_s \quad (25)$$

$$\hat{i}_s = \frac{1}{(2D-1)}\hat{i}_{in} \quad (26)$$

The power stage of the inverter can be described by the transfer functions $G_{iub}(s)$, $G_{id}(s)$, and $G_{ui}(s)$. The control block diagram of the Single-phase inverter is shown in Fig. 8

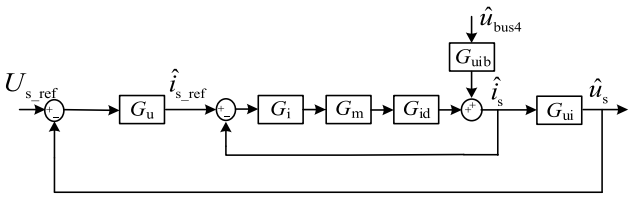

FIGURE 8. Control block diagram of the single-phase inverter.

Combining the main circuit and control transfer functions, the closed-loop input impedance of the Single-phase inverter $Z_{inv}(s)$ is obtained as follows:

$$Z_{inv}(s) = \left.\frac{\hat{u}_{bus4}}{\hat{i}_{in}}\right|_{\hat{u}_{s\_ref}=0} = \frac{1+G_{ui}(s)G_v(s)T_{i\_inv}(s)+T_{i\_inv}(s)}{G_{iu_b}(s)(2D-1)} \quad (27)$$

where the T_{i_inv} (s) is the open loop transfer function of the current inner loop.

$$T_{i\_inv}(s) = G_i(s)G_m(s)G_{id}(s) \quad (28)$$

Substituting the relevant parameters of the Single inverter shown in Table 3, the closed-loop input impedance Bode diagram of the Single inverter is shown in Fig. 9.

TABLE 3. Parameters of single-phase inverter.

Parameter	Symbol	Value
Bus voltage	U_{bus4} /V	380
AC load voltage	U_s/V	220
Inductance	L_s/mH	2
Capacitance	C_s/μF	15
Current regulator	K_{ip}	2
Current regulator	K_{ii}	0
Voltage regulator	K_{vp}	0.05
Voltage regulator	K_{vi}	5
Duty	D	0.53

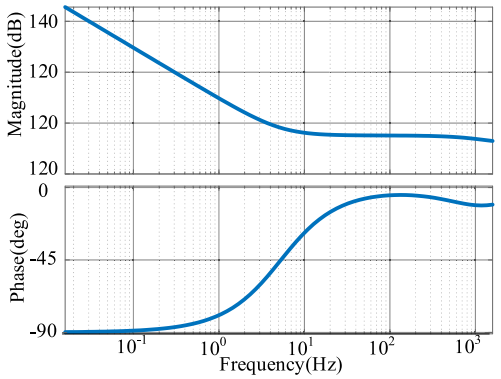

FIGURE 9. Single inverter input impedance bode diagram.

D. OUTPUT IMPEDANCE MODEL OF THE ACTIVE CAPACITOR CONVERTER

The active capacitor converter is connected to the DC bus to compensate the secondary ripple power by using dual loop control. The topology of the active capacitor converter is shown in Fig. 2. Its working principle is to detect the bus voltage U_{bus1}, and then provide the capacitive current. The equivalent capacitive impedance can be controlled relatively small, so the secondary ripple power on the DC bus can be absorbed by the active capacitor converter. The DC voltage ripple can be eliminated accordingly.

The linearized circuit equations of the active capacitor converter around an operation point are as follows:

$$sL_{ac}\hat{i}_{ac} = (D_1-1)\hat{u}_{ac} + \hat{u}_{bus1} + U_{ac}\hat{d}_1 \quad (29)$$

$$sC_{ac}\hat{u}_{ac} = (1-D_1)\hat{i}_{ac} - I_{ac}\hat{d}_1 \quad (30)$$

where the duty cycle of S_1 is D_1, combined with (29) and (30), the state variable $\hat{u}_{ac}$ and $\hat{i}_{ac}$ can be shown as

$$\hat{i}_{ac} = \underbrace{\frac{sC_{ac}}{s^2L_{ac}C_{ac}+(1-D_1)^2}}_{G_{iu_0}(s)}\hat{u}_{bus1} + \underbrace{\frac{sC_{ac}U_{ac}-I_{ac}(D_1-1)}{s^2L_{ac}C_{ac}+(1-D_1)^2}}_{G_{id}(s)}\hat{d}_1 \quad (31)$$

$$\hat{u}_{ac} = \underbrace{\frac{-s^2L_{ac}C_{ac}I_{ac}+sC_{ac}U_{ac}(1-D_1)}{s^2C_{ac}^2U_{ac}-sC_{ac}I_{ac}(D_1-1)}}_{G_{ui}(s)}\hat{i}_{ac} + \underbrace{\frac{sC_{ac}I_{ac}}{s^2C_{ac}^2U_{ac}-sC_{ac}I_{ac}(D_1-1)}}_{G_{uu_0}(s)}\hat{u}_{bus1} \quad (32)$$

The power stage of the active capacitor converter can be described by the transfer functions $G_{iu0}(s)$, $G_{id}(s)$, $G_{uu0}(s)$ and $G_{ui}(s)$. The control block diagram of the active capacitor converter is shown in Fig. 10.

Combining the main circuit and control block diagram, the closed-loop output impedance of the active capacitor

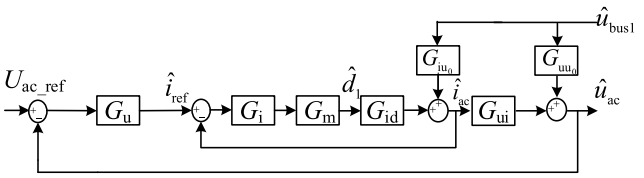

FIGURE 10. Control block diagram of the active capacitor converter.

converter $Z_{out\_boost}(s)$ is obtained as follows:

$$Z_{out\_boost}(s) = -\frac{\hat{u}_{bus1}}{\hat{i}_{ac}}\Big|_{\hat{u}_{ac\_ref}=0} = -\frac{1 + T_{v\_boost}(s) + T_{i\_boost}(s)}{G_{iu_0}(s) - G_{uu_0}(s)G_u(s)T_{i\_boost}(s)} \quad (33)$$

where the T_{v_Boost} (s) is the open-loop transfer function of the voltage outer loop, $T_{i\_Boost}(s)$ is the open loop transfer function of the current inner loop.

$$T_{v\_boost}(s) = G_u(s)T_{i\_boost}(s)G_{ui}(s) \quad (34)$$

$$T_{i\_boost}(s) = \frac{G_iG_mG_{id}}{1 + G_iG_mG_{id}} \quad (35)$$

Substituting the relevant parameters of the active capacitor converter shown in Table 4, the closed-loop output impedance Bode diagram of the inverter is shown in Fig. 11.

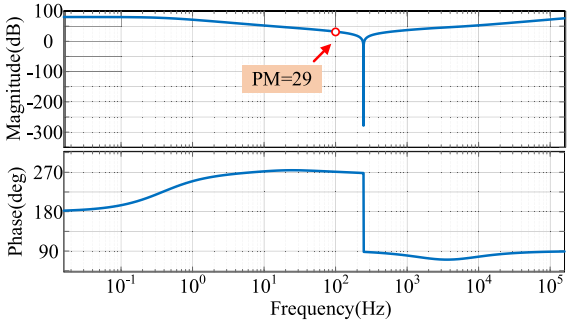

FIGURE 11. Output impedance bode diagram of the active capacitor converter.

It can be seen that $|Z_{out\_boost}(s)|$ is about 29dB (28.2) at 100Hz. In order to actively control the secondary ripple power into the active capacitor converter, it is necessary to further reduce the output impedance of the active capacitor converter at 100Hz. The next section will specifically introduce the impedance coordination control method.

TABLE 4. Parameters of active capacitor converter.

Parameter	Symbol	Value
Bus voltage	U_{bus1} /V	380
DC reference voltage	U_{ac}/V	650
Inductance	L_{ac}/mH	0.47
Capacitance	C_{ac}/μF	300
Current regulator	K_{ip}	0.1
Current regulator	K_{ii}	0
Voltage regulator	K_{vp}	0.05
Voltage regulator	K_{vi}	0.001
Voltage regulator	K_{vr}	5

IV. PROPOSED IMPEDANCE BASED COORDINATION CONTROL STRATEGY FOR SECONDARY RIPPLE SUPPRESSION

A. OVERALL IMPEDANCE MODEL OF THE DC MICROGRID

Based on the theoretical derivation in Section III and the power transmission characteristics of the secondary ripple currents, the equivalent impedance model of the DC microgrid and its secondary ripple equivalent circuit are obtained, as shown in Fig. 12 and Fig. 13.

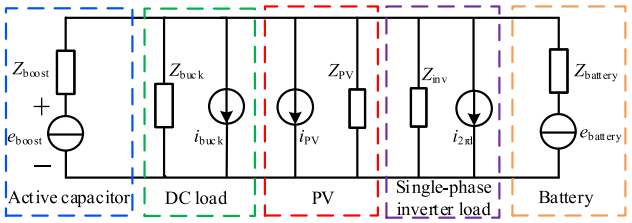

FIGURE 12. Impedance model of the DC microgrid.

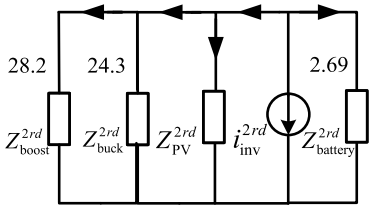

FIGURE 13. Secondary frequency equivalent circuit.

Fig. 12 shows the impedance model of the DC microgrid. In the microgrid, the energy storage unit is a balance node, and the active capacitor unit is a PV node. The PV unit, DC load unit, and single-phase inverter load unit are PQ nodes. Therefore, the active capacitor unit is equivalent to a voltage source e_{boost} and impedance Z_{boost} connected in series. The energy storage unit is equivalent to a voltage source $e_{battery}$ and impedance $Z_{battery}$ in series. The DC load is equivalent to a current source and impedance in parallel. PV is equivalent to a current source i_{PV} and impedance Z_{PV} in parallel. The single-phase inverter load is equivalent to a current source i_{2rd} and impedance Z_{inv} in parallel.

Fig. 13 shows the equivalent circuit at double line frequency, where single-phase AC load is the main origin for the secondary ripple power in the DC microgrid, so it can be equivalent to a current source i^{2rd}_{inv}. Due to the fact that active capacitors do not generate ripple power and only absorbs secondary ripple power, so it can be equivalent to be an impedance Z^{2rd}_{boost}. Due to the fact that the secondary ripple current flows towards the DC load side and the battery side, both of the two units are equivalent to the secondary frequency impedance, as Z^{2rd}_{buck} and $Z^{2rd}_{battery}$.

As shown in Fig. 14, at 100Hz, the energy storage battery converter $Z^{2rd}_{battery}$ is the smallest and the active capacitor converter Z^{2rd}_{boost} is the largest with traditional control methods. According to the power deliver characteristics, under the traditional dual loop control, the secondary ripple power will

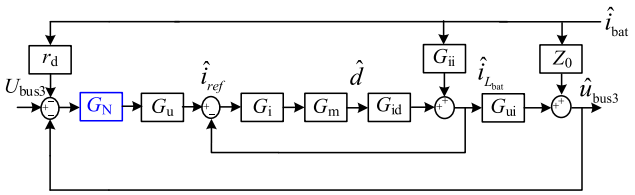

FIGURE 14. Coordinated control block diagram of the energy storage bidirectional Buck/boost converter.

flow more into the energy storage. Therefore, an optimized control strategy needs to be adopted to force the second ripple power to flow into the active capacitor.

In order to achieve the goal of coordinated management of secondary ripple, the specific method is as follows: increase the output impedance of the energy storage bidirectional converter at 100Hz, so that its output impedance at this frequency is as close as possible to the input impedance of the DC load Buck converter, and ultimately reduce the transmission of secondary ripple power to the energy storage side. By reducing the output impedance of the active capacitor converter at 100Hz, the output impedance at that frequency is much smaller than that of the energy storage converter, ultimately forcing the secondary ripple power to flow as much as possible to the active capacitor.

B. IMPEDANCE MODIFICATION OF THE ENERGY STORAGE CONVERTER

In order to increase the output impedance of the energy storage converter at 100Hz, the dual closed-loop control block diagram with a coordinated control is shown in Fig. 14.

The secondary ripple current can be reduced by reducing the voltage loop gain at 100Hz. The secondary frequency reference current $\hat{u}_{bus3}$ of the current inner loop can be reduced by filtering out the secondary ripple voltage in the feedback branch $\hat{u}_{bus3}$ through the notch filter $G_N(s)$.

The current inner loop is designed as a PIR controller for tracking AC components, and its transfer function is as follows:

$$G_i(s) = K_{ip} + K_{ii} + \frac{2K_{ir}\varepsilon\omega_n s}{s^2 + 2\varepsilon\omega_n s + \omega_1^2} \tag{36}$$

where the K_{ip} and K_{ii} are the proportion and integration coefficient of the current inner loop, respectively. K_{ir} is the resonance coefficient, $\varepsilon\omega_n$ is the cutoff frequency, ω_1 is the fundamental frequency of the system.

A notch filter can be adopted to reduce the voltage outer loop gain. The expressions of $G_N(s)$ is shown as follows:

$$G_N(s) = \frac{1}{\alpha^2}\frac{1 + 2q_1 \cdot s/\omega_N + (s/\omega_N)^2}{1 + 2q_2 \cdot s/(\alpha\omega_N) + (s/(\alpha\omega_N))^2} \tag{37}$$

where the ω_N is the center frequency of the notch filter, q_1 and q_2 are two coefficients related to the notch bandwidth and depth, and α is the phase correction coefficient.

According to Fig. 14, after adding $G_N(s)$, the output impedance of the energy storage converter $Z_{out\_bat\_N}(s)$ is shown as follows:

$$Z_{out\_bat\_N}(s) = -\left.\frac{\hat{u}_{bus3}}{\hat{i}_{bat}}\right|_{\hat{U}_{bus3}=0} = \frac{Z_{oc} + r_d T_{v\_bat\_N}}{1 + T_{v\_bat\_N}} \tag{38}$$

where the $T_{v\_bat\_N}$ is the improved voltage outer-loop open-loop transfer function.

$$T_{v\_bat\_N} = T_v \cdot G_N = G_v T_{iop} G_{ui} G_N \tag{39}$$

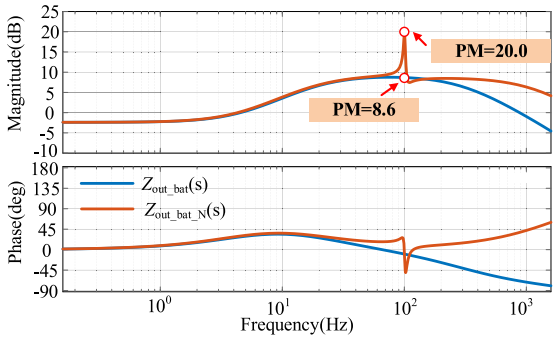

FIGURE 15. Bode diagram of output impedance of the energy storage converter with and without coordinated control.

The Bode diagram of the output impedance of the energy storage converter with and without coordinated control is shown in Fig. 15. Among them, the bandwidth of the notch filter is 17Hz, and the notch depth is −62dB, $\alpha = 1.04$, $q_1 = 5 \times 10^{-5}$, $q_2 = 5 \times 10^{-2}$. $|Z_{in\_Bat}(s)|$ is the closed-loop output impedance value of the energy storage converter with traditional control, $|Z_{out\_bat\_N}(s)|$ is the closed-loop output impedance value of the energy storage converter with virtual impedance control.

It can be seen from Fig. 15 that after adding $G_N(s)$, |Zout_bat_N(s)| is about 20dB (10), which is 3.7 times that of |Zout_bat(s)|, significantly improving the closed-loop output impedance of the energy storage converter at 100Hz.

In order to investigate the effect of the resonant filter $G_N(s)$ on the stability of the converter, stability analysis of the open-loop transfer function $T_{v\_bat\_N}(s)$ with different α is presented. The Bode diagram of the open-loop transfer function $T_{v\_bat\_N}(s)$ is shown in Fig. 16.

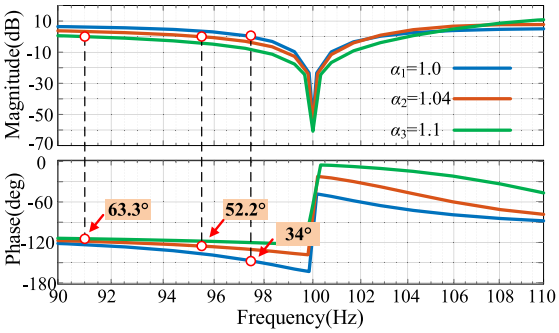

FIGURE 16. Bode diagram of open loop transfer function Tv_bat_N(s).

From Fig. 16, it can be seen that the change of α mainly affects the crossing frequency. As α increases, the crossing

frequency decreases. Gradually increasing α, the phase angle margin has been increased from 34° to 63.3°, significantly improving the stability of the system. According to the fact that the phase angle margin of the converter is greater than 45°, good system stability can be achieved. When α is equal to 1, the phase margin is less than 45°, resulting in poor system stability. Therefore, the final choice of α is 1.04, the phase angle margin of the open loop system is 52.2°.

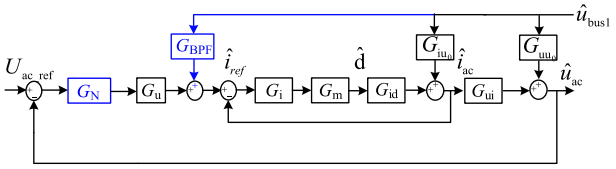

FIGURE 17. Block diagram of active capacitor converter with coordinated control strategy.

C. IMPEDANCE MODIFICATION OF THE ACTIVE CAPACITOR CONVERTER

In order to decrease the output impedance of the active capacitor converter at 100Hz, the dual closed-loop control block diagram with a coordinated control strategy is shown in Fig. 17.

The secondary ripple voltage component can be amplified at 100Hz by introducing the DC bus $\hat{U}_{bus1}$ through the resonant filter $G_{BPF}(s)$, and the output is added to the current inner loop reference. The secondary ripple component in the feedback branch $\hat{U}_{ac}$ is filtered out through the notch filter $G_N(s)$ to reduce the secondary ripple component in the current inner loop reference branch $\hat{i}_{ref}$.

The notch filter $G_N(s)$ used is the same as the one used in the energy storage converter mentioned earlier. The resonant filter adopted in this paper is as

$$G_{BPF}(s) = \frac{2K_r\varepsilon\omega_n s}{s^2 + 2\varepsilon\omega_n s + \omega_1^2} \tag{40}$$

where K_r is the gain, $\varepsilon\omega_n$ is the cutoff frequency, ω_1 is the resonant frequency. Selectivity and dynamic performance are considered, so the cutoff frequency is set to be $0.707\omega_n$.

According to the transfer function shown in Fig.17, the closed-loop output impedance of the active capacitor with coordinated control is obtained as $Z_{out\_boost\_BN}(s)$:

$$\begin{aligned} &Z_{out\_boost\_BN}(s) \\ &= -\frac{\hat{u}_{bus1}}{\hat{i}_{ac}}\bigg|_{\hat{u}_{ac\_ref}=0} \\ &= -\frac{1+T_{v\_boost\_BN}(s)+T_{i\_boost}(s)}{G_{iu_0}(s)-G_{uu_0}(s)G_u(s)G_N(s)T_{i\_boost}(s)+G_{BPF}(s)T_{i\_boost}(s)} \end{aligned} \tag{41}$$

where the $T_{v\_boost\_BN}(s)$ is the open-loop transfer function of the voltage outer loop, and $T_{i\_Boost}(s)$ is the open-loop transfer function of the current inner loop.

$$T_{v\_boost\_BN}(s) = G_N(s)G_u(s)G_{ui}(s)T_{i\_boost}(s) \tag{42}$$

$$T_{i\_boost}(s) = G_i(s)G_m(s)G_{id}(s) \tag{43}$$

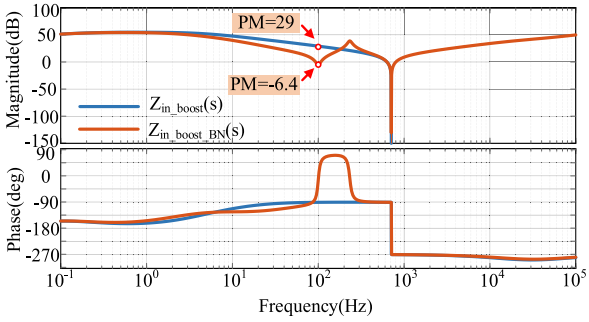

FIGURE 18. Bode diagram of output impedance of active capacitor converter with and without coordinated control.

The Bode diagram of the output impedance of the active capacitor converter before and after adding coordinated control is shown in Fig. 18. Among them, $\alpha = 1.04$, $q_1 = 5 \times 10^{-5}$, $q_2 = 5 \times 10^{-2}$. $|Z_{out\_Boost}(s)|$ is the closed-loop output impedance value of an active capacitor converter with traditional control, and $|Z_{out\_boost\_BN}(s)|$ is the closed-loop output impedance value of the active capacitor converter with virtual impedance.

As shown in Fig. 18, the closed-loop output impedance of the active capacitor converter with coordinated control $|Z_{out\_boost\_BN}(s)|$ is approximately −6.4 dB (0.5), which is greater than the closed-loop output impedance value of the active capacitor without coordination control $|Z_{out\_Boost}(s)|$. $|Z_{out\_boost\_BN}(s)|$ is relatively less than the impedance value of other converters in the system at 100Hz, which means that the secondary ripple power on the DC bus will mainly flow into the active capacitor circuit.

Stability analysis of the open-loop transfer function $T_{v\_boost\_BN}(s)$ with different α is presented. The Bode diagram of the open-loop transfer function $T_{v\_boost\_BN}(s)$ is shown in Fig. 19.

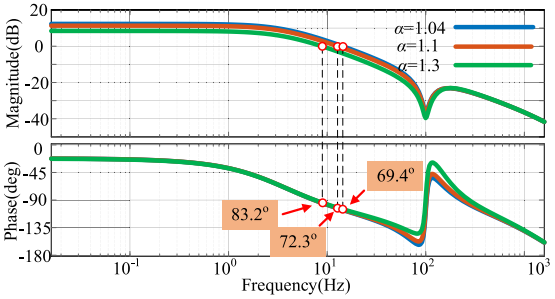

FIGURE 19. Bode diagram of open loop transfer function of $T_{v\_boost\_BN}(s)$.

As shown in Fig. 19, Bode diagram of the open-loop system varies different α, thereby affecting the system stability. From Fig. 19 (a), it can be seen that, the phase margin increases with the increase of α, and the open loop cutoff frequency deceases with the increase of α. Therefore, α is selected as 1.1 in this paper by considering dynamic performance stability of the system.

V. SYSTEM STABILITY ANALYSIS AND KEY PARAMETER IMPACT

Impedance matching is an important theory for improving and evaluating system stability. The stability of a single converter is analyzed in previous section, while the impact of different converters connected to the microgrid on system stability will be analyzed in this section.

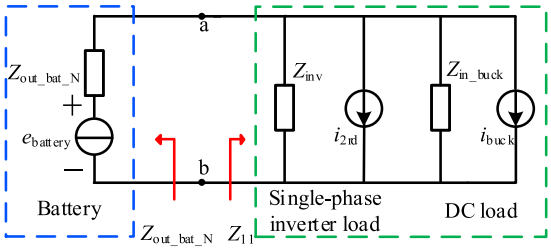

FIGURE 20. Small signal equivalent circuit of the system without active capacitor converter.

A. SYSTEM STABILITY ANALYSIS WITH AND WITHOUT THE ACTIVE CAPACITOR

1) SYSTEM STABILITY ANALYSIS WITHOUT THE ACTIVE CAPACITOR CONVERTER

The small signal equivalent circuit diagram of the system without the active capacitor converter is shown in Fig. 20. The stability of the system without the active capacitor converter can be judged by the ratio of the total impedance of voltage source converter and the total impedance of the load converters. The impedance ratio T_{ab} in this situation is defined as

$$T_{ab} = \frac{Z_{out\_bat\_N}}{Z_{11}} \tag{44}$$

where Z_{11} is the parallel impedance of the single-phase inverter closed-loop input impedance Z_{inv} and the DC load closed-loop input impedance Z_{in_buck}. Z_{11} is as

$$Z_{11} = \frac{Z_{inv}Z_{in\_buck}}{Z_{inv} + Z_{in\_buck}} \tag{45}$$

Fig. 21 shows the Nyquist curve of T_{ab}. It can be seen that the curve does not surround the $(-1, j0)$ point, so the system is stable.

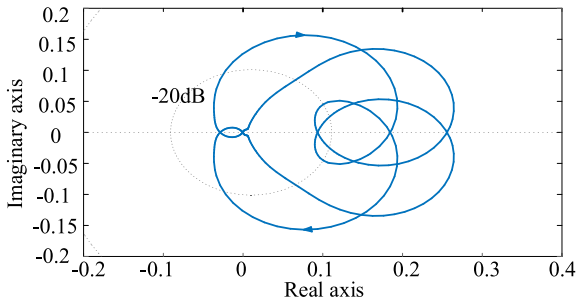

FIGURE 21. The Nyquist curve of T_{ab}.

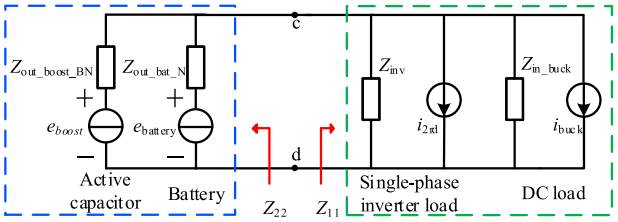

FIGURE 22. Small signal equivalent circuit of the system with the active capacitor converter.

2) STABILITY ANALYSIS OF THE SYSTEM WITH AN ACTIVE CAPACITOR CONVERTER

The small signal equivalent circuit diagram of the system with the active capacitor converter is shown in Fig. 22. The stability of the system with the active capacitor converter can be determined by the ratio of the closed-loop output impedance Z_{22} of the source converter and the closed-loop input impedance Z_{11} of the load converter. The impedance ratio T_{cd} in this situation is defined as

$$T_{cd} = \frac{Z_{22}}{Z_{11}} \tag{46}$$

where Z_{22} is the parallel impedance of the active capacitor converter closed-loop output impedance $Z_{out\_boost\_BN}$ and the energy storage converter closed-loop output impedance $Z_{out\_bat\_N}$. Z_{22} can be expressed as

$$Z_{22} = \frac{Z_{out\_boost\_BN}Z_{out\_bat\_N}}{Z_{out\_boost\_BN} + Z_{out\_bat\_N}} \tag{47}$$

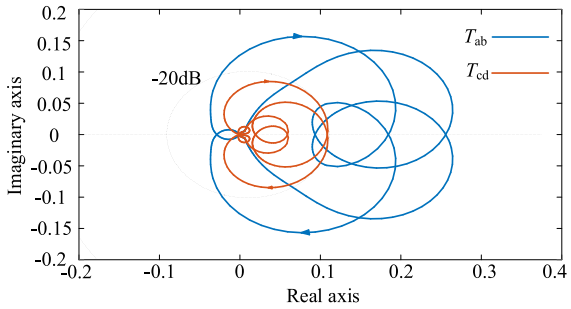

FIGURE 23. The Nyquist curve of T_{ab} and T_{cd}.

Fig. 23 shows the Nyquist curves of T_{ab} and T_{cd}. It can be seen that the Nyquist curve of T_{cd} does not surround the $(-1, j0)$ point, so the system is also stable. Compared to the system without the active capacitor, the T_{cd} is far from the $(-1, j0)$ point, so the system stability can be improved with the active capacitor.

B. THE IMPACT OF KEY PARAMETER ON SYSTEM STABILIT

1) THE IMPACT OF ACTIVE CAPACITOR K_R

Keeping the other parameters unchanged, the impact of different K_r values on T_{cd} are analyzed. The parameter values are selected as 1, 5, 10, 15, and 50 respectively, and the corresponding Nyquist curves are shown in Fig. 24.

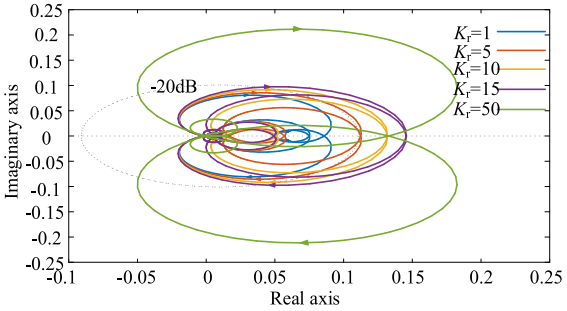

FIGURE 24. The Nyquist curve of T_{cd} with K_r changed.

As shown in the Fig. 24, as K_r increases, the Nyquist curve gradually approaches the $(-1, j0)$ point, reducing the stability margin of the system, which is not perfectible to its stability.

The gain of active capacitor converters at 100Hz can be improved by increasing K_r, but stability analysis shows that K_r cannot be arbitrarily increased. A larger K_r can certainly reduce the impedance of the active capacitor at 100Hz and allocate more second harmonic power to the active capacitor in the system, but it will reduce the system stability margin, so it is necessary to choose K_r reasonably.

2) THE IMPACT OF ACTIVE CAPACITOR K_{VP} AND K_{VI}

Firstly, keeping other parameters unchanged, and only the voltage outer loop parameter K_{vp} is changed. The parameter values are 1, 0.1, and 0.01, respectively, and the corresponding Nyquist curve is shown in Fig. 25.

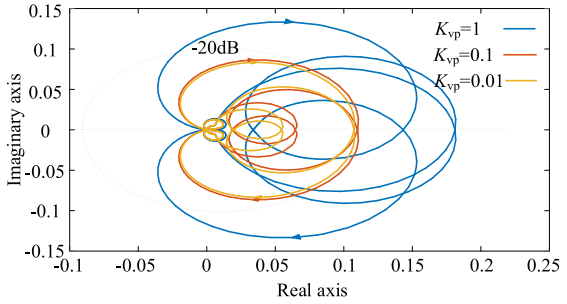

FIGURE 25. The Nyquist curve of T_{cd} with K_{vp} changed.

As shown in Fig 25, as K_{vp} decreases, the Nyquist curve moves away from the $(-1, j0)$ point. Stability margin of the system is increased, which is beneficial for system stability.

Secondly, keeping other parameters unchanged, and only changing the voltage outer loop parameter K_{vi}. The parameter values are 5, 15, and 25, respectively, and the corresponding Nyquist curve is shown in Fig. 26.

As shown in Fig. 26, as K_{vi} increases, the Nyquist curve gradually approaches the $(-1, j0)$ point, reducing the stability margin of the system, which is not preferable to its stability.

3) THE IMPACT OF ACTIVE CAPACITOR C_{AC}

Take three different sets of C_{ac} values, while keeping the other parameters unchanged, and analyze the impact of different C_{ac} values on T_{cd}. The parameter values are 0.2mF, 0.3mF, and 0.4mF, respectively, and the corresponding Nyquist curve is shown in Fig. 27.

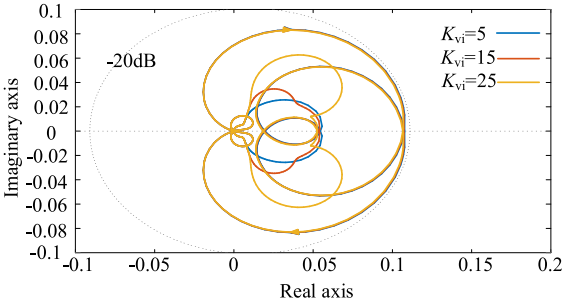

FIGURE 26. The Nyquist curve of T_{cd} with K_{vi} changed.

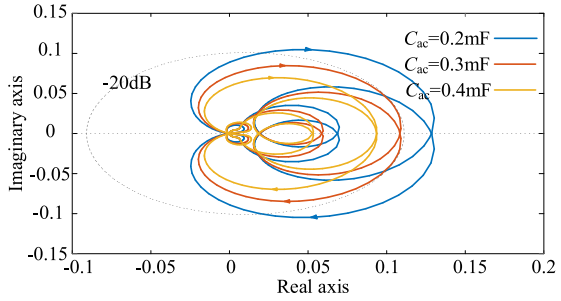

FIGURE 27. The Nyquist curve of T_{cd} with C_{ac} changed.

As shown in Fig. 27, with the increase of C_{ac}, the Nyquist curve gradually moves away from the $(-1, j0)$ point, and the stability margin of the system increases, which is beneficial for the stability of the system.

4) THE IMPACT OF ACTIVE CAPACITOR INDUCTOR L_{AC}

Keeping the other parameters unchanged, and analyze the impact of different L_{ac} values on T_{cd}. The parameter values are 0.3mH, 0.4mH, and 0.5mH, respectively. The corresponding Nyquist curve is shown in Fig. 28.

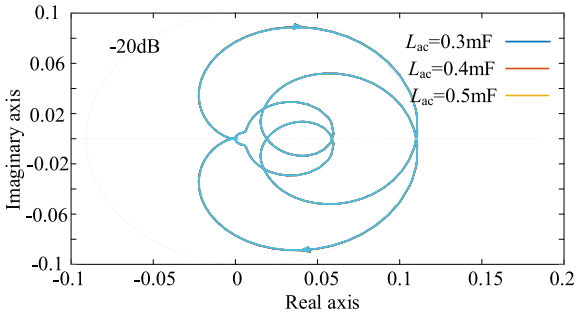

FIGURE 28. The Nyquist curve of T_{cd} with L_{ac} changed.

As shown in Fig. 28, as L_{ac} increases, the Nyquist curve remains almost unchanged, indicating that L_{ac} has almost no effect on the stability of the system.

5) THE IMPACT OF ENERGY STORAGE CONVERTER A

Take three different sets α value, keeping parameters unchanged. the impact α on T_{cd} is analyzed. The parameter

values are 1, 1.04, and 1.1, respectively, and the corresponding Nyquist curve is shown in Fig. 29.

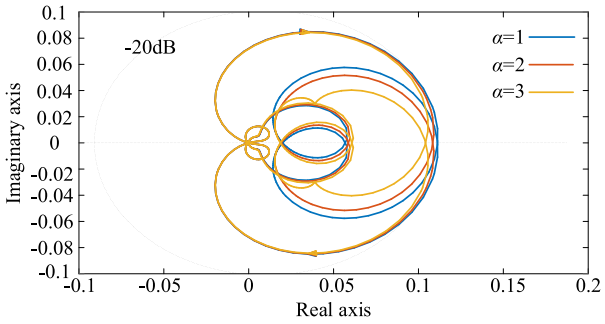

FIGURE 29. The Nyquist curve of T_{cd} with α changed.

As shown in Fig. 29, with the α increases, the Nyquist curve gradually moves away from the $(-1, j0)$ point, and the stability margin increases, which is beneficial to the stability of the system.

6) THE IMPACT OF ENERGY STORAGE CONVERTER R_D

Keeping the other parameters unchanged, and the impact of different r_d values on T_{cd} is analyzed. The parameter values are 0.3, 0.5, and 0.7, respectively, and the corresponding Nyquist curve is shown in Fig. 30.

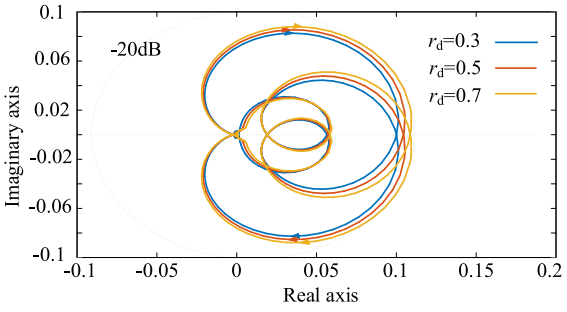

FIGURE 30. The Nyquist curve of T_{cd} with r_d changed.

As shown in Fig. 30, as r_d increases, the Nyquist curve gradually approaches the $(-1, j0)$ point, and the stability margin decreases, which is not preferable to system stability.

7) THE IMPACT OF ENERGY STORAGE CONVERTER K_{VP} AND K_{VI}

Firstly, the impact of the voltage outer loop control K_{vp} of the parameter energy storage converter on T_{cd} ia analyzed. Keeping other parameters unchanged, and only changing K_{vp}. The parameter values are 0.5, 0.7, and 1, respectively. The corresponding Nyquist curve is shown in Fig. 31.

As shown in Fig. 31, as K_{vp} decreases, the Nyquist curve gradually approaches the $(-1, j0)$ point, and the stability margin decreases, which is not preferable to system stability.

Secondly, the impact of the voltage outer loop control parameter K_{vi} of the energy storage converter on T_{cd} is analyzed, keeping other parameters unchanged, and only changing the voltage outer loop parameter K_{vi}. The parameter values are 50, 100, and 150, respectively. The corresponding Nyquist curve is shown in Fig. 32.

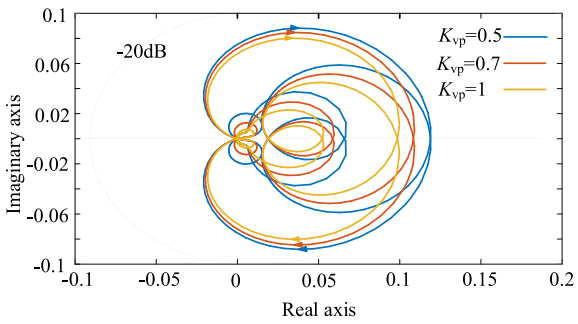

FIGURE 31. The Nyquist curve of T_{cd} with K_{vp} changed.

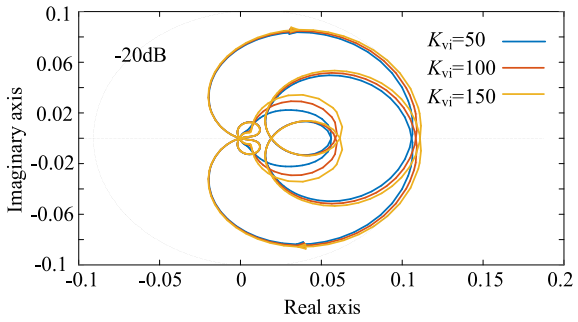

FIGURE 32. The Nyquist curve of T_{cd} with K_{vi} changed.

As shown in Fig. 32, as K_{vi} increases, the Nyquist curve gradually moves away from the $(-1, j0)$ point, and the stability margin increases, which is beneficial to the stability of the system.

VI. SIMULATION RESULTS

In this section, the proposed control strategies are modeled in MATLAB/Simulink, and its performance are analyzed in detail. The structure of the simulation system is the same with Fig.2. The control strategies and system parameters are same with theoretical parts.

Fig.33 shows the waveforms of energy storage converters before and after impedance modification. It can be seen that by increasing the output impedance of the bidirectional Buck/boost converter at 100Hz at 0.2s, the secondary ripple currents flown into energy storage battery is greatly reduced, but more secondary ripple voltage on the DC bus is presented.

Fig.34 shows the waveforms of system power quality for the active capacitor converter with and without impedance modification. It can be seen that when the impedance of the active capacitor Boost converter at 100Hz is reduced at 0.2s, most of the secondary ripple power on the DC bus flows into the active capacitor, and the secondary ripple content on the DC bus is greatly reduced.

Fig.35 shows the waveforms of power quality before and after adding coordinated control. It can be seen that the power quality of DC bus voltage and battery currents has

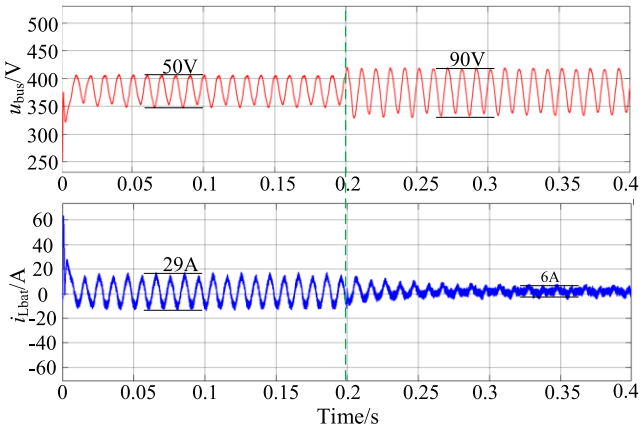

FIGURE 33. Waveforms of energy storage converters before and after impedance modification.

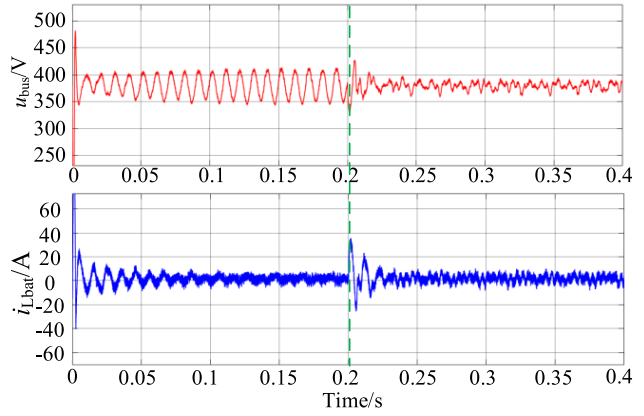

FIGURE 34. Waveforms of system power quality for the active capacitor converter with and without impedance modification.

been significantly improved after the addition of coordinated control strategy at 0.2s, and the DC Buck voltage still maintains good power quality. This further confirms that after the addition of coordinated control strategy, the direction of the second harmonic power in the system will change, and more will flow into the active capacitor circuit.

Fig.36 shows Transient waveforms with different control strategies. It can be seen that there are no secondary ripple components on the DC bus, battery side, and DC load side at 0-0.2s. After the single-phase inverter AC load is connected to the system at 0.2s, there are secondary ripple components presented at DC bus voltage, DC Buck voltage and battery currents, but the secondary ripple flowing into the DC load side will be relatively less, which is because the larger input impedance of the Buck converter. When the impedance of the bidirectional Buck/boost converter is increased at 100Hz at 0.4s, the secondary ripple currents flown into the energy storage battery side is greatly reduced, but the DC bus voltage will have more secondary ripple. When the improved active capacitor converter is connected to the system at 0.6s, most of the secondary ripple power of the DC bus flows into the

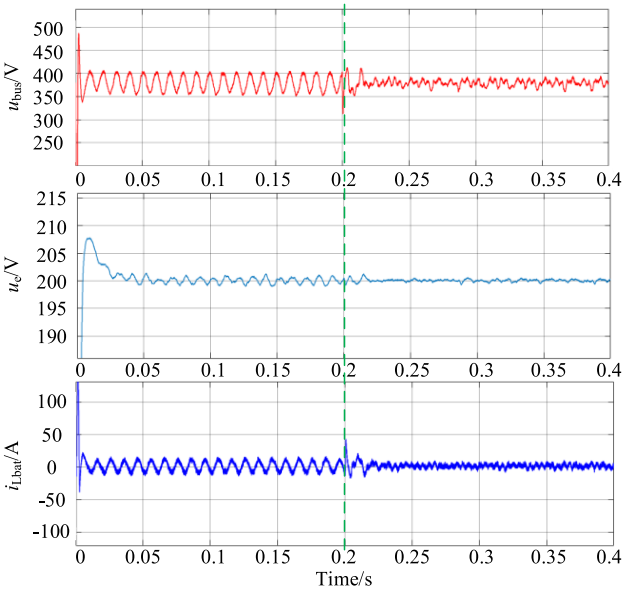

FIGURE 35. Waveforms of power quality before and after adding coordinated control.

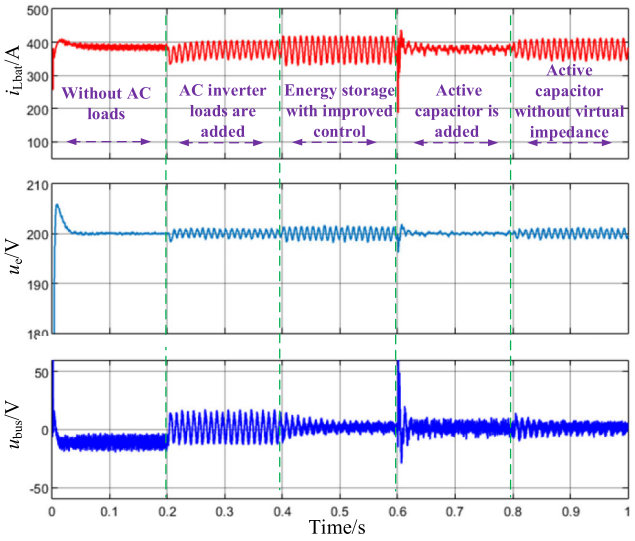

FIGURE 36. Transient waveforms with different control strategies.

active capacitor converter, and the secondary ripple DC bus voltage and battery currents both greatly reduced. When the virtual impedance in the improved active capacitor control strategy is removed at 0.8s, due to the insufficient impedance of the active capacitor converter at 100Hz, the secondary ripple power of the DC bus cannot easily flow into the active capacitor, resulting in increased secondary ripples at DC bus voltage and Buck load voltage.

Based on the above simulation, it can be obtained that the proposed impedance coordinated control strategy can not only eliminate the second harmonic current flowing into the energy storage battery, but also suppress the second harmonic voltage of the DC bus, and the system shows good dynamic and stable performance.

VII. CONCLUSION

In order to solve the problems of secondary ripple currents and voltages caused by single-phase AC inverter loads in DC microgrids, an impedance model based coordinated control strategy is proposed in this paper. The proposed control methods can not only reduce the secondary ripple currents flowing into energy storage units, but also suppress the DC bus ripple voltages appeared on the DC bus effectively.

The impedance models of the key units in the DC microgrid show that the energy storage units with droop control usually have a relatively small output impedance, which lead to large secondary current ripple flowing into energy storage units. The secondary current ripples can be reduced by improving the output impedance of energy storage converters and reducing the output impedance of the active capacitor converters through impedance reconstruction method. The secondary voltage ripples appeared on the DC bus can also be suppressed by reducing the output impedance of the active capacitor converters. Stability analysis results show that the DC microgrid has a good stability performance with the proposed impedance model based coordination control strategy.

The future work of this paper is to improve the compatible of the proposed method by considering more types of DC units. Besides, the future work will apply proposed method to real-word DC microgrid engineering, improving the adaptability of DC microgrids to AC loads and the power quality of DC microgrids.

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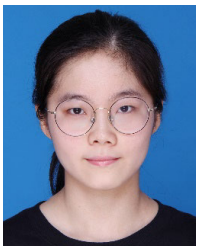

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