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RESEARCH ARTICLE

A New Second Order Nonlinear Formulation for Fast-SPICE Circuit Simulation

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ABSTRACT A new second-order matrix formulation is proposed in this work to model any nonlinear electronic system. This new formulation is developed and implemented by using a recasting method that increases the number of variables but limits the non-linearity to a quadratic form. Nonlinearity is modeled without any approximation and can model complex nonlinearities such as exponential and Tanh-based models. The new quadratic method is applied to the extended tanh MOSFET model and an exponential diode model to illustrate the power and reliability of this method. The method also has the advantage of directly stamping transistors and diodes into matrix forms in ways similar to linear elements. To demonstrate the validity of the new formulation, several circuits are examined, and the results compare very well to SPICE simulations. The simulation time as well as numerical stability improve significantly when using time marching techniques with the quadratic formulation as compared to directly stamping transistor and diode exponential nonlinearities.

INDEX TERMS Time-marching, nonlinear system, second-order recasting, stamping method.

I. INTRODUCTION

As VLSI technologies become denser and as chips operate at higher frequencies, circuit simulators face the challenge of increasing circuit complexity [1], [2], [3], [4]. Circuit simulations are important to understand the dynamics of complex systems of interacting elements, to test new concepts, and to optimize the designs. It is a very economical way to test complex designs. In integrated circuits (ICs), it is important to verify the design's accuracy before fabrication to avoid unnecessary prototypes.

Designers typically simulate the whole chip using dynamic simulators such as HSPICE, Spectre, and ELDO because such full chip accurate simulations are needed to guarantee the correct functionality of these chips under very tight design requirements [5], [6], [7]. However, a very fast-growing market has emerged for fast, reasonably accurate, simulators that can simulate very large designs much faster than full simulators with minimal errors. These simulators are generally called fast-SPICE and use approximate device models and simplified simulation techniques. Examples are NanoSim, Spectre FX, and Synopsys XA simulators [8], [9], [10].

As CMOS technology scaled down to the nanometer regime, many papers proposed various MOS transistor models to capture the transistor behavior in that regime [11], [12], [13], [14], [15], [16], [17], [18], [19]. Accuracy and complexity are the main factors that distinguish these MOS models. One such model is the alpha-power law MOSFET Model [20], which was introduced to include the carrier velocity saturation effect, which becomes eminent in short-channel MOSFETs. The alpha power law model is an extension of Shokley's square-law MOS model in the saturation region [21], [22]. The model is simple, has high fidelity, and is the basis for the widely used current source model in static timing analysis [23]. This model can be applied to handle MOSFET circuits rapidly and can predict the circuit behavior in the nanometer regime with reasonable accuracy.

A more accurate MOSFET model is the Tanh law model which uses a continuous model for the transistor across the

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linear and triode regimes [25]. The extended tanh model was extended to predict the temperature dependence of the drain current by including the temperature dependence of the threshold voltage and the mobility [24]. This model has several attractive features compared to SPICE level 2, especially at high temperatures.

A third popular MOSFET model is the modified Shichman Hodges (mSH) model, the three operation regions can be described utilizing a single equation [26], [29]. The mSH model combines the linear and saturation regions into a single equation giving a smoother transition compared to the original model, which causes a more abrupt switchover.

A new method for the simulation of circuits with nonlinear elements is proposed in this work. The method is based on a quadratic order recasting method that converts a complex nonlinearly into a standard second-order system with auxiliary extra variables. This particular formulation is efficient from a computational standpoint since the new second-order matrix formulation method depends on directly stamping any nonlinear system into matrix forms in ways similar to linear elements and eliminates the need to evaluate complex nonlinear functions repetitively during time marching. The simulation time as well as numerical stability improve significantly under time marching techniques when using the quadratic formulation as compared to directly stamping transistor and diode nonlinearities. The method has been tested with the aforementioned transistor models here, and the results are compared to an accurate full SPICE simulation.

The rest of this work is organized as follows: The Nonlinear Quadratic Formulation (NQF) is introduced in section II. Using the proposed model in nonlinear time-domain simulations is described in section III. The results of using the NQF for simulating several circuits are given in section IV and compared to traditional circuit simulators, Finally, conclusions are given in section V.

II. NONLINEAR QUADRATIC FORMULATION (NQF)

In this section, it is shown that any nonlinear system can be represented using the following Matrix equation:

$$G_1 V + (G_{21} V) \otimes (G_{22} V) + C\frac{dV}{dt} = B \tag{1}$$

where, G_1, G_{21},G_{22}, and C are matrices that represent the non-linear circuit, V is a vector that contains the circuit voltage variables (current and voltage variables in case of circuits with inductance) and auxiliary variables, and the operator $\otimes$ represents element-wise multiplication between two vectors. This representation can generate only up to a second power of a variable or the multiplication of two variables as given by the second term using G_{21},G_{22} in (1). However, as will be shown, circuits with higher-order nonlinearities, or more complicated nonlinearities such as exponentials, sinusoidal functions, or hyperbolic functions, can be recast to a second-order system without approximation with a recasting method that will be described below. The recasting method results in extra variables (auxiliary variables) in addition to the original voltage and current variables of the circuit. Nonlinear device models can be recast into a matrix format that can be easily stamped into the system in (1), resulting in the convenience of treating nonlinear elements the same way as linear elements when forming nodal matrix equations. Also, simple time-marching techniques can be used with this NQF without having to evaluate exponentials every time step or solve complex nonlinear equations as required in traditional Newton-Raphson methods for nonlinear circuits. Importantly, the Jacobian of the NQF formulation has a generic, circuit-independent closed form.

A. SECOND ORDER RECASTING METHOD

In this section, the second-order recasting method in [27] is described and applied to the extended tanh-law model and then stamped in the proposed NQF. The nonlinearity covered in this section includes tanh function nonlinearity.

1) RECASTING THE EXTENDED TANH LAW MODEL INTO THE SECOND-ORDER FORMULATION

The tanh MOSFET model proposed earlier by Shousha & Aboulwafa [25] was extended [26] to include the temperature dependence of the drain current since temperature affects the threshold voltage and mobility, which in turn affects the drain current. The model requires fewer temperature-dependent parameters as compared to SPICE models. The extended model shows good agreement between measurement and simulation of devices with different device geometries over a wide temperature range (−27 to 200 C°).

The extended tanh law model is described by the following set of equations [25]

$$I_{DS} = I_{D0}\, F(T)^{\alpha} \tanh\left(\frac{V_{DS}}{V_{D0}(\frac{F(T)}{2})^{\frac{\alpha}{2}}}\right). U\,(V_{GS} - V_{th}) \tag{2}$$

where V_{GS} is the gate-source voltage, V_{th} is the threshold voltage, $a(T)$ is the velocity saturation index, and the function $F(T)$ can be defined as

$$F(T) = \frac{V_{GS} - V_{th}(T)}{V_{DD} - V_{th}(T)} \tag{3}$$

and the parameters I_{D0} and V_{D0} are given by

$$\begin{aligned} I_{D0} &= \frac{W}{L}\mu(T) C_{ox} \frac{(V_{DD} - V_{th}(T))^2}{2a(T)} \\ V_{D0} &= \frac{V_{DD} - V_{th}(T)}{a(T)} \end{aligned} \tag{4}$$

and

$$U\,(V_{GS} - V_{th}) = \frac{e^{g(V_G - V_S - V_{th})}}{1 + e^{g(V_G - V_S - V_{th})}} \tag{5}$$

hich is a factor introduced by the authors of this paper to the model in [25] to describe the whole operation of the transistor including the cutoff region with one equation. The function in (4) is a good approximation of a unit step function for a large g.

By applying the proposed method in the tanh Law MOSFET model in equation (2). Two additional variables V_{a1} and V_{a3} are introduced as

$$V_{a_1} = e^{g(V_G - V_S - V_{th})} \tag{6}$$

and

$$V_{a_3} = U(T) \tag{7}$$

so equation (5) is written as:

$$V_{a_3} = \frac{V_{a1}}{1 + V_{a1}} \tag{8}$$

By differentiating V_{a1} we get:

$$\dot{V_{a_1}} = g(\dot{V_G} - \dot{V_S}) e^{g(V_G - V_S - V_{th})} \tag{9}$$

Equation (8) can be recast into three equations

$$V_{a_2} = \dot{V_G} - \dot{V_S} \tag{10}$$
$$\dot{V_{a_1}} = g\, V_{a_2} V_{a_1} \tag{11}$$
$$V_{a_1} = V_{a_3} + V_{a_3} V_{a_1} \tag{12}$$

By introducing an additional variable V_{a_4} as:

$$V_{a_4} = F(T)^{\alpha/2} \tag{13}$$

An additional variable V_{a_5} is introduced

$$V_{a_5} = \dot{V_{a_4}} = \frac{\alpha}{2} \frac{F(T)^{\alpha/2}}{F(T)} \dot{F(T)} \tag{14}$$

Therefore, combining (3), (13), and (14) results

$$\frac{\alpha}{2} V_{a_4} V_{a_2} + V_{a_5}(V_s - V_G) + V_{a_5} V_{th} = 0 \tag{15}$$

An additional variable V_{a_6} is introduced as

$$V_{a_6} = V_{a_4} V_{a_2} \tag{16}$$

Then equation (15) can be written as:

$$\frac{\alpha}{2} V_{a_6} + V_{a_5}\,(V_S - V_G) + V_{a_5} V_{th} = 0 \tag{17}$$

An additional variable V_{a_7} can be introduced as

$$V_{a_7} - V_{a_4}^2 = 0 \tag{18}$$

By introducing an additional variable V_{a_8}

$$V_{a_8} = \frac{V_D - V_S}{V_{D_0} \frac{V_{a_4}}{2^{\alpha/2}}} \tag{19}$$

or equivalently,

$$V_{a_4} V_{a_8} V_{D_0} - 2^{\alpha/2} V_D + 2^{\alpha/2} V_S = 0 \tag{20}$$

Let

$$V_{a_9} = \tanh V_{a_8} \tag{21}$$

Using two additional variables, $V_{a_{10}} \sinh V_{a_8}$ and $V_{a_{11}} = \cosh V_{a_8}$, the equation can be recast into the following quadratic, differential-algebraic system:

$$\dot{V_{a_{10}}} = \dot{V_{a_8}} \cosh V_{a_8} \tag{22}$$

$$\dot{V_{a_{11}}} = \dot{V_{a_8}} \sinh V_{a_8} \tag{23}$$

Let

$$V_{12} = \dot{V_{a_8}} \tag{24}$$

So, (22) and (23) will be

$$\dot{V_{a_{10}}} - V_{a_{12}} V_{a_{11}} = 0 \tag{25}$$
$$\dot{V_{a_{11}}} - V_{a_{12}} V_{a_{10}} = 0 \tag{26}$$
$$V_{a_9} = \frac{V_{a_{10}}}{V_{a_{11}}} \tag{27}$$

By substituting with equations (8), (18), and (27) in the model equation, we obtain

$$I_{DS} = I_{D_0} V_{a_7} V_{a_9} V_{a_3} \tag{28}$$

An additional variable $V_{a_{13}}$ is introduced as

$$V_{a_{13}} = V_{a_9} V_{a_3} \tag{29}$$

so tanh law model in equation (2) is rewritten as:

$$I_{DS_o} = I_{D_0} V_{a_7} V_{a_{13}}, \tag{30}$$

where I_{DSo} is the normalized transistor current with a width to length ratio of 1.

Thus, the extended tanh model can be recast to a system of 13 second order equations (10)-(12), (15)-(18), (20), (24)-(27), and (29) with 13 extra auxiliary variables ($V_{a1} - V_{a13}$). Additionally, there are 4 more equations for the 4 physical variables of the transistors, I_{DS}, V_G, V_D, and V_S. Four extra equations are needed for these physical variables. The equation for I_{DS} is simple and is always given by

$$I_{DS} = \frac{W}{L} I_{DS_0} \tag{31}$$

The three other equations for V_G, V_D, and V_S, can be found from the circuit structure using the standard nodal method. To illustrate this part of the formulation, consider the single-transistor inverter circuit shown in Fig. 1. The three circuit equations are:

$$C R \dot{V_D} + \frac{W}{L} R\, I_{DS} + V_D = V_{DD} \tag{32}$$
$$V_G = V_{in} \tag{33}$$
$$V_S = 0 \tag{34}$$

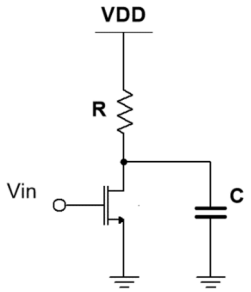

FIGURE 1. MOSFET inverter circuit.

The circuit part is the only part that depends on the circuit structure and only affects the matrices G_1, and C in the formulation since this part can only result in linear equations.

B. APPLYING THE STAMPING METHOD TO CIRCUITS WITH MULTIPLE NONLINEAR ELEMENTS

In this section, the general standard method for stamping nonlinear circuits into the NQF is described. The recasting of the transistor model described in the previous section is used here to model transistors. The next subsection starts by illustrating the stamping of a single transistor into the matrices of the NQF. It is shown in the following subsection that the stamping of circuits with multiple transistors is as easy as creating block diagonal matrices of those of a single transistor, which is independent of the circuit connections. The actual circuit connections are included in two sub-matrices that can be formed using the standard nodal method similar to linear circuits as illustrated in the previous section.

1) GENERAL MATRIX FORM FOR A SINGLE NONLINEAR ELEMENT

To separate the nonlinear recast model of the transistors from the external variables used in circuit connections with other elements, the variables in the nonlinear formulation are organized as follows:

1. The auxiliary variable whose number is n_a
2. I_{D_o} representing the normalized drain current of the transistor with $W/L = 1$
3. V_G, V_D and V_S represent the gate, drain, and source voltages of the transistor, respectively. Note that, the variables I_{D_o}, V_G, $V_{D,}$ and V_S are the variables that take part in the circuit equations.

The matrices in the NQF in equation (1) are subdivided into several sub-matrices as shown. The purpose of this particular division is to create sub-matrices that are independent of the circuit structure or the sizing of the nonlinear element (such as W/L of a transistor). Hence, this part does not change for a given nonlinear device in a given technology and is represented by the submatrices: $G_{1_{aa}}$, $G_{1_{VGDS}}$,$G_{1_{ID}}$,$G_{21_{aa}}$,$G_{21_{VGDS}}$,$G_{21_{ID}}$,$G_{22_{aa}}$,$G_{22_{VGDS}}$,$G_{22_{ID}}$,$C_{V_{GDS}}$ and C_{aa}. The only sub-matrices that depend on circuit connections are one submatrix of the G_1 matrix ($G_{1_{cir}}C$ matrix (C_{cir}*does not* stamp the nonlinear matrices (G_{21} and $G_{22}G_{aa}$ captures the intrinsic relations between the auxiliary variables of the transistor model. The first row after the auxiliary variables in each matrix contains the normalized current I_{D_0} as a function of the auxiliary variables. I_{D_0} is the drain current without the *W/L* size factor. The last three columns/rows represent the transistor voltages V_G, V_D, and V_S. The last part of the matrix is the circuit elements $G_{1_{cir}}$ which are based on the circuit connections. The circuit connections are related to the real variables V_G, V_D, $and I_{D_0}$, where I_D is given by $W/L \times I_{D_0}$.

$$G_1 = \begin{array}{c} \\ n_a \\ 1 \\ 3 \end{array} \begin{array}{c} \begin{array}{ccc} n_a & 1 & 3 \end{array} \\ \left[\begin{array}{c|c|c} G_{1aa} & \begin{array}{c}0\\ \vdots \\ 0\end{array} & G_{1V_{GDS}} \\ \hline G_{1ID} & 1 & 0\ldots 0 \\ \hline 0\ldots 0 & & G_{cir} \end{array}\right] \end{array}$$

$$G_{21} = \begin{array}{c} \\ n_a \\ 1 \\ 3 \end{array} \begin{array}{c} \begin{array}{ccc} n_a & 1 & 3 \end{array} \\ \left[\begin{array}{c|c|c} G_{21aa} & \begin{array}{c}0\\ \vdots \\ 0\end{array} & G_{21V_{GDS}} \\ \hline G_{21ID} & 0 & 0\ldots 0 \\ \hline \begin{array}{c}0\cdots 0\\ \vdots \ddots \vdots \\ 0\cdots 0\end{array} & & \begin{array}{c}0\cdots 0\\ \vdots \ddots \vdots \\ 0\cdots 0\end{array} \end{array}\right] \end{array}$$

$$G_{22} = \begin{array}{c} \\ n_a \\ 1 \\ 3 \end{array} \begin{array}{c} \begin{array}{ccc} n_a & 1 & 3 \end{array} \\ \left[\begin{array}{c|c|c} G_{22aa} & \begin{array}{c}0\\ \vdots \\ 0\end{array} & G_{22V_{GDS}} \\ \hline G_{22ID} & 0 & 0\ldots 0 \\ \hline \begin{array}{c}0\cdots 0\\ \vdots \ddots \vdots \\ 0\cdots 0\end{array} & & \begin{array}{c}0\cdots 0\\ \vdots \ddots \vdots \\ 0\cdots 0\end{array} \end{array}\right] \end{array}$$

$$C = \begin{array}{c} \\ n_a \\ 1 \\ 3 \end{array} \begin{array}{c} \begin{array}{ccc} n_a & 1 & 3 \end{array} \\ \left[\begin{array}{c|c|c} C_{aa} & \begin{array}{c}0\\ \vdots \\ 0\end{array} & C_{V_{GDS}} \\ \hline 0\cdots 0 & 0 & 0\ldots 0 \\ \hline \begin{array}{c}0\cdots 0\\ \vdots \ddots \vdots \\ 0\cdots 0\end{array} & & C_{cir} \end{array}\right] \end{array}$$

2) STAMPING OF A GENERAL CIRCUIT WITH MULTIPLE NONLINEAR ELEMENTS

The stamping method in the previous section can be seamlessly and elegantly expanded to circuits with any number of transistors. To achieve this task, the variables of all the transistors are organized such that the circuit-independent parts of all transistors are listed first followed by the circuit-dependent parts of all the transistors.

The variables in the multiple nonlinear formulation are organized as follows:

1- The auxiliary variables of all the transistors start with the first transistor, then the second, and so on $n_{a_{b1}}$, $n_{a_{b2}}, \ldots, n_{a_{bn}}$
2- I_{D_1} followed by I_{D_2} till I_{D_n} representing the normalized drain currents of the transistors with W/L=1
3- $V_{G_1}, V_{D_1}, V_{S_1}$ followed by $V_{G_2}, V_{D_2}, V_{S_2}$ till $V_{G_n}, V_{D_n}, V_{S_n}$ representing the gate, drain, and source voltages of all the transistors, respectively.

With this ordering of the variables, G_1 can be formed using the following block diagonal matrices. Note that all these matrices are independent of the circuit connections and are formed simply by repeating the corresponding matrix from a single transistor in the previous section if all transistors are similar. If the transistor models are different, the corresponding matrix of each transistor is stamped in a block diagonal format. As shown in the equation at the bottom of the next page, where G_{1aa_1} to G_{1aa_n} are block diagonal and contain the coefficients of the auxiliary variables in the model. I_{D_1} to I_{D_n} are diagonal columns that are coefficients of real voltages and current. I_{D_1} to I_{D_n} rows represent the relationship of the drain current to the auxiliary variables resulting from the recasting method.

The analysis results in two types of variables: physical variables (voltages and currents) and auxiliary variables to form the NQF from any nonlinearity. In the tanh model for example, the auxiliary variables are from V_{a1} to V_{a13} and physical variables are V_G, V_D, V_S, and I_{DS}. The matrix elements represent the coefficients of all variables. The matrix elements represent the coefficients of all variables. The tanh model is mathematically represented in the row from 1 to 14. These rows are independent of the circuit's connections. The matrix is divided into blocks for ease of handling and stamping in the NQF. The matrices G_{1aa},G_{1aGDS}, G_{1GDSa}, I_{DO}, and I_{aD} are the same for any transistor in the circuit while G_{1cir} is determined based on the circuit connections which are related to the real variables, V_G, V_D, V_S and I_D.

G_{1aa} contains the coefficients of the auxiliary variables in the tanh model. I_D column and G_{1aGDS} are coefficients of physical voltages. The I_D rows represent the relationship of the drain current to the auxiliary variables resulting from the recasting method form. G_{1cir} describes the nodal relations of real variables and is dependent on the circuit connections. G_{GDS_a} usually contains zero elements except there is a nonlinear function in circuit parts.

The list of all these matrices for G_1 as an example is given by:
The set of circuit-independent matrices are:

G_{1aa_1} to G_{1aa_n} are diagonal blocks that represent the coefficients of the auxiliary variables in the model.

$I_{D_{col_1}}$ to $I_{D_{col_n}}$ refers to diagonal columns with an element coefficient equal to zero.

$G_{1V_{GDS_1}}$ to $G_{1V_{GDS_n}}$ contain the coefficients of the real voltages.

$I_{D_{row_1}}$ to $I_{D_{row_n}}$ represent the coefficients of the real current.

$I_{D_{iden_1}}$ to $I_{D_{iden_n}}$ refers to the identity diagonal block with diagonal elements.

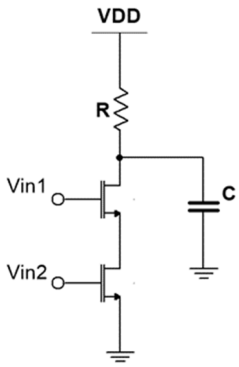

FIGURE 2. MOSFET two input NAND gate model.

The circuit dependent part is given by:
G_{1cir} describes the nodal relations of real variables and is dependent on the circuit connections.

To explain the concept, consider Fig,2, which depicts a double transistor circuit. The circuit independent matrices are composed by replicating the alpha power law single transistor circuit independent matrices two times in a block diagonal format. The circuit dependent part is found by applying the nodal analysis to the circuit and results in the matrices below.

$$\mathrm{G_{1_{Cir}}} = \begin{bmatrix} 0 & 0 & 1 & 0 & 0 & 0 & 0 & 0 \\ \frac{W}{L} \times R & 0 & 0 & 1 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 1 & 0 & -1 & 0 \\ 0 & 0 & 0 & 0 & 0 & 1 & 0 & 0 \\ \frac{W}{L} \times 1 & \frac{W}{L} \times -1 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 1 \end{bmatrix}$$

$$\mathrm{C_{Cir}} = \begin{bmatrix} 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & R \times C & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \end{bmatrix}$$

$$B = [[0; 0; 0; 0; 0; 0; 0; 0; 0; 0; 0; 0; 0; 0; V_{\mathrm{in}}; 1; V_{\mathrm{DD}}; 0];$$
$$[0; 0; 0; 0; 0; 0; 0; 0; 0; 0; 0; 0; 0; 0; V_{\mathrm{in2}}; 0; 0]]$$

III. USING THE PROPOSED MODEL IN NONLINEAR TIME-DOMAIN SIMULATIONS

The time-marching approach is the most common computer-aided circuit analysis technique to solve the system of ordinary differential equations that represent the circuit [30], [31], [32].

In this section, it is shown how to use the time marching technique to solve the NQF efficiently. The method proposed uses the Jacobian-Newton method to solve the nonlinear differential equations.

The NQF can be posed as the solution of $F = 0$ where F is given by:

$$F = G_1.V_j + G_{21}.V_j \otimes G_{22}.V_j + C\frac{dV}{dt} - BU = 0, \quad (35)$$

The NQF can be discretized in the time domain by using backward Euler discretization of differentiation as follows:

$$F = G_1.V_i + G_{21}.V_i \otimes G_{22}.V_i + C\frac{V_i - V_{i-1}}{dt} - BU = 0, \quad (36)$$

The Newton iteration used to solve nonlinear equations at each time step i as given by:

$$V_{i,j+1} = V_{i,j} - J^{-1} \times F \quad (37)$$

Using the differentiation rule of the operator given in Appendix, the Jacobian of F with respect to V_i can be found in a closed, generic form as:

$$J = G_1 + G_{21}.V_{i,j} \otimes G_{22} + G_{21} \otimes G_{22}.V_{i,j} + \frac{C}{dt} \quad (38)$$

Note that the Jacobian can be calculated in a closed form directly from the stamped matrices by using initial conditions

$$G_1 = \begin{array}{c} \\ nx13 \\ nx1 \\ nx3 \end{array} \begin{array}{c} \begin{array}{ccc} nx13 & nx1 & nx3 \end{array} \\ \left[\begin{array}{c|c|c} \begin{array}{ccc} G_{1aa_1} & & \\ & \ddots & \\ & & G_{1aa_n} \end{array} & \begin{array}{c} 0 \dots 0 \\ \vdots \ddots \vdots \\ 0 \dots 0 \end{array} & \begin{array}{ccc} G_{V_{GDS_1}} & & \\ & \ddots & \\ & & G_{V_{GDS_n}} \end{array} \\ \hline \begin{array}{ccc} I_{D_1} & & \\ & \ddots & \\ & & I_{D_n} \end{array} & \begin{array}{c} 1 \\ \ddots \\ 1 \end{array} & \begin{array}{c} 0 \dots 0 \\ \vdots \ddots \vdots \\ 0 \dots 0 \end{array} \\ \hline \begin{array}{c} 0 \dots 0 \\ \vdots \ddots \vdots \\ 0 \dots 0 \end{array} & G_{cir} & \end{array}\right] \end{array}$$

$$G_{12},\ G_{22} = \begin{array}{c} \\ nx13 \\ nx1 \\ nx3 \end{array} \begin{array}{c} \begin{array}{ccc} nx13 & nx1 & nx3 \end{array} \\ \left[\begin{array}{c|c|c} \begin{array}{ccc} G_{12,22aa_1} & & \\ & \ddots & \\ & & G_{12,22aa_n} \end{array} & \begin{array}{c} 0 \cdots 0 \\ \vdots \ddots \vdots \\ 0 \cdots 0 \end{array} & \begin{array}{ccc} G_{12,22V_{GDS_1}} & & \\ & \ddots & \\ & & G_{12,22V_{GDS_n}} \end{array} \\ \hline \begin{array}{ccc} G_{12,22I_{D_1}} & & \\ & \ddots & \\ & & G_{12,22I_n} \end{array} & \begin{array}{c} 0 \cdots 0 \\ \vdots \ddots \vdots \\ 0 \cdots 0 \end{array} & \begin{array}{c} 0 \dots 0 \\ \vdots \ddots \vdots \\ 0 \dots 0 \end{array} \\ \hline \begin{array}{c} 0 \cdots 0 \\ \vdots \ddots \vdots \\ 0 \cdots 0 \end{array} & \begin{array}{c} 0 \cdots 0 \\ \vdots \ddots \vdots \\ 0 \cdots 0 \end{array} & \end{array}\right] \end{array}$$

$$C = \begin{array}{c} \\ nx13 \\ nx1 \\ nx3 \end{array} \begin{array}{c} \begin{array}{ccc} nx13 & nx1 & nx3 \end{array} \\ \left[\begin{array}{c|c|c} \begin{array}{ccc} C_{aa_1} & & \\ & \ddots & \\ & & C_{aa_n} \end{array} & \begin{array}{c} 0 \cdots 0 \\ \vdots \ddots \vdots \\ 0 \cdots 0 \end{array} & \begin{array}{ccc} C_{V_{GDS_1}} & & \\ & \ddots & \\ & & C_{V_{GDS_n}} \end{array} \\ \hline \begin{array}{c} 0 \cdots 0 \\ \vdots \ddots \vdots \\ 0 \cdots 0 \end{array} & \begin{array}{c} 0 \cdots 0 \\ \vdots \ddots \vdots \\ 0 \cdots 0 \end{array} & \begin{array}{c} 0 \dots 0 \\ \vdots \ddots \vdots \\ 0 \dots 0 \end{array} \\ \hline \begin{array}{c} 0 \cdots 0 \\ \vdots \ddots \vdots \\ 0 \cdots 0 \end{array} & G_{cir} & \end{array}\right] \end{array}$$

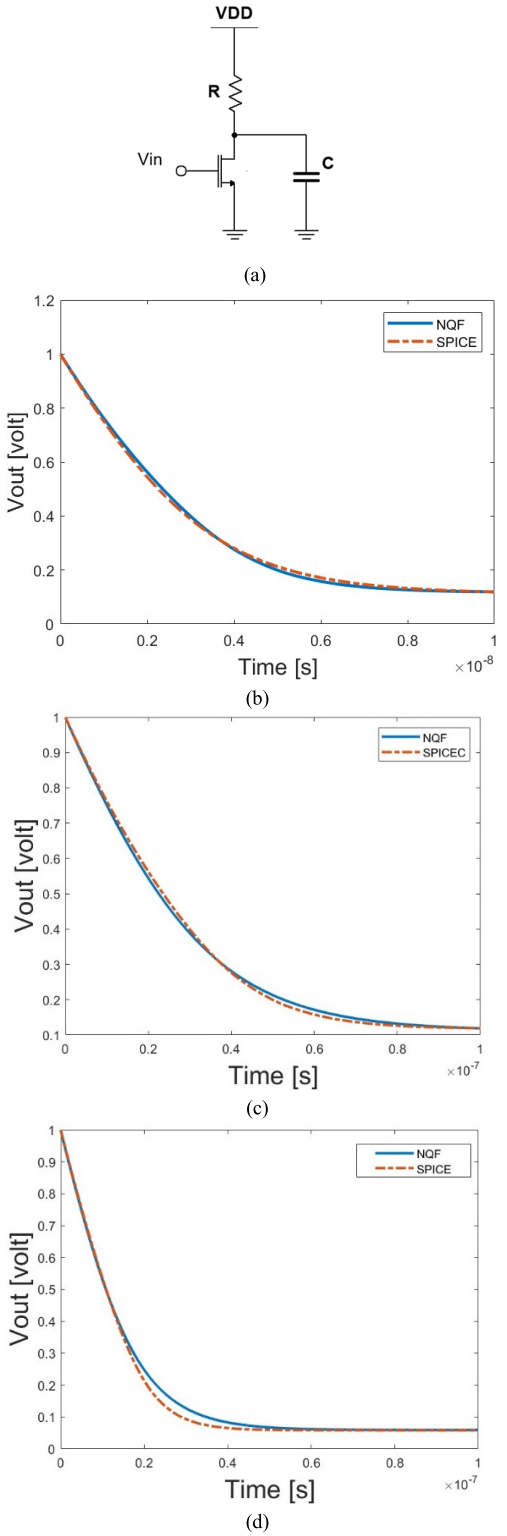

FIGURE 3. MOSFET inverter with L = 45nm: a) the circuit diagram, b) the output voltage results for W = 100nm, C = 1pF, c) W = 100nm, C = 10pF, and d) W = 200nm, C = 10pF.

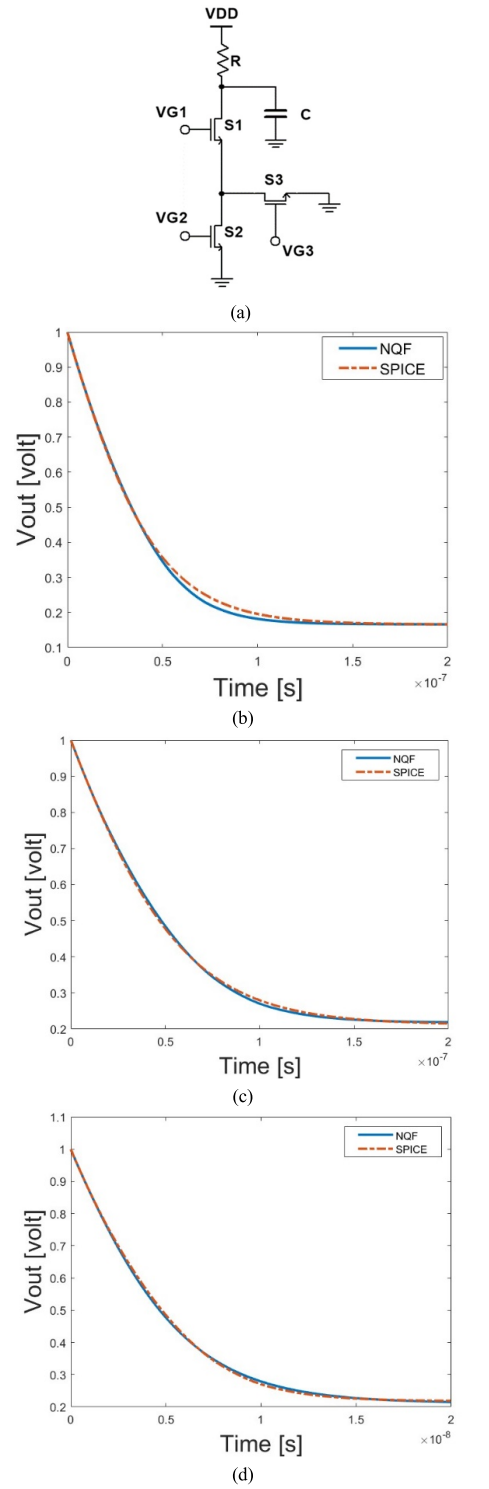

FIGURE 4. Three-transistors circuit with C = 10pF: a) the circuit diagram, b) the output voltage results for the three transistors are on, c) S3 off, and d) S3 is off and C = 1pF.

for the auxiliary variables and does not require the substitution in random nonlinear transistor functions. It can be noted that the nonlinear function part was moved to the initial conditions instead of inside the time marching loop as in traditional techniques.

IV. USING RESULTS FOR TIME MARCHING TECHNIQUE BASED ON THE SECOND ORDER FORMULATION

Simulations using the NQF time marching method described above with modified tanh model for the circuit are applied to three different circuits and compared to SPICE simulations. The first circuit is a single transistor circuit, while

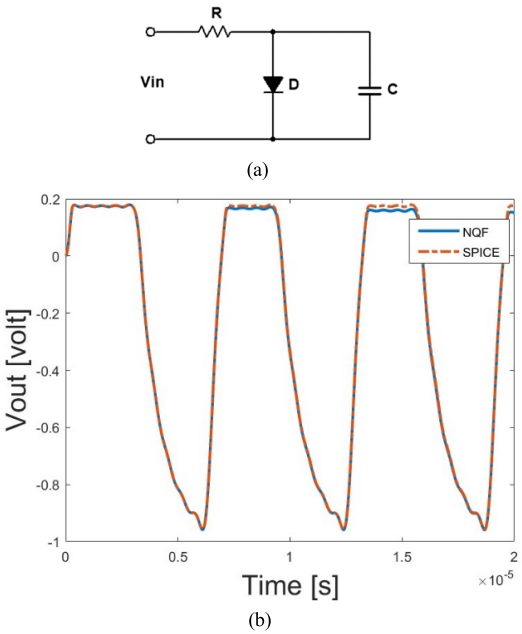

FIGURE 5. single-diode circuit [28]: a) the circuit diagram, b) the output voltage.

the second is a multiple-transistor circuit and the third is a diode-based circuit (Fig. 3, 4, and 5). Note that the simulation results closely match SPICE simulations with an accurate transistor model. Note also that these simulations are large signal simulations with extreme nonlinearity rather than a weekly nonlinear circuit simulation. It was observed that the convergence of the Newton-Jacobian method with the new NQF was much better than with the exponential transistor models due to the simpler nonlinearity. This resulted in a threefold improvement in simulation time on average with the circuits under test.

V. CONCLUSION

A new second-order matrix formulation is proposed to convert a complex nonlinearly into a standard second order system with auxiliary extra variables. This new formulation is developed and implemented to limit the non-linearity of the quadratic form. This new quadratic method is applied to the extended tanh MOSFET model and an exponential diode model to illustrate the power reliability of this method. The method also has the advantage of directly stamping transistors and diodes into matrix forms in ways similar to linear elements. Several examples are provided, and results compared very well to existing nonlinear simulation techniques.

APPENDIX

A pseudocode for the time marching technique used here is shown which solves the NQF nonlinear equations by using two nested loops. The code implements a simplified time marching method by using a loop along the time axis with a step of $dt = t_{end}/N$. The inner while loop solves the system of nonlinear equations by using Newton and Jacobean methods at each time step. The error is calculated at each iteration and the code moves to the next point in time when the error from the inner while loop is below 10^{-3}.

$$
\begin{aligned}
&t_{end} = 100; N = 3000; dt = \frac{t_{end}}{N}; t = [0 : n-1] \times dt \\
&V = zeros\,(n, N) \\
&Fori = 1 : N \\
&V_j = V_{O_1}; \\
&err = 1; \\
&j = 0; \\
&while\left(err > 10^{-3}\right) \\
&j = j + 1; \\
&J = G_1 + G_{21} \otimes \left(G_{22} \times V_j\right) + \left(G_{21} \times V_j\right) \otimes G_{22} + (\frac{C}{dt}); \\
&F = G_1 \times V_j + \left(G_{21} \times V_j\right) \otimes \left(G_{22} \times V_j\right) + \left(\frac{C}{dt}\right) \\
&\qquad \times V_j - \left(\frac{C}{dt}\right) \times V_{O_1} - B \\
&V_k = V_j - J^{-1} \times F; \\
&err = sum(abs(G_1 \times V_k + (G_{21} \times V_k) \otimes (G_{22} \times V_k) \\
&\qquad + \left(\frac{C}{dt}\right) \times V_k - \left(\frac{C}{dt}\right) \times V_{O_1} - B \\
&V_j = V_k; \\
&[ijV_k\,(1)\,err] \\
&end
\end{aligned}
$$

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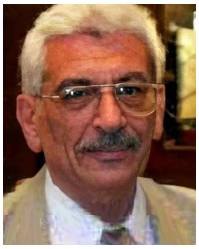

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