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APPLIED RESEARCH

Broadband Over Power Line Communication Prototype Development for Next Generation Smart Meters: Validation in Access Electric Power Distribution Networks

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ABSTRACT Broadband over Power Line (BPL) technologies are a successful solution for setting up communication networks in domestic environments. Several standards such as ITU-T G.hn and IEEE 1901 have evolved over the years, and commercial solutions based on them are currently available. However, most existing BPL technologies have not been designed to perform in Low Voltage (LV) access power distribution networks, so there is a need to adapt to the specificities of the communications channel found there. To accommodate the attainable performances of BPL technologies to the access segment of the grid, a communications prototype has been developed that injects custom BPL waveforms with different physical layer configurations and then measures performance. This prototype is an instrumental part of a process to define the most suitable physical layer parameters of Smart Grid BPL devices (namely, next generation BPL smart meters). In the absence of such a prototype, it is not feasible to obtain a proper characterization of the LV grid, as devices capable of producing OFDM (Orthogonal Frequency Division Multiplexing) modulations (typical of BPL technologies) with a varied set of adjustable features, and prepared to connect to the LV access grid, are not available in the market. The prototype is being used to carry out a measurement campaign in Iberdrola's LV grid in Spain. This paper shows how the prototype has been field validated and derives initial conclusions to drive the future of BPL in LV access grids for Smart Metering and other Smart Grids applications.

INDEX TERMS Smart meter, smart grid, BPL, PLC, prototype, access electric power distribution network.

I. INTRODUCTION

Broadband over Power Lines (BPL) for Low Voltage (LV) access electric power distribution networks remains a widely unexplored field. 'Access' segment is used in this paper, as opposed to the 'inside-the-home' segment of the LV grid.

BPL has been deployed in both Medium Voltage (MV) distribution networks and in-home LV grids. MV scenarios have been covered mainly with first generation BPL technologies [1], [2], [3], [4], [5]; some research and development programs [6] helped technology companies become expert in this segment, which can only be operated by utilities following strict procedures. Hence, assets (e.g., power lines and switchgears) that were not initially designed for it are now part of telecommunication networks. Technology companies also took advantage of the easy access to the part of the grid that belongs to the end-user (i.e., in-home scenarios); BPL technologies were adapted to work in this scenario

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(e.g., ITU-T G.hn [7], [8] and IEEE 1901 [9]) and, did find niche demand in the in-home networking market.

The LV access distribution network is a fundamental part of the grid in many world regions. In Europe, e.g., Distribution System Operators (DSOs) connect around 300 million customers with 10 million km of power lines; 60% of them are LV lines [10]. LV access grids start at Secondary Substations (SSs) where MV/LV transformers convert MV grid voltages into the most common three-phase electricity LV $3\times$ 230.400V service that is delivered to residential, commercial and industrial customers. Main assets in this grid segment include LV busbars, LV feeders consisting of LV powerline cables/wires of different dimensions and composition, street cabinets where cables are organized to reach different areas, splices to connect cables, fuse boxes, and finally electric meters that measure energy. LV grids are heterogeneous, with different topologies and widely distributed across territories. LV is well analyzed when it comes to narrowband Power Line Communications (PLC) technologies working below 500 kHz [11], [12], [13], [14], [15], [16], [17], but it has not been thoroughly characterized for the behavior of BPL technologies working above 1.8 MHz. There are studies, mostly in Europe, dating from the 1990s and early 2000s, but they just considered BPL technologies available at the time.

Modern BPL technologies have not been specifically developed for the LV access grid scenario or, are not the result of a large characterization effort of the LV access grid. Their selection of technological options was not that needed for the Smart Grid, involving near real-time communication latencies and stable broadband capabilities. By means of an example, Gbps throughputs are not necessary for Smart Grid applications, however reliability and stability of connections are needed; furthermore, the traffic in Smart Grid applications is different from the in-home entertainment scenario [18].

BPL standards such as G.hn and HomePlug AV2 (HPAV2) [19], which are advertised as capable of reaching speeds of up to several Gbps in domestic environments, are unable to provide adequate connectivity in the LV access distribution network, the main problem being that their physical layers (PHYs) have been designed for channels which characteristics are substantially different. For instance, both G.hn and HPAV2 employ Orthogonal Frequency Division Multiplexing (OFDM) modulations on the band between 1.8 MHz and $\sim$80 MHz (OFDM in different formats and with different parameters is to be conserved the de-facto standard in BPL [20]). However, field tests and measurements show that the BPL channel in the LV access grid often presents significant attenuation above 10 MHz, rendering these frequencies generally unusable for communications. IEEE 1901.1-2018 [21] relies on this fact when proposing the usable channel below 12 MHz. Hence, when BPL technologies are deployed over LV grids, only a fraction of all the available subcarriers are used. Specific modes for harsh conditions, such as Robust Communications Mode in G.hn and Robust OFDM (ROBO) in HPAV2, which employ additional repetition coding in the transmitter and receiver chains, do not completely solve reliability and stability issues. Consequently, one of the aspects to be investigated in this work is the effect of reducing the signal bandwidth and transmitting on frequencies that are known to provide less attenuation in the LV access grid.

Another aspect that can be optimized for BPL communications in the LV access segment is the channel coding schemes. Channel coding, in the form of Forward Error Correction (FEC), is a technique by which the information to be transmitted through a channel is protected from random errors by adding some extra information called redundancy. Turbo codes and Low-Density Parity Check (LDPC) codes are two of the most popular FEC's used in BPL; the former was adopted in HPAV2 and the latter in G.hn and IEEE 1901-2020 (among other alternatives). However, the decoding process complexity at the receiver is significant in both types of FEC, which sets lower bounds in the cost of the hardware required for BPL nodes. Hence, one aspect that needs to be further investigated is whether simpler FEC schemes –such as the classic Reed Solomon (RS) and convolutional encoder could be enough to achieve reasonable performance in the LV access grid when the characteristics of the communications waveforms (e.g., bandwidth and frequencies) match the channel.

This work presents a communications prototype that solves the major difficulty of performing tests on the field, that can render the LV access grid channel information needed, to derive a cost-effective solution for BPL communications in Smart Metering and Smart Grid applications. The prototype can transmit and receive OFDM waveforms with flexible configurations in terms of bandwidth and subcarrier spacing. The center frequencies of the transmitted signals can be defined from 1.8 MHz to 27 MHz. Also, different FEC's are supported, including the LDPC codes used in G.hn and 5G New Radio, turbo codes (as in LTE -4G-), and traditional convolutional + RS codes. The rest of the baseband processing chain follows the specifications in the G.hn standard, including constellations, scrambling, repetition encoding and the frame structure.

The goal of this prototype is to be able to test different PHY configurations in the field and analyze the performance each one provides, with a clear perspective on the implementation cost and implications of each alternative. The merit of this approach is that it does not require complex LV grid simulation models, which not always capture the nuances of the noise and frequency dependence in the LV access grid. Nonetheless, the architecture and nature of this prototype is such that the transmitter and receiver can easily be evaluated in end-to-end simulations, which can be useful to obtain preliminary dry run characterization results that complement field tests. This work has been organized as follows: Section II deals with the selection of PHY-layer parameters for BPL in the LV access grid and the associated trade-offs and implications; Section III presents the BPL communications prototype developed to test the performance of different PHY configurations; Section IV describes the

validation methodology of the prototype, and Section V the results. Finally, Section VI presents the conclusions of this work.

II. BPL PHY LAYER DESIGN FOR LV ACCESS CHANNELS

The electrical grid certainly supports PLC signals but was never intended or designed for this purpose. PLC can be considered opportunistic in the same way xDSL (Digital Subscriber Line) was; both technologies make use of an existing network to provide a new usage for it. In both cases, the limitations of existing assets deserve consideration. However, while a few changes were introduced in telephone networks for the support of new xDSL services, no change in the grid is expected in order to support PLC. This fact, together with the variety of grid topologies, variable noise sources, etc., makes PLC more challenging than other technologies.

Thus, PLC needs to adapt to the existing grid and its limitations. The design of narrowband PLC is relatively simple, for two reasons. Firstly, lower frequencies (kHz range) propagate further than higher frequencies (MHz range); secondly, smaller bandwidths can perform over lower-SNR (Signal-to-Noise Ratio) channels due to their lower expected throughputs.

The challenges of BPL are more complex in the LV grid domain. On the one hand, MHz range frequencies cannot typically support propagation distances of hundreds of meters within reasonable power budgets; on the other, wider channels (tens of MHz) neither present a uniform transfer function, nor do have low, uniform noise levels. So, some minimum LV grid reference considerations have to be derived, such that they can be used as BPL design criteria.

BPL signal will be typically connected in the SS, in some of the LV feeders reaching the electricity supply points. Although the typology of SSs is varied ([22] offers a classification based on quantity and density of meters per fuse box), it is expected that the SSs with the higher number of electricity supply points will be the main target of BPL systems. These SSs are typically found in urban areas, where distances among them, and with the street cabinets (fuse boxes) they connect to, are not large. Still, from a study recently made by i-DE (Iberdrola's DSO in Spain) for certain urban areas, it was found that the first street cabinet down the line (per LV feeder) can be expected to be further than 120 m (linear distance) in 45% of the cases, whereas 18% of the cases we can expect the first street cabinet to be 180 m away or further. The effect of distance can be relevant if we take into consideration the characterization of [23], where a 0.4 dB/m is calculated from field measurements in the 1.7 to 100 MHz range.

Taking this into consideration, subsequent subsections explore the various aspects that require attention to design robust BPL waveforms intended for the LV access segment of the grid.

A. FREQUENCY ASPECTS

It is a general understanding that LV access channels are more limited in frequency than the range typically used by in-home solutions such as G.hn/HPAV2.

While G.hn specification includes a Low Complexity Mode to limit energy below 25 MHz, both IEEE 1901.1-2018 and IEEE 1901-2020 address this limitation with channels below 12 MHz and 7.8125 MHz, respectively.

Thus, the prototype must support narrowing the bandwidth of BPL signals to match the channel bandwidth, to avoid wasting transmission power (energy efficiency) on subcarriers that will likely be received with much degraded SNR. In the current implementation, this can be achieved in several ways: by switching off some OFDM subcarriers given a particular subcarrier spacing; by decreasing subcarrier spacing while keeping the number of active subcarriers; or by modifying both subcarrier spacing and number of active subcarriers simultaneously. These capabilities offer a great deal of flexibility to test different OFDM waveform designs and parameter combinations, since the usable subcarrier spacing is bound by the channel statistical characteristics, reflected in parameters such as the coherence bandwidth and coherence time, among others [24], [25].

Similarly, the prototype also allows the selection of several Guard Interval (GI) lengths for its OFDM waveforms. Currently, the GI is based on the G.hn design, where OFDM symbols include a Cyclic Prefix (CP) and the whole symbol is windowed and overlapped. Windowing is an important feature for the transmitted signal to achieve a better spectral confinement within a given bandwidth, as well as deeper notches should some frequencies within the available bandwidth be protected (such as international amateur radio bands). The windowed sections are also time-overlapped on successive OFDM symbols to achieve a better spectral efficiency, since the windowed sections are not useful for the receiver. However, the better spectral confinement due to windowing comes at the price of decreasing the maximum excess delay spread of the channel that the receiver can fully equalize given a total GI length. Note as well that several references concluded that fully equalizing the channel may be a suboptimal strategy [26], [27], which means that using a GI length that is slightly shorter than the maximum excess delay spread, but long enough to avoid the majority of Inter-Symbol Interference (ISI), leads to improvements in the achievable throughput. Consequently, the prototype is designed with enough flexibility to test a variety of GI lengths, and different windowing functions and symbol overlapping factors may be tested with minor software modifications.

B. SNR ASPECTS

Having channels that are constrained in bandwidth and available SNR implies that the use of deep constellations (e.g., 4096-QAM -Quadrature Amplitude Modulation-) is most likely impractical in the LV access grid. Thus, it would be non-practical to design a prototype to be able to support them.

On the contrary, constellations up to 16-QAM, 64-QAM, and 256-QAM would be the maximum expected orders (this hypothesis is to be checked on the field).

Frame duration is a key transmission aspect in constrained channels, specifically in those where synchronous impulsive noise is to be expected [28]. There are examples of this in other PLC technologies used in LV access grid, where the maximum number and size of higher layer packets to be transferred in each frame is limited (using segmentation and reassembly techniques -e.g., [29]). Thus, the prototype is able to send short frames, as required by the channel, to address the impedance changes produced whenever any of the AC (Alternating Current) waveforms in a three-phase system crosses zero. While the transmission technique of AC cycle synchronization used by some PLC MAC layers is useful, the 3.3 or 6.6 ms limit (the 50 Hz wave period divided by 6 or 3, roughly, depending on various scenarios caused by the phase crosstalk in a three-phase system) is to be considered.

Fortunately, shorter frames contribute as well to minimize the effects of CFO (Carrier Frequency Offset). CFO estimation errors cause a cumulative phase offset that increases with time. If the CFO and channel are estimated only at the beginning of a given PHY frame (with the preamble and any channel-estimation symbols that may exist, for instance), the first payload symbols will show a near-perfect phase alignment, but as time advances, any CFO error will cause a phase offset build-up that will progressively degrade SNR, potentially causing demodulation errors further along payload symbols. Hence, short frames with few OFDM symbols ease down requirements in the demodulator, thus helping to reduce the total cost of devices. However, as the use of high-order constellations is not reasonable to shorten frames, this limitation will result in lower throughputs.

It is to be noted that to improve CFO estimations, the insertion of channel estimation OFDM symbols or reference subcarriers carrying pilot symbols may be useful. Even though these resources can provide a phase reference to avoid cumulative phase offsets due to CFO estimation errors, they will increase the frame duration and degrade efficiency. Another approach to tackle this problem is to adopt transmitter and receiver architectures that entirely avoid frequency up / down conversions in the time domain. Note that CFO is introduced when the signal is upshifted and downshifted in the spectrum with local oscillators that do not share the same exact frequency, and that these processes can be avoided by adopting OFDM de/modulators that cover all the band from DC (Direct Current) to the maximum channel frequency. This can be achieved by selecting the appropriate size for the IFFT/FFT (Inverse Fast Fourier Transform) blocks at the transmitter and receiver, allowing for spectral up/down shifting in the frequency domain. Even though this approach effectively avoids the need for local oscillators, the complexity of the OFDM de/modulators increases, and it can be shown that residual SCO (Sampling Clock Offset) between transmitter and receiver can still introduce CFO-like effects.

C. FORWARD ERROR CORRECTION ASPECTS

In BPL there are three major trends with regard to FEC schemes: turbo codes, LDPC codes, and a concatenation of a Reed Solomon code and a convolutional code (RS-CC). Turbo codes are employed by technologies such as HomePlug AV and HomePlug AV2, included in IEEE 1901-2020 as the FFT-based PHY. LDPCs were favored by G.hn, and RS-CC codes were added in the HD-PLC specification, now included in the Flexible Channel Wavelet PHY of IEEE 1901-2020.

A comprehensive comparative analysis focusing on duo-binary turbo codes (a variant employed in standards like DVB-RCS/RCS2 and 802.16 WiMAX) and Quasi-Cyclic LDPCs (QC-LDPC, chosen for standards like DVB-S2 and 5G New Radio) carried out before the actual specification of G.hn was completed showed several insights [7], [30], [31]. QC-LDPC exhibited a similar performance to turbo codes in AWGN (Additive White Gaussian Noise) conditions, with dependence on block length. Turbo codes, in contrast, manifested a higher error floor at higher SNRs, and their computational demands were proven to be more substantial in terms of computational complexity for decoding, as it was shown that turbo codes require fewer iterations, but each iteration carries a heavier computational load than LDPCs. Moreover, the practical implementation of the corresponding decoders is significantly influenced by various factors, including the selected architecture and decoding algorithms, which in turn affect other parameters such as memory requirements. Additionally, the choice of underlying hardware, whether it be Field-Programmable Gate Arrays (FPGA) or Application-Specific Integrated Circuits (ASIC), can decisively impact the final cost balance.

On the other hand, RS-CC FECs have been employed for decades in space communication links and as part of standards such as DVB-S. This type of FEC is characterized by its simplicity and low cost, although it has more limited error correction capabilities, resulting in stricter SNR requirements.

The selection of a FEC strategy greatly influences the design of a communications waveform and the cost of the resulting implementations. Consequently, G.hn LDPC, HomePlug AV Turbo Codes and RS-CC are supported by the prototype (see section III-C) for future testing.

III. BPL COMMUNICATIONS PROTOTYPE DEVELOPMENT

The following sections provide the details of the implementation and development process of the BPL prototype to transmit and receive frames over a LV access grid.

A. DESIGN AND ARCHITECTURE

The BPL communications prototype was designed with two main goals, namely: high flexibility, and agile development. The prototype was expected to support a variety of OFDM-based waveforms with different PHY configurations, with minimum effort required to develop new configurations or modify the existing ones. Hence, the prototype follows the

Software-Defined Radio (SDR) paradigm, by which the behavior of the hardware is defined by software components. Particularly, the transmitter and receiver baseband processing functions were coded as two independent Matlab [32] programs, which simulate all the algorithms required to produce the transmitted waveforms, and all the routines involved in the receiver demodulation and decoding stages, respectively. These software elements are combined with an FPGA-based hardware platform which injects transmission waveforms on one end and samples received signals at the other end. Therefore, the hardware platform is merely a signal generator/signal recorder with minimum signal processing functionality, which greatly simplifies the development process.

Also, one of the main requirements during prototype development was to obtain results in the field as early as possible. Hence, the hardware platform comprises mainly COTS (Commercial Off-The-Shelf) components and blocks. As a matter of fact, the core of the hardware platform is a ZCU111 RFSoC development kit provided by Xilinx [33]. RFSoCs are System-on-Chips (SoCs) that integrate an FPGA, an ARM processor, and several high-speed Digital-to-Analog and Analog-to-Digital Converters capable of synthesizing and sampling broadband RF (Radio Frequency) signals. The ZCU111 also includes all the auxiliary elements required by the RFSoC, so there is no need for any external components such as PLLs (Phase-Locked Loop) or clock sources. In between the ZCU111 and the electrical grid there is a custom PLC front-end that merely amplifies the transmitted and received signals and, filters out the 230 VAC component. This approach allowed for quick design iterations without having to undergo costly and complex hardware modifications, since the behavior of the hardware platform is defined by the SoC firmware, and the custom board amplifiers were designed so that their gains could be easily tweaked in the lab. Fig. 1 shows a schematic view of the prototype.

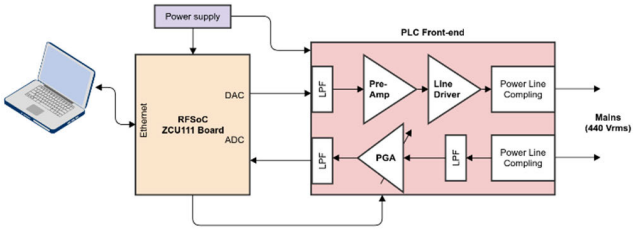

FIGURE 1. Block diagram of the prototype showing the components of the hardware prototype, as well as a laptop where the software components run.

To ease the process of generating test waveforms and analyzing sampled signals, two Graphical User Interface (GUI) applications were developed using the Matlab App Designer framework, which provides a number of controls that the user can interact with in order to configure parameters and execute the back-end transmitter and receiver routines. A third GUI application was also developed to assist the user in operating the hardware platform, providing an easy way of selecting a waveform for transmission, and taking a sample of the received signal.

The process required to test a given waveform configuration is as follows:

- Step 1: Generate a sample of the signal to be tested.
- Step 2: Send the sample to the hardware platform that acts as the transmitter.
- Step 3: Use the hardware platform that acts as a receiver to sample the received waveform.
- Step 4: Process the sample to demodulate the received signal.

Steps 1 and 4 can be performed offline, i.e. all signal samples can be pre-generated prior to field deployment, and all signal samples can be further processed in the laboratory after all the tests are done. Fig. 2 shows a possible deployment in the field in which two prototypes are used, one at a SS (left) and a second one at a fuse box.

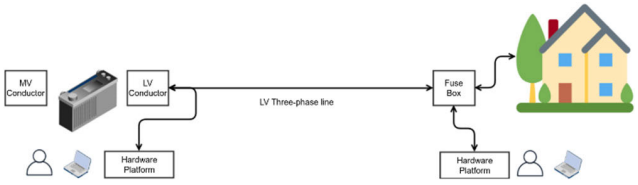

FIGURE 2. On-field use of the complete test platform.

The following subsections provide details about the prototype hardware and software design and implementation.

B. HARDWARE PLATFORM

The prototype hardware platform consists of two main components: the ZCU111 RFSoC development kit and the PLC front-end. The kit can be configured either as a signal transmitter or as a signal recorder by means of downloading the appropriate firmware; the ZCU111 includes a line driver to amplify the transmitted signal, and the front-end a low-noise amplifier for the received signal. These elements are used alternatively depending on the mode of operation configured in the ZCU111. Regardless of the mode, the ARM integrated in the ZCU111 runs an embedded Linux operating system in which the appropriate software routines are launched for each mode.

To better understand how the hardware platform works, its behavior is explained hereinafter for both operational modes.

When the prototype is configured as a transmitter (Fig. 3), a transmission server routine is launched in the embedded Linux, and then a specific firmware is downloaded to the RFSoC FPGA. This firmware includes an external DDR4 memory controller, a block to perform sampling rate matching in the transmitted signals, and an upconverter that feeds one of the RFSoC's Digital-to-Analog Converters (DACs). The DAC is further connected to the transmission path of the PLC front-end. Once the transmission server is up and running and the FPGA configuration ends, the platform is ready

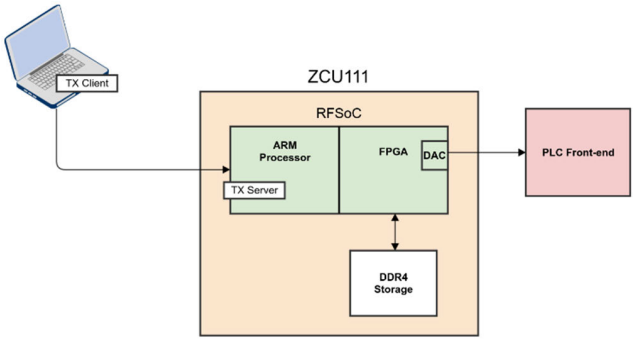

FIGURE 3. Prototype configured as a signal transmitter.

to generate signals, but remains silent until the user provides a signal sample. This process is carried out as follows:

1) The transmission server routine is contacted by a client routine (running on a laptop connected to the RFSoC by an Ethernet cable), who immediately sends a file containing the signal sample. The server stores this file in a DDR4 memory connected to the RFSoC's FPGA.
2) After the file is completely transferred, the server routine configures the remaining blocks in the FPGA to read the signal sample, perform the appropriate sampling rate adaptation, and upconvert the signal to the desired output frequency. At this point, the prototype starts generating a waveform matching the contents of the file with the signal sample, and continues this process cyclically (i.e., when the transmitter reaches the end of the file, it starts back again from the beginning).
3) To generate a different waveform, the server is contacted again by a client application and receives a new file, which is again stored in the external DDR4 memory. During this process, the FPGA blocks that read samples from this memory are halted, so the prototype remains silent until the file is completely transferred, at which point signal generation is resumed. This process can be repeated any number of times.

Note that communications between the server and client routines are TCP/IP (Transmission Control Protocol / Internet Protocol) based and follow a simple protocol by which each signal sample is encoded in 4 consecutive bytes, the first 16 bits reserved for the real part and the remaining 16 bits for the imaginary part. The sampling rate of any signal sample is fixed to 30.72 MSPS (Mega Samples Per Second), and internally upsampled to 245.76 MSPS in the sampling rate matching block. The upconverter is implemented by specific hard blocks within the RFSoC, represented by the Xilinx RFSoC RF Data Converter IP Core.

Considering that the external DDR4 memory can store up to 4 GB of data, the prototype can generate signal samples of up to 35 seconds, approximately.

When the prototype is configured as a receiver (Fig. 4), a reception server routine is launched in the embedded Linux, and then a specific firmware is downloaded to the RFSoC FPGA. In this case, the firmware contains a downconverter that receives signals from one of the RFSoC Analog-to-Digital Converters (ADC). Also, the rate matching block downsamples the signal from 245.76 MSPS to 30.72 MSPS. Consequently, the process to take a signal sample is as follows:

1) The reception server routine is contacted by a client routine (running on a laptop connected to the RFSoC by an Ethernet cable), that requests a signal sample of a given length.
2) The server configures the FPGA blocks to store the requested amount of data in the DDR4 memory and waits until completion.
3) Lastly the server reads back the stored waveform and sends it to the client.

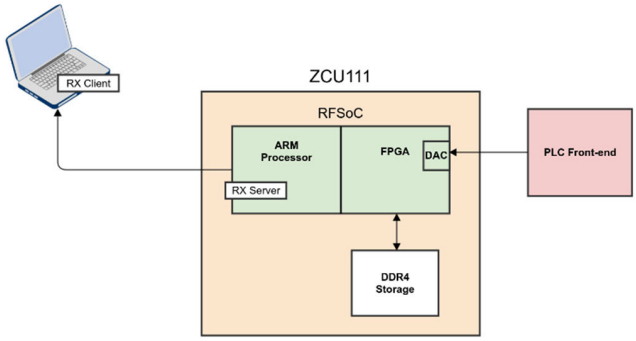

FIGURE 4. Prototype configured as a signal receiver.

To facilitate interactions with the prototype, a GUI application was developed using the Matlab App Designer framework. This application allows users to send and request signal samples to/from the prototype, calling the corresponding client applications with the appropriate parameters.

The PLC front-end block diagram is represented in Fig. 5. The transmission chain is represented on top and the reception chain at the bottom. The transmitter comprises a 27 MHz filter, a THS6222 [34] line driver that amplifies the signal, a transformer that provides galvanic isolation, some protection elements to avoid damage due to Electric Fast Transients (EFTs), and a high pass filter that removes the 230 V_{rms} AC (RMS is Root Mean Square) component. The design of the receiver is analogous to the transmitter, the main difference being that a THS7001 [35] Programmable Gain Amplifier (PGA) provides the required signal amplification in this case. The THS7001 PGA is also preceded by an additional low-pass filter that removes high-frequency noise, with a third-order Butterworth response and cutoff frequency of 27 MHz. Combined with the high-pass AC removal stage, this filter forms a band-pass channel selection stage. This filtering stage is further improved by a second 27 MHz low-pass filter at the end of the receiver chain, which acts as an anti-aliasing filter for the RFSoC ADC.

One important aspect of the PLC front-end design is the selection of the transmitter output impedance and the receiver

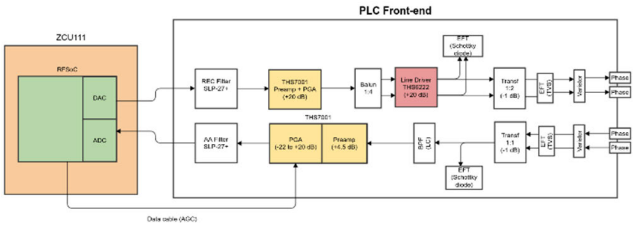

FIGURE 5. Block diagram of the PLC front-end.

input impedance. Ideally, if the transmitter were connected to the receiver through a transmission line with a given characteristic impedance to maximize power transfer, the output impedance of the transmitter should be zero and the input impedance of the receiver should be matched to the transmission line. However, setting the transmitter output impedance to zero may lead to large currents generated at its output, which could put the line driver at risk. This situation will happen if the magnitude of the impedance seen by the transmitter becomes small at any frequency where the transmitter is generating signals. Therefore, to avoid high currents at the transmitter output while not incurring in significant power losses, a small resistor should be placed at the output of the line driver. In the current design, this resistor has a value of 10 Ω, as it was determined this would guarantee that the line driver is safe even while driving impedances of a few Ohms.

Regarding the receiver impedance, in practice the characteristic impedance of the power line is highly frequency-dependent, and it can vary from a few tens of Ohms to several hundred Ohms. Therefore, there is no single value that maximizes power transfer for all frequencies, and thus a compromise choice must be selected. In the current design, the receiver impedance is set to 240 Ω.

Lastly, the receiver PGA is controlled by an Automatic Gain Control (AGC) scheme. The AGC scheme was implemented as a Matlab routine that is part of the GUI application that is used to operate the prototype. To establish the optimal gain, the AGC routine performs the following actions:

1) Set the minimum gain
2) Take a short signal sample.
3) Calculate the RMS value of the signal sample, x_{rms}.
4) Calculate the optimal gain as $G = x_{optimal} / x_{rms}$.

where $x_{optimal}$ is the desired RMS value at the input of the RFSoC ADC. Ideally, the value of $x_{optimal}$ should be such that the incoming signal fully covers the ADC input dynamic range without any clipping, and it can be calculated considering the ADC Full Scale values and the OFDM Crest Factor.

C. SIGNAL GENERATION AND ANALYSIS SOFTWARE

To generate and demodulate signal samples, a complete BPL transmission processing chain and the corresponding reception processing chain were independently modelled in Matlab. The transmission and reception functional blocks are represented in Fig. 6 and 7, respectively.

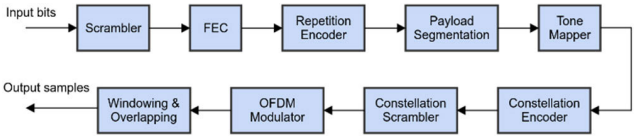

FIGURE 6. Baseband processing chain for the transmitter.

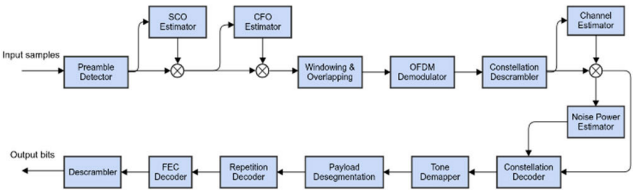

FIGURE 7. Baseband processing chain for the receiver.

Every frame comprises a preamble, a header symbol, up to 7 Additional Channel Estimation (ACE) symbols [7], and several payload symbols. The preamble waveform is G.hn-compliant and contains 7 repeated short symbols plus 2 additional inverted short symbols at the end. All OFDM symbols are generated with overlapping and windowing, for which a Raised Cosine window is employed.

As per the number of subcarriers (N) and subcarrier spacing (F_{SC}), the supported modes are based on the profiles defined in G.hn for powerlines and are summarized in Table 1. In all cases, the GI length of header and ACE OFDM symbols is 3N/8, whilst the CP length for all the remaining payload symbols can be selected as $(4+k)N/32$, with k being an integer from 1 to 8.

TABLE 1. List of supported OFDM transmission modes.

Mode	Number of subcarriers (N)	Subcarrier spacing (F_{SC}) [kHz]
1	1,024	24.4140625
2	1,024	12.20703125
3	1,024	6.103515625
4	1,024	3.0517578125
5	512	48.828125

Another difference is the support for different types of FEC. In addition to the G.hn FEC, it is possible to use the LTE turbo encoder, the 5G New Radio LDPC, or an SCCC (Serial Concatenated Convolutional Code). The LTE turbo encoder corresponds to the one defined in section 5.1.3.2 of [36]. It allows encoding blocks of size 960 or 4,352 bits, with outputs of size 2,892 and 13,068 bits respectively for the payload. The header is always encoded in a single block of size 168 bits, from which 516 bits are delivered. The 5G NR LDPC corresponds to the one defined in section 5.2.2 of [37], it encodes blocks of size 960 bits at rates of 1/5, 1/2, 2/3, 5/6 and 11/12 for the payload and a single bock of size 176 bits at rate of 1/2 for the header. On the other hand, the SCCC is composed of a RS outer encoder and a 1/2 rate convolutional inner encoder. The encoders are separated by

an interleaver block. The primitive polynomial of the RS encoder is $p(x) = x^3 + x + 1$. It operates with a Galois field (GF) of size 128 (GF 128), an input of 100 RS symbols ($k_{RS} = 700$ bits) and an output of 127 RS symbols ($n_{RS} = 889$ bits) for the payload. In the case of the header, it operates with a GF 64, an input of 28 RS symbols ($k_{RS} = 128$ bits) and an output of 63 RS symbols ($n_{RS} = 378$ bits). The convolutional encoder is based on the convolutional block of the PRIME (ITU-T G.9904) standard [38], which operates with the polynomials $p(x) = x^6 + x^5 + x^4 + x^3 + 1$ and $p(x) = x^6 + x^4 + x^3 + x + 1$. In summary, the full SCCC encoder allows encoding blocks of size 700 bits with output of size 1778 bits for the payload part, while for the header it encodes blocks of size 128 bits with output of size 756 bits.

Regarding the receiver, whose block diagram is shown in Fig. 7, it must cope with certain impairments introduced by the hardware itself, such as sampling rate deviations (SCO) and frequency offsets (CFO) that may exist between the transmitter and receiver platforms.

The SCO estimation method is based on knowing the exact number of samples between two points far enough apart so that the drift between transmitter and receiver clocks is appreciable. For this purpose, all frames are transmitted with a constant sample spacing between each frame and known to the receiver. Thus, if the receiver can detect two different frames and obtain the distance between them, it can calculate how many samples the separation obtained differs from the theoretical separation with which the signal was transmitted. For this calculation, the method proposed in section III-A of 40] is used. This value is measured in parts per million (ppm), which indicates the number of deviation samples after receiving one million samples.

The CFO estimation algorithm is based on the method proposed in section III-A of [40]. This algorithm compares the phase of two consecutive OFDM symbols received, eliminating the influence of modulation by multiplying by the conjugate of the same OFDM symbols transmitted. From this phase shift, the estimation of the frequency offset is obtained. To perform this estimation, the OFDM symbols used must be known to the receiver, so it can only be performed over the non-overlapped preamble short symbols or ACE symbols. The algorithm needs at least two OFDM symbols to operate and, in case more than two are used, an average of the estimates made every two consecutive symbols is performed.

The receiver also incorporates a channel estimator, in charge of compensating the amplitude and phase effects caused by the channel in the transmitted signal, which in general will have memory and be time-variant. Channel estimation is performed on symbols known to the receiver, such as the non-overlapping short symbols of the preamble, and the ACE symbols. For each OFDM symbol used for estimation, an estimate of the channel is obtained, and an average of all of them is taken. Once the average is obtained, the estimate is employed to equalize the channel. Lastly, the received information is decoded in the FEC stage and the information bits are descrambled.

The transmitter and receiver models generate and take complex baseband signals as outputs and inputs, respectively. It is the hardware platform that up converts and down converts these signals to/from the appropriate center frequency. Note that this approach was selected to minimize the memory capacity required to store a given signal sample, as this design leads to the lowest possible sampling rate. As we have already mentioned, the prototypes are capable of handling signal samples that are approximately 35 seconds long, which may contain thousands of frames for further analysis.

Lastly, several graphical applications have been developed to simplify the hardware platform management, signal generation and analysis. Fig. 8 and 9 show two of these applications.

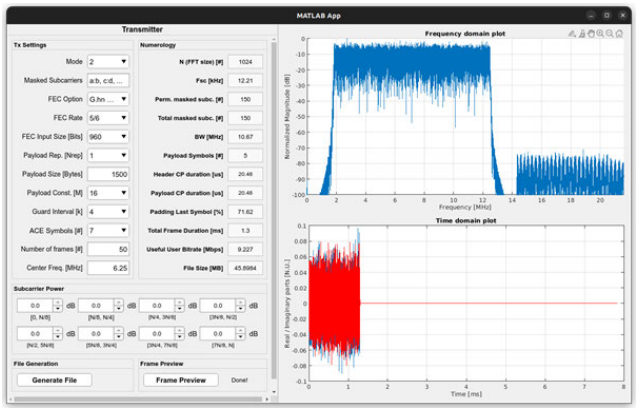

FIGURE 8. Signal generation application.

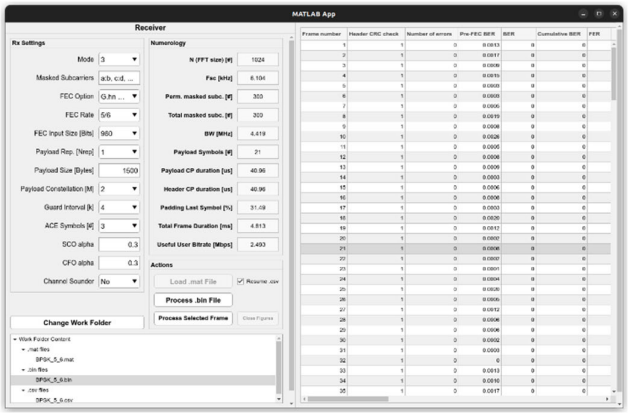

FIGURE 9. Signal analysis application.

IV. PROTOTYPE VALIDATION PROCESS

Once the prototypes have been thoroughly tested and characterized in the laboratory, they need to be validated on the field.

The validation has been performed in a real field deployment that today is using devices provided by Corinex [41]. Specifically, there is a Head-end device [42] connected in the SS, and BPL (so-called) high-performance repeaters [43] in street cabinets and meter rooms of the building. Fig. 10 shows the LV access network topology.

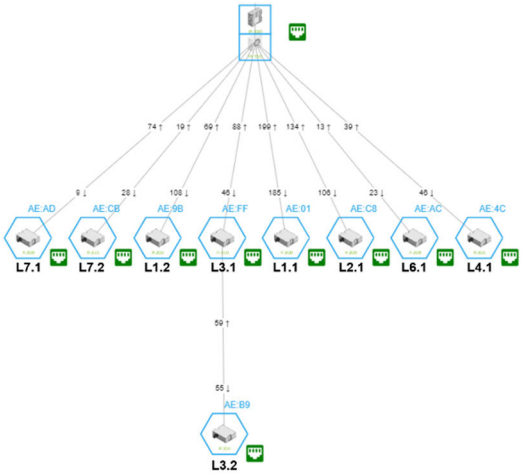

FIGURE 10. Secondary Substation in Spain, used for the LV access prototype validation.

The injection of the BPL field devices is as follows. At SSs, the Head-end injects BPL signals in several LV feeders (typically 1 to 3 feeders) with external LV BPL capacitive couplers connected to the three phases of each LV feeder. If more than one coupler is needed, then an additional 1:2 splitter or 1:3 splitter is also required to share the BPL signal. The propagation of the BPL signal is favored by its induction from one LV feeder to others following the same path from the SS to customer premises.

Down the LV feeders, LV BPL repeaters are connected to the 3 phases and neutral of each LV feeder; the capacitive coupler is internal to the BPL repeater. BPL signal uses spectrum from 2 to 28 MHz although some specific frequency ranges are notched (the corresponding carriers are deactivated). Additionally, the vendor reports that the BPL devices use MIMO (Multiple Input, Multiple Output) techniques: in the repeaters, channel 1 uses phases 1 and 3, and channel 2 uses neutral and phase 2 (the latter usually presents a higher noise level).

A. METHODOLOGY

Iberdrola intends to derive a relation between the results that today can be extracted from the performance values of the BPL network, and those that can be derived from the prototypes in similar working conditions. However, due to the limitations of the prototypes (i.e., they just implement a physical layer, and they can just send data from one end, and receive it on the other end, in a point-to-point fashion) a like-for-like comparison cannot be drawn. Thus, to understand the available scenario and data, some further details on the conditions are given in the following subsections.

1) SECONDARY SUBSTATION BPL OPERATION

The BPL network in the chosen location is in operation. Any telecommunications operational technology in Iberdrola is monitored, typically using an element or network management solution provided by the solution vendor, and some standard mechanisms that allow a controlled monitoring of the network.

In the case of the network under study, there is a network management system that can process the available bit rate at physical layer of every link between the Head-end and repeaters. This is shown, for a certain instant of time, in Fig. 11.

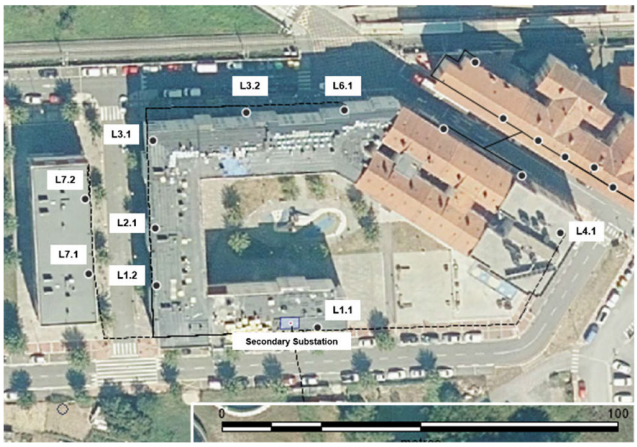

FIGURE 11. Instant physical layer raw bit rate of BPL links in the Secondary Substation under test.

The network management system can also record these data over a period of time, to derive statistical system performance parameters.

2) PROTOTYPE MEASUREMENTS

The BPL prototype consists of a pair of devices capable of working as transmitter or receiver (each prototype can be configured to act in one of the roles). Each device is attached to a PC that is used to drive the BPL transmission, or process and record the received BPL signal. The devices can be seen in Fig. 12.

FIGURE 12. BPL prototypes during laboratory tests (left) and real deployment (right).

TABLE 2. Physical layer parameters of the prototype.

Aspect	Available	Tested
Bandwidth (min. freq. - max. freq.)	2 - 27 MHz	2 – 12.67 MHz
Frame structure	Preamble + Header + 0 to 7 ACEs + Payload	Preamble + Header + 3 ACEs + Payload
Number of OFDM subcarriers	512 1,024	1,024
OFDM subcarrier separation (kHz)	48.828125 24.4140625 12.20703125 6.103515625 3.0517578125	24.4140625 12.20703125 6.103515625 3.0517578125
Payload constellations	All defined in G.hn (2^k-QAM with k from 1 to 12)	BPSK, QPSK, 8-QAM
CP lengths	Header: $\frac{3N}{8}$ Payload: $(4+k)\frac{N}{32}$ $k = 1, 2, \ldots, 8$	Header: $\frac{3N}{8}$ Payload: $\frac{3N}{8}$
Forward Error Correction (FEC) schemes	SCCC (RS-CC) G.hn QC-LDPC LTE turbo code 5G QC-LDPC	G.hn QC-LDPC (block size of 960 bits)

The test scenario considers that one of the devices is always connected at the SS, and the other device is moved in sequence to the different locations were the performance needs to be analyzed (i.e., street cabinets and meter rooms). For each measurement, one of the devices acts as the transmitter and the other as receiver, to eventually reverse the configuration so as to analyze BPL bidirectionally, from the SS to the meter locations, and the other way around.

The physical connection of the prototype is the same as the operational devices; clamps are the most common method at both sides. BPL injection uses signal coupling via a traditional 2-wire connection. At the SS, the transmitter is connected to the LV line that feeds the electrical point where the receiver is installed; at each receiving point, the prototype is directly connected to the same 2 phases (typically phases 1 and 3 on both sides of the LV line. Prototypes and regular operation devices use a LV capacitive coupler internal to them.

B. MEASUREMENT PARAMETERS SELECTION

1) PHYSICAL LAYER PARAMETER SELECTION

The prototype can be configured with a wide range of options. Specifically, Table 1 shows the available parameters in the prototype, and the subset of parameters that were tested.

As it can be seen in Fig. 13, each PHY frame follows a structure inspired in G.hn, starting with a preamble comprising a total of 9 short symbols (i.e. OFDM symbols with a subcarrier separation of $8F_{SC}$ but only N/8 subcarriers),

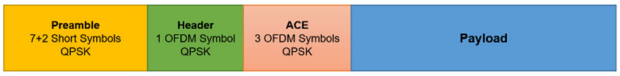

FIGURE 13. Physical layer frame structure.

followed by a header that spans a single OFDM symbol that carriers QPSK symbols, a total of 3 ACEs for channel estimation, and a payload formed by a variable number of OFDM symbols, all of them carrying pseudo-random information encoded in a given constellation from Table 2. All symbols in the same field share the same OFDM modulation parameters.

2) OTHER PARAMETER'S SELECTION

Prior to the definitive tests on the field, covering a complete SS, some unit tests were performed to limit the amount of possible test combinations on the field. On the one side, to perform all possible combinations in every bidirectional BPL channel is unaffordable due to measurement time limitations (because of cost and disturbance to residents living in the area). On the other side, the measurements intend to derive parameters to solve channel limitations in LV access networks, this is, to solve channel conditions rather than achieve the high performances expected in in-home scenarios.

Field measurement activity is time consuming. Adding to this, the bulk analysis of the data in the office is also a cumbersome process. Thus, not only the combination of parameters has been controlled, but the number of frames that are tested in each measurement round. While the initial tests used 2,000 and 1,000 frames, eventually the tests were performed with 250.

The channel limitation condition was also tested. Preliminary evidence of poor performance in some LV access channels was confirmed on the field. This made the selection of parameters to be focused on achieving robustness, rather than on higher throughput scenarios. This was also confirmed on the field in some selected locations, where regular BPL devices had shown to perform badly; when the BPL prototypes were connected and tested, higher order modulations and high-rate codes became useless. Some basic signal conditions were fixed to produce a BPL signal that could be comparable to the BPL signals that existing regular BPL devices were using. Thus:

- OFDM modulations with 1,024 subcarriers are used.
- BPSK (Binary Phase Shift Keying), QPSK (Quadrature Phase Shift Keying) and 8-QAM modulations.
- Bandwidths of 10.7, 4.4 and 1.3 MHz, centered below 12 MHz; all of them staring at 2 MHz, except the 1.3 MHz modes, where one of them starts at 4 MHz.
- Error correction based on LDPC, specifically with 1/2 and 5/6 rates.

Table 3 shows the 24 combinations tested on the field.

Due to the impulsive noise nature of PLC communications, 256-byte packets have been used. There is clear evidence of the impulsive noise influence on PLC [44], specifically

TABLE 3. BPL signal combinations tested on the field.

Mode	FREQUENCY RANGE (MHz)	Bandwidth (MHz)	Modulation	Error correction
A	2 - 12.67	10.67	BPSK	LDPC 1/2
A	2 - 12.67	10.67	BPSK	LDPC 5/6
A	2 - 12.67	10.67	QPSK	LDPC 1/2
A	2 - 12.67	10.67	QPSK	LDPC 5/6
A	2 - 12.67	10.67	8-QAM	LDPC 1/2
A	2 - 12.67	10.67	8-QAM	LDPC 5/6
C	2 - 6.42	4.42	BPSK	LDPC 1/2
C	2 - 6.42	4.42	BPSK	LDPC 5/6
C	2 - 6.42	4.42	QPSK	LDPC 1/2
C	2 - 6.42	4.42	QPSK	LDPC 5/6
C	2 - 6.42	4.42	8-QAM	LDPC 1/2
C	2 - 6.42	4.42	8-QAM	LDPC 5/6
E	2 - 3.29	1.29	BPSK	LDPC 1/2
E	2 - 3.29	1.29	BPSK	LDPC 5/6
E	2 - 3.29	1.29	QPSK	LDPC 1/2
E	2 - 3.29	1.29	QPSK	LDPC 5/6
E	2 - 3.29	1.29	8-QAM	LDPC 1/2
E	2 - 3.29	1.29	8-QAM	LDPC 5/6
F	4 - 5.29	1.29	BPSK	LDPC 1/2
F	4 - 5.29	1.29	BPSK	LDPC 5/6
F	4 - 5.29	1.29	QPSK	LDPC 1/2
F	4 - 5.29	1.29	QPSK	LDPC 5/6
F	4 - 5.29	1.29	8-QAM	LDPC 1/2
F	4 - 5.29	1.29	8-QAM	LDPC 5/6

with noise of periodic nature aligned with the 20 ms cycle of the electricity signal (50 Hz wave). Also, some initial tests on the field showed the dependence of performance on this parameter. Furthermore, thinking in Smart Grid applications, 256-byte packets are a common maximum value of many of the telecontrol protocols such as IEC 60870-5-104. One of the design targets of BPL systems in LV access grids may be keeping transmit times below 1/3 of the 10 ms semi-cycle, considering the three-phase nature of the electricity grid, and the crosstalk among phases.

V. RESULTS AND DISCUSSION

The PHY data rates of operational devices recorded over a 1-week period are shown in Table 4. The color code in the table shows a scale that assigns full red for a minimum value of 10 Mbps, and full green for a maximum of 100 Mbps; 50 Mbps is pictured as the middle point in the range.

The data rate results of the field measurements with the prototypes are shown in Tables 6–14. These measurements include different internal prototype values to analyze the results. Each table shows results in the Location when the signal in transmitted from the SS (tables A), and the reception in the SS when the signal is injected in the Location (tables B). FER (Frame Error Rate) and MER (Modulation Error Rate) values are provided. Additionally, each measurement includes a final result named "Absolute Frame Error Rate (ABS. FER)"; this result is calculated as the percentage of PHY frames that have been correctly received, out of the

TABLE 4. PHY data rates per repeater, extracted from the BPL network management system.

Location	Rx Data Rate (Mbps)	Tx Data Rate (Mbps)
L1.1	187.8	182.2
L1.2	77.7	100.4
L2.1	96.8	107.8
L3.1	75.7	65.9
L3.2	15.3	19.4
L4.1	35.5	40.5
L6.1	9.3	16.1
L7.1	66.3	17.3
L7.2	19.4	23.1

TABLE 5. Correlation of results for Mode A.

Modulation	FEC	Correlation
BPSK	1/2	-0.626
BPSK	5/6	-0.530
QPSK	1/2	-0.502
QPSK	5/6	-0.613
8-QAM	1/2	-0.488
8-QAM	5/6	-0.544

total number of the transmitted frames. The colors in the table show a relative scale to visually be able to compare results.

The visual inspection of these data leads us to some first conclusions that, even if they have low statistical support, are worth highlighting:

- So-called "A modes" -as in tables A.I to A.IX- tend to perform (in terms of availability) worse than "C modes". This fact supports (and is backed by) the known fact that higher frequencies behave worse for PLC.
- So-called "E" and "F modes" tend to perform (in terms of availability) better than "C modes". This implies that concentrating the prototype's available transmit power in the lowest part of the PLC channel, usually improves availability.
- Both previous observations imply that a solution that concentrates available transmit power in the best parts of the channel is needed.
- It is still to be studied what is the influence of the reduction in subcarrier spacing, without reducing the bandwidth, as the previous results have been obtained with a constant number of subcarriers.
- Frame Error Rate across the different test is coherent with theoretical and preliminary laboratory tests, where received SNR is found to be the highest in the case of BPSK 1/2, and then in descending order QPSK 1/2, BPSK 5/6, QPSK 5/6, 8PSK 1/2 and 8PSK 5/6.

TABLE 6. Results measured with the BPL prototype in location L1.1.

			Received in L1.1					Received in SS, from L1.1				
			Frames sent	FER	Header MER (dB)	ACE & Payload MER (dB)	ABS. FER.	Frames sent	FER	Header MER (dB)	ACE & Payload MER (dB)	ABS. FER.
A	BPSK	1/2	250	0,0%	24,0	26,0	0,0%	250	0,0%	24,7	27,1	0,0%
A	BPSK	5/6	250	0,0%	23,9	26,4	0,0%	250	0,0%	24,8	27,7	0,0%
A	QPSK	1/2	250	0,0%	23,8	26,5	0,0%	250	0,0%	24,7	27,6	0,0%
A	QPSK	5/6	250	0,0%	24,1	27,6	0,0%	250	0,0%	24,5	28,2	0,0%
A	8QAM	1/2	250	0,0%	24,3	27,0	0,0%	249	0,0%	24,8	27,7	0,4%
A	8QAM	5/6	209	23,0%	17,6	18,3	35,6%	250	0,0%	24,0	27,3	0,0%
C	BPSK	1/2	250	0,0%	27,9	25,2	0,0%	250	0,0%	29,9	26,4	0,0%
C	BPSK	5/6	250	0,0%	28,2	27,1	0,0%	250	0,0%	29,4	27,8	0,0%
C	QPSK	1/2	250	0,0%	28,4	28,0	0,0%	249	0,0%	30,2	29,9	0,4%
C	QPSK	5/6	250	0,0%	28,2	28,8	0,0%	249	0,0%	29,4	29,5	0,4%
C	8QAM	1/2	249	0,0%	28,2	28,5	0,4%	250	0,0%	29,7	29,9	0,0%
C	8QAM	5/6	250	2,0%	28,1	29,2	2,0%	250	0,8%	29,2	30,6	0,8%
E	BPSK	1/2	241	0,0%	26,1	16,3	3,6%	245	0,0%	25,0	16,0	2,0%
E	BPSK	5/6	250	0,0%	25,0	18,4	0,0%	249	0,0%	25,6	18,3	0,4%
E	QPSK	1/2	247	0,0%	24,9	19,3	1,2%	250	0,0%	25,6	19,5	0,0%
E	QPSK	5/6	250	0,4%	25,5	21,1	0,4%	225	36,4%	26,1	10,0	42,8%
E	8QAM	1/2	249	0,0%	25,4	20,9	0,4%	249	0,0%	25,6	21,2	0,4%
E	8QAM	5/6	248	8,9%	25,1	23,0	9,6%	237	19,4%	12,0	14,8	23,6%
F	BPSK	1/2	250	0,0%	33,6	24,4	0,0%	249	0,0%	33,9	24,9	0,4%
F	BPSK	5/6	250	0,0%	33,8	27,0	0,0%	250	0,0%	34,3	27,3	0,0%
F	QPSK	1/2	250	0,0%	34,4	28,8	0,0%	250	0,0%	34,5	28,7	0,0%
F	QPSK	5/6	250	0,0%	34,5	30,4	0,0%	249	0,0%	33,7	30,0	0,4%
F	8QAM	1/2	249	0,0%	33,5	29,7	0,4%	250	0,0%	34,4	30,6	0,0%
F	8QAM	5/6	249	0,0%	34,3	32,9	0,4%	249	0,0%	34,0	32,9	0,4%

TABLE 7. Results measured with the BPL prototype related to location L1.2.

			Received in L1.2					Received in SS, from L1.2				
			Frames sent	FER	Header MER (dB)	ACE & Payload MER (dB)	ABS. FER.	Frames sent	FER	Header MER (dB)	ACE & Payload MER (dB)	ABS. FER.
A	BPSK	1/2	250	0,0%	23,6	25,2	0,0%	248	0,0%	25,0	26,9	0,8%
A	BPSK	5/6	249	0,0%	23,7	25,7	0,4%	247	0,0%	22,1	23,7	1,2%
A	QPSK	1/2	250	0,0%	23,7	25,6	0,0%	250	0,0%	25,1	27,3	0,0%
A	QPSK	5/6	250	0,0%	23,6	26,2	0,0%	250	0,0%	22,1	24,4	0,0%
A	8QAM	1/2	250	0,0%	23,5	25,4	0,0%	248	0,0%	25,0	27,0	0,8%
A	8QAM	5/6	250	0,0%	23,9	26,3	0,0%	249	0,0%	22,3	24,1	0,4%
C	BPSK	1/2	250	0,0%	24,9	24,7	0,0%	250	0,0%	26,6	25,4	0,0%
C	BPSK	5/6	250	0,0%	25,5	26,1	0,0%	250	0,0%	28,4	27,9	0,0%
C	QPSK	1/2	250	0,0%	25,3	26,3	0,0%	249	0,0%	26,8	27,2	0,4%
C	QPSK	5/6	249	0,0%	25,4	26,8	0,4%	250	0,0%	27,1	28,1	0,0%
C	8QAM	1/2	250	0,0%	25,3	26,3	0,0%	250	0,0%	28,5	28,8	0,0%
C	8QAM	5/6	250	0,0%	25,1	27,1	0,0%	250	0,0%	29,4	30,5	0,0%
E	BPSK	1/2	249	0,0%	23,7	21,2	0,4%	248	0,0%	27,8	21,2	0,8%
E	BPSK	5/6	250	0,0%	25,2	22,4	0,0%	249	0,0%	27,7	22,9	0,4%
E	QPSK	1/2	250	0,0%	25,4	23,5	0,0%	250	0,0%	27,5	24,0	0,0%
E	QPSK	5/6	250	0,0%	25,8	24,7	0,0%	250	0,0%	27,2	24,8	0,0%
E	8QAM	1/2	249	0,0%	25,8	24,5	0,4%	250	0,0%	27,6	24,9	0,0%
E	8QAM	5/6	250	0,0%	25,5	25,7	0,0%	248	0,8%	27,8	26,5	1,6%
F	BPSK	1/2	249	0,0%	36,8	28,4	0,4%	248	0,0%	35,7	25,9	0,8%
F	BPSK	5/6	248	0,0%	36,6	29,2	0,8%	250	0,0%	34,8	28,7	0,0%
F	QPSK	1/2	249	0,0%	36,5	30,8	0,4%	248	0,0%	35,7	30,6	0,8%
F	QPSK	5/6	249	0,0%	36,6	32,9	0,4%	247	0,0%	35,2	31,4	1,2%
F	8QAM	1/2	250	0,0%	36,8	33,2	0,0%	249	0,0%	35,6	31,7	0,4%
F	8QAM	5/6	246	0,0%	32,9	32,3	1,6%	248	0,0%	34,6	33,4	0,8%

TABLE 8. Results measured with the BPL prototype related to location L2.1.

			Received in L2.1					Received in SS, from L2.1				
			Frames sent	FER	Header MER (dB)	ACE & Payload MER (dB)	ABS. FER.	Frames sent	FER	Header MER (dB)	ACE & Payload MER (dB)	ABS. FER.
A	BPSK	1/2	250	0,0%	25,1	26,3	0,0%	250	0,0%	24,2	25,3	0,0%
A	BPSK	5/6	250	0,0%	24,9	26,7	0,0%	250	0,0%	26,7	29,1	0,0%
A	QPSK	1/2	249	0,0%	24,9	26,7	0,4%	249	0,0%	26,6	28,9	0,4%
A	QPSK	5/6	250	0,8%	24,8	27,5	0,8%	250	0,0%	26,8	29,9	0,0%
A	8QAM	1/2	249	0,0%	25,1	26,7	0,4%	250	0,0%	26,9	29,5	0,0%
A	8QAM	5/6	250	0,8%	24,8	26,9	0,8%	250	0,0%	27,0	29,6	0,0%
C	BPSK	1/2	250	0,0%	25,9	24,3	0,0%	250	0,0%	29,4	26,2	0,0%
C	BPSK	5/6	250	0,0%	26,7	26,3	0,0%	250	0,0%	30,1	28,5	0,0%
C	QPSK	1/2	250	0,0%	26,7	27,0	0,0%	250	0,0%	30,4	29,8	0,0%
C	QPSK	5/6	250	0,0%	27,0	27,8	0,0%	250	0,0%	30,6	31,0	0,0%
C	8QAM	1/2	250	0,0%	26,8	27,4	0,0%	250	0,0%	29,8	29,7	0,0%
C	8QAM	5/6	250	0,0%	27,0	28,2	0,0%	250	0,0%	30,0	31,7	0,0%
E	BPSK	1/2	250	0,0%	26,7	19,6	0,0%	250	0,0%	29,2	21,4	0,0%
E	BPSK	5/6	249	0,0%	27,1	22,1	0,4%	250	0,0%	28,4	22,8	0,0%
E	QPSK	1/2	250	0,0%	27,2	23,6	0,0%	250	0,0%	28,5	24,3	0,0%
E	QPSK	5/6	250	0,0%	27,5	24,6	0,0%	249	0,0%	28,7	25,7	0,4%
E	8QAM	1/2	250	0,0%	27,6	24,8	0,0%	249	0,0%	29,0	25,7	0,4%
E	8QAM	5/6	250	0,0%	26,9	26,3	0,0%	250	0,0%	28,4	27,4	0,0%
F	BPSK	1/2	250	0,0%	29,6	18,4	0,0%	250	0,0%	32,8	15,3	0,0%
F	BPSK	5/6	249	0,0%	30,5	20,9	0,4%	250	0,0%	29,9	20,6	0,0%
F	QPSK	1/2	248	0,0%	31,2	23,5	0,8%					
F	QPSK	5/6	249	0,0%	31,6	25,6	0,4%					
F	8QAM	1/2	249	0,0%	30,7	25,1	0,4%	250	0,0%	31,2	24,9	0,0%
F	8QAM	5/6	249	0,0%	29,5	27,2	0,4%	250	0,0%	31,2	28,2	0,0%

TABLE 9. Results measured with the BPL prototype related to location L3.1.

			Received in L3.1					Received in SS, from L3.1				
			Frames sent	FER	Header MER (dB)	ACE & Payload MER (dB)	ABS. FER.	Frames sent	FER	Header MER (dB)	ACE & Payload MER (dB)	ABS. FER.
A	BPSK	1_2	250	0,0%	24,4	26,3	0,0%	246	0,0%	22,5	23,9	1,6%
A	BPSK	5_6	250	0,0%	24,3	26,9	0,0%	249	0,0%	22,7	24,6	0,4%
A	QPSK	1_2	250	0,0%	24,3	27,0	0,0%	249	4,0%	15,8	15,6	4,4%
A	QPSK	5_6	250	0,0%	24,3	27,5	0,0%	247	1,6%	22,5	25,0	2,8%
A	8QAM	1_2	244	0,0%	24,5	27,1	2,4%	249	0,0%	20,8	22,2	0,4%
A	8QAM	5_6	249	0,0%	24,5	27,5	0,4%	250	5,2%	22,7	25,0	5,2%
C	BPSK	1_2	249	0,0%	21,8	21,9	0,4%	250	0,0%	23,8	22,4	0,0%
C	BPSK	5_6	249	0,0%	26,7	27,2	0,4%	249	0,0%	22,6	22,4	0,4%
C	QPSK	1_2	248	0,0%	27,0	27,8	0,8%	250	0,0%	23,7	23,8	0,0%
C	QPSK	5_6	249	0,0%	27,0	28,2	0,4%	249	0,8%	24,3	24,7	1,2%
C	8QAM	1_2	249	0,0%	18,5	19,4	0,4%	250	9,2%	12,0	10,9	9,2%
C	8QAM	5_6	248	0,0%	26,2	27,8	0,8%	249	3,6%	22,0	22,9	4,0%
E	BPSK	1_2	246	0,0%	26,4	21,9	1,6%	245	0,0%	21,1	18,1	2,0%
E	BPSK	5_6	238	0,8%	26,3	23,3	5,6%	241	0,0%	23,1	19,6	3,6%
E	QPSK	1_2	239	0,4%	16,3	16,1	4,8%	243	0,0%	22,8	20,4	2,8%
E	QPSK	5_6	246	0,0%	26,5	25,4	1,6%	245	0,0%	21,7	20,6	2,0%
E	8QAM	1_2	241	0,0%	26,8	25,6	3,6%	238	0,4%	23,1	21,0	5,2%
E	8QAM	5_6	243	0,0%	26,4	26,7	2,8%	244	1,2%	21,9	21,9	3,6%
F	BPSK	1_2	248	0,0%	36,0	27,0	0,8%	250	0,0%	30,8	25,3	0,0%
F	BPSK	5_6	249	0,0%	35,7	29,5	0,4%	249	0,0%	30,5	27,1	0,4%
F	QPSK	1_2	248	0,4%	36,0	30,3	1,2%	248	0,0%	30,4	27,7	0,8%
F	QPSK	5_6	250	0,0%	35,3	32,0	0,0%	249	0,0%	34,5	31,0	0,4%
F	8QAM	1_2	250	0,0%	34,9	31,8	0,0%	250	0,0%	30,3	28,6	0,0%
F	8QAM	5_6	250	0,0%	35,0	33,6	0,0%	249	0,0%	33,8	32,2	0,4%

TABLE 10. Results measured with the BPL prototype related to location L3.2.

			Received in L3.2					Received in SS, from L3.2				
			Frames sent	FER	Header MER (dB)	ACE & Payload MER (dB)	ABS. FER.	Frames sent	FER	Header MER (dB)	ACE & Payload MER (dB)	ABS. FER.
A	BPSK	1_2	247	0,4%	13,9	13,8	1,6%	250	0,0%	13,0	13,1	0,0%
A	BPSK	5_6	245	2,0%	13,9	14,1	4,0%	248	0,0%	17,6	18,4	0,8%
A	QPSK	1_2	250	0,0%	13,9	14,0	0,0%	250	0,0%	17,7	18,5	0,0%
A	QPSK	5_6	250	6,4%	13,9	14,2	6,4%	246	0,4%	17,6	18,7	2,0%
A	8QAM	1_2	241	2,9%	14,1	13,7	6,4%	250	0,4%	17,9	18,4	0,4%
A	8QAM	5_6	235	31,9%	14,1	14,2	36,0%	246	6,1%	17,9	18,8	7,6%
C	BPSK	1_2	249	0,0%	22,2	20,9	0,4%	249	0,0%	24,7	22,6	0,4%
C	BPSK	5_6	250	0,0%	21,7	21,4	0,0%	249	0,0%	25,1	24,2	0,4%
C	QPSK	1_2	250	0,0%	22,4	22,7	0,0%	248	0,0%	24,9	24,8	0,8%
C	QPSK	5_6	250	0,0%	22,8	23,4	0,0%	250	0,0%	25,0	25,5	0,0%
C	8QAM	1_2	248	0,0%	22,3	22,6	0,8%	249	0,0%	21,6	22,1	0,4%
C	8QAM	5_6	246	0,0%	22,2	23,1	1,6%	249	0,0%	25,6	25,3	0,4%
E	BPSK	1_2	245	0,0%	25,8	21,6	2,0%	246	0,0%	27,6	21,7	1,6%
E	BPSK	5_6	245	0,0%	25,5	22,9	2,0%	245	0,0%	28,8	23,2	2,0%
E	QPSK	1_2	247	0,0%	25,8	23,9	1,2%	245	0,0%	27,8	24,1	2,0%
E	QPSK	5_6	247	0,0%	25,7	24,8	1,2%	246	0,0%	28,6	25,5	1,6%
E	8QAM	1_2	243	0,0%	25,6	24,4	2,8%	245	0,0%	28,5	25,3	2,0%
E	8QAM	5_6	242	0,0%	25,3	25,3	3,2%	246	0,0%	28,9	27,3	1,6%
F	BPSK	1_2	245	0,0%	28,7	19,9	2,0%	245	0,0%	30,5	20,0	2,0%
F	BPSK	5_6	244	0,0%	28,8	22,6	2,4%	243	0,0%	30,7	23,5	2,8%
F	QPSK	1_2	238	0,0%	29,0	24,2	4,8%	245	0,0%	30,6	24,8	2,0%
F	QPSK	5_6	242	0,0%	29,5	25,7	3,2%	245	0,0%	30,8	26,9	2,0%
F	8QAM	1_2	245	0,0%	28,7	25,4	2,0%	247	0,0%	32,3	27,9	1,2%
F	8QAM	5_6	246	0,0%	28,6	27,4	1,6%	244	0,0%	30,4	28,9	2,4%

TABLE 11. Results measured with the BPL prototype related to location L4.1.

			Received in L4.1					Received in SS, from L4.1				
			Frames sent	FER	Header MER (dB)	ACE & Payload MER (dB)	ABS. FER.	Frames sent	FER	Header MER (dB)	ACE & Payload MER (dB)	ABS. FER.
A	BPSK	1_2	247	0,0%	16,7	16,4	1,2%	236	2,1%	8,7	8,3	7,6%
A	BPSK	5_6	247	12,6%	13,4	12,1	13,6%	243	0,4%	18,1	18,4	3,2%
A	QPSK	1_2	250	3,2%	13,4	12,1	3,2%	244	0,0%	18,1	18,3	2,4%
A	QPSK	5_6	249	22,5%	13,5	12,3	22,8%	240	48,3%	9,1	9,5	50,4%
A	8QAM	1_2	248	4,0%	17,1	15,7	4,8%	243	0,4%	18,1	18,3	3,2%
A	8QAM	5_6	250	54,0%	14,5	13,7	54,0%	241	7,5%	18,3	18,6	10,8%
C	BPSK	1_2	250	0,0%	23,3	21,8	0,0%	248	0,0%	22,8	21,7	0,8%
C	BPSK	5_6	249	0,0%	23,4	23,4	0,4%	249	0,0%	18,8	19,4	0,4%
C	QPSK	1_2	250	0,0%	23,2	23,7	0,0%	250	0,0%	23,2	23,6	0,0%
C	QPSK	5_6	249	0,0%	23,3	24,2	0,4%	248	0,0%	23,2	24,1	0,8%
C	8QAM	1_2	250	1,2%	23,2	23,7	1,2%	249	0,0%	23,0	23,6	0,4%
C	8QAM	5_6	250	0,4%	23,5	24,6	0,4%	248	0,8%	21,9	23,1	1,6%
E	BPSK	1_2	250	0,0%	29,5	21,4	0,0%	250	0,0%	27,9	21,3	0,0%
E	BPSK	5_6	250	0,0%	29,8	23,9	0,0%	250	0,0%	27,2	23,2	0,0%
E	QPSK	1_2	250	0,0%	29,5	25,4	0,0%	250	0,0%	24,2	22,6	0,0%
E	QPSK	5_6	249	0,0%	30,1	27,0	0,4%	250	0,0%	24,3	23,0	0,0%
E	8QAM	1_2	250	0,0%	30,2	27,1	0,0%	249	0,0%	28,3	26,0	0,4%
E	8QAM	5_6	250	0,0%	29,4	28,9	0,0%	249	0,0%	28,1	27,6	0,4%
F	BPSK	1_2	250	0,0%	23,0	16,1	0,0%	248	0,0%	22,6	16,2	0,8%
F	BPSK	5_6	250	0,0%	21,1	17,7	0,0%	240	3,3%	23,1	17,3	7,2%
F	QPSK	1_2	250	0,0%	23,1	19,2	0,0%	250	0,0%	21,7	18,6	0,0%
F	QPSK	5_6	250	0,0%	23,2	20,8	0,0%	248	0,0%	19,4	18,7	0,8%
F	8QAM	1_2	249	0,0%	22,5	20,3	0,4%	248	0,0%	22,1	20,1	0,8%
F	8QAM	5_6	249	0,0%	23,0	22,2	0,4%	238	2,9%	23,6	22,1	7,6%

TABLE 12. Results measured with the BPL prototype related to location L6.1.

			Received in L6.1					Received in SS, from L6.1				
			Frames sent	FER	Header MER (dB)	ACE & Payload MER (dB)	ABS. FER.	Frames sent	FER	Header MER (dB)	ACE & Payload MER (dB)	ABS. FER.
A	BPSK	1_2	196	3,1%	8,0	7,3	24,0%	161	0,0%	11,4	11,6	35,6%
A	BPSK	5_6	216	34,7%	8,5	7,2	43,6%	204	99,5%	1,8	0,9	99,6%
A	QPSK	1_2	197	4,1%	8,0	7,6	24,4%	182	70,9%	1,4	0,7	78,8%
A	QPSK	5_6	206	81,6%	8,3	7,3	84,8%	193	100,0%	2,1	1,4	100,0%
A	8QAM	1_2	206	28,2%	8,4	7,1	40,8%	194	100,0%	1,7	1,3	100,0%
A	8QAM	5_6	212	100,0%	8,3	7,3	100,0%	195	100,0%	1,9	1,6	100,0%
C	BPSK	1_2	240	0,0%	19,3	18,5	4,0%	236	0,0%	18,0	17,2	5,6%
C	BPSK	5_6	242	0,0%	19,9	19,9	3,2%	246	0,0%	19,4	19,2	1,6%
C	QPSK	1_2	244	0,0%	19,8	20,2	2,4%	242	0,0%	15,7	16,5	3,2%
C	QPSK	5_6	241	0,0%	20,0	20,8	3,6%	244	0,0%	19,9	20,5	2,4%
C	8QAM	1_2	244	45,5%	7,1	6,3	46,8%	244	0,0%	19,1	19,6	2,4%
C	8QAM	5_6	245	0,0%	19,9	21,2	2,0%	241	0,0%	19,9	21,0	3,6%
E	BPSK	1_2	242	0,0%	28,0	19,1	3,2%	239	0,0%	28,3	19,1	4,4%
E	BPSK	5_6	244	0,0%	26,9	21,0	2,4%	245	0,0%	24,5	19,9	2,0%
E	QPSK	1_2	242	0,0%	26,8	22,1	3,2%	245	0,0%	28,1	22,3	2,0%
E	QPSK	5_6	239	0,0%	26,8	23,3	4,4%	238	0,0%	28,0	23,8	4,8%
E	8QAM	1_2	239	0,0%	27,1	23,1	4,4%	240	0,0%	28,2	23,6	4,0%
E	8QAM	5_6	239	0,0%	26,9	25,2	4,4%	237	0,0%	28,2	26,0	5,2%
F	BPSK	1_2	244	0,0%	18,5	16,2	2,4%	230	0,0%	19,5	16,0	8,0%
F	BPSK	5_6	247	0,0%	26,2	19,6	1,2%	231	0,0%	24,7	18,8	7,6%
F	QPSK	1_2	247	0,0%	18,5	17,5	1,2%	232	0,0%	25,7	20,8	7,2%
F	QPSK	5_6	249	0,0%	26,6	22,6	0,4%	224	0,0%	23,1	20,7	10,4%
F	8QAM	1_2	248	0,0%	26,3	22,4	0,8%	234	0,0%	23,2	20,8	6,4%
F	8QAM	5_6	242	0,0%	25,8	24,6	3,2%	227	0,0%	25,5	24,0	9,2%

TABLE 13. Results measured with the BPL prototype related to location L7.1.

			Received in L7.1					Received in SS, from L7.1				
			Frames sent	FER	Header MER (dB)	ACE & Payload MER (dB)	ABS. FER.	Frames sent	FER	Header MER (dB)	ACE & Payload MER (dB)	ABS. FER.
A	BPSK	1_2						250	0,0%	22,2	22,8	0,0%
A	BPSK	5_6						249	0,0%	22,5	23,8	0,4%
A	QPSK	1_2						250	0,0%	22,4	23,8	0,0%
A	QPSK	5_6						250	0,0%	22,3	24,3	0,0%
A	8QAM	1_2	1	100,0%	11,1	-1,4	100,0%	250	0,0%	23,3	24,9	0,0%
A	8QAM	5_6	1	0,0%	11,9	14,5	99,6%	250	0,8%	22,5	24,4	0,8%
C	BPSK	1_2	1	0,0%	7,2	11,5	99,6%	250	0,0%	26,6	24,2	0,0%
C	BPSK	5_6						250	0,0%	26,9	25,9	0,0%
C	QPSK	1_2						250	0,0%	27,5	27,1	0,0%
C	QPSK	5_6	1	0,0%	14,5	13,6	99,6%	250	0,0%	27,5	28,0	0,0%
C	8QAM	1_2						249	0,0%	26,6	27,3	0,4%
C	8QAM	5_6						250	0,0%	27,3	28,2	0,0%
E	BPSK	1_2	3	0,0%	15,8	11,5	98,8%	243	0,0%	27,0	21,0	2,8%
E	BPSK	5_6	3	0,0%	12,1	10,8	98,8%	242	0,0%	27,6	22,5	3,2%
E	QPSK	1_2	7	0,0%	14,3	11,5	97,2%	244	0,0%	27,6	23,4	2,4%
E	QPSK	5_6	12	16,7%	16,3	13,0	96,0%	243	0,0%	27,6	24,5	2,8%
E	8QAM	1_2	18	11,1%	14,6	12,1	93,6%	242	0,0%	27,8	24,6	3,2%
E	8QAM	5_6	28	50,0%	13,6	12,4	94,4%	246	0,0%	26,5	25,1	1,6%
F	BPSK	1_2	19	0,0%	9,7	13,8	92,4%	250	0,0%	34,2	23,4	0,0%
F	BPSK	5_6	67	0,0%	19,1	12,7	73,2%	250	0,0%	33,9	26,4	0,0%
F	QPSK	1_2	100	2,0%	20,9	14,8	60,8%	249	1,6%	33,9	28,3	2,0%
F	QPSK	5_6	97	0,0%	20,3	17,8	61,2%	250	0,0%	34,4	29,7	0,0%
F	8QAM	1_2	95	1,1%	20,0	17,8	62,4%	250	0,0%	33,7	29,7	0,0%
F	8QAM	5_6	132	15,9%	20,2	20,1	55,6%	250	0,0%	33,2	32,0	0,0%

TABLE 14. Results measured with the BPL prototype related to location L7.2.

			Received in L7.2					Received in SS, from L7.2				
			Frames sent	FER	Header MER (dB)	ACE & Payload MER (dB)	ABS. FER.	Frames sent	FER	Header MER (dB)	ACE & Payload MER (dB)	ABS. FER.
A	BPSK	1_2	168	1,2%	13,5	13,0	33,6%	230	0,9%	9,7	13,6	8,8%
A	BPSK	5_6	166	3,6%	13,5	14,1	36,0%	235	4,3%	9,2	14,2	10,0%
A	QPSK	1_2	165	0,0%	13,7	14,0	34,0%	233	1,3%	9,4	14,1	8,0%
A	QPSK	5_6	173	5,8%	14,0	14,9	34,8%	237	7,2%	10,4	14,6	12,0%
A	8QAM	1_2	186	4,3%	14,1	14,2	28,8%					
A	8QAM	5_6	194	17,5%	13,7	14,8	36,0%	246	35,4%	9,3	14,3	36,4%
C	BPSK	1_2	164	6,1%	14,6	10,0	38,4%	241	0,0%	16,2	14,8	3,6%
C	BPSK	5_6	194	26,3%	15,0	11,4	42,8%	243	3,7%	18,7	17,3	6,4%
C	QPSK	1_2	187	15,0%	16,0	12,4	36,4%	240	1,3%	16,3	16,7	5,2%
C	QPSK	5_6	191	27,2%	14,9	13,3	44,4%	242	5,8%	16,6	17,1	8,8%
C	8QAM	1_2	197	20,8%	16,3	13,0	37,6%	243	2,9%	16,4	16,6	5,6%
C	8QAM	5_6	216	36,1%	14,1	13,9	44,8%	247	17,0%	16,6	17,1	18,0%
E	BPSK	1_2	223	0,9%	22,5	12,7	11,6%	250	0,0%	21,2	16,5	0,0%
E	BPSK	5_6	206	14,6%	22,9	15,0	29,6%	231	0,0%	21,3	16,9	7,6%
E	QPSK	1_2	222	0,9%	22,9	15,0	12,0%	230	0,9%	21,6	17,8	8,8%
E	QPSK	5_6	231	18,6%	23,0	15,9	24,8%	232	0,4%	21,8	18,9	7,6%
E	8QAM	1_2	236	12,7%	22,9	15,6	17,6%	230	0,4%	21,8	18,6	8,4%
E	8QAM	5_6	234	19,2%	19,0	16,5	24,4%	230	0,0%	21,7	20,3	8,0%
F	BPSK	1_2	155	23,9%	12,7	7,9	52,8%	155	9,7%	20,7	12,7	44,0%
F	BPSK	5_6	181	44,8%	12,8	10,0	60,0%	190	31,6%	19,9	13,9	48,0%
F	QPSK	1_2	192	39,6%	12,6	10,0	53,6%	194	26,3%	21,0	16,3	42,8%
F	QPSK	5_6	198	40,9%	13,5	11,8	53,2%	203	20,7%	21,3	18,0	35,6%
F	8QAM	1_2	195	40,5%	13,6	11,8	53,6%	203	18,7%	21,1	18,2	34,0%
F	8QAM	5_6	206	46,1%	12,4	12,9	55,6%	213	18,3%	20,0	19,9	30,4%

We can also focus on the so-called Mode A, which is the most similar to OFDM modulation employed by the operational field devices. It is quite immediate to see that there is a similar trend between both, so that, when the PHY data rates of the field devices show good or bad performance, so happens with the field prototype results. To verify this numerically, the normalized correlation coefficient between the bitrates attained by the field devices and the FER reported by the prototype is calculated for each of the six test results (one per modulation and FEC type). Correlations include measurements and data rates collected from both the uplink and downlink; results can be seen in Table 14. There are data that cannot be used in the comparison (e.g., no data exists; or it cannot be compared since the operational network uses an intermediate repeater). Significant negative correlation coefficients between FER and bitrate are indicative of high correlation and so, of valid results produced by the BPL prototype.

VI. CONCLUSION

This paper has presented and described a BPL prototype that has been developed with the purpose of performing the analysis of LV grid access channels. The technical decisions in the development process have been shown, together with the flexibility of the platform to perform different tests, with a variety of combinations of frequency ranges, bandwidths, OFDM signal numerology, modulation schemes, FEC strategies, etc.

An experimental and practical methodology has been used to validate the prototype and its performance: taking advantage of existing commercial products already operational in the grid, representative field tests have been carried out, using a combination of configuration parameters that emulate their functioning in the prototype. The high correlation of both results demonstrate that the prototype can be used for its intended purpose, and that the results and conclusions will be valid when further combinations of parameters are tested.

Along the process, some initial conclusions identifying the most appropriate LV access grid channel-related parameters (mainly useable bandwidth, frequency carrier spacing, and FEC) on the feasibility of BPL in LV access grids have been extracted, and they will drive future work with the prototypes (field measurement campaigns), to find the most suitable parameters for BPL in LV access grid channels for Smart Metering and Smart Grid applications.

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