IEEE Access
Multidisciplinary | Rapid Review | Open Access Journal

Received 25 January 2024, accepted 12 February 2024, date of publication 19 February 2024, date of current version 28 February 2024.

Digital Object Identifier 10.1109/ACCESS.2024.3367284

RESEARCH ARTICLE

Ripple Attenuation and Aliasing Suppression in Multisampling Digitally Controlled Inverters

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ABSTRACT The application of multisampling technology in voltage-source inverters (VSIs) systems can significantly reduce the control delay and break the bandwidth limitations of traditional synchronous sampling schemes. However, when sampling the capacitor voltage, the high-frequency ripple is introduced into the control loop, leading to the local vertical crossing (VC) phenomenon. Previous studies have demonstrated that a moving average filter (MAF) or improved repetitive filter (IRF) can effectively remove the high-frequency ripple. However, they introduce additional phase lag, which undermines the advantages of multisampling technology in terms of phase boost. The approach of spectrum analysis can be used to study the impact of voltage ripple. The results indicate that after modulation, the output signal contains low-frequency harmonics, and the superposition of the ripple makes the modulation process more susceptible to saturation. Therefore, a 20k ripple notch filter (RNF) is proposed to attenuate the ripple signal while introducing a more minor phase lag. Additionally, a 90° phase shift filter is proposed to suppress the aliasing signals generated in the system. Finally, the effectiveness of the proposed methods is verified through the experimental test of a 10kW single-phase VSI system.

INDEX TERMS Aliasing, control delay, voltage source inverters (VSIs), multisampling, low-order harmonics.

I. INTRODUCTION

With the continuous updating of power electronics, the distributed power generation system based on renewable energy sources has received increasing attention. Conventionally, the distributed power generation system is connected to the grid via current vector-controlled voltage source inverters (VSIs) with phase-locked loops (PLLs), commonly referred to as grid-following (GFL) converters. GFL converters have the advantages of fast response and a high power factor. However, due to the nature of its output as a current source, GFL converters cannot provide voltage support. More importantly, the adverse effect of the PLL can render the system unstable in weak grid conditions. Grid-forming (GFM) converters have been widely applied to address these problems [1], [2]. By varying the phase/amplitude of the output voltage to adjust the active/reactive power output, GFM converters can provide voltage support for the system and work in both isolated and grid-connected modes. In weak grids, GFM converters are more flexible than GFL converters in regulating frequency and voltage, which is conducive to the stable operation of the system and has a broader range of applications. However, to realize these advantages, it is necessary to choose the appropriate control algorithms. The classical inverter control algorithms based on the transfer function model have gained widespread usage owing to their mature and stable characteristics. The control schemes can be categorized into single-loop [3], [4], [5], [6] and dual-loop control [7], [8], [9] based on the number of feedback control variables. Single-loop and dual-loop control utilize an LC filter to suppress high-frequency harmonic signals. However, the problem of resonance in LC filters imposes greater demands on the design of the control system. Both active and passive damping effectively eliminate the resonance peak but do not fundamentally solve the problem of delay, which affects the stability of the system [10].

The associate editor coordinating the review of this manuscript and approving it for publication was Pinjia Zhang.

In the voltage control system for single-phase VSIs, the implementation process inevitably introduces the control delay, which limits the proportional gain of the controller. The proportional gain of the controller determines the bandwidth of the system; a larger gain provides a higher bandwidth and, consequently, a faster transient response. Two aspects can be considered to reduce the control delay: compensation and sampling. Zhang et al. [11] proposed a model-free predictive control method by connecting a second-order general integrator (SOGI) in series within the feedback loop. This approach utilizes the phase lead characteristic of the SOGI to compensate for the phase lag introduced by the control delay. However, this method increases the complexity of the system, and the selection of parameters for SOGI brings additional workload. Ma et al. [12] proposed a real-time sampling method based on capacitive current feedback, which shifts the current sampling instant to the next sampling instant. However, due to the deviation from the traditional intermediate sampling instant, low-order harmonics are introduced into the spectrum of the capacitor current. Zhang et al. [13] proposed a method of inverter-side current multisampling, which reduces the control delay and accelerates the dynamic response of the system.

Nevertheless, the high-frequency ripple injected into the feedback loop is not taken into account, and the ripple is highly susceptible to triggering output voltage distortion. The filter-based method is widely used to remove the high-frequency ripple. The MAF is used in [14] but introduces additional phase lag, diminishing the advantages of multisampling technology in improving the phase margin. Another type of filter is the repetitive filter (RF) [15]. Although the RF does not introduce delay, it is unsuitable for AC applications [16].

In addition, the non-linear components in the control loop will result in severe distortion of the output voltage. Improving the waveform quality of the output voltage and current has been a widely discussed topic. Some scholars have tried to reduce the total harmonic distortion (THD) of the output voltage through the control algorithms. For example, the repetitive controller is used to regulate the output voltage and calculate the compensation component by measuring the output voltage signal to attain a low THD output voltage waveform under steady-state conditions [17].

Some other scholars have investigated aliasing from a sampling perspective. The analysis method based on frequency domain transformation [18] shows that high-frequency signals transition into low-frequency signals through sampling aliasing. Therefore, it is proposed to use an analog anti-aliasing filter to remove high-frequency signals before sampling. However, the filter introduces additional dynamic performance in the control loop, resulting in a trade-off between filtering performance and stability. A selective delay sampling strategy is proposed in [19], where the mutual cancellation of positive and negative frequency aliasing signals can be achieved by adjusting the magnitude of the sampling delay. The disadvantage is that it only considers the output harmonics based on natural sampling and does not analyze the digital signal processing methods. The relationship between the degree of aliasing and the sampling instant is investigated in [20], the method of overlaying the results of multiple sampling can offset the low-order harmonics generated by the sideband harmonics around integer multiples of the switching frequency. Nevertheless, to achieve complete cancellation, eight sampling channels need to be stacked together, increasing the design cost and complexity.

This paper aims to address the problems of aliasing distortion and high-frequency ripple in multisampled digitally controlled systems. In terms of ripple elimination, a low-order digital filter is adopted, which can effectively attenuate the sideband signals around the 20k frequency. Compared with

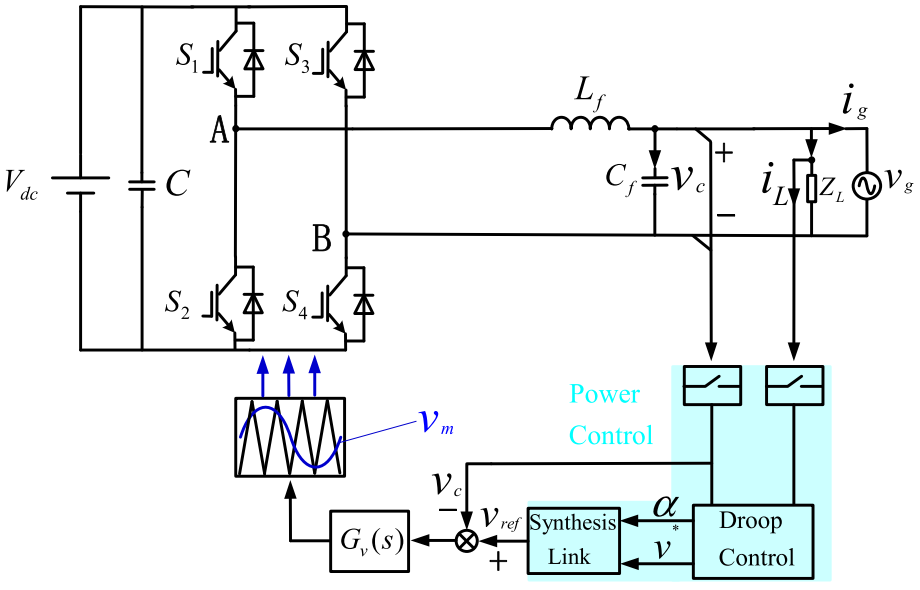

FIGURE 1. The control diagram of voltage control system for single-phase VSIs.

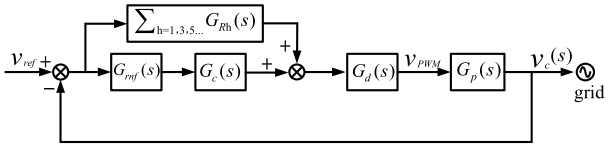

FIGURE 2. The block diagram of voltage control system for single-phase VSIs.

traditional schemes, the phase lag introduced by it can be ignored and has better control effects. In addition, in order to improve the waveform quality of the output voltage, a 90° phase shift filter is introduced. According to this method, high-frequency signals greater than the Nyquist frequency are lagged by 90° without amplifying low-frequency harmonics, which can effectively suppress aliasing distortion. In addition, an optimized control algorithm based on the multisampling approach is proposed, which can significantly reduce the computational delay and enhance the crossover frequency of the system.

Following the introduction, Section II discusses the aliasing signal sources by analyzing the signal transmission path of the control system. Section III quantitatively analyzes the control delay of the voltage control system for single-phase VSIs when using the multisampling approach. Section IV proposes the ripple attenuation method, and Section V introduces the aliasing suppression method. In Section VI, experimental results are presented to verify the effectiveness of the proposed design. Finally, Section VII provides a summary of this article.

II. SYSTEM DESCRIPTION

A. MATHEMATICAL MODEL OF SINGLE-PHASE VSIs

The control diagram of the voltage control system for single-phase VSIs is shown in Figure 1, where V_{dc} represents the DC-link voltage of the inverter, Z_L represents the load, C_f and L_f denote the filter capacitor and the filter inductor, respectively. Additionally, v_g indicates the grid voltage, i_g indicates the grid current, and i_L indicates the load current. The inverter parameters are detailed in Table 1. The output voltage v_c is taken as the control object. The amplitude of the reference voltage v^* and the phase angle of the reference voltage α are obtained through the power control of the outer loop, such as droop control. After the voltage synthesis component, the reference voltage of the inner loop v_{ref} is obtained. The voltage controller generates the modulation signal $v_m(t)$, and the drive signals of S_1——S_4 are generated through the PWM.

According to Figure 1, the corresponding block diagram is shown in Figure 2, where v_{PWM} is the output voltage of the inverter. The transfer function from v_{PWM} to v_c is expressed as

$$G_p(s) = \frac{1 + sR_cC_f}{L_fC_fs^2 + R_cC_fs + 1} \tag{1}$$

where R_c represents the equivalent series resistance (ESR) of the capacitor, the transfer function of the type-III voltage controller can be expressed as

$$G_c(s) = \frac{A_0}{s} + K_v + K_i\frac{1}{Z_c(s)} \tag{2}$$

where

$$Z_c(s) = \frac{L_cC_fs^2 + R_cC_fs + 1}{C_fs} \tag{3}$$

$Z_c(s)$ represents the equivalent impedance of the capacitor, where L_c is the equivalent series inductance of the capacitor, K_v represents the proportional gain, A_0 is the gain of the pole at the origin, and K_i denotes the gain associated with the equivalent impedance of the capacitor. $Z_c(s)$ is used to obtain capacitance current information from output voltage information to achieve active damping [21]. The resonant controller $G_{R_h}(s)$ is represented as

$$G_{Rh}(s) = k_{Rh}\frac{2\xi w_h s}{s^2 + 2\xi w_h s + w_h^2} \tag{4}$$

where k_{Rh} represents the gain of the resonant controller, ω_h represents the center frequency, and ξ represents the damping factor of the resonant controller. The total time delay in the continuous s-domain can thus be denoted by $G_d(s)$, which is given by

$$G_d(s) = e^{-sT_d} \tag{5}$$

where T_d is the time delay.

B. ANALYSIS OF THE ALIASING INJECTION

The sampling switch in the feedback loop is used to oversample the output voltage, converting continuous domain voltage signals into digital signals. After the multisampling component, the results are resampled at a lower sampling rate before being sent to the branch where the resonant controller is located. This approach addresses two problems: firstly, it reduces the computational burden of the resonant controller as the operating rate decreases, and secondly, it places less demands on the accuracy of the parameters. As a result, there are two operating rates in the digital domain.

As illustrated in Figure 3, the injection of aliasing signals in the voltage control system can be classified as follows:

1) DPWM (DIGITAL PULSE WIDTH MODULATION) ALIASING INJECTION n_{EXT}

The high-frequency components in the PWM output signal are fed back into the control loop via the sampling component. If the feedback information contains high-frequency components, more considerable fundamental and lower-order harmonics will appear after the PWM component, resulting in DPWM distortion at v_c [22].

2) INDUCTOR SATURATION ALIASING INJECTION n_{LS}

In the voltage control system for single-phase VSIs, the inverter is connected to the grid via an LC filter. However, the inductor saturation results in poor steady-state current waveform quality and the presence of low-order harmonics in the output voltage [23].

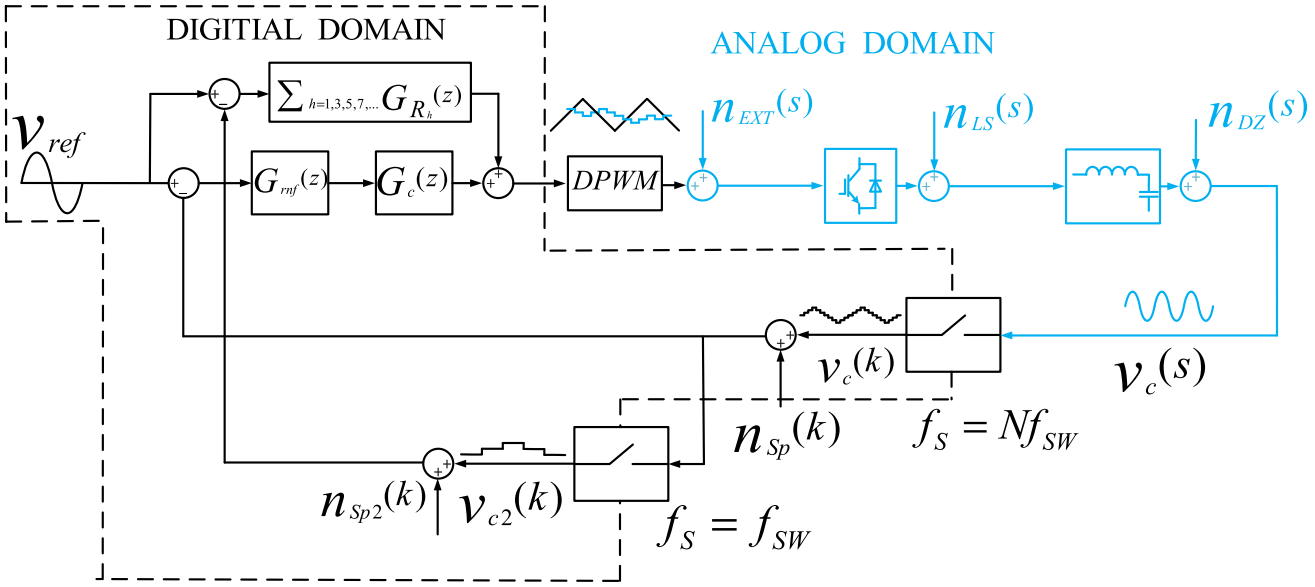

FIGURE 3. The aliasing injection diagram.

3) DEAD TIME ALIASING INJECTION n_{DZ}

In order to prevent the straight-through phenomenon between the upper and lower bridge arms caused by the switch-off delay effect of the switching tube, it is necessary to set a dead time to avoid this problem. However, setting a dead time will bring about voltage error, leading to the presence of fundamental and odd-order harmonics in v_{pwm} [24].

4) SAMPLING ALIASING INJECTION n_{Sp}

When sampling the output voltage, according to the Shannon sampling theorem, if the frequency of the signal is lower than the Nyquist frequency, it becomes difficult to reconstruct the original signal from the sample.

When the aliasing injection is located in the forward channel, it can be suppressed by increasing the loop gain. However, for other aliasing injections, additional measures need to be taken.

III. MUITISAMPLING PWM CONTROL

A. MULTISAMPLING TECHNIQUE

As depicted in Figure 4(a), the state variables are sampled once per switching period in the traditional sampling approach.

The data obtained from the sampling participates in the operation of the controller, and the resulting command signal is used to regulate the output voltage. The multisampling technique [16], [25] involves oversampling the state variables, with the sampling frequency f_S being an integer multiple of the switching frequency f_{SW}, as expressed in equation (6).

$$f_S = Nf_{SW} \quad N = 1, 2, 3, 4, \ldots \tag{6}$$

Figure 4(b) shows the timing diagram for voltage four-sampling, where A_W represents the amplitude of the carrier signal, T_{SW} represents the switching period, T_S represents the sampling period, and $m_h(t)$ represents the carrier signal that varies periodically with time.

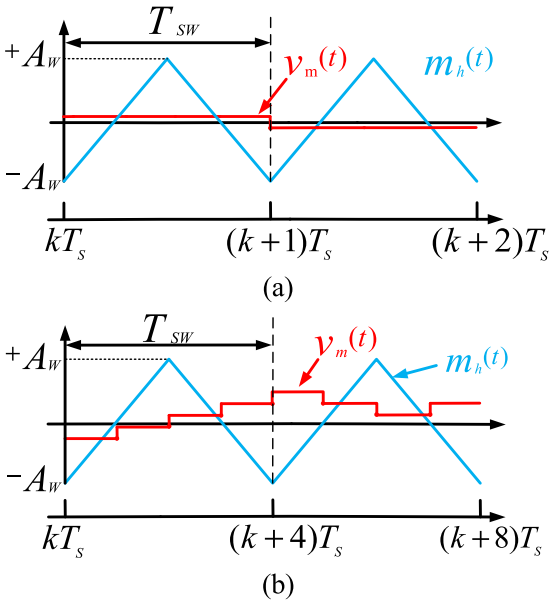

FIGURE 4. (a) The timing diagram for single sampling approach. (b) The timing diagram for multisampling approach.

B. ANALYSIS OF THE CONTROL DELAY UNDER THE MULTISAMPLING APPROACH

Natural sampling has no delay [26], whereas the delay of regular sampling originates from the time between the instant when the sampling window is closed and the update of the modulation signal [27]. This delay includes computational delays and PWM delays. Considering the computation time

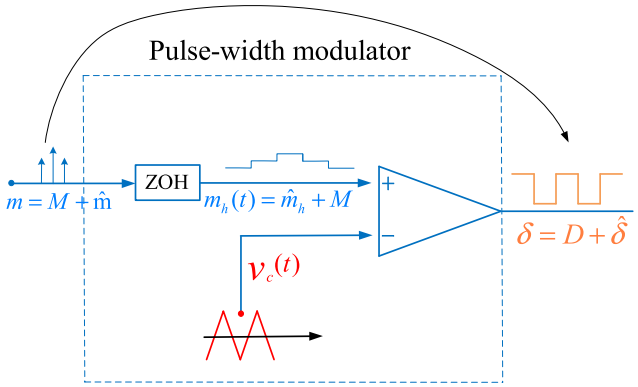

FIGURE 5. Small-signal analysis for the PWM modulator.

of the control algorithm, the computational delay T_{cl} should be equal to one sampling period [28]. In the multisampling approach, the modulator is modeled using the small signal analysis method [16], as shown in Figure 5.

$$\begin{aligned} &G_{DPWM}(j\omega) \\ &= \frac{\hat{\delta}(j\omega)}{\hat{m}(j\omega)} \\ &= \frac{1}{2A_W}\cos\left(\omega\left(ND - 2\,floor\left(\frac{ND}{2}\right) - 1\right)\frac{T_{SW}}{2N}\right)e^{-j\omega\frac{T_{SW}}{2N}} \\ &\cong \frac{1}{2A_W}e^{-j\omega\frac{T_{SW}}{2N}} \end{aligned} \tag{7}$$

A small AC disturbance $\hat{m}$ is superimposed on the steady-state modulation signal M, and the resulting disturbance $\hat{\delta}$ is then evaluated in the duty cycle δ. Subsequently, the transfer function of the modulator is derived. As shown in equation (7), where D is the steady-state duty cycle, the modulation signal perturbation and the corresponding duty cycle perturbation are $\hat{m}(j\omega)$ and $\hat{\delta}(j\omega)$, respectively. The function floor(x) denotes the largest integer that does not exceed x. Observing equation (7), the size of the PWM delay T_{pwm} is $\frac{T_{SW}}{2N}$. The total time delay under the multisampling approach can be expressed as

$$T_d = \frac{T_{SW}}{N} + \frac{T_{SW}}{2N} = \frac{3T_{SW}}{2N} \tag{8}$$

The above equation illustrates that T_{cl} is the primary component of the control delay, and the larger N is, the smaller T_d becomes.

C. ANALYSIS OF THE CONTROL DELAY AFTER OPTIMIZING THE CONTROL ALGORITHM

In Figure 6(a), the composition of the computational delay is analyzed. The sampled value is obtained at the instant the sampling window closes. Following the completion of sampling, an analog-to-digital (AD) conversion is performed, and the time required for the AD conversion is T_{C1}, which is related to the operating rate and the resolution of the analog-to-digital converter (ADC). For a 12-bit ADC, the conversion process requires 12.5 clock cycles and can be completed within 0.3us. The data obtained from the conversion is then used to execute the control algorithm, which takes time T_{C2}. After the calculation is completed, the duty cycle is updated following a waiting period T_{C3}. The total computational delay T_{cl} is one sampling period.

After optimizing the control algorithm, only one multiply-accumulate step is required to complete the operation of the control algorithm [29]. From loading the data into the data register to writing the result of the operation into the destination register, which takes no more than ten cycles in total and can be completed within 0.1us. The result of the operation is then summed up with the output of the resonant controllers, and the sum is multiplied by the period of the PWM counter to get the size of the duty cycle. Subsequently, the limiter is added to obtain the output value. The entire operation process does not exceed 0.5us, and with the addition of a particular waiting time, the calculation can be completed within 1us. Therefore, the control delay after optimizing the control algorithm is

$$T_d = 1us + \frac{T_{sw}}{2N} \tag{9}$$

The timing diagram of the multisampling approach after optimizing the control algorithm is shown in Figure 6(b).

D. ANALYSIS OF THE DYNAMIC PERFORMANCE OF THE SYSTEM AFTER OPTIMIZING THE CONTROL ALGORITHM

The analysis above indicates that the optimization of the control algorithm significantly reduces the computational delay. Taking the capacitor voltage eight-sampling as an example, the dynamic performance of the system is studied after optimizing the control algorithm. $T_O(s)$ is the open-loop transfer function from $v_c^*(s)$ to $v_c(s)$, expressed as

$$T_O(s) = G_{lf}(s)G_c(s)G_d(s)G_p(s) \tag{10}$$

From equation (8) and (9), it can be seen that under the multisampling approach, $T_d = 6.25\ us + 3.125\ us = 9.375us$, and after optimizing the control algorithm $T_d = 1us + 3.125us = 4.125us$. According to equation (10), the frequency characteristics of $T_O(s)$ can be plotted, as shown by the solid line in Figure 7.

Comparing the red curve with the black curve, the phase margin of the system is 45° before and after optimization, but the crossover frequency increases from 5.12kHz to 6.89kHz after optimization. The optimization of the control algorithm can significantly enhance the bandwidth of the system and improve its dynamic response while maintaining the stability margin unchanged.

IV. HIGH-FREQUENCY RIPPLE

A. SELECTION OF THE RIPPLE NOTCH FILTER

The high-frequency ripple is usually eliminated by connecting an analog anti-aliasing filter in the feedback channel of the controlled variable. However, conventional anti-aliasing filters can significantly lag the control frequency signal while removing the high-frequency ripple, thereby reducing the

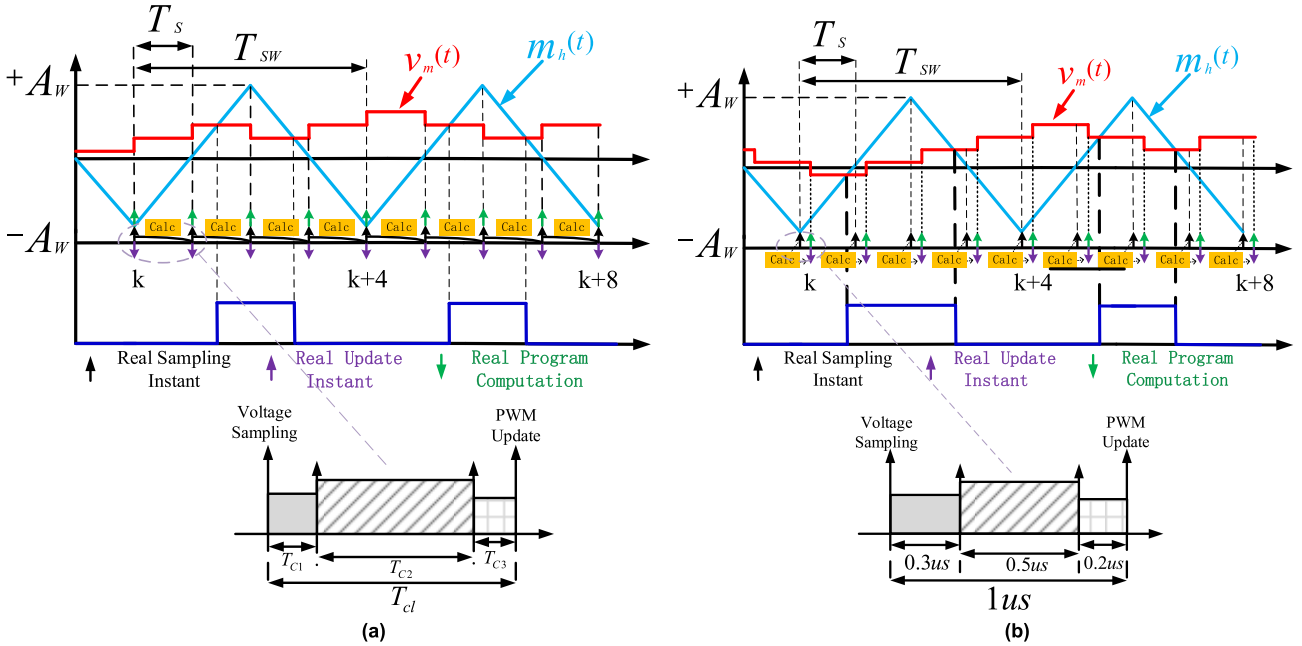

FIGURE 6. (a) Timing diagram of the multisampling approach. (b) Timing diagram of the multisampling approach after optimizing the control algorithm.

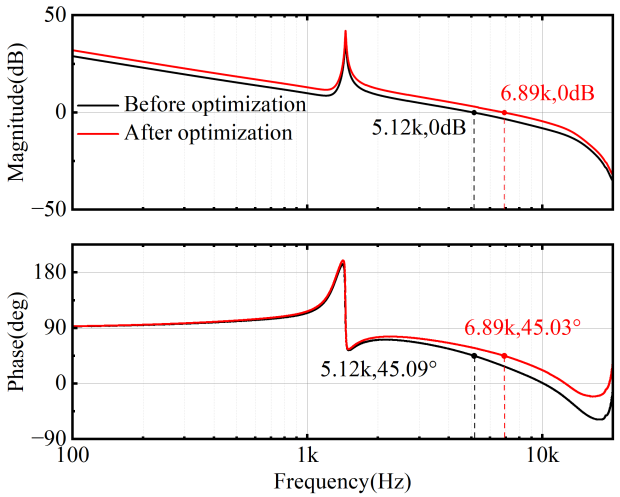

FIGURE 7. The open-loop frequency characteristics of the system.

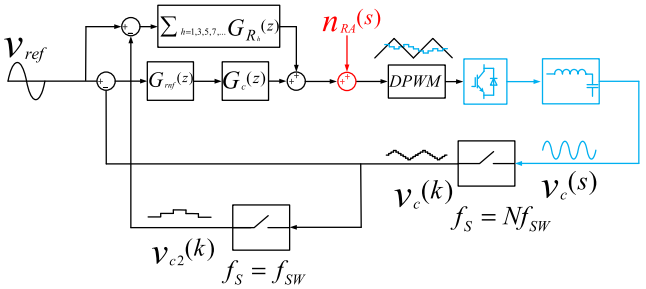

FIGURE 8. Equivalent injection of ripple aliasing.

stability margin of the system. Consequently, the method of connecting an analog anti-aliasing filter in series at the input of the sampling component is not applicable. When using the multisampling approach to obtain the capacitor voltage information, all the high-frequency harmonics up to the N/2-th order are introduced into the base-band spectrum of the loop.

According to the above analysis, the residual ripple, after being filtered by the ripple notch filter, easily overlaps with the low-frequency band during the PWM process. Therefore, the generation of ripple aliasing is equivalent to injecting disturbance at the input of the DPWM component. As shown in Figure 8, the ripple aliasing is injected into the forward channel, but this can be mitigated by a high loop gain. At the same time, the superimposition of the ripple makes the modulation component more susceptible to saturation and reduces the ability of the control system to regulate the capacitor voltage. Using an MAF to process the sampling error signal is one method of eliminating the high-frequency ripple. The expression of MAF in the discrete domain is given by equation (11).

$$MAF(z) = \frac{1}{N}\sum_{N-1}^{k=0} z^{-k} \tag{11}$$

Figure 9 shows the frequency characteristics of the MAF when N is 8. The MAF can remove high-frequency harmonics around integer multiples of the switching frequency, but this filtering behavior significantly deteriorates the phase margin of the system. In comparison, the implementation of SRF is simpler by delaying the ripple-affected error signal by half of a switching period and then adding it to the original waveform to obtain equation (12).

$$SRF(z) = \frac{1}{2}\left(1 + z^{-N/2}\right) \tag{12}$$

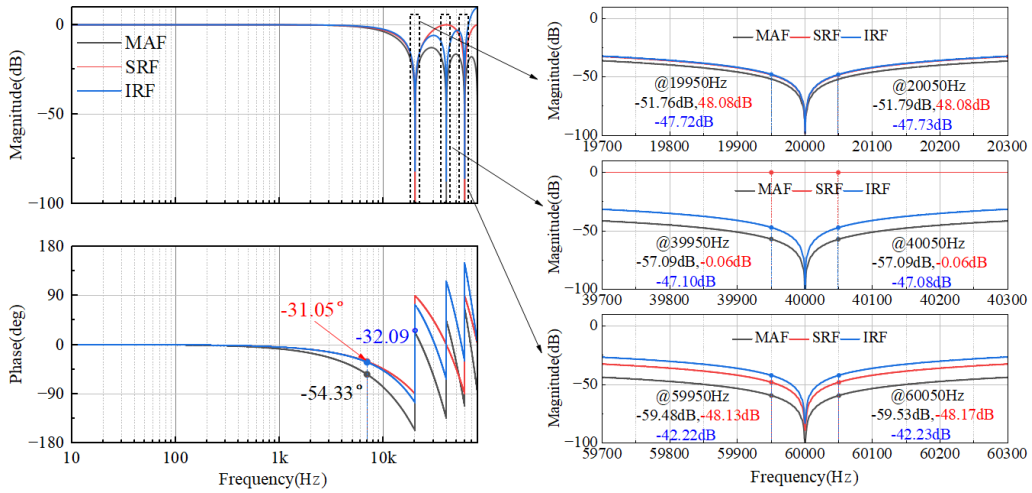

FIGURE 9. Filter frequency response.

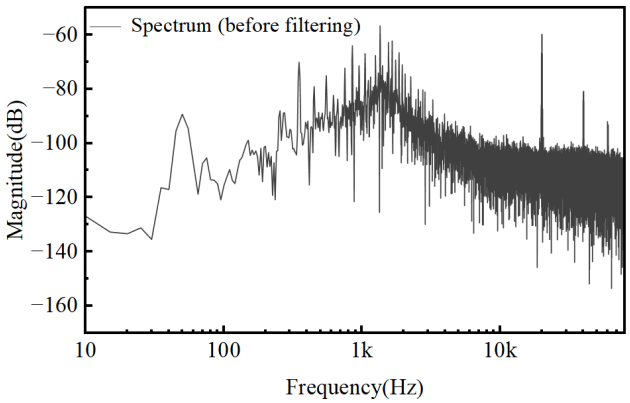

FIGURE 10. Ripple spectrum.

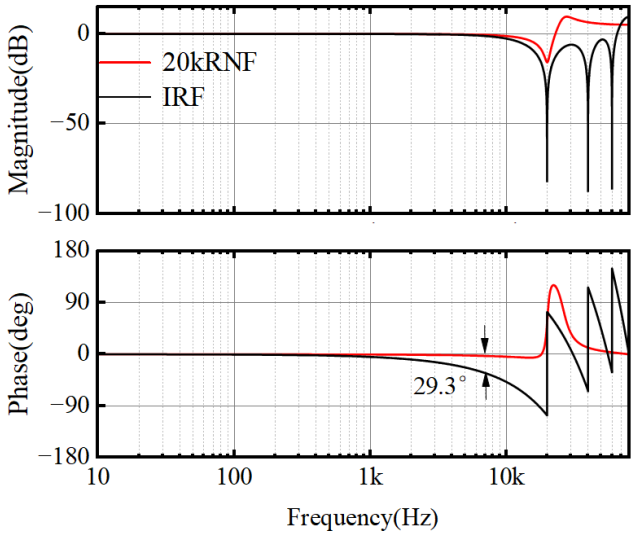

FIGURE 11. Comparison between the IRF and 20kRNF.

When N is 8, the frequency characteristics of the SRF are shown in Figure 9. It has notches at odd multiples of the switching frequency, and the high-frequency harmonics around even multiples of the switching frequency cannot be removed. Additionally, the ability of the SRF to remove high-frequency harmonics diminishes as the multisampling rate increases. Unlike the previously mentioned filters, the IRF is represented by equation (13).

$$IRF(z) = \frac{2}{N}\left(1 + z^{-2} + z^{-4} + \cdots z^{-(N-2)}\right) \times \left(3\log_2 N - 7 - \left(3\log_2 N - 8\right) z^{-1}\right) \quad (13)$$

Figure 9 shows that the phase lag caused by the MAF is 54.33°, while the phase lag caused by the IRF is 32.09°. The IRF fully utilizes the advantages of both the SRF and MAF. It effectively eliminates sideband harmonics around both odd and even multiples of the switching frequency, and the phase lag is comparable to the SRF. By utilizing the IRF as the ripple notch filter, the system will exhibit a greater phase margin and closed-loop bandwidth, taking full advantage of the benefits of the multisampling technique in terms of phase boost.

According to the above analysis, it is evident that different types of filters possess varying degrees of filtering efficacy and are responsible for imposing different degrees of delay. Therefore, when selecting a filter, it is necessary to consider the characteristics of the object to be filtered and choose the appropriate filter to remove the ripple signal.

As illustrated in Figure 10, the capacitor voltage eight-sampling control without filters contains high-frequency harmonics around odd and even multiples of the switching frequency. There is a significant voltage spectrum peak near the switching frequency for the capacitor voltage, with the first-order, third-order, and fifth-order harmonics being the main ones.

Since the IRF exhibits infinite gain at both odd and even multiples of the switching frequency, it can eliminate all

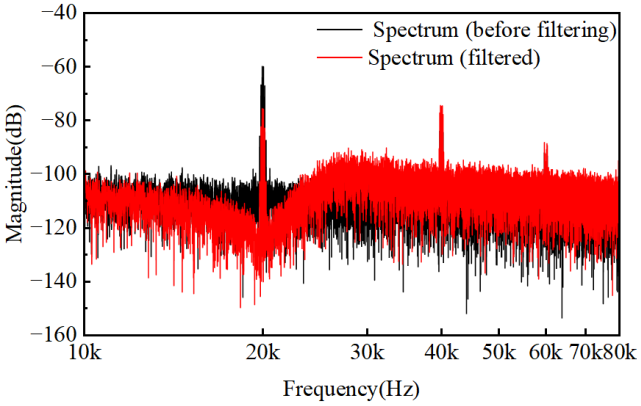

FIGURE 12. Spectrum of ripple signals after filtering.

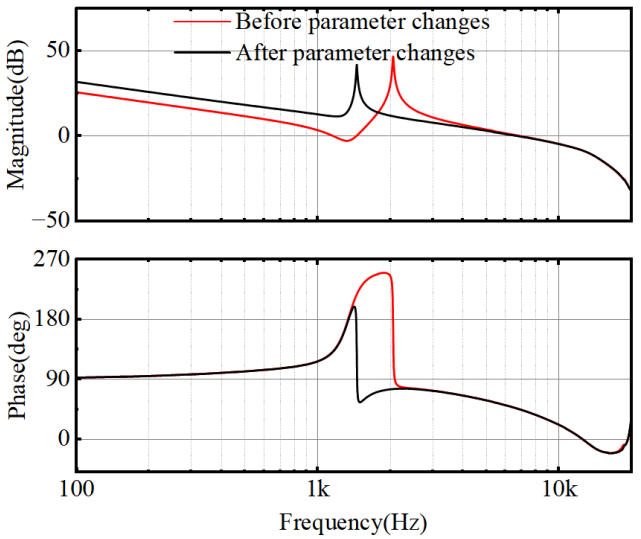

FIGURE 13. The open-loop frequency characteristic curve of the system.

high-frequency harmonics. As the order of the filter increases, the cost and complexity also increase. Suppose incomplete high-frequency harmonics removal can be tolerated. In that case, the filtering of high-frequency harmonics can be simplified by only filtering out the peak with the highest amplitude in the spectrum.

The frequency characteristic curve of the 20KRNF is depicted by the red line in Figure 11, and it is notched only at the 20k frequency. Compared to the 20kRNF, the IRF introduces an additional phase lag of 29.3°. This results in an increase in gain at high frequencies, approximately 6dB at the 40kHz frequency.

B. EFFECT OF THE 20KRNF ON RIPPLE

The 20kRNF effectively attenuates high-frequency harmonics around the switching frequency, as shown in Figure 12. After filtering, it approaches the peak at the 40kHz frequency. However, the spectral peak of the voltage ripple has been reduced to below -75dB in the frequency range above twice the switching frequency so that no additional notch is required.

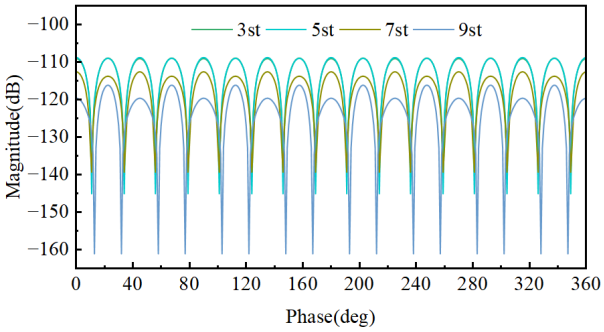

FIGURE 14. The variation in harmonic amplitude with sampling phase after voltage eight-sampling.

C. IMPACT OF THE PASSIVE FILTER ON THE RIPPLE

In the voltage control system for single-phase VSIs, the grid voltage remains constant. When determining the sampling method and sampling the capacitor voltage with a specific sampling delay, the magnitude of the delay in the control loop remains constant, and it determines the closed-loop bandwidth of the control system. Figure 13 shows the open-loop amplitude-frequency curve of the voltage control system for single-phase VSIs. Near the crossover frequency, the open-loop amplitude-frequency curve crosses the 0dB line with a slope of -20dB/Dec. On the premise of ensuring that the stability margin remains unchanged, the amplitude of the cross frequency will not change when the parameters of the passive filter change. Therefore, the variation in the parameters of the passive filter will not affect the magnitude of the ripple.

V. STUDY OF ALIASING SUPPRESSION SCHEMES

Figure 14 shows the variation of the amplitude of every order harmonic with the sampling phase after the capacitor voltage eight-sampling, and the aliasing is consistently negligible regardless of the variation of the sampling phase. However, after the multisampling component, the aliasing is inevitable when sampling voltage at the switching frequency, according to Shannon's sampling theorem. Based on the above analysis, the sampling aliasing differs from the ripple aliasing, and additional measures must be taken to suppress it.

A. ALIASING DISTORTION

According to the literature [19], equation (14)-(16) establish the relationship between the amplitude, frequency, and phase angle of the alias signal and the original signal.

$$\theta_{alias} = \begin{cases} \theta_x + m\omega_s t_0, & m\omega_s \le \omega_x \le m\omega_s + \dfrac{\omega_s}{2} \\ -(\theta_x + m\omega_s t_0), & m\omega_s - \dfrac{\omega_s}{2} \le \omega_x \le m\omega_s \end{cases} \tag{14}$$

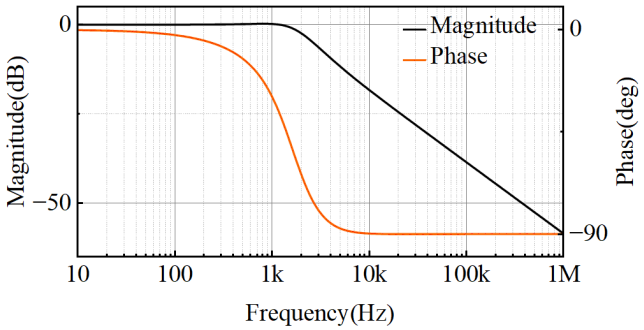

FIGURE 15. The frequency characteristics of the 90° phase shift filter.

$$w_{alias} = \begin{cases} w_x - m\omega_s, m\omega_s \le \omega_x \le m\omega_s + \dfrac{\omega_s}{2} \\ m\omega_s - w_x, m\omega_s - \dfrac{\omega_s}{2} \le \omega_x \le m\omega_s \end{cases} \tag{15}$$

$$A_{alias} = A_x \tag{16}$$

where

θ_x	phase angle of the original signal
w_x	angular frequency of the original signal
A_x	amplitude of the original signal
θ_{alias}	phase angle of the alias signal
w_{alias}	angular frequency of the alias signal
A_{alias}	amplitude of the alias signal
ω_s	sampling angular frequency
t_0	sample delay

The above equations show that the alias signal has the same amplitude as the original signal but an opposite phase. As shown in equation (17), as shown at the bottom of the page,

ω_o	fundamental angular frequency
ω_c	carrier angular frequency
f_o	fundamental frequency
f_c	carrier frequency
M	modulation ratio
m, n	multiplier factor of carrier wave and modulation wave
θ_0	initial phase angle of the signal

the output voltage harmonics between bridge arms under a single-phase inverter with unipolar multifrequency PWM based on asymmetric rule sampling are analyzed as an example.

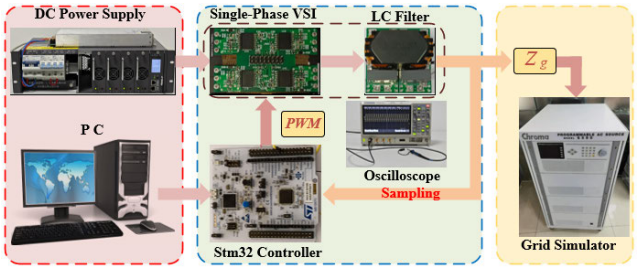

FIGURE 16. Experimental setup.

TABLE 1. Parameters of a single-phase VSIs.

Symbol	Description	Value
U_{dc}	DC-link voltage	400V
f_{sw}	Switching frequency	20kHz
f_s	Sampling frequency	160kHz
A_w	Carrier amplitude	1.25V
L_f	Filter inductor	800uH
C_f	Filter capacitor	15uF
f_r	Resonance frequency	1kHz

From equation (17), it is evident that the output voltage harmonics consist of two parts. The first component comprises the fundamental and odd-order harmonics, and the other is the odd-order sideband harmonics around the even multiple carrier frequencies.

when $2n-1>0$, $mf_c+(2n-1)f_o$ represents the right-band harmonics, when $2n-1<0$, $mf_c+(2n-1)f_o$ represents the left-band harmonics. The corresponding aliasing harmonic signals are called the left-band aliasing signals and the right-band aliasing signals in the following text.

According to equation (15), the amplitude of the alias signal at the $|2n-1|f_o$ is the superposition of the left-band aliasing signals and right-band alias signals. The phase angle of the symmetrical sideband harmonics in the original signal can be further obtained from equation (17), as shown in equation (18)

$$\begin{cases} \theta_r = \theta_0 + m\omega_s t_0, & m\omega_s \le \omega_x \le m\omega_s + \dfrac{\omega_s}{2} \\ \theta_l = \theta_0 + m\omega_s t_0, & m\omega_s - \dfrac{\omega_s}{2} \le \omega_x \le m\omega_s \end{cases} \tag{18}$$

The grid-connected side of the inverter usually requires an LC filter, which causes a phase lag of 180° in the output

$$U_{\text{inv}} = \frac{8V_{dc}}{\pi} \left\{ \begin{array}{l} \displaystyle\sum_{n=1}^{\infty} \frac{1}{[2n-1]\omega_o/\omega_c} \sin\left([2n-1]\frac{\pi}{2}\right) J_{2n-1}\left([2n-1]\frac{\omega_o}{\omega_c}\frac{\pi}{2}M\right) \cos\left((2n-1)[\omega_o t]\right) \\ + \displaystyle\sum_{m=1}^{\infty} \sum_{\substack{n=-\infty \\ n-1\neq 0}}^{\infty} \frac{1}{q'} \left\{\cos([m+n+1]\pi) J_{2n-1}\left(q'\frac{\pi}{2}M\right) \cos\left(2m[\omega_c t] + (2n-1)[\omega_o t] + \theta_0\right)\right\} \end{array} \right\} \tag{17}$$

where q'=2m+$[2n-1]\dfrac{\omega_o}{\omega_c}$

TABLE 2. Comparison of control effects 1.

Index	No filter	Ripple notch filter	Filter+ resonant controller
third-order harmonic (%)	0.082%	0.012%	0.00098%
fifth -order harmonic (%)	0.055%	0.0094%	0.0015%

voltage between the bridge arms. The phase angle of the symmetric sideband harmonics of the capacitor voltage is given by equation (19).

$$\begin{cases} \theta_{\mathrm{rc}} = -\pi + \theta_0 + m\omega_s t_0, & m\omega_s \le \omega_x \le m\omega_s + \dfrac{\omega_s}{2} \\ \theta_{\mathrm{lc}} = -\pi + \theta_0 + m\omega_s t_0, & m\omega_s - \dfrac{\omega_s}{2} \le \omega_x \le m\omega_s \end{cases} \tag{19}$$

Combining equation (14), the phase angle of the alias signal can be obtained as

$$\begin{cases} \theta_{aliasr} = -\pi + \theta_0 + m\omega_s t_0, & m\omega_s \le \omega_x \le m\omega_s + \dfrac{\omega_s}{2} \\ \theta_{aliasl} = -(-\pi + \theta_0 + m\omega_s t_0), & m\omega_s - \dfrac{\omega_s}{2} \le \omega_x \le m\omega_s \end{cases} \tag{20}$$

According to equation (20), it is evident that the sample delay leads to a change in the phase angle of the alias signal, ultimately affecting the magnitude of the alias signal. The phase difference between the left-band alias signals and the right-band alias signals is

$$\theta_\Delta = 2\theta_0 + 2mw_s t_0 \tag{21}$$

The phase angle of the alias signals is closely related to the sampling process. It is affected by both the sampling instant and the initial phase angle of the original signal.

B. ALIASING-FREE SAMPLING SCHEME

To effectively suppress the aliasing, this paper proposes an aliasing-free sampling scheme. The phase difference between the left-band alias signals and right-band alias signals is given by equation (21). When $t_0 = 0$, this value is only related to the initial phase angle. The phase angle of the left-band alias signals and right-band alias signals can be complementary by adjusting the size of the initial phase angle, thus eliminating the low-order harmonics generated by the aliasing. This scheme needs to meet the following conditions.

$$\theta_\Delta = 2\theta_0 = \pm\pi \tag{22}$$

From equation (22), it can be observed that setting θ_Δ to 90° ensures the complementary phase angle between the left-band alias signals and the right-band alias signals.

A 90° phase shift filter can be introduced to utilize the phase lag characteristics of the filter within a specific frequency range, achieving a 90° phase lag in the high-frequency harmonics without amplifying low-frequency harmonics. The frequency characteristics of the 90° phase shift filter are shown in Figure 15.

TABLE 3. Comparison of control effects 2.

Index	No aliasing suppression scheme	Aliasing suppression scheme
third-order harmonic (%)	0.163%	0.0331%
fifth-order harmonic (%)	0.108%	0.00984%
seventh-order harmonic (%)	0.036%	0.0126%
ninth-order harmonic (%)	0.0163%	0.0140%
eleventh-order harmonic (%)	0.00877%	0.00344%

VI. EXPERIMENTAL VERIFICATION

To validate the theoretical analysis presented in this paper, the experimental setup diagram is depicted in Figure 16. The experiment is based on a 10kW single-phase VSI prototype, and the specific parameters are provided in Table 1. The digital controller is implemented by STMicroelectronics on the STM32G474RE, featuring several 12-bit ADC/DAC converters onboard. A constant-voltage (400 V) DC power supply is used to power the DC-link of the VSIs. Additionally, in the experiment, a programmable AC power supply (Chroma 6590) is utilized for grid simulation, and the impedance of the grid is simulated by adding an inductor in series.

A. VALIDATION OF THE OPTIMIZED CONTROL ALGORITHM

The voltage reference step experiments were conducted to show improvements in voltage track with the optimized algorithm. Figure 17 illustrates the voltage waveforms when the voltage control system for single-phase VSIs undergoes a 10%(32 V) voltage reference step change. In order to clearly show the voltage tracking dynamics changing, the output voltage and reference voltage are normalized. As observed in Figure 17(a), after optimizing the control algorithm, the voltage tracked the voltage reference quickly and arrived at a steady state in less than 5 ms. However, in Figure 17(b), when the control algorithm is not optimized, the transient of the voltage reference tracking becomes slow, an apparent oscillation exists, and the overshoot is 5%, which is larger than the situation after optimizing the control algorithm, which is consistent with the analysis in Section III.

B. VERIFICATION OF THE 20KRNF

The eight-sampling control without the filter exhibits fast dynamic performance. However, low-order aliased harmonics are introduced in the capacitor voltage. In the multi-sampling control system, in order to investigate the effect of high-frequency ripple on the THD of the output voltage, the ripple signal is employed as an input to the modulation component, and the 20kRNF is used as the ripple notch filter in the experimental setup. The comparison of the PWM output voltage spectrum for the three schemes is depicted in Figures 18-20. Under the condition of no ripple notch

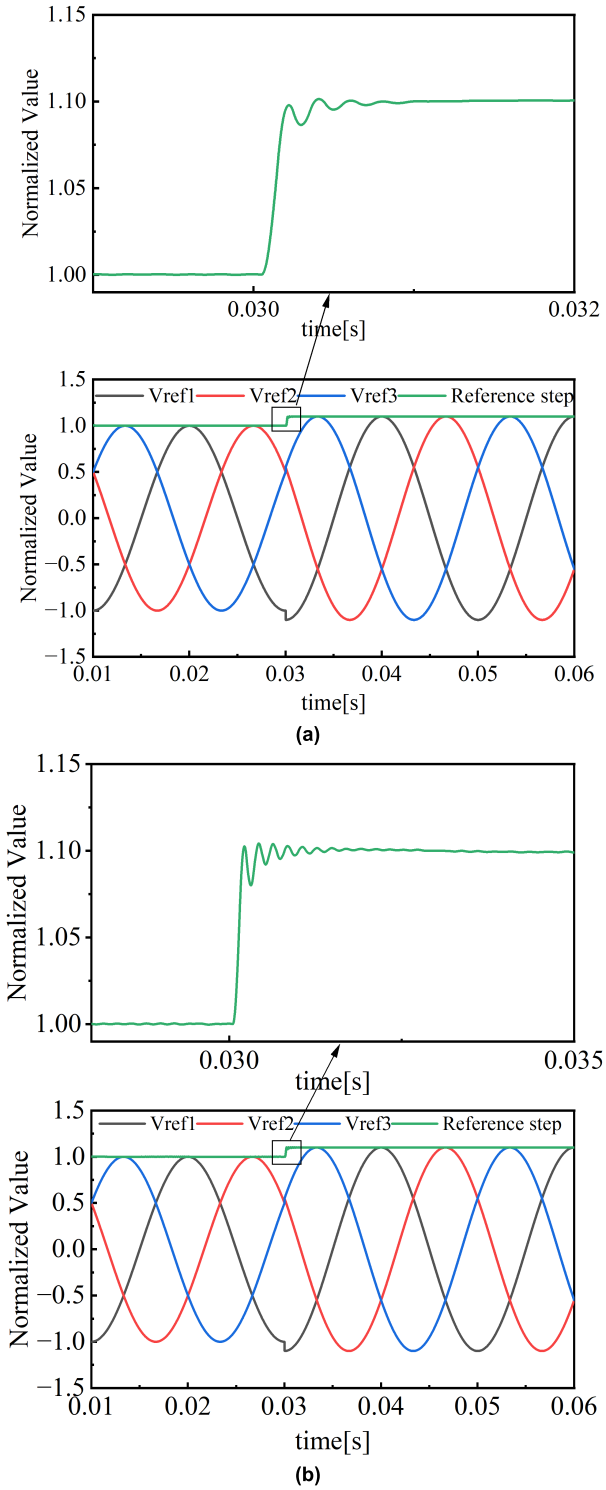

FIGURE 17. Experimental waveforms of the voltage control system for single-phase VSIs under a 10% voltage step change. (a) After optimizing the control algorithm. (b) Before optimizing the control algorithm.

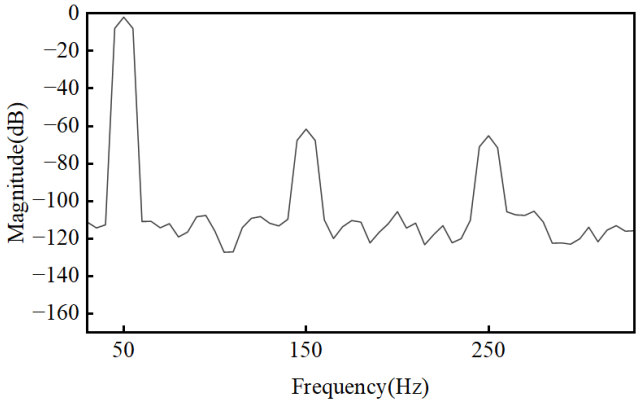

FIGURE 18. Spectrum of ripple after PWM (without filter).

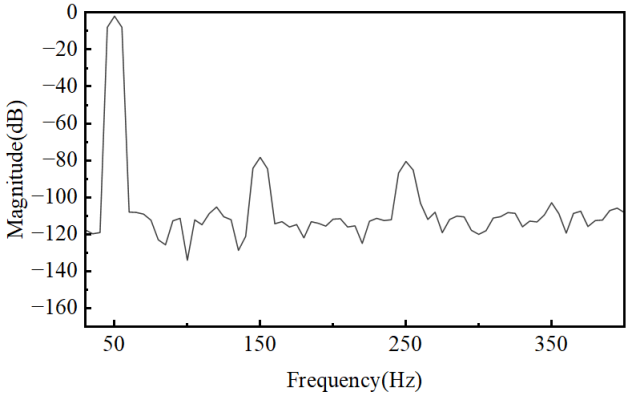

FIGURE 19. Spectrum of ripple after PWM (After Filtering).

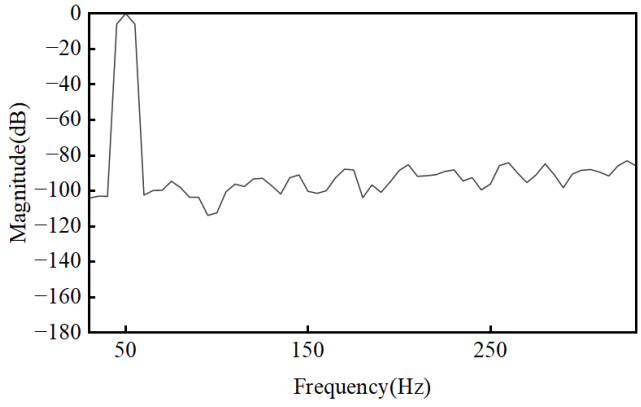

FIGURE 20. Spectrum of ripple after PWM (filter + resonant controller).

filter, the THD of the voltage waveform is significantly higher than that with the ripple notch filter, and the use of the resonant controllers can further reduce the THD of the voltage waveform. A comparison of the harmonic content for every order harmonic across the three schemes is presented in Table 2. The third-order harmonic content is 0.082% without the ripple notch filter scheme. The application of the 20kRNF results in a significant reduction, with a value of 0.012% for the third-order harmonic. Furthermore, the implementation of the resonant controllers leads to a further reduction, bringing the third-order harmonic down to an insignificant level, rendering the effect of ripple negligible in this scenario.

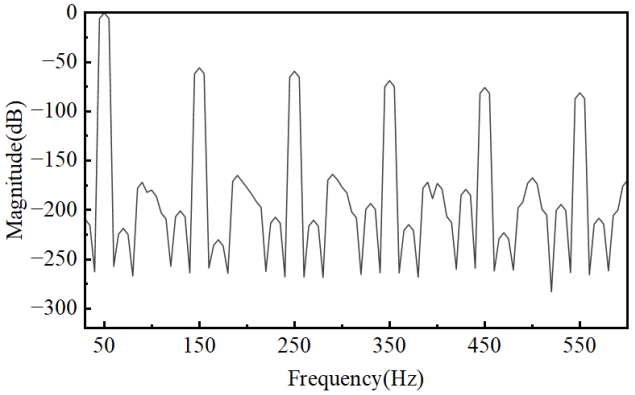

FIGURE 21. The spectrum of the output voltage without an aliasing suppression scheme.

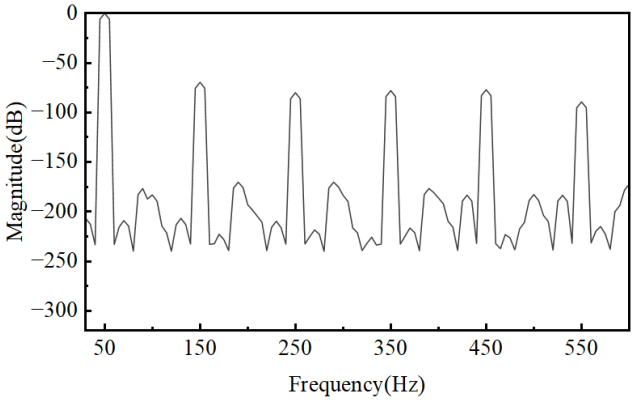

FIGURE 22. The spectrum of the output voltage after implementing the alias-free sampling scheme.

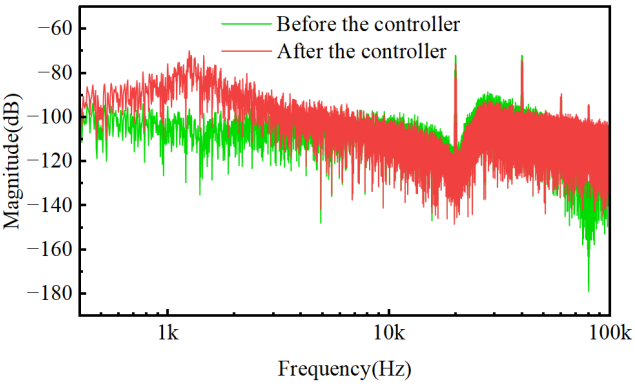

FIGURE 23. The spectrum of the ripple signal before and after passing through the type-III controller.

C. VERIFICATION OF THE ALIASING-FREE SAMPLING SCHEME

To validate the effectiveness of the alias-free sampling scheme in suppressing the low-order aliased harmonics of the capacitor voltage. Figure 21 presents the experimental results of the capacitor voltage rule sampling. It is evident from the theoretical calculations in equation (17) that the capacitor voltage rule sampling leads to significant levels of low-order aliased harmonics.

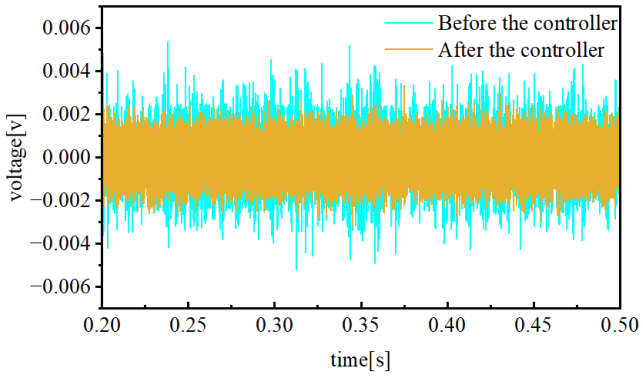

FIGURE 24. Time domain waveform of ripple signal before and after passing through the type-III controller.

Figure 22 shows the spectrum of the capacitor voltage with a 90° phase-shift filter. From Figure 22, it can be seen that adding a filter with a certain phase lag before the sampling component can effectively suppress the frequency aliasing caused by the sampling. The data in Table 3 indicates that under the alias-free sampling scheme, every order harmonic is effectively suppressed.

D. VERIFICATION OF THE INFLUENCE OF TYPE III VOLTAGE CONTROLLER ON RIPPLE

According to the literature, the system takes current as the control variable, and the current controller is a proportional action, which only affects the amplitude of the ripple [25]. However, in the voltage control system for single-phase VSIs, where the voltage is employed as the control variable, the type-III voltage controller affects both the amplitude and phase angle of the ripple. The red line in Figure 23 displays the spectrum of the ripple signal after undergoing the control action, resulting in an attenuation effect within the frequency range of 400Hz to the crossover frequency. The corresponding time domain waveform is shown in Figure 24, where the type-III controller effectively attenuates the amplitude of the ripple.

VII. CONCLUSION

This article first analyzes the impact of high-frequency ripple from both the frequency domain and time domain perspectives. In the frequency domain, it results in the ripple aliasing, while in the time domain, it makes PWM saturation more likely to occur. A ripple attenuation scheme has been proposed to address the problem of time-domain saturation without significant performance loss. Combined with the resonant controller, it effectively suppresses the distortion caused by ripple. However, the sampling aliasing is different from the ripple aliasing. The phase angle of the aliasing harmonics is mathematically derived, and a 90° phase shift filter is proposed to suppress the aliasing signals generated in the system. The theoretical analysis is verified through the experiment.

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