IEEE Access
Multidisciplinary | Rapid Review | Open Access Journal

IEEE VEHICULAR TECHNOLOGY SOCIETY SECTION

Received 13 January 2024, accepted 13 February 2024, date of publication 19 February 2024, date of current version 23 February 2024.

Digital Object Identifier 10.1109/ACCESS.2024.3366934

RESEARCH ARTICLE

A Novel Control Scheme for Traction Inverters in Electric Vehicles With an Optimal Efficiency Across the Entire Speed Range

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This work was supported by NSERC Canada.

ABSTRACT In the context of the electric vehicle (EV) industry, multi-level inverters (MLIs) have garnered increasing attention due to their potential to harness the advantages of higher DC link voltages. Among the various MLIs, the three-level T-type neutral-point-clamped (T-NPC) topology stands out as a superior alternative to the conventional two-level six-switch counterpart. This paper presents an adaptive Space Vector Modulation (SVM) technique for the typical three-level T-NPC inverter, with the aim of enhancing inverter performance across a wide speed spectrum in EVs. Through a comprehensive process of design, simulation, and experimental analysis, the findings reveal improvements in efficiency when compared to both the two-level six-switch inverter and the T-NPC inverter employing conventional three-level SVM. These results underscore the advantages and effectiveness of the introduced control scheme, which increases efficiency without incurring additional costs of any additional circuit components or control effort. The paper provides a complete set of in-agreement simulation and experimental results, to provide the proof of concept.

INDEX TERMS T-NPC inverter, SVM, low-speed range analysis, PMSM.

I. INTRODUCTION

This The advent of multi-level inverters (MLIs) marked a significant shift away from the conventional two-level six-switch topology in a wide range of applications [1]. In applications using medium-voltage high-power to high-voltage high-power, MLIs have demonstrated their superiority over the conventional counterpart. The utilization of MLIs has effectively addressed several key challenges in high-voltage high-power circuits, including issues such as high dv/dt, higher current and voltage harmonics, and higher device voltage stress [2], [3], [4]. However, while MLIs have proven advantageous for high and medium-power applications, the two-level topology continues to dominate in application where the DC link voltage remains below 650 Vdc [5]. This preference is due to its well-established design, off-the-shelf availability, and simple control circuit.

In response to the pressing need to reduce greenhouse gas emissions and mitigate environmental impacts, the transition from internal combustion engine vehicles (ICEVs) to energy-efficient electric vehicles (EVs) has become paramount [6]. Traction inverters play a pivotal role in all types of EVs, facilitating the transfer of electric power between sources and electric machines (EMs). In alignment with the EV industry roadmap set forth by the US Department of Energy (DoE), the 2025 targets for electric motor power and traction inverters with boost converters are set at 50 kW/L and 100 kW/L, respectively [7]. To achieve comparable travel times with ICEVs, especially with current battery capacities, it is imperative to employ charger systems exceeding 400 kW. This necessitates the use of extreme fast chargers (XFCs) operating at output voltages exceeding 800 Vdc [8]. To meet the

The associate editor coordinating the review of this manuscript and approving it for publication was Jie Gao.

DoE's targets and accommodate higher DC link voltages, traditional inverter topologies face substantial challenges, as previously outlined. Another critical concern in EVs utilizing two-level technology for their traction inverters is their lower performance at low-speed ranges. Operating at low-speed ranges is another critical issue where traction inverter operates at a partial of its nominal power leading to deteriorates on its performance. This drawback becomes particularly important when considering that Urban EVs (UEVs) often operate within this speed range exceeding 50% of their typical drive cycles [9], [10]. Here are some potential challenges and issues associated with operating a traction inverter at low-speed ranges with reduced power demand:

1. Efficiency Loss: Traction inverters are typically designed to operate near maximum efficiency within a certain power loading range. Operating at lower loading conditions or below this range will result in a deteriorating or reduced efficiency, as the inverter controller will not be able to optimize its performance for the lower power output, according to the limitations of the traditional space vector modulation techniques. In other words, at low speed ranges the ratio of the switching losses to the output power increases considerably. This will result in increased energy loss and reduced driving range for electric vehicles, especially if these cars are in an urban driving cycle with low speed for most of the time [11], [12].

2. Inverter Instability: Some traction inverters may have stability issues when operating at low speeds with reduced power. This can lead to suboptimal performance, including issues like torque ripple in electric motors [13].

3. Reduced Motor Performance: Electric motors in vehicles may not perform optimally at low speeds with reduced power input. This can result in decreased torque, slower acceleration, and reduced overall vehicle performance [14].

To address these issues, manufacturers of traction inverters and electric vehicles often implement control strategies that aim to optimize inverter performance at low-speed ranges. This may involve adjusting modulation schemes, current control, and other parameters to maintain efficiency and stability [15], [16], [17].

Multilevel topologies offer promising solutions for addressing the limitations associated with the use of conventional topologies at higher DC-link voltages while also avoiding additional unavoidable costs, as previously discussed [2], [18], [19]. Among all kind of multilevel topologies that have been conducted by researchers in the last few decades, Neutral Point-clamped (NPC), Flying Capacitors (FC), and T-type neutral-point-clamped (T-NPC) are well-known topologies that can be potentially substituted with their conventional counterparts. While the NPC topology presents an advantage in terms of lower switching losses due to the reduced blocking voltage across semiconductors, it is important to acknowledge certain technical and practical issues. These issues include increased conduction losses at nominal power levels due to the presence of multiple series semiconductors and uneven power distribution across these semiconductors, as discussed in prior studies [2]. Generally, FC topology is not an appropriate substitute for its conventional counterparts because capacitors are the most voluminous parts of traction inverters and have a higher failure rate than other components. A three-level T-NPC is depicted in Fig. 1, and compared to the three-level NPC, uses an active bidirectional switch to provide a zero-level voltage which connects to the midpoint of DC-link voltage and utilizes two diodes less per phase [20]. A T-NPC topology combines the advantages of the two-level topology, such as lower conduction loss, low number of components, and a simple control strategy, with the advantages of a three-level inverter, such as lower switching losses, superior voltage and current THD quality, and lower Electromagnetic Interference (EMI) issues [21].

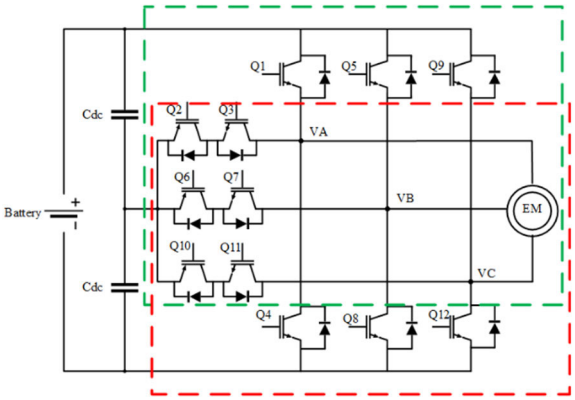

FIGURE 1. A typical three-level T-NPC scheme.

Fault ride-through is another important criterion in terms of utilizing power converters and is more important in the EV industry. Generally, two types of faults can be considered in a typical semiconductor: switch short-circuit (SSC) and switch open-circuit (SOC). Although an SSC faulty condition may cause serious damage to the converter, it may lead to an SOC by using a suitable fault-isolating element. Several studies in the literature have been conducted to improve the reliability of the three-level inverter topologies [20], [22], [23], [24]. In addition to the previously mentioned advantages, the T-NPC topology allows traction inverters to continue operating at partial nominal power during SOC failure. This unique feature originates from the three-level T-type NPC topology, which consists of two independent two-level inverters. Therefore, using a precise method to detect and remove the faulty element, a supplementary modulation technique can utilize the traction inverter in the new condition.

In alignment with DoE directives and the imperative shift toward higher DC-link voltages, the selection of a three-level T-NPC inverter stands out as the most optimal choice among the other well-established MLIs. To deploy each inverter effectively, as a standalone entity if needed, a specific switching pattern must be meticulously applied to the switches. The Space Vector Modulation (SVM) technique demonstrates a

distinct advantage over other pulse width modulation (PWM) techniques, owing to its superior utilization of the DC-link voltage considering redundancy of switching states to have fewer switching actions, and superior total harmonic distortion (THD) [22]. However, it has its own limitations for an entire speed range.

In summary, this paper overcomes these shortfalls, as it proposes a new modified comprehensive control modulation technique based on SVM focusing on the T-NPC inverter topology. In this approach, the central controller dynamically selects the most suitable modulation technique to enhance EVs performance across a broad spectrum of operating speeds. In other words, as the speed level reaches below a predefined low threshold value, the central controller shapes the control command to change the modulation technique such that it is not the conventional three-level SVM. This technique enhances the modulation index by utilizing half of the DC-link voltage, resulting in improved inverter efficiency by forcing the modulation signal to shape a two-level waveform instead of a three-level waveform while keeping the voltage stress half of the DC-link voltage value. On the other hand, when EVs operate at high speeds, the conventional three-level SVM is used where the modulation command forms a three-level voltage waveform that utilizes full DC-link voltage capacity. This comprehensive control scheme, integrated within the proposed modulation technique, contributes to an overall increase in the efficiency of EVs. Based on verified simulation results, the efficiency of traction inverter increases up to 2.5% compared to the standard SVM without the need for additional elements and extra cost. Rest of this paper is organized as follows:

Section II discusses the proposed control scheme and the modified modulation technique. Section III presents the details of the case study and the proposed approach for selecting the appropriate switching pattern. In Section IV, all simulation and experimental results are demonstrated. Finally, conclusions are presented in Section V.

II. CONCEPT OF THREE-LEVEL SVM AND MODIFIED SVM TECHNIQUE

In the context of EVs operations, the three-level T-NPC inverter employs two distinct modulation techniques:

a) Mode 1 incorporates the modified modulation which is introduced in this paper for low-speed ranges.

b) Mode 2 utilizes a standard three-level SVM for high-speed ranges. The diagram in Fig. 2 shows the operational limits for these modes. Within the standard three-level SVM, there exist four types of voltage vector magnitudes as illustrated in Fig. 3. Small vectors, denoted as $(\vec{V}_1), (\vec{V}_2), \ldots, (\vec{V}_3)$, have magnitudes of $1/3V_{dc}$. Medium vectors, represented by $(\vec{V}_7), (\vec{V}_8), \ldots, (\vec{V}_{12})$, have magnitudes of $\sqrt{3}/3V_{dc}$.

Lastly, the large vectors, $(\vec{V}_{13}), (\vec{V}_{14}), \ldots, (\vec{V}_{18})$, have magnitudes equal to $2/3V_{dc}$. In contrast to the large vectors, the medium and small vectors exert significant effects on the neutral point (NP) voltage deviation. As a result, during each sampling frequency, it is essential to consider the dominant

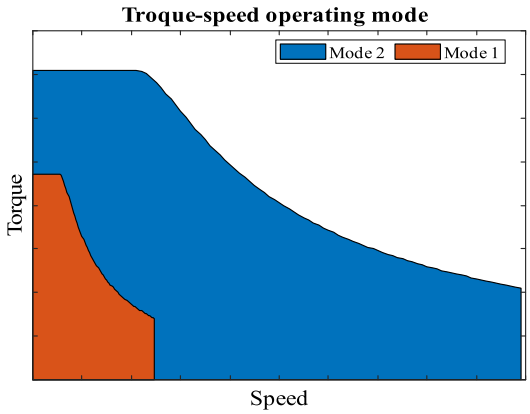

FIGURE 2. Speed-torque boundaries for EVs' operation.

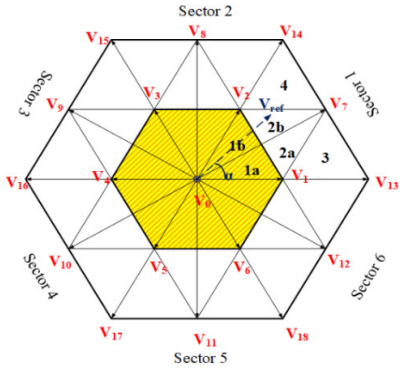

FIGURE 3. The standard three-level SVM hexagonal.

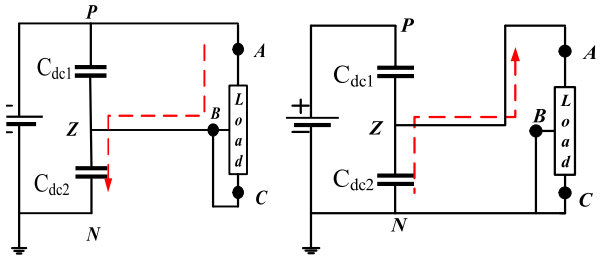

FIGURE 4. The current path in different switching pattern and its effect on the potential of NP; a) P_{MODE}; and b) N_{MODE}.

vector with its complementary vector [20]. As illustrated in Fig. 4, when the DC source feeds the load (indicated by the red line) and assumed that the tip of the voltage reference is located in section Ia (as per Fig. 3), the two nearest small vectors are $(\vec{V}_1)$ and $(\vec{V}_2)$, with $(\vec{V}_1)$ being the dominant vector. Two distinct vector configurations yield small vectors, as exemplified by the vectors [P 0 0] and [0 N N], resulting in a small vector denoted as $(\vec{V}_1)$. In the case of the [P 0 0] vector, unlike Phase A, which is linked to the positive terminal of C_{dc1} capacitor, the other two phases (B and C) are connected to the NP. This arrangement causes C_{dc2} to undergo a charging process. Conversely, in the [0 N N] vector, as depicted in Fig. 4.b, Phase A is connected to the NP while the two

remaining phases are connected to the negative terminal of the lower DC-link capacitor. Vector [0 N N] is a complement of vector [P 0 0], as it discharges C_{dc2}. The complete set of smaller vectors and their corresponding complementary vectors are depicted in Fig. 5a and 5b, referred to as P_{MODE} and N_{MODE}, respectively.

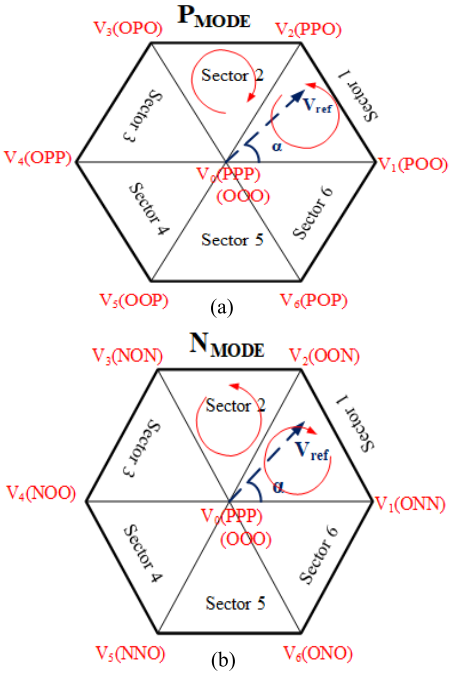

FIGURE 5. Categorized small vectors at low-speed range (a) P_{MODE}; (b) N_{MODE}.

The proposed modified modulation technique can utilize the T-NPC topology as two independent two-level inverters. The definitions of the switching states are listed in Table 1. The implementation of a three-level SVM considers two important factors: the reference voltage magnitude, which determines the sector, and the sector where the tips of the reference voltage is located. A central control system momentarily measures the reference voltage amplitude to determine the operational region of the electric motor. The following criteria are used to find the region, commonly referred to as Mode 1 and Mode 2:

$$V_{threshold}: \begin{cases} Mode1: & 0 < V_{ref} \leq \dfrac{1}{2*\sqrt{3}} V_{dc} \\ Mode2: & \dfrac{1}{2*\sqrt{3}} V_{dc} < V_{ref} \leq \dfrac{\sqrt{3}}{3} V_{dc} \end{cases} \quad (1)$$

Through this approach, the system can accurately identify the operational region of the EVs. The region represented by the yellow area has a radius of $1/((2*\sqrt{3})V\_dc)$. By calculating the angle of the reference voltage (θ=$tan(-1)((V\_\beta/V\_\alpha))$), the sector is achieved where the reference voltage is located. where V_α is a real part and V_β is imaginary part of the reference voltage. By calculating θ, the three voltage vectors are achieved that show the switching patterns. The generalized form of θ that can be applied for the whole six sectors is obtained by (2).

$$\acute{\theta} = \theta - (k-1)\pi/3, \quad for\ 0 < \acute{\theta} < \pi/3 \quad (2)$$

where k = 1, 2, 3, …., 6 for the sector one to six, respectively. In section one, the relation between dwell times and switching frequency with the magnitude of the voltage reference is shown in (3).

$$\vec{V}_1.T_a + \vec{V}_2.T_b + \vec{V}_0.T_c = \frac{V_{ref}}{F_s} e^{j\theta} \quad (3)$$

The dwell time for the proposed modulation technique can be calculated using Eq. (4), as follows:

$$\begin{cases} T_a = 2m.T_s.\sin(\dfrac{\pi}{3} - \acute{\theta}) \\ T_b = 2m.T_s.\sin(\acute{\theta}) \\ T_c = \left[1 - 2\text{m}.\sin\left(\dfrac{\pi}{3} + \acute{\theta}\right)\right].T_s \end{cases} \quad (4)$$

where m denotes the modulation index, and T_a, T_b, and T_c are the dwell times for the vector $\vec{V}_1$, $\vec{V}_2$, and $\vec{V}_3$, respectively. This will lead to the following modulation scheme values as given in Table 1.

TABLE 1. Switching states in three-level T-NPC topology.

Switching State	Semiconductors States (Phase A)				Phase Voltage V_{AZ}
	Q1	Q2	Q3	Q4	
P	ON	ON	OFF	OFF	$+\frac{V_{dc}}{2}$
O	OFF	ON	ON	OFF	0
N	OFF	OFF	ON	ON	$-\frac{V_{dc}}{2}$

Depending on the modulation technique (the standard form or the proposed method), the maximum modulation index varies and can be calculated using (5).

$$\begin{cases} Mode1: & m_{max} = \sqrt{3}\dfrac{V_{ref}}{(\frac{V_{dc}}{2})}; 0 < |V_{ref}| \leq \dfrac{1}{2*\sqrt{3}} V_{dc} \\ Mode2: & m_{max} = \sqrt{3}\dfrac{V_{ref}}{V_{dc}}; \dfrac{1}{2*\sqrt{3}} V_{dc} < |V_{ref}| \leq \dfrac{\sqrt{3}}{3} V_{dc} \end{cases}$$
$$\Longrightarrow \begin{cases} Mode1: & 0.0 < m_{proposed} \leq 0.5 \\ Mode2: & 0.5 < m_{standard} \leq 1.0 \end{cases} \quad (5)$$

Table 2 illustrates the switching patterns form the sector1 to sector3 for both the standard form and the proposed modified SVM. As it can be inferred from table 2, for the proposed modified two-level modulation technique, the system is more active (P-mode or N-mode) than the inactive mode (in which the current passes through the neutral leg) compared to the standard form. For example, the number of zero vectors for the standard three-level SVM were 15 states, whereas this

metric is 12 for the proposed technique. Since the conduction loss has a direct relation to the path along which the current flows, the fewer elements the current passes, the less conduction loss will be. The reduction in power losses of the T-NPC inverter will be improved due to the implementation of the proposed modulation technique, driven by two following distinct factors:

1) For each switching interval, one semiconductor is switched less or switched only when the current passes from the inverse diode. This results in zero-voltage switching compared to the standard modulation techniques. This, in turn, leads to a reduction in the switching losses.

2) As governed by (5) the modulation index has an inverse relationship with the DC-link voltage V_{dc}. Thus, the proposed modulation technique effectively doubles the modulation index effect, given that the DC-link voltage becomes half compared to the standard technique. Moreover, the number of states that the inverter maintains in inactive mode decreases with the proposed technique. Consequently, the current flows through the NP leg for a shorter time period at each sampling frequency, in contrast to the conventional modulation methods. Given that the NP leg comprises two elements (a switch and a diode), this leads to an increase in conduction losses at a lower modulation index rate.

III. CASE STUDY

A permanent magnet synchronous machine (PMSM) is fed by a DC source within the inverter interface. A multistage control strategy was used to control the PMSM. A PMSM drive control with the maximum torque per ampere in the constant torque region, and a field weakening and maximum torque-per-voltage strategy in the constant power region are utilized to guarantee that the PMSM works efficiently.

Fig. 6(a) shows the control block diagram of the PMSM drive system with its central controller. The central controller acts based on the logics that are shown in Fig. 6(b) and 6(c), respectively.

The output in Fig. 6(b) shows the type of modulation technique that should be used. If the reference voltage is less than the threshold, the UEV operates in the low-speed range, and the proposed modulation is applied to the taction inverter. Otherwise, a standard SVM is utilized. Fig. 6(c) shows the strategy for maintaining the DC-link voltage balance. In the following, the procedure for vector group selection is explored.

A. IN MOTOR MODE (DC SOURCE FEEDS THE EMs)

• If the error signal is positive (the voltage across the bottom capacitor is higher than the half of the DC-link voltage), the lower DC-link capacitor is in the charging mode. Therefore, to maintain the DC-link voltage balance, N_{MODE} should be selected to toggle the bottom capacitor in the discharging mode.

• If the error signal is negative, the lower capacitor is in discharging mode. Subsequently, the P_{MODE} vector groups must be selected to charge the bottom capacitor.

TABLE 2. Switching states in the standard form and the related proposed method form.

Section I	Standard three-level SVM	$\overrightarrow{V_1}$ Dominant	T_a /4	T_b /2	T_0 /2	T_a /2	T_0 /2	T_b /2	T_a /4
			ONN	OON	OOO	POO	OOO	OON	ONN
		$\overrightarrow{V_2}$ Dominant	T_b /4	T_0 /2	T_a /2	T_b /2	T_a /2	T_0 /2	T_b /4
			OON	OOO	POO	PPO	POO	OOO	OON
	Proposed technique *N Mode*		T_0 /4	T_b /2	T_a /2	T_0 /2	T_a /2	T_b /2	T_0 /4
			OOO	OON	ONN	NNN	ONN	OON	OOO
	Proposed technique *P Mode*		T_0 /4	T_a /2	T_b /2	T_0 /2	T_b /2	T_a /2	T_0 /4
			OOO	POO	PPO	PPP	PPO	POO	OOO
Section II	Standard three-level SVM	$\overrightarrow{V_2}$ Dominant	T_a /4	T_b /2	T_0 /2	T_a /2	T_0 /2	T_b /2	T_a /4
			OON	OOO	OPO	PPO	OPO	OOO	OON
		$\overrightarrow{V_3}$ Dominant	T_b /4	T_0 /2	T_a /2	T_b /2	T_a /2	T_0 /2	T_b /4
			NON	OON	OOO	OPO	OOO	OON	NON
	Proposed technique *N Mode*		T_0 /4	T_a /2	T_b /2	T_0 /2	T_b /2	T_a /2	T_0 /4
			OOO	OON	NON	NNN	NON	OON	OOO
	Proposed technique *P Mode*		T_0 /4	T_b /2	T_a /2	T_0 /2	T_a /2	T_b /2	T_0 /4
			OOO	OPO	PPO	PPP	PPO	OPO	OOO
Section III	Standard three-level SVM	$\overrightarrow{V_3}$ Dominant	T_a /4	T_b /2	T_0 /2	T_a /2	T_0 /2	T_b /2	T_a /4
			NON	NOO	OOO	OPO	OOO	NOO	NON
		$\overrightarrow{V_4}$ Dominant	T_b /4	T_0 /2	T_a /2	T_b /2	T_a /2	T_0 /2	T_b /4
			NOO	OOO	OPO	OPP	OPO	OOO	NOO
	Proposed technique *N Mode*		T_0 /4	T_b /2	T_a /2	T_0 /2	T_a /2	T_b /2	T_0 /4
			OOO	NOO	NON	NNN	NON	NOO	OOO
	Proposed technique *P Mode*		T_0 /4	T_a /2	T_b /2	T_0 /2	T_b /2	T_a /2	T_0 /4
			OOO	OPO	OPP	PPP	OPP	OPO	OOO

B. IN REGENERATIVE MODE (EMs SUPPLY THE DC SOURCE)

• If the error signal is positive, the lower capacitor should be placed in the discharging mode, and then the P_{MODE} vector groups should be applied.

• Finally, if the error signal is negative, the N_{MODE} vector groups should be selected to charge the lower capacitor.

In summary, there are two distinctive modes as per the controller logic in a vice-versa fashion. A comparison study conducted, and the results depicted in Fig. 7 to elaborate that which kind of the inverter performs better for voltage exceeding 900 Vdc. While the two-level inverters demonstrate superior performance for voltages below 650 Vdc,

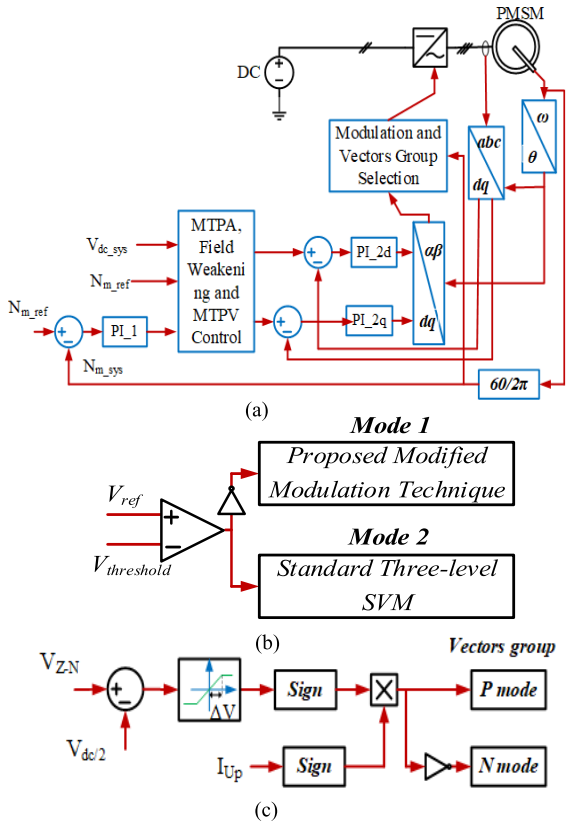

FIGURE 6. (a) The control schematic; (b) Modulation technique selection; and (c) vector group selection.

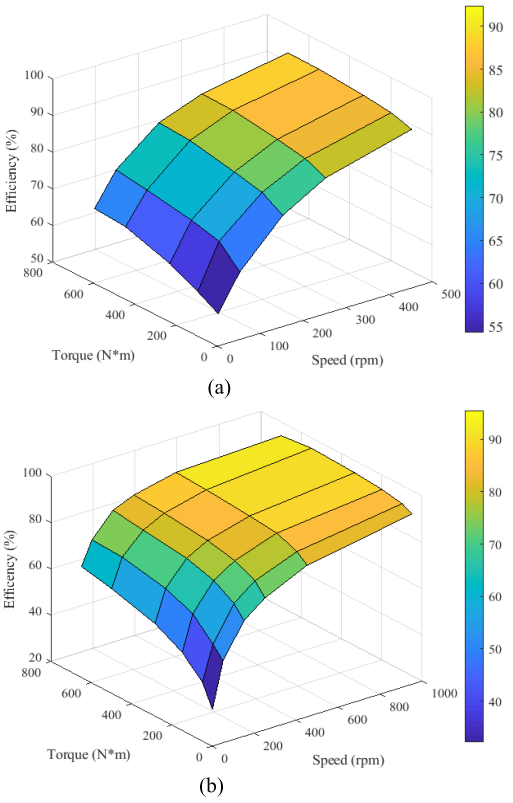

FIGURE 8. Low-speed and low-torque efficiency; a) three-level T-NPC, b) two-level inverter.

their effectiveness declines at higher voltages, as indicated in Fig. 7. This inefficiency becomes more pronounced at higher switching frequencies. While the three level T-NPC topology prevails with the best performance amongst other topologies in comparison.

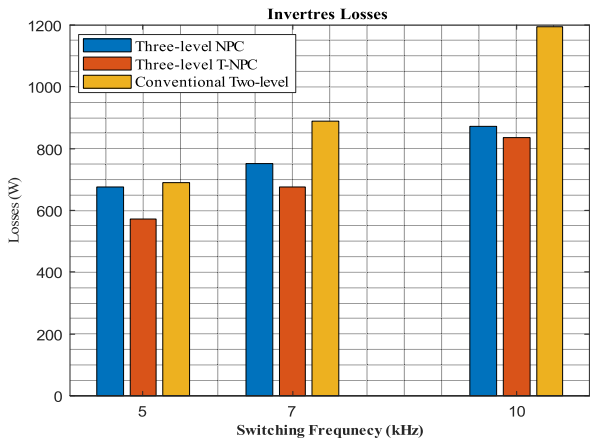

FIGURE 7. Comparison study of inverters' losses.

Regardless of the topology, a notable reduction in efficiency becomes apparent when operating in low-speed regimes. This phenomenon is visually demonstrated in Fig. 8(a) for the three-level T-NPC inverter and Fig. 8(b) for the two-level inverters. For instance, at a 10 kHz switching frequency with a 900 Vdc input, the efficiency of the two-level inverter registers at 56.67% when operating at 100 rpm with a torque of 100 Nm.

In contrast, the three-level T-NPC inverter achieves an efficiency of 64.2% under the same conditions. When the speed is increased to 1000 rpm while maintaining the torque at 100 Nm, the efficiency improves significantly, reaching 91.16% for the two-level inverter and 94.10%.

Therefore, there are 34.49% and 29.9% differences between the nominal load and low load operation for the two-level and three-level T-NPC topologies, respectively. It is worth mentioning that the system efficiency is calculated using the equation below:

$$\eta_{sys} = \frac{P_{out}}{P_{in}} = \frac{3/2(V_d.I_d + V_q.I_q)}{V_{dc}.I_{dc}} \tag{6}$$

where P_{in} and P_{out} represent the input and output active powers and P_{out} is achieved in the dq frame. The application of the proposed modulation technique results in improved efficiency for the three-level T-NPC inverter, as illustrated in Fig. 9(a) in comparison to the standard three-level SVM, and in Fig. 9(b) in comparison to two-level inverters. The comparison assessment of the efficiency is conducted using (7), as shown below:

$$\eta_{enhanced} = \left(\eta_{proposed} - \eta_{convetional}\right) \times 100 \tag{7}$$

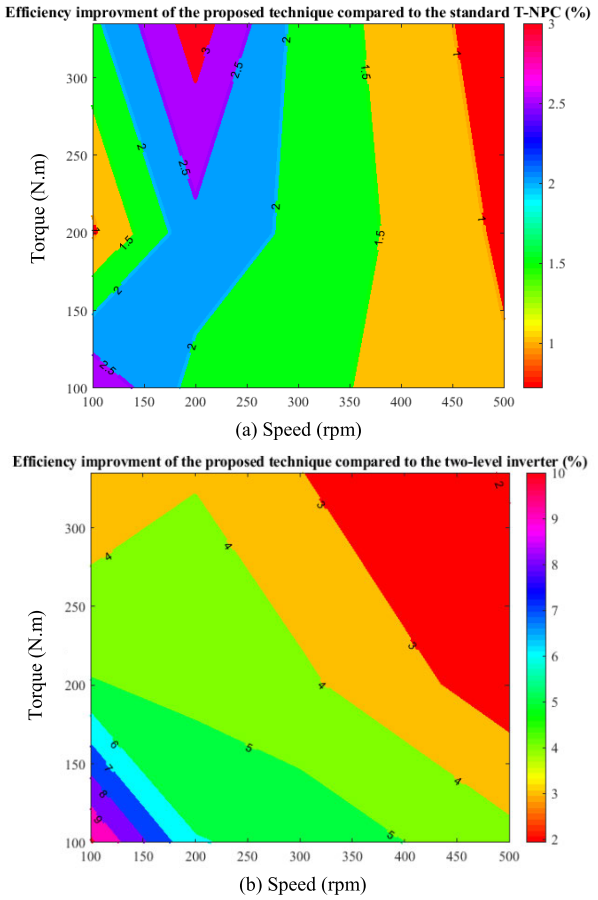

FIGURE 9. The maps of efficiency improvement compared; a) to the standard three-level SVM; b) to the two-level inverter.

where $\eta_{enhanced}$ represents the level of increased efficiency achieved by the proposed technique in comparison to conventional topology (two-level) and approaches (standard three-level SVM). As illustrated in Fig. 9(a), the novel modulation method exhibits a noteworthy efficiency improvement of up to 2.5% when compared to the conventional three-level space vector modulation (SVM). this enhancement reaches up to 9% when comparing the proposed modulation technique to the conventional two level.

It can be seen from Fig. 9(a) and Fig. 9(b) that the enhancement of efficiency is achieved in the low-speed and low torque range. This is achieved without adding a cost to the controller structure or control effort. Assessing the THD of the phase voltage constitutes a significant factor in the traction inverter performance. However, the current THD holds less prominence as the EMs effectively act as highly inductive loads, effectively serving as current filters. The evaluation of the phase voltage THD criterion in the low-speed range is visually depicted in Fig. 10.

The comparison analysis of THD between the proposed modulation technique and with two other systems is derived from (8).

$$THD_{Comparison} = \left(THD_{proposed} - THD_{conventional}\right) \times 100 \tag{8}$$

TABLE 3. Related parameters in simulation results.

PMSM Parameters	Value	Controllers	Value
Back EMF constant (Kd)	147.95	Current Controller	
Poles	4	d-axis proportional gain	0.021
Stator winding resistance	0.0203	d-axis, time constant	0.074
d-axis inductance	0.0015	q-axis proportional gain	0.069
q-axis inductance	0.005	q-axis, time constant	0.245
Moment of inertia	0.026	Speed Controller	
Shaft time constant	100	proportional gain	7.875
Maximum motor speed	10000	time constant	0.016

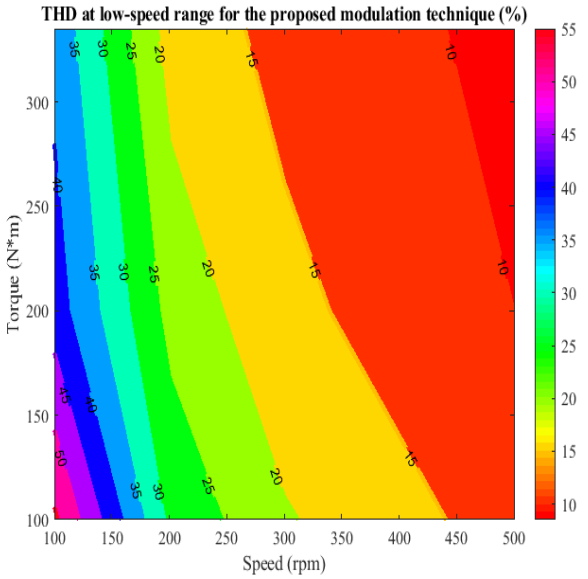

FIGURE 10. The THD of the proposed technique at a low-speed range with 10 kHz switching frequency at fundamental frequencies.

where $THD_{proposed}$ is the amount of THD in the proposed modulation technique, and the $THD_{conventional}$ is related to the conventional two-level and standard three-level T-NPC inverters, as depicted in Fig. 11(a) and Fig. 11(b). A thorough comparison of voltage THD is conducted with the standard three-level NPC inverter, where the conventional SVM with minimal NP voltage deviation is employed. The outcomes of this comparison affirm that the proposed modulation technique leads to an improvement in THD ranging from 2% to 14%, as demonstrated in Fig. 11(a). Furthermore, this comparative study extends to two-level traction inverters. The findings highlight the substantial enhancement in THD achieved through the application of the proposed modulation technique in contrast to the two-level inverter, as presented in Fig. 11(b).

IV. SIMULATION AND EXPERIMENTAL RESULTS

A. SIMULATION RESULTS

All the related parameters of the described system under study to extract simulation results are shown in Table 3. Two scenarios are considered to show the system's outputs: 1) at the nominal power demand, and 2) at low-speed range or low power demand. For the high-speed range (nominal

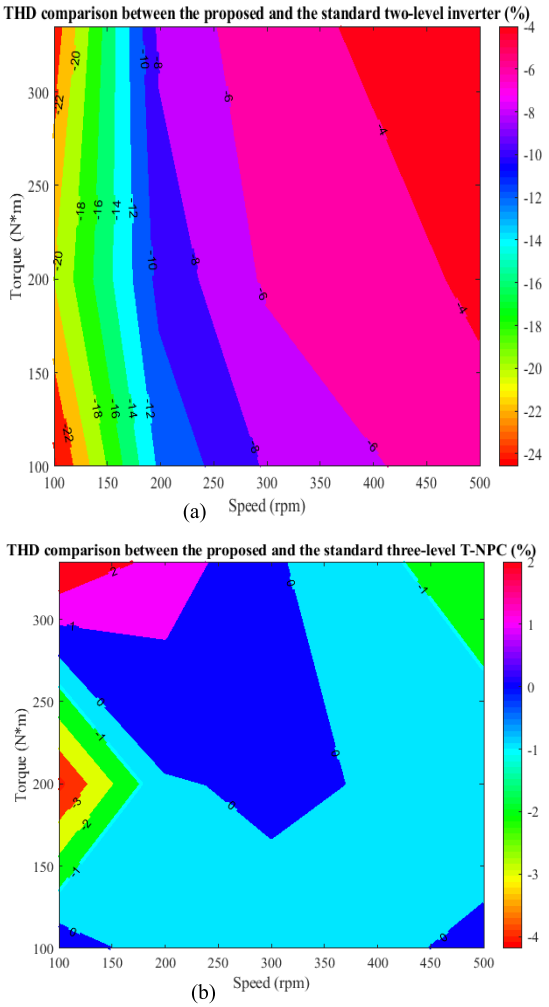

FIGURE 11. The THD enhancements for the proposed topology compared to; a) the two-level inverter, b) the three-level T-NPC.

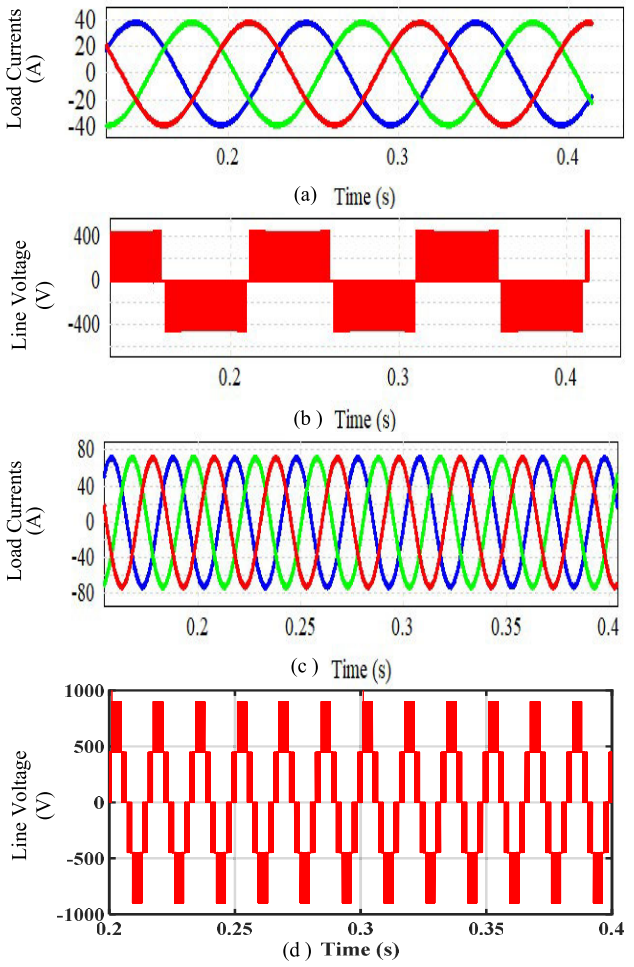

FIGURE 12. Low-speed range: a) three-phase load currents, b) line-to-line voltage, and high-speed range: c) three-phase load currents, d) line-to-line voltage.

power demand), the requested torque is 100 Nm, and speed is 1000 rpm, while for the low-speed range, these values are 50 Nm and 300 rpm, respectively. Hence, the simulation results are shown from Fig. 12(a) to Fig. 12(d) in which the three-level T-NPC inverter operates in two modes: 1) as a two-level at low loads (Fig. 12(a) and Fig. 12(b)), and 2) as a three-level at nominal load (Fig. 12(c) and Fig. 12(d)).

B. EXPERIMENTAL RESULTS

To demonstrate the effectiveness of the proposed central control circuit and modulation technique, a downsize 1.2 KW laboratory prototype was built. The IGBT based three-phase inverter was used to implement the three-level T-NPC topology, and the IGBTs used was 650 V, 25 A and part number STGF10M65DF2. Generally, a three-level T-NPC topology needs 9 isolated gate drivers for IGBT switch control. Three more isolated gate drivers (optocoupler) were required for the middle of the neutral leg switches compared to the two-level inverter and the technology that was used is the UCC23513DWYR. The control signals, coming from the DSP which is TMS320F28335, were sent to the primary side of gate drivers which are 3.3 V PWM signals. The UCC23513DWYR input is current controlled and does not require any primary side power supply. The secondary side was powered by a +15 V and −8 V which were referenced to the IGBT emitters. The secondary side of the gate drivers were supplied through the two flyback buck converters that each of them included four outputs and each output consisted +15/−8 V with 300 mA. A coupling of an induction motor (IM) with a permanent magnet synchronous motor (PMSM) is employed to extract experimental results, as depicted in Fig. 13. Additionally, a three-phase RL load is utilized to demonstrate the effectiveness of proposed modulation technique, with the corresponding results illustrated in Fig. 14 and Fig. 15. Under the steady-state condition with the rms load current of 142.5 mA, the prototype inverter operates with the standard three-level SVM, as shown in Fig. 14. As can be seen, the standard three-level SVM generates the appropriate signals to provide a three-phase sinusoidal current and five level line-to-line voltage. When the load current decreased

to the threshold, system switched to the to the low-speed range in EVs. Therefore, the proposed modulation technique is applied to the system and inverter operates as a two-level topology. The three-phase load current and line-to-line voltage are shown in Fig. 15.

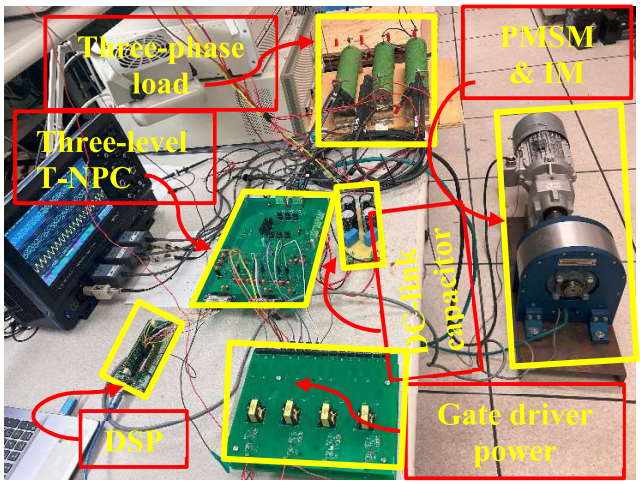

FIGURE 13. Scaled-down a three-level T-NPC inverter prototype.

Performance of the proposed control scheme and modulation technique also verified in an IM and PMSM system where IM is coupled with PMSM. The PMSM is controlled by the T-NPC using the proposed SVM method and through the shaft coupling turns the IM so that the IM acts as a generator. The output of the IM is connected to the three-phase resistive load to dissipate the generated electricity into heat. Fig.16 indicates the line voltage for the PMSM in green which is at 165 Vrms and the three-phase stator currents at around 2.28 Arms. As it can be seen the stator electrical frequency is around 50Hz. Since the PMSM under experiments has 4 poles, at this stator frequency its shaft synchronous speed is equal to 1500 rpm. It is worth mentioning that since the back EMF of the PMSM motors are trapezoidal, we expect a trapezoidal voltage across the PMSM line voltages. As Fig.16 indicates, the PMSM line voltage under the proposed SVM method has a trapezoidal shape while the line currents keep their sinusoidal waveforms which confirms the theory and effectiveness of the proposed modulation technique.

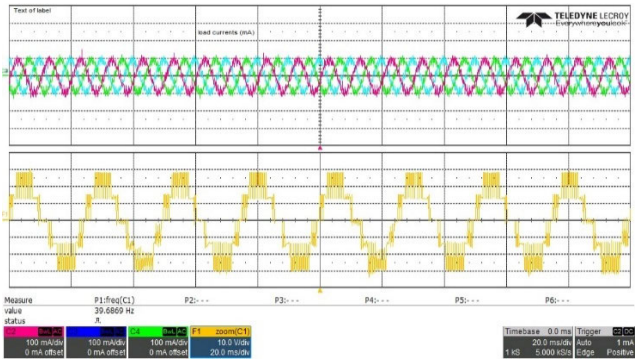

FIGURE 14. Three-phase load currents and voltage line at 55 V dc-link voltage.

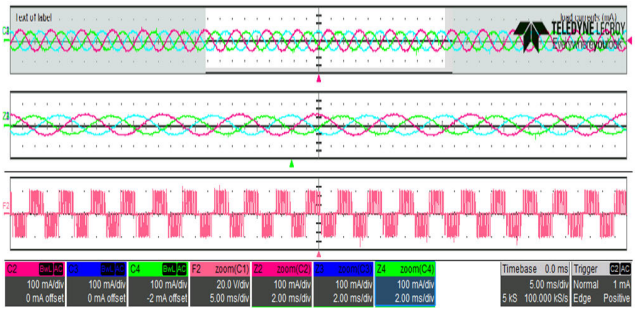

FIGURE 15. Three-phase load currents and voltage line at 30 V dc-link voltage.

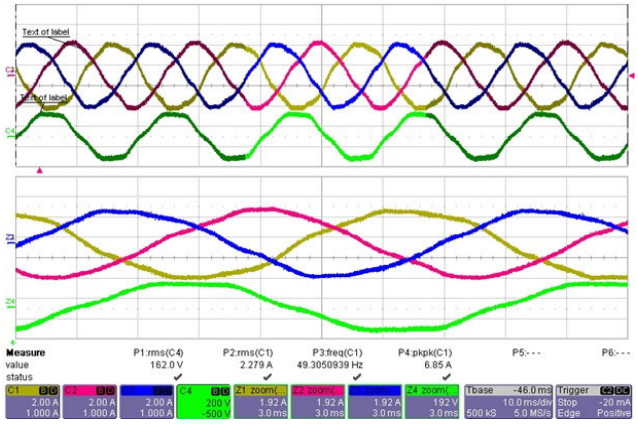

FIGURE 16. The line-to-line voltage and three-phase current of the PMSM.

V. CONCLUSION

The T-NPC topology has demonstrated its prowess in delivering enhanced performance and advantages, particularly in applications featuring a DC-link voltage exceeding 650 V. The critical role of modulation techniques in influencing inverter performance has been underscored throughout this study. The innovative modulation approach introduced in this research emerges as a key driver in elevating inverter efficiency within low-speed operational ranges for the T-NPC topology. Notably, this novel technique offers substantial efficiency gains, ranging from 2% to 9% across various low-speed ranges compared to two-level inverter. In comparison to the conventional three-level T-NPC topology, which relies on a three-level SVM method with minimal NP voltage deviation, this enhancement amounts to an impressive 2.5%. Furthermore, a comprehensive analysis of THD has shown the positive impact of the proposed modulation technique on power quality. For example, this approach results in a significant 24% reduction in THD compared to the two-level T-NPC configuration and a notable 4% reduction when compared to the standard three-level T-NPC inverter. These findings

collectively underscore the substantial benefits and promise of the proposed modulation technique in advancing inverter efficiency and power quality, particularly in the context of EV applications.

REFERENCES

[1] S. Kouro, M. Malinowski, K. Gopakumar, J. Pou, L. G. Franquelo, B. Wu, J. Rodriguez, M. A. Pérez, and J. I. Leon, "Recent advances and industrial applications of multilevel converters," *IEEE Trans. Ind. Electron.*, vol. 57, no. 8, pp. 2553–2580, Aug. 2010, doi: 10.1109/TIE.2010.2049719.

[2] A. Poorfakhraei, M. Narimani, and A. Emadi, "A review of multilevel inverter topologies in electric vehicles: Current status and future trends," *IEEE Open J. Power Electron.*, vol. 2, pp. 155–170, 2021, doi: 10.1109/ojpel.2021.3063550.

[3] K. Wand. *High performance 800v E-Motor for Automotive Application*. Accessed: 2016. [Online]. Available: https://www.profemag.ch/en/downloads-2/15avl-hochleistungs-800-v-e-motor-wand/viewdocument/212

[4] A. Bubert, K. Oberdieck, H. Xu, and R. W. De Doncker, "Experimental validation of design concepts for future EV-traction inverters," in *Proc. IEEE Transp. Electrific. Conf. Expo (ITEC)*, Jun. 2018, pp. 795–802, doi: 10.1109/ITEC.2018.8450253.

[5] Y. Jafarian, J. Ebrahimi, O. Salari, M. Z. Youssef, and A. Bakhshai, "A modified modulation scheme for T-type traction inverters to enhance low-speed range efficiency in electric vehicles," in *Proc. IEEE Appl. Power Electron. Conf. Exposit. (APEC)*, Mar. 2023, pp. 842–847, doi: 10.1109/APEC43580.2023.10131239.

[6] Z. Cao, H. Wen, Q. Bu, H. Shi, P. Xu, Y. Yang, and Y. Du, "Constant power load stabilization with fast transient boundary control for DAB converters-based electric drive systems," *IEEE Trans. Ind. Electron.*, vol. 71, no. 2, pp. 1863–1874, Feb. 2024, doi: 10.1109/TIE.2023.3253947.

[7] (Oct. 2017). *U.S. Drive Electrical and Electronics Technical Team Roadmap*. [Online]. Available: https://www.energy.gov/eere/vehicles/downloads/us-drive-electrical-and-electronics-technical-teamroadmap

[8] D. Ronanki, A. Kelkar, and S. S. Williamson, "Extreme fast charging technology—Prospects to enhance sustainable electric transportation," *Energies*, vol. 12, no. 19, p. 3721, Sep. 2019, doi: 10.3390/en12193721.

[9] S. Bhattacharya, D. Mascarella, and G. Joos, "Space-vector-based generalized discontinuous pulsewidth modulation for three-level inverters operating at lower modulation indices," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 5, no. 2, pp. 912–924, Jun. 2017, doi: 10.1109/JESTPE.2017.2666153.

[10] S. S. Williamson, A. Emadi, and K. Rajashekara, "Comprehensive efficiency modeling of electric traction motor drives for hybrid electric vehicle propulsion applications," *IEEE Trans. Veh. Technol.*, vol. 56, no. 4, pp. 1561–1572, Jul. 2007, doi: 10.1109/TVT.2007.896967.

[11] G. Nadh and A. Rahul S, "Clamping modulation scheme for low-speed operation of three-level inverter fed induction motor drive with reduced CMV," *IEEE Trans. Ind. Appl.*, vol. 58, no. 6, pp. 7336–7345, Nov. 2022, doi: 10.1109/TIA.2022.3199193.

[12] X. Li and S. S. Williamson, "Efficiency analysis of hybrid electric vehicle (HEV) traction motor-inverter drive for varied driving load demands," in *Proc. 33rd Annu. IEEE Appl. Power Electron. Conf. Expo.*, Feb. 2008, pp. 280–285, doi: 10.1109/APEC.2008.4522734.

[13] S. Devabhaktuni, "Low speed performance improvement of constant switching frequency DTC of five phase induction motor," in *Proc. Nat. Power Electron. Conf. (NPEC)*, Dec. 2021, pp. 1–6, doi: 10.1109/NPEC52100.2021.9672519.

[14] K. M. So, P. Gruber, D. Tavernini, A. E. H. Karci, A. Sorniotti, and T. Motaln, "On the optimal speed profile for electric vehicles," *IEEE Access*, vol. 8, pp. 78504–78518, 2020, doi: 10.1109/ACCESS.2020.2982930.

[15] K. Li, A. Bouscayrol, S. Cui, and Y. Cheng, "A hybrid modular cascade machines system for electric vehicles using induction machine and permanent magnet synchronous machine," *IEEE Trans. Veh. Technol.*, vol. 70, no. 1, pp. 273–281, Jan. 2021, doi: 10.1109/TVT.2020.3047219.

[16] D. Zhou, J. Wang, N. Hou, Y. Li, and J. Zou, "Dual-port inverters with internal DC–DC conversion for adjustable DC-link voltage operation of electric vehicles," *IEEE Trans. Power Electron.*, vol. 36, no. 6, pp. 6917–6928, Jun. 2021, doi: 10.1109/TPEL.2020.3040709.

[17] J. Zhu, H. Kim, H. Chen, R. Erickson, and D. Maksimovic, "High efficiency SiC traction inverter for electric vehicle applications," in *Proc. IEEE Appl. Power Electron. Conf. Expo. (APEC)*, Mar. 2018, pp. 1428–1433, doi: 10.1109/APEC.2018.8341204.

[18] D. Ronanki and S. S. Williamson, "Modular multilevel converters for transportation electrification: Challenges and opportunities," *IEEE Trans. Transport. Electrific.*, vol. 4, no. 2, pp. 399–407, Jun. 2018, doi: 10.1109/TTE.2018.2792330.

[19] J. I. Leon, S. Vazquez, and L. G. Franquelo, "Multilevel converters: Control and modulation techniques for their operation and industrial applications," *Proc. IEEE*, vol. 105, no. 11, pp. 2066–2081, Nov. 2017, doi: 10.1109/JPROC.2017.2726583.

[20] M. Schweizer and J. W. Kolar, "Design and implementation of a highly efficient three-level T-type converter for low-voltage applications," *IEEE Trans. Power Electron.*, vol. 28, no. 2, pp. 899–907, Feb. 2013, doi: 10.1109/TPEL.2012.2203151.

[21] D. Dwivedi, I. Roy, and K. A. Chinmaya, "Investigation of three-level dual output T-type NPC for EV application," in *Proc. Int. Conf. Smart Energy Syst. Technol. (SEST)*, Sep. 2022, pp. 1–6, doi: 10.1109/SEST53650.2022.9898482.

[22] S. Xu, J. Zhang, and J. Hang, "Investigation of a fault-tolerant three-level T-type inverter system," *IEEE Trans. Ind. Appl.*, vol. 53, no. 5, pp. 4613–4623, Sep. 2017, doi: 10.1109/TIA.2017.2697844.

[23] K. Ma and F. Blaabjerg, "Modulation methods for neutral-point-clamped wind power converter achieving loss and thermal redistribution under low-voltage ride-through," *IEEE Trans. Ind. Electron.*, vol. 61, no. 2, pp. 835–845, Feb. 2014, doi: 10.1109/TIE.2013.2254099.

[24] U. Choi and K. B. Lee, "Space vector modulation strategy for neutral-point voltage balancing in three-level inverter systems," *IET Power Electron.*, vol. 6, no. 7, pp. 1390–1398, Aug. 2013, doi: 10.1049/iet-pel.2012.0597.

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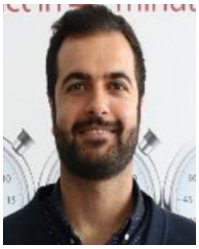

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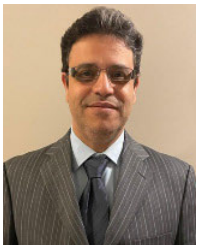

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