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RESEARCH ARTICLE

A ZVZCS Full-Bridge Converter Suitable for Renewable Energy-Based MVDC Collection System

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ABSTRACT A zero-voltage zero-current-switching (ZVZCS) full-bridge DC-DC converter, based on a dual transformer with two output filter capacitors, is proposed in this paper. The proposed topology is suitable for application in renewable energy at medium voltage, integrated with a DC collection system. To realize voltage and power regulation for the converter, pulse width modulation (PWM) is employed with a fixed duty cycle for the main switches. Through careful design of the turns ratio of the main transformer, most of the power under full load range is delivered by the main full-bridge circuit, which also achieves zero-voltage switching (ZVS). This significantly reduces the switching losses. A small portion of the total power is delivered by the auxiliary circuit that realizes ZVZCS. Therefore, the turns ratio of the auxiliary transformer can be optimized such that the efficiency of the proposed converter can be improved. The optimzation is discussed in detail, along with the design parameters of the proposed converter. A prototype of 200V-2kV/3kW has been developed to verify the simulation results and validate the working of the proposed scheme.

INDEX TERMS Full-bridge converter, medium voltage direct current (MVDC), zero voltage zero current switching (ZVZCS), high power DC-DC converter, energy efficient.

I. INTRODUCTION

The impact of gas emissions and pollution on the environment is alarmingly increasing, due to which the renewable energy sources have been attracting the attention of researchers all around the world. Renewables, such as offshore wind farms and large solar photovoltaic (PV) systems, are mainly connected at the grid stations on a medium voltage level, and then stepped up to high voltages, for the bulk transmission and distribution of electrical power [1], [2].

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While comparing the medium voltage AC (MVAC) and medium voltage DC (MVDC) voltages for large-scale integration of renewable energy sources, it can be seen that MVDC has significant advantages over MVAC. These advantages include higher efficiency, increased stability, lower system weight, low cost and absence of reactive power [3], [4]. Hence, for the large scale integration of renewable energy sources, MVDC technology is recommended. Furthermore, the renewable energy sources output DC power, which makes it easier to integrate multiple sources with the MVDC collection system. This system is free from the problems of frequency stability and reactive power compensation.

Therefore, this DC collection system is the future trend in power systems.

Different types of high-gain power electronic DC-DC converters have been proposed in literature. Non-isolated power electronic DC-DC converters have been reported in [5] and [6] for MVDC systems, offering advantages such as lower power rating. A switched-capacitor DC-DC converter has been reported in [7], which provides low power rating and output capacitance. A high efficiency and low switching loss converter has been observed in [8], which utilizes a soft-switching topology for its resonant switched-capacitor power electronic converter. However, the main drawback of using these non-isolated power electronic DC-DC converters, is the use of passive components, which result in power losses and high voltage stresses, when used for high voltage applications.

The isolation between the power electronic DC-DC converters can be achieved by using a frequency transformer, depending upon the voltage levels, such as medium-to-high. As a result of this galvanic isolation, the required protection in renewable energy sources is reduced, and the need for high-voltage switches is eliminated. Therefore, the isolated power electronic DC-DC converters have been widely chosen for high power applications, such as phase-shift full-bridge converters [9], [10], [11], LCC series-parallel resonant converters [12], [13], bridge converter of single active type [14], [15] and three phase dual active bridge DC-DC converter [16]. The aforementioned converters are constructed by the full-bridge structure for high-power applications.

For these full-bridge converter topologies, there are two techniques which are used to achieve soft-switching. They reduce the power and switching losses in order to achieve a high gain. The first technique is the ZVS [11], [17], [18]. The second technique is ZVZCS [19], [20]. MOSFETs have a high parasitic capacitance, due to which ZVS is most appropriate [13]. Due to their limited current and voltage ratings, MOSFETs are usually employed in low power applications. On the other hand, IGBTs offer high current and voltage ratings in comparison with MOSFETs, and thus are becoming more prevalent for high power applications. Nonetheless, the IGBTs suffer from tail current effect [21], [22].

The tail current effect can be minimized by the zero-current switching (ZCS) approach, as it reduces the turn-off switching loss [23], [24]. However, to achieve ZCS, the current has to reach zero before the commutation takes place. This is achieved by either the resonance mode [25] or through the current reset mode [26]. The auxiliary circuits of [27] and [28] have achieved the resonance mode by altering the structure of the converter. The resonance techniques, as used in the LCC resonance type, is beneficial to successfully achieve ZCS, and the output voltage can be regulated by controlling the frequency of the switch [29].

The main drawback of these auxiliary circuits is that the inductive filter and electromagnetic compatibility design becomes complex as variable switching frequency is being used [29], [30]. The single active bridge converter in [15] employs interleaving currents to reduce the output current ripple. The main drawback of this method is that the conversion efficiency is reduced due to large turn-off currents of the switches. The three phase dual active bridge converter proposed in [16], presented a soft-switching analysis on a large range of operation. However, the switches have to withstand high voltage stresses, which makes it less suitable for high voltage applications. The researchers in [31] have presented a topology using full-bridge cells and a dual transformer, for the main IGBT switches while achieving ZCS. However, the transformer and conduction loss increased as a result of the high amplitude triangular current. As a result, the inductive filter design becomes complex and costly to fabricate. All these limitations greatly impact the efficiency, practicality and feasibility of the converter.

In this paper, a full-bridge ZVZCS DC-DC converter based on a dual transformer with two output filter capacitors is proposed, particularly suitable for renewable energy of medium voltage DC collection system. Pulse width modulation (PWM) is adopted in the auxiliary circuit to realize power and voltage regulation of the whole converter. This allows for the basic full-bridge four switches to operate with the fixed duty cycle, which has the advantages of simple control. From optimization, the turns ratio of the primary transformer and the primary full-bridge converter can transfer significant power, and concurrently achieve ZCS, within the full load range. This remarkably reduces the switching losses. In addition, the turns ratio of the secondary transformer can be optimized to further reduce the converter losses, and improve the conversion efficiency. Moreover, the converter adopts output capacitive filtering for medium and high output voltages, and avoids using large inductance and high voltages.

This paper is organized as follows. Section II presents the circuit design and the operating principle of the proposed converter. The parameter design is reported in Section III. Section IV presents the simulation analysis to validate the design of the proposed converter. To validate the simulation results and effectiveness of the proposed topology. Experimental testing has been performed on a hardware prototype and the results are reported in Section V. Section VI summarizes the findings of this paper.

II. CIRCUIT DESIGN AND OPERATION PRINCIPLE

The full-bridge converter structure is employed to accommodate IGBTs for high power applications. To achieve high efficiency at high power levels, ZVZCS can be realized for the switches, such that it will operate with a 50% fixed duty cycle, without the requirement of additional control circuitry. This is adopted in the discontinuous conduction mode (DCM), which is usually employed in resonant transformers and traction systems. However, its main drawback is that this mode is unable to sustain in high power applications. To eliminate the aforementioned drawback, an auxiliary circuit is realized in Fig. 1, such that its control will allow the IGBTs to operate

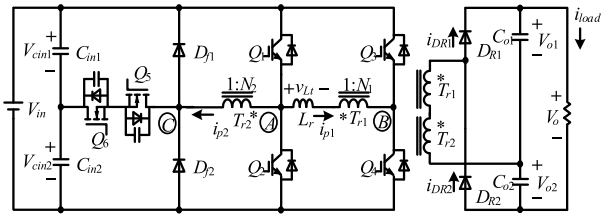


FIGURE 1. Proposed converter.

in DCM, where both the currents and voltages will decline to zero. By adjusting the transformer turns ratios, the current can be set such that larger current flows through the main switches and a smaller current flows through the auxiliary switches, which results in smaller control current and low switching losses.

A ZVZCS full-bridge converter is proposed, according to the above analysis. The proposed converter is responsible for ZVZCS operation, and is shown in Fig. 1. The full-bridge circuit is a combination of four main IGBT switches Q_1-Q_4, an inductor L_r and a transformer T_{r1}, with a turns ratio N_1. The auxiliary circuit consists of two MOSFET switches Q_5 and Q_6, driving capacitors C_{in1} and C_{in2}, diodes for freewheeling operations D_{f1} and D_{f2}, and a transformer T_{r2}, with a turns ratio N_2. It can be observed from Fig. 1 that both the secondary terminals of the transformers are connected. This is done to achieve an input of voltage-doubler rectifier circuit, such that the current remains the same. The distribution of power is such that approximately 90% power is delivered by the full-bridge converter and the remaining power is delivered by the auxiliary circuit.

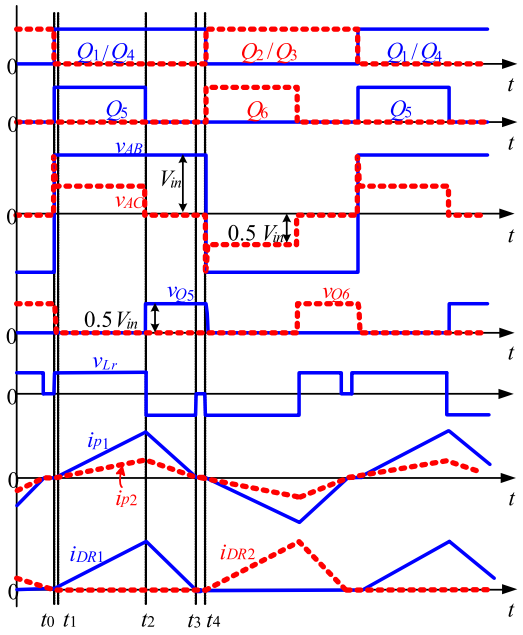


FIGURE 2. Key waveforms of the proposed converter.

Fig. 2 shows the key waveforms of the proposed converter. The gating pulse alternates for the switches Q_1,Q_4 and Q_2,Q_3, with a fixed duty cycle of 50% and adequate dead time. The switches Q_1/Q_4 and Q_2/Q_3 are out of phase. For the switches Q_5,Q_6, PWM based control is used, which acts on the leading edges of Q_1,Q_4. The output voltages of the proposed converter are controlled by the duty pulses of Q_5,Q_6. The following assumptions are in place for the analyses:

1) All the semiconductor devices being used are considered as ideal devices.
2) The input capacitors C_{in1},C_{in2} are kept of the same value which results in $V_{cin1} = V_{cin2} = V_{in}/2$.
3) The filter capacitors C_{o1},C_{o2} are kept of same large value which helps the output voltage reach steady state such that $V_{o1} = V_{o2} = V_o/2$.
4) The leakage inductance of the auxiliary transformer T_{r2} is deemed negligible due to small value.

For simplicity, only the half-cycle of the proposed circuit will be discussed. The four operation modes of the converter are shown in Fig. 3. The new cycle of switching starts at time t_0. At the instant of t_0, the switches Q_1,Q_4,Q_5 are turned-ON and Q_2,Q_3 are turned-OFF. No current flows through any of the switches before the starting time instant t_0. The switches Q_1,Q_4 are turned-ON with ZCS and Q_2,Q_3 are turned-OFF with ZCS. Furthermore, the voltage across Q_5 is zero, and thus it is turned-ON with ZVZCS, whereas the voltage across Q_6 in $V_{in}/2$. The complete analysis is presented as follows:

Mode 1) This mode operates from t_0 to t_1. The primary current i_{p1} from T_{r1} flows through Q_1,Q_4,L_r,T_{r1} and C_{in1}, which results in $v_{AB} = V_{in}$. Similarly, the primary current i_{p2} from T_{r2} flows through the windings of Q_1,Q_4,Q_5,T_{r2}, the parasitic capacitance of Q_6 and C_{in1}. At the instant t_0, the voltages across Q_6 discharges from $0.5V_{in}$ to zero, which results in $v_{AC} = 0.5V_{in}$. Fig. 3(a) shows that current i_{p1} flows through Q_1,L_r,T_{r1} and Q_4, while i_{p2} flows through T_{r2},Q_5 and Q_1. Thus, the current flowing through the switches Q_1,Q_4 is the sum of both i_{p1},i_{p2}.

Mode 2) This mode operates from t_1 to t_2. Due to the voltage across Q_6 is reduced to zero in the previous mode at instant t_1, the current i_{p2} also flows through the body diode of the switch Q_6. This results in the similar path taken by i_{p1}. This causes a linear increase in the current through L_r. The point voltages at this instant are the same as in Mode-1 i.e., $v_{AB} = V_{in}$ and $v_{AC} = 0.5V_{in}$. The primary current i_{p2} from T_{r2} flows through Q_1,Q_4,Q_5 and C_{in1}. The voltages at the secondary terminal of T_{r1} is $0.5(V_o - N_2V_{in})$ and that of T_{r2} is $0.5V_{in}N_2$. For proper working of the circuit in this mode, v_{Lr} much be greater than zero. This results in linear increments in i_{p1}, i_{p2}, i_{DR1} and v_{p1} whereas v_{p2} decreases in a nonlinear manner as shows in Fig. 4. The current i_{p2} now flows through the anti-parallel diode of Q_6. Fig. 3(b) shows the current flowing through the switches Q_1,Q_4 as the sum of both i_{p1},i_{p2}.

$$V_{Lr} = V_{in} + 0.5N_2V_{in}/N_1 - V_o/2N_1 \quad (1)$$

$$i_{p1}(t) = \frac{V_{in} + 0.5N_2V_{in}/N_1 - V_o/(2N_1)}{L_r}(t - t_0) \quad (2)$$

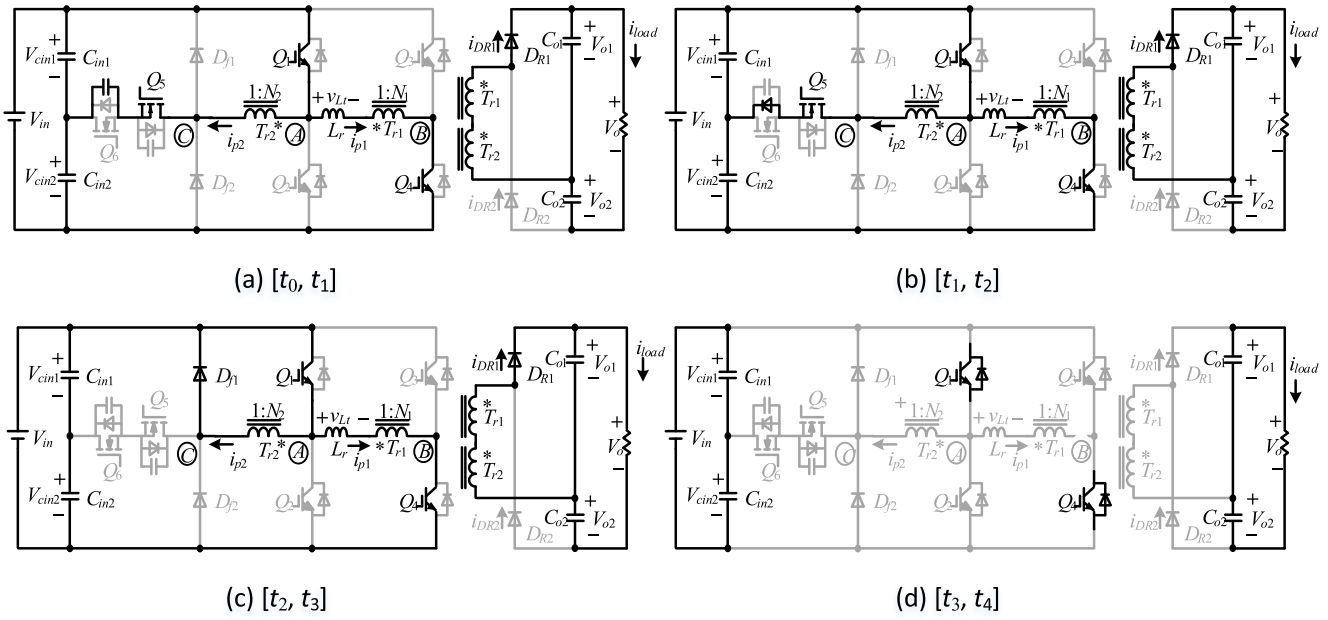


FIGURE 3. Circuit paths of the four modes of operation of the proposed converter.

$$i_{p2}(t) = i_{p1}(t)\, N_2/N_1 \tag{3}$$
$$i_{DR1}(t) = i_{p1}(t)\, /N_1 \tag{4}$$

Mode 3) This mode operates from t_2 to t_3. The switch Q_5 is turned-OFF with ZCS. The current i_{p2} which was flowing through the body diode of Q_6, now starts to charge the parasitic capacitance of Q_5, resulting in a shorter charge time, which is thus negligible. The voltages across Q_5 approaches $0.5V_{in}$, thus causing the current i_{p2} to now flow through Q_1 and D_{f1}. There is no current flow through the switches Q_5,Q_6 which results in $v_{AC} = 0$

$$i_{Lr} = V_{in} - V_o/(2N_1) \tag{5}$$

For proper working of this mode, v_{Lr} must be smaller than zero, which causes a linear decay in the currents i_{p1},i_{p2},i_{DR1}, given as:

$$i_{p1}(t) = \frac{V_{in} + \frac{N_2 V_{in} - V_o}{2N_1}}{L_r}\frac{D}{T_s} + \frac{V_{in} - \frac{V_o}{2N_1}}{L_r}(t - t_1) \tag{6}$$
$$i_{DR1}(t) = i_{p1}(t)\, /N_1 \tag{7}$$
$$i_{p2}(t) = i_{p1}(t)\, N_2/N_1 \tag{8}$$

Here, the duty ratio for the switches Q_5,Q_6 is denoted by D. The switching time period is given by T_s. Fig. 3(c) shows the current flowing the switch Q_4, as the sum of both i_{p1},i_{p2}.

Mode 4) This mode operates from t_3 to t_4. Through proper design on L_r,N_1,N_2, the currents i_{p1},i_{p2},i_{DR1} decrease to zero at the instant t_3. The diodes D_{f1},D_{R1} are turned-OFF with ZCS. The magnitude of the reflected voltage is smaller than the rectified voltage such that $N_1 V_{in} - N_2 < 0.2V_0$. The switches Q_1,Q_4 are turned-ON in this mode but no current flows through them. The load is supplied by i_{p1},i_{p2},i_{DR1},C_{o1} and C_{o2}. Fig. 3(d) shows the current path of Mode-4.

The instant t_4 marks the end of the first half switching cycle and at the same time the start of the second half switching cycle. Now, the switches Q_2,Q_3,Q_6 are turned-ON with ZCS and Q_1,Q_4 are turned-OFF with ZCS, as the L_t is responsible for the limiting of the current rise. Due to the voltage across the switch Q_6 being zero from Mode-3 to Mode-4, it is thus turned-ON with ZVZCS.

A fixed gating sequence method has been employed for the switches Q_1 Q_4. However, they can also be operated with PWM such that at instant t_3, the switches Q_1,Q_4 can be turned-OFF. As there is no current flowing through these switches, the PWM based control will not affect the operation and working of the proposed converter. The main drawback of employing the PWM based control for switches Q_1 Q_4 is that a current sensor is required to verify ZCS switching to note the exact time instant of t_3. Hence, the PWM based control is not selected for the first four switches. To summarize, the switches Q_1 Q_4 need to withstand V_{in} so that they can be turned-ON and OFF with ZCS. The switches Q_5,Q_6 need to withstand $0.5V_{in}$ to be turned-ON with ZVZCS and turned-OFF with ZVS. Table 1 presents the switching characteristics of the switches and diodes considered in the above mentioned analysis.

TABLE 1. Voltage Stress and Switching Characteristics.

	Q_1 Q_4	Q_5,Q_6	D_{f1},D_{f2}	D_{R1},D_{R2}
Turn-ON	ZCS	ZVZCS	—	—
Turn-OFF	ZCS	ZVS	ZCS	ZCS
Voltage Stress	V_{in}	$0.5V_{in}$	V_{in}	V_o

III. PARAMETER DESIGN

The specifications of the proposed converter for this experimental research is presented in Table 2.

TABLE 2. Specifications.

Input Voltage V_{in}	1.5 kV
Output Voltage V_o	15 kV
Rated Power P_N	1 MW
Switching Frequency f_s	1 kHz

A. TURNS RATIO

The turns ratio is an important design parameter for every industrial application. The turns ratio of the transformer must be sized such that the full-bridge part provides most of the power, and the auxiliary circuit provides the remaining power. To keep the discussion simple, only the first half-cycle will be discussed to demonstrate the effect of the turns ratio on the distribution of power between the two parts of the circuit. Assuming that the transmission efficiency of the proposed converter is 100%, the total power P_{tot} of $[t_0,t_4]$ can be expressed as:

$$P_{tot} = \frac{2}{T_s}\frac{V_o}{2}\int_{t_0}^{t_3} i_{DR1}dt = \frac{V_o}{T_s}\int_{t_0}^{t_2} i_{DR1}dt \tag{9}$$

During $[t_0,t_4]$, the power transferred by the T_{r1} is expressed as:

$$P_m = \frac{2}{T_s}V_{in}\int_{t_0}^{t_3} i_{p1}dt = \frac{2V_{in}}{T_s}\int_{t_0}^{t_2} i_{p1}dt \tag{10}$$

From (3) and (7), P_m also can be expressed as:

$$P_m = \frac{2V_{in}}{T_s}\int_{t_0}^{t_2} N_1 i_{DR1}dt = \frac{2N_1V_{in}}{T_s}\int_{t_0}^{t_2} i_{DR1}dt \tag{11}$$

Combining (9) and (11), one can obtain

$$\frac{P_m}{P_{tot}} = \frac{2N_1V_{in}}{V_o} \tag{12}$$

The power transferred by the auxiliary circuit as a result of the law of conservation of energy is expressed by the following:

$$P_a = P_{tot} - P_m \tag{13}$$

The power distribution is given as follows from (12) and (13):

$$\frac{P_m}{P_a} = \frac{P_m}{P_{tot}-P_m} = \frac{2N_1V_{in}}{V_o - 2N_1V_{in}} \tag{14}$$

The ratio of P_m/P_a is estimated once N_1 and the voltages are calculated. Fig. 4 shows the power ratios and their specifications. It can be observed that with the increase in N_1, the ratio P_{in}/P_{tot} increases and the ratio P_a/P_{tot} decreases. Therefore, this is clear indication that the value of N_1 is the deciding factor for the power distribution between the full-bridge and the auxiliary circuit. Furthermore, the value of N_1 must be large such that it can process greater power for the full-bridge circuit as compared to the auxiliary circuit. From Fig 4, if the value of N_1 is set to be 4.5, then the ratio of $P_{in}/P_{tot} = 90\%$, $P_a/P_{tot} = 10\%$ and $P_m/P_a = 9:1$. The rise time of this half-cycle is greater than that of the fall time from the Fig 2, and thus the time ratio r_t of the rise time to fall time can be either smaller, larger or equal to 1, as determined

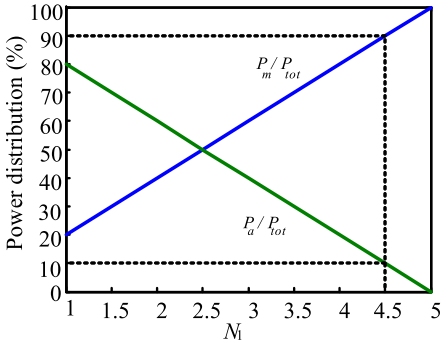


FIGURE 4. Power distribution versus N_1.

from N_2. From (15) and the law of volt-second balance of the inductor, the value of r_t is given by:

$$r_t = \frac{t_1 - t_0}{t_2 - t_1} = \frac{V_o/2 - N_1V_{in}}{N_1V_{in} + 0.5N_2V_{in} - V_o/2} \tag{15}$$

This equation can be rearranged to get the following:

$$N_2 = \frac{(V_o - 2N_1V_{in})(1 + r_t)}{V_{in}r_t} \tag{16}$$

As we have assumed the value of N_1 to be 4.5, then from (16), the curve of r_t versus N_2 is given in Fig. 5. It can be observed that with the decrease of r_t, the value of N_2 increases. Therefore, this shows the effect of the value of N_2 on the power loss of the converter.

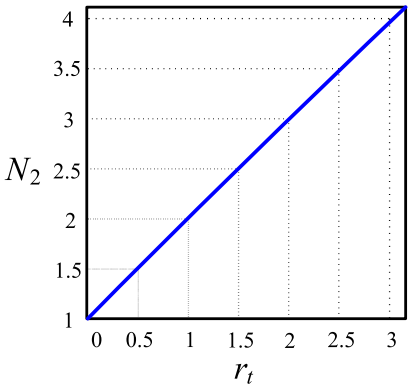


FIGURE 5. Curve of r_t versus N_2 when $N_1 = 4.5$.

B. INDUCTOR 'L_R'

The use of a high-voltage inductor must be minimized along with decreasing the low-voltage inductance. The total of the rise time and fall time equals $T_s/2$. These times are expressed as:

$$T_r = t_1 - t_0 = T_s r_t/(2 + 2r_t) \tag{17}$$

$$T_f = t_2 - t_1 = T_s/(2 + 2r_t) \tag{18}$$

The inductance can be expressed from (2) and (17) as:

$$L_r = T_s\frac{(N_1V_{in} + \frac{1}{2}N_2V_{in} - \frac{V_o}{2})(V_o - 2N_1V_{in})}{2N_1N_2V_{in}I_{peak}} \tag{19}$$

where I_{peak} represents the peak current of i_{p1}, at the rated power. For proper operation of the converter, the value of the inductor must be kept smaller than the value calculated in (19).

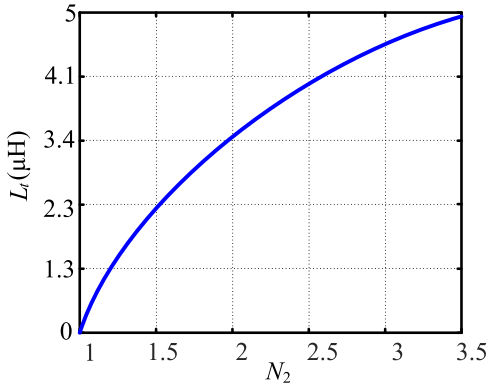


FIGURE 6. Relationship of L_t and N_2 when $N_1 = 4.5$.

The relationship curve of L_r and N_2 is given in Fig. 6, from (19). It can be observed that the inductance increases with increase in N_2.

C. OUTPUT FILTER CAPACITORS 'C_{O1} & 'C_{O2}'

The voltage-doubler rectifier configuration is employed to reduce the turns ratio of the main transformer, and the output filter capacitors are employed to reduce the high voltage ripples caused as a result of high current ripples. The charging stage of C_{o1} is represented by "U'', such that $i_{Co1} = i_{DR1} - I_{load} > 0$ and the discharging state is represented by "D'', such that $i_{Co1} < 0$. This causes the areas "U'' equal to "D'' at the steady state condition. The load current can be expressed as:

$$I_{load} = \frac{P_N}{V_o} = \frac{1}{T_s}\int_{t_0}^{t_3} i_{DR1}dt = \frac{1}{4}\frac{I_{peak}}{N_1} \tag{20}$$

where the peak value of i_{DR1} is given by the ratio I_{peak}/N_1. From (17) and (20), it is estimated that the time interval for "U'' is $3T_s/8$ for any value of r_t. From this estimation, the value of the peak-to-peak voltage ripple is given as:

$$\Delta V_{pp} = \frac{1}{C_{o1}}\left(\frac{I_{peak}/N_1 - I_{load}}{2}\right)\frac{3Ts}{8} \tag{21}$$

Both (20) and (21) are combined to give the values of the output filter capacitors as:

$$C_{o1} = C_{o2} = \frac{9}{64}\frac{I_{peak}}{N_1 \Delta V_{pp} f_s} \tag{22}$$

D. DESIGN EXAMPLE

This subsection provides a step by step design example, which is reported as Case A in the next section of Simulation Analysis. First of all, the input voltage V_{in} and output voltage V_o is determined to be 1.5 kV and 15 kV, respectively. The switching frequency f_s of the converter is 10 kHz, and the rated power is 1 MW. The time ratio r_t is designed according to (15), which is selected as 0.5. From the previous subsection and Fig 4, N_1 is set to be 4.5 and N_2 is selected according to (16), which turns out to be 1.5. The load current I_{load} is determined from (20) based upon the rated power and the output voltage, and is 67 A. Equation (20) can also be used to determine the peak current I_{peak} based upon the load current value, and is calculated to be 1.2 kA. The inductor L_r value is calculated from (19), and is 2.315 μH. For estimating the output filter capacitors, the peak-to-peak voltage ripple ΔV_{pp} is calculated from (21), which is nearly 1% of the output voltage, and is 150 V. Finally, the output capacitors C_{o1} and C_{o2} are estimated to be 25 μF from (22).

E. COMPARISON WITH OTHER CONVERTERS

A number of dual transformer based converter topologies are proposed in the literature. In order to demonstrate the excellent performance and effectiveness of the proposed converter, a comparison of the existing literature with the proposed converter is provided in Table 3.

IV. SIMULATION ANALYSIS

To verify the operating principle of the proposed converter, and estimating the effect of the turns ratio N_2 on the losses and the current magnitude, a simulation is performed using PLECS software. Three cases A,B and C have been developed for the simulation analysis with different parameters. These key parameters used in the simulation are listed in Table 4. For all the cases, the value of the turns ratio N_2 is kept different to analyze its effect on the inductor L_r and capacitors C_{o1} and C_{o2}, along with the other parameters to verify ZVZCS. The theoretical power P_N is slightly larger than the real power P_o.

The turns ratio of N_1 is the main determinant in the power transfer between the main full-bridge and the auxiliary full-bridge circuits. However, the turns ratio N_2 has significant impact on the overall power losses of the converter. To determine the affect of the turns ratio N_2, three cases A ($N_2 = 1.5$, $n = 0.5$), B ($N_2 = 1.25$, $n = 0.25$) and C ($N_2 = 1.1$, $n = 0.1$) have been considered, while keeping the turns ratio $N_1 = 4.5$ similar for all the cases, to keep the power distribution same for any value of N_2. Three different current waveforms are represented by these cases, which are $T_r < T_f$, $T_r = T_f$ and $T_r > T_f$, respectively. For the three cases, the value of the inductance L_r can be determined from (19) for different values of N_2. From (20), the average and peak values of i_{p1} are same for the three cases. As the currents flowing through the secondary windings of both the transformers is identical, the primary current i_{p2} and the currents flowing through Q_5,Q_6 are directly proportional to the value of N_2. The currents through Q_3,Q_4 are the sum of both i_{p1},i_{p2}, therefore, they also vary directly with the value of N_2. To ensure the working of the converter in DCM, the total power P_{tot} of the converter is taken lower than the rated power of 1 MW.

The Fig. 7 shows the simulation waveforms of v_{AB},v_{AC},v_{Lr},i_{p1} and i_{p2} for the three cases. The Fig. 8 shows the waveforms of i_{p1},i_{p2} and current through Q_1 for the three

TABLE 3. Comparison of proposed converter with similar topologies in literature.

	[24]	[19]	[32]	[33]	[28]	Proposed
Switching Frequency	5 kHz	10 kHz	15 kHz	20 kHz	10 kHz	10 kHz
No. of Switches	6	6	10	10	6	6
No. of Diodes	4	6	0	0	6	4
Rated Power	1.4 kW	1.4 kW	1.2 kW	0.3 kW	1.4 kW	3 kW
Soft-switching	ZVS & ZCS	ZVS & ZCS	ZVS	ZVS	ZVS & ZCS	ZVS & ZCS
Full-load Efficiency	97.3%	97.3%	96.5%	94%	97.2%	97%

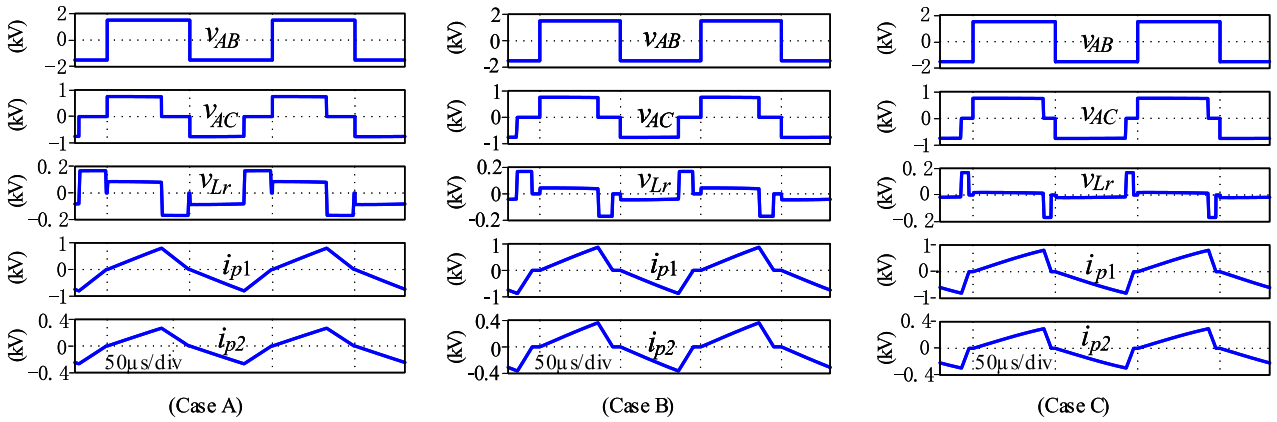


FIGURE 7. Simulation waveforms showing v_{AB},v_{AC},v_{Lr},i_{p1} and i_{p2} for the three cases.

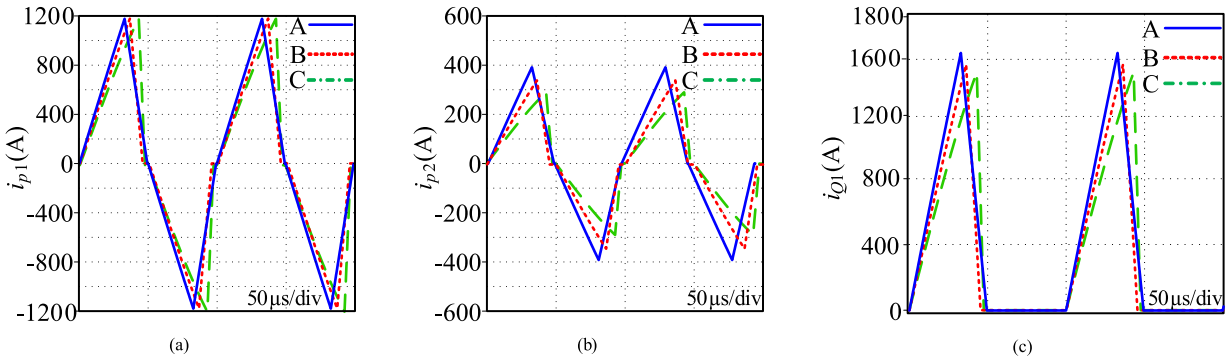
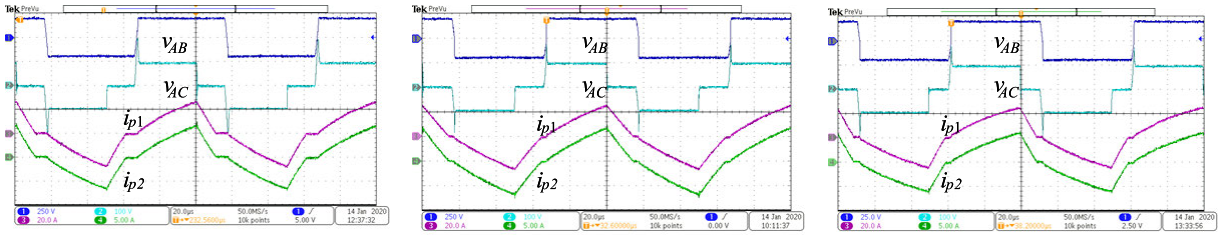


FIGURE 8. Simulation waveforms of the three cases. (a) i_{p1}, (b) i_{p2}, (c) Current flowing through switch Q_1.

TABLE 4. Simulation parameters.

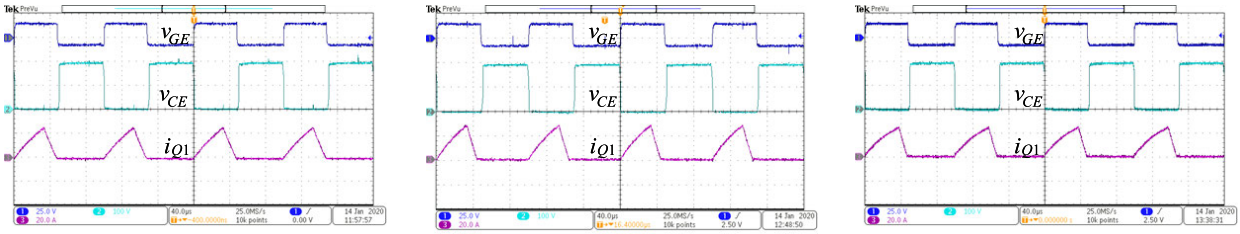
Parameters	A	B	C
Theoretical Power P_N	1 MW		
Input Voltage V_{in}	1.5 kV		
Output Voltage V_o	15 kV		
Switching Frequency f_s	1 kHz		
Time Ratio r_t	0.5	0.25	0.1
Turns Ratio N_1	4.5		
Turns Ratio N_2	1.5	1.25	1.1
Inductance L_r	2.315μH	1.389μH	0.631μH

cases. From Fig. 8(a), the primary current i_{p1} has the same average and peak values for different time ratio r_t. Thus, the losses in the switches Q_1,Q_2 are the same in all the three cases for different N_2. From Fig. 8(b), the values of i_{p2} are different for all the cases with significant differences in both the average and peak values. The conduction loss can be categorized as A>B>C, due to the fact that the turn-OFF currents of Q_5,Q_6 are equal to the peak current value of i_{p2}, thus implying that case C has the minimum conduction losses. From Fig. 8(c), it can be observed that the current through $Q_3(Q_4)$ is the sum of the currents through Q_2,$Q_6(Q_1$,$Q_5)$, where the smallest value current flows through $Q_3(Q_4)$. It can be observed from these three cases that the smaller the value of N_2, the smaller the average and peak current values through the switches Q_3 Q_6, which results in reduced switching and conduction



(Case A) (Case B) (Case C)

FIGURE 9. Experimental results of v_{AB}, v_{AC}, i_{p1} and i_{p2} for the three cases.



(Case A) (Case B) (Case C)

FIGURE 10. Experimental results of v_{GE}, v_{CE} and current of Q_1 for the three cases.

losses. One point to note is that ideal transformers have been used in the above simulation analysis without considering their losses. The main transformer processes same power, same turns ratio, same average and peak values for all the three cases. Therefore, the losses of the main transformer is approximately the same for all the three cases. The auxiliary transformer for all the three cases also processes the same power and current values, but in case C, it has a much smaller value of primary current than in cases A and B, which leads to the conclusion that the auxiliary transformer of case C is the most loss effective. To summarize the simulation results, the value of N_2 must be kept small such that the inductance required is also small and the conversion efficiency is high.

V. EXPERIMENTAL RESULTS

From the theoretical calculations and simulation analysis, and to verify the performance of the proposed scheme, low-power prototypes have been designed for the three cases. For the three cases, the value of N_1 has been kept the same and N_2 is different for each case. The semiconductor devices used in this experiment are presented in Table 5 and the parameters of the proposed converter for each respective case is mentioned in Table 6. As given from the simulation, to ensure the working of the converter in DCM, the output P_o is kept less than the rated power P_N. The transformers are built using toroidal ferrite cores from TDK (PE22 T96 × 20x70 and T72 × 20x48) suitable for high power applications and a EE ferrite core from TDK (PE22 EE70), is used for building the inductors. Litz wire is used for the windings of both the transformers and the inductor.

TABLE 5. Semiconductor devices.

Semiconductor	Type	Voltage/Current Stress
$Q_1 - Q_4$	FZ3600R17HP4	1700V/3600A
Q_5, Q_6	STW40N60M2	600V/34A
D_{f1}, D_{f2}	DD600N16K	1600V/600A
D_{R1}, D_{R2}	DD500S65K3	6500V/500A

TABLE 6. Experimental parameters.

Parameters	A	B	C
Theoretical Power P_N	3 kW		
Input Voltage V_{in}	200 V		
Output Voltage V_o	2 kV		
Switching Frequency f_s	10 kHz		
Time Ratio r_t	0.5	0.25	0.1
Turns Ratio N_1	4.5		
Turns Ratio N_2	1.5	1.25	1.1
Inductance L_r	13.72 μH	8.23 μH	3.741 μH

The currents of the primary side for both transformers and the waveforms of the voltages v_{AB},v_{AC} is presented in Fig. 9 for the three cases. The peak value of v_{ab} is 200 V, equal to V_{in}. A small spike can be observed in the waveform of v_{ac} at the start of each half switching cycle with an amplitude of $0.5V_{in}$. It can be observed from Fig. 9 that the peak current i_{p1} is the same in all three cases, thus representing the same amount of power due to same value of N_1. The value of primary current i_{p2} is greater in case A as compared to cases B and C, because the value of N_2 is smaller in cases B and C. Moreover, due to

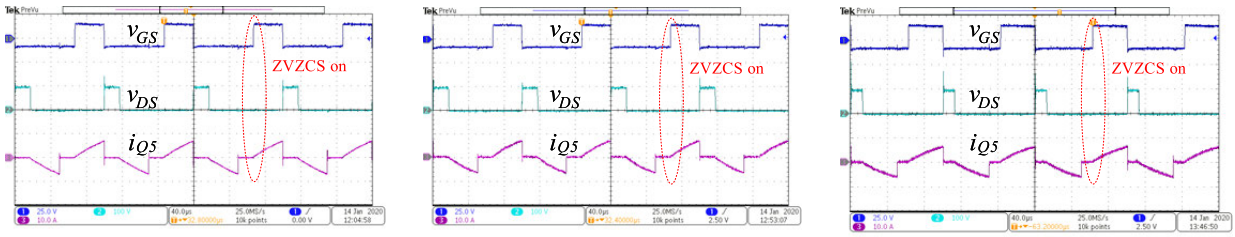


FIGURE 11. Experimental results of v_{GS}, v_{DS} and current of Q_5 for the three cases.

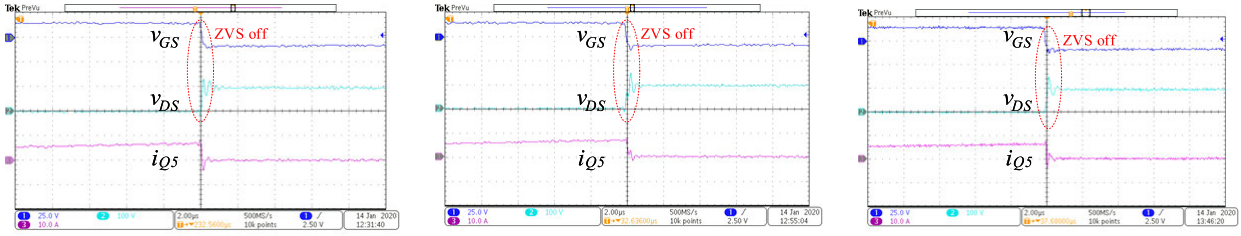


FIGURE 12. Zoomed in results of switch Q_5 turn-OFF for the three cases.

small N_2, the peak current value of i_{p2} is also small, which validates the theoretical and simulation analysis.

The waveforms of gate-emitter voltage v_{GE}, collector-emitter voltage v_{CE} and the collector current of the switch Q_1 is presented in Fig. 10. The switching of Q_1 is realized by ZCS for both turn-ON and turn-OFF. Due to the small magnetic inductance of T_{r1}, small current ripples are observed when the currents decay to their lowest values. At rated power, the peak current of Q_1 is greater than the magnetic current. The turn-OFF current of Q_5 is also greater than the magnetic current. Therefore, high conversion efficiency can be achieved while reducing the switching losses considerably. Soft-switching for all the switches is achieved due to DCM operation of the proposed converter, especially for light loads.

The current and voltage waveforms for the switch Q_5 is presented in Fig. 11. The peak voltage of the switch Q_5 with $0.5V_{in}$ is 100 V. Before the turn-OFF of Q_5, its voltage is zero and current has also decayed to zero. Therefore, ZVZCS is realized for the switch Q_5. When compared to Fig. 12, it can be observed that the peak current of the switch Q_5 is smaller in the cases B and C, as compared to case A, where the turn-OFF current equals the smaller current value. Hence, the case A has the least switching and conduction losses. A minimal parallel parasitic capacitance exists between the source and the drain for the auxiliary switches to realize turn-OFF by ZVS. The gate-source voltage v_{GS}, drain-source voltage v_{DS} and drain current i_{Q5} for switch Q_5 is presented in Fig. 12, which clearly shows that the switch Q_5 is turned-ON with ZVZCS and in the zoomed-IN part, turned-OFF with ZVS.

For the three cases, the conversion efficiencies are presented in Fig. 13. It can be observed that the conversion efficiency of the proposed converter is above 95.8%, for a wide range of load. The efficiency of case C is slightly more than that of cases A and B.

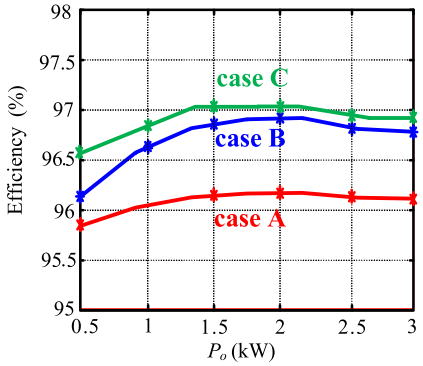


FIGURE 13. Efficiency curves for the three cases.

VI. CONCLUSION

A ZVZCS full-bridge DC-DC converter based on a dual transformer with two output capacitive filter working in DCM, has been proposed in this paper. The proposed converter contains four main switches, two auxiliary switches, one main and one auxiliary transformer. The current stress and power processed by the auxiliary switches are much lower and smaller than that of main switches, respectively. The turns ratio of the main transformer determines the power distribution between the two transformers. A full-bridge DC-DC converter is proposed based on ZCS approach, which realizes ZCS for all the main switches. As the voltage stresses in the auxiliary switches are lower than the main switches, MOSFETs can be employed for the auxiliary switches, which

can realize ZVZCS turn-ON. As a result, high efficiency can be obtained while significantly reducing the switching loss of the converter. The design parameters have been derived along with detailed discussion of the operation principles of the proposed PWM based full-bridge converter. Simulation results are in accordance with the derived operation principles and experimental results further verify the performance of the proposed converter. High experimental efficiency has been achieved over a wide load range.

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