IEEE Access
Multidisciplinary ⋮ Rapid Review ⋮ Open Access Journal

Received 19 January 2024, accepted 12 February 2024, date of publication 14 February 2024, date of current version 27 February 2024.

Digital Object Identifier 10.1109/ACCESS.2024.3366224

RESEARCH ARTICLE

Improvement of the Symmetry and Linearity of Synaptic Weight Update by Combining the InGaZnO Synaptic Transistor and Memristor

TAE JUN YANG[1], JUNG RAE CHO[1], HYUNKYU LEE[1], HEE JUN LEE[1], SEUNG JOO MYOUNG[1], DA YEON LEE[1], SUNG-JIN CHOI[1], JONG-HO BAE[1], (Member, IEEE), DONG MYONG KIM[1], (Member, IEEE), CHANGWOOK KIM[1], JIYONG WOO[2], (Associate Member, IEEE), AND DAE HWAN KIM[1], (Senior Member, IEEE)

[1]School of Electrical Engineering, Kookmin University, Seoul 02707, Republic of Korea
[2]School of Electronics Engineering, Kyungpook National University, Daegu 41566, Republic of Korea

Corresponding authors: Changwook Kim (ncwkim@kookmin.ac.kr), Jiyong Woo (jiyong.woo@knu.ac.kr), and Dae Hwan Kim (drlife@kookmin.ac.kr)

This work was supported in part by the National Research Foundation of Korea (NRF) Grant funded by the Korean Government (MSIT) under Grant RS-2023-00208661, and in part by the Institute of Information and Communications Technology Planning and Evaluation (IITP) Grant funded by the Korean Government (MSIT) under Grant 2021-0-01764-001. The work of Jiyong Woo was supported by the National Research and Development Program through NRF funded by the Ministry of Science and ICT under Grant RS-2023-00258227.

ABSTRACT Obtaining symmetrical and highly linear synapse weight update characteristics of analog resistive switching devices is critical for attaining high performance and energy efficiency of the neural network system. In this work, based on the two-terminal one transistor-one memristor (1T1M) block, the improvement of the symmetry and linearity of synaptic weight update is demonstrated by combining the InGaZnO synaptic transistor and memristor. Due to the symmetric and linear weight update characteristic, a pattern recognition accuracy of 88% is achieved after 50 epochs in the on-chip learning simulation of the hand-written digit images (MNIST) data set. The proposed 1T1M device saves the hardware burden and additional power consumption required to implement non-identical programming pulses.

INDEX TERMS InGaZnO thin-film transistors, analog resistive switching synapse, symmetric and linear synaptic weight update, synaptic transistor, memristor, neural network.

I. INTRODUCTION

Amorphous indium-gallium-zinc-oxide (a-IGZO) thin-film has been recently demonstrated as the promising material for either the active layer of thin-film transistor (TFT) [1], [2], [3], [4] or the resistive switching (RS) layer of analog RS synapse device [5], [6], [7]. On the other hand, in today's data-centric era, numerous patterns as unstructured data, such as images, voices, letters, and movement, need to be measured and classified. If a large amount of unstructured data has to be processed through the cloud server system, energy consumption will become uncontrollable, and the limitation of the bandwidth of data processing may lead to serious latency problems. Therefore, the need for an edge device with pre-trained learning results is emerging to infer vast amounts of unstructured data quickly and energy-efficiently. Here, symmetry and linearity are the most crucial figure of merits (FoMs) of analog RS synapses [8], [9], [10], [11]. For obtaining better FoMs for analog RS synapses, several programming voltage schemes for improving the linearity and symmetry have been investigated, such as pulse-pair scheme [12], pulse-width and amplitude modulation [13], [14], [15], [16], [17], [18], hybrid programming scheme [19], and codesign of cell structure and programming scheme [20].

The associate editor coordinating the review of this manuscript and approving it for publication was Sai-Weng Sin.

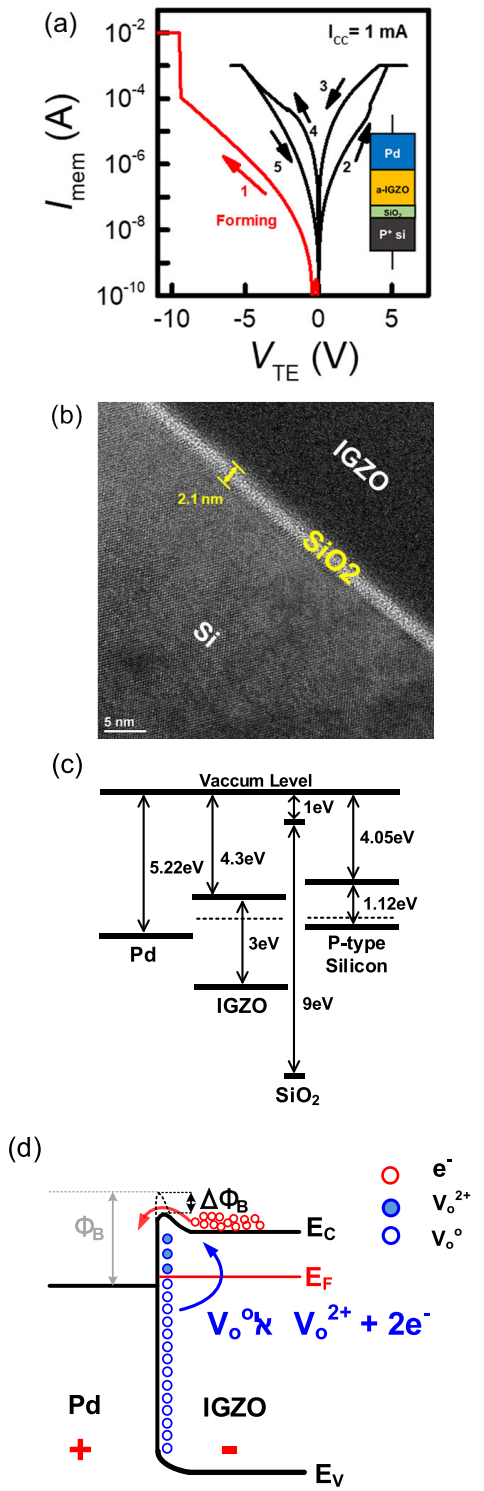

FIGURE 1. (a) $I-V$ characteristic and the device structure (inset) of Pd/IGZO/SiO_2/Si memristor. (b) Cross-section TEM image of Pd/IGZO/SiO_2/Si memristor. Energy band diagrams of the Pd/IGZO/SiO_2/Si memristor under (c) before junction and (d) SET (potentiation) conditions.

However, to implement non-identical pulses, additional complicated circuits are required, which increases the hardware burden. Indeed, a read-before-write method makes parallel operation unacceptable, and the complex circuitry significantly increases energy consumption and degrades the learning efficiency [8], [9], [10], [17]. Therefore, the simple two-terminal block of which synaptic weight update is symmetric and linear under the identical programming pulse is critical for the hardware implementation of efficient and reliable neural network applications.

In this work, the 1T1M (one-transistor one-memristor) block is proposed for a synaptic weight element by combining the a-IGZO synaptic transistor and memristor. The voltage applied to the 1T1M was divided into the introduced transistor and memristor. In particular, the threshold voltage (V_T) of the transistor was tuned by sequentially addressed pulses, so that the effective voltage across the memristor continued to increase or decrease even though the identical pulse scheme was used. This allowed synaptic weights to be updated linearly and symmetrically.

II. DEVICE STRUCTURE AND FABRICATION PROCESS

The a-IGZO-based memristor and TFT devices were fabricated on a SiO_2 (300 nm)/p^+-Si substrate. First, the IGZO memristor was fabricated. The 40-nm-thick p^+-Si was deposited as a bottom electrode (BE) using e-beam evaporation. After annealing in the oven at 110 °C for 15 minutes, the 60-nm-thick a-IGZO film was sputter-deposited at room temperature (RT) as the RS layer with a gas flow of $Ar/O_2 = 3{:}2$ sccm. Finally, the 30-nm-thick Pd was deposited and patterned as a top electrode (TE) using e-beam evaporation and lift-off. The area of the IGZO RS layer is 200 μm × 200 μm.

Next, the synaptic a-IGZO TFT fabrication process with bottom gate (BG) structure is as follows. The 30-nm-thick Cu was deposited and patterned as a BG electrode by the e-beam evaporation and lift-off process. Then, the 40-nm-thick Al_2O_3 as a gate insulator (GI) was deposited at a low temperature (LT) of 80 °C using atomic layer deposition (ALD) with $Al(CH_3)_3$ (trimethylaluminum; TMA) and H_2O as a precursor.

Subsequently, the 35-nm-thick a-IGZO was sputter-deposited at RT with 150 W rf power, a gas flow of $Ar{:}O_2 = 3{:}0.1$ sccm, and pressure of 5 mTorr, and was patterned as the TFT active layer. The 40-nm-thick Cu was then deposited and patterned as a source/drain (S/D) electrode by the e-beam evaporation and lift-off. The channel width (W) and length (L) of TFT are 50 μm and 50 μm.

III. RESULT AND DISCUSSION

RS characteristic of the Pd/IGZO/p^+-Si memristor is shown in Fig. 1(a), as the TE voltage (V_{TE}) versus the current flowing through memristor (I_{mem}) curve with the grounded BE. After forming with a negative bias, a gradual and reasonably symmetric RS behavior is observed at a compliance current (I_{CC}) = 1 mA. In Fig. 1(b), the cross-sectional transmission electron microscope (TEM) image of the IGZO/p^+-Si interface suggests that a thin SiO_2 layer (~2.1 nm) is grown during the annealing at 110 C° for 15 minutes.

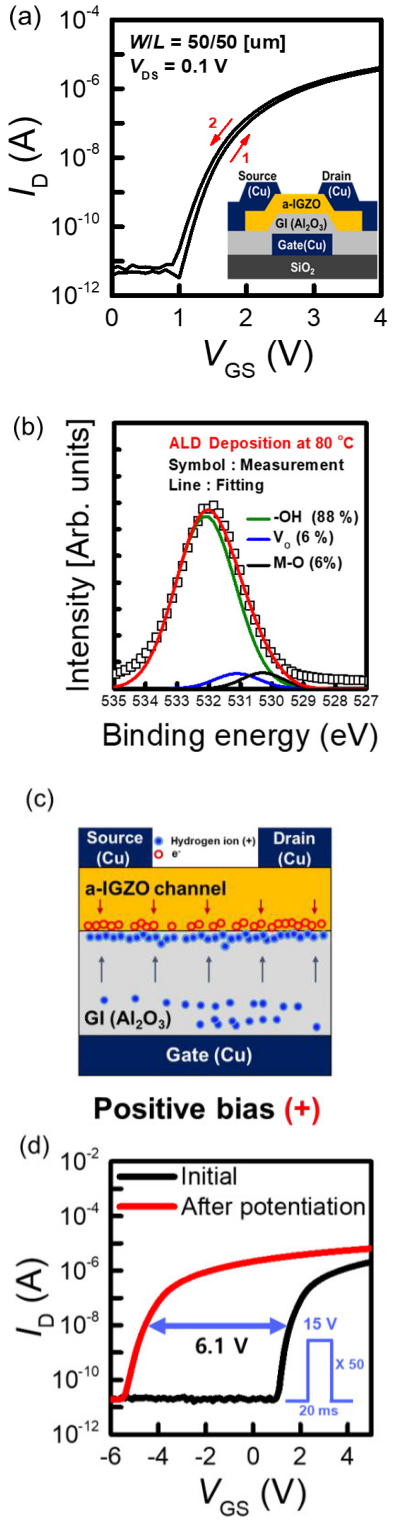

FIGURE 2. (a) Transfer characteristic and the BG TFT structure (inset) of a-IGZO synaptic TFT. (b) XPS spectra of the Al_2O_3 GI layer in a-IGZO TFT. (c) Schematic view of the a-IGZO synaptic TFT under a positive gate bias (potentiation) condition. (d) Transfer characteristics of the a-IGZO synaptic TFT under the initial and after applying 50 potentiation pulses.

Hence, the device structure is illustrated in Fig. 1(a) inset as the Pd/IGZO/SiO_2/p^+-Si memristor. Energy band diagrams of the Pd/IGZO/SiO_2/p^+-Si memristor under before

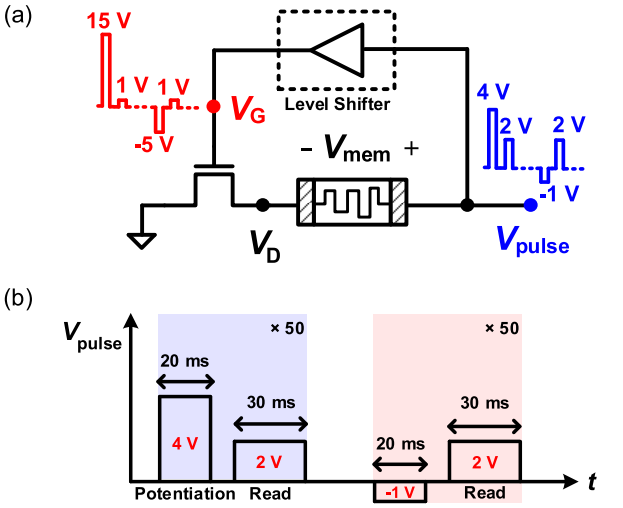

FIGURE 3. (a) Schematic view of the proposed 1T1M block. (b) The V_{pulse} conditions of P/D and readout pulses.

junction and SET (potentiation) conditions are shown in Fig. 1(c) and (d).

The memristive characteristic originates from the Schottky barrier (SB) between the Pd TE layer and IGZO RS layer. The SB height (Φ_B) is modulated by applying a potentiation/depression (P/D) pulse.

On the other hand, the transfer characteristic of synaptic IGZO TFT at a drain-to-source voltage (V_{DS}) = 0.1 V is shown in Fig. 2(a). The device structure is illustrated in Fig. 2(a) inset. The V_T and hysteresis of 1.6 V and −0.08 V are observed at the drain current (I_D) =10^{-8} A. In Fig. 2(b), the X-ray photoelectron spectroscopy (XPS) spectra of the Al_2O_3 GI layer in a-IGZO TFT suggests that the LT ALD-deposited Al_2O_3 layer contains a large number of hydrogens [21], which plays a role in synaptic behavior [22], [23].

As shown in Fig. 2(c), by applying positive gate bias, the migration of hydrogens in the Al_2O_3 GI layer toward the IGZO channel lowers V_T because these H^+ ions induce the channel to more accumulated. Transfer characteristics of the a-IGZO synaptic TFT under the initial and after applying 50 potentiation pulses (15 V for 20 ms as seen in the inset) are shown in Fig. 2(d). A negative V_T shift of 6.1 V is observed. It suggests that the migration of hydrogens toward and away from the IGZO channel by applying the P/D pulses lowers/heightens V_T, respectively.

Figure 3(a) shows the proposed 1T1M block, which combines the Pd/IGZO/SiO_2/p^+-Si memristor and the a-IGZO synaptic TFT through wiring connections. The amplitude and duration of P/D pulse are used as 4 V/ −1 V for 20 ms, and the memristor readout pulse of 2 V for 30 ms is used. They are applied to memristor as V_{pulse} as shown in Fig. 3(b). The TFT gate voltage (V_G) P/D and readout pulses can be synchronized with V_{pulse} by using a simple circuit, e.g., level shifter. In this work, instead of the level shifter, the synchronized V_{pulse} and V_G pulses are applied by using the Keithley 4200A-SCS

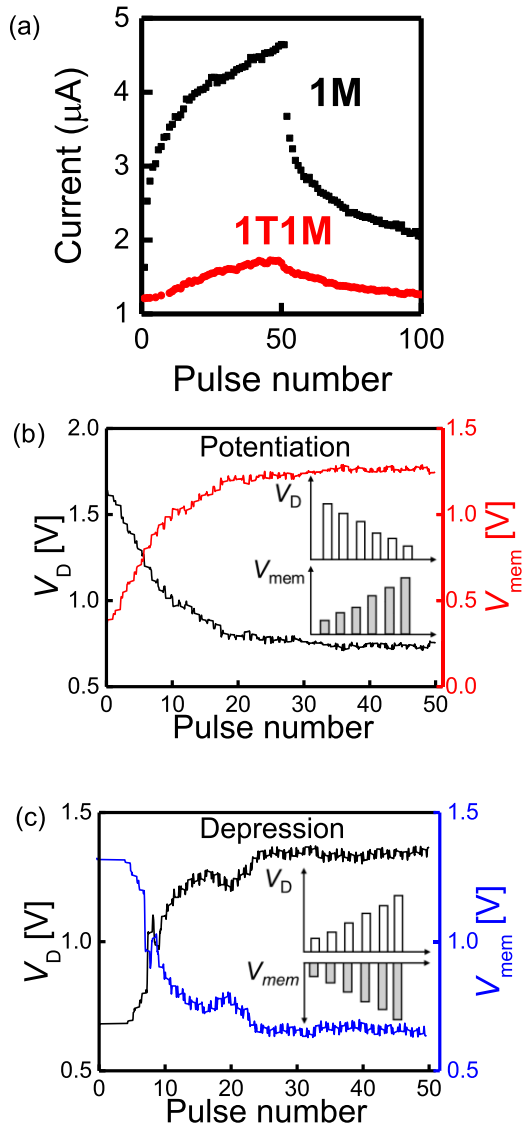

FIGURE 4. (a) Synaptic weight update characteristic of the 1T1M block compared to 1M. Measured V_D and V_{mem} during the consecutive 50 pulses in (b) potentiation (SET) and (c) depression (RESET) conditions. Inset illustrates the pattern of changes of V_{mem} and V_D with the increase in the number of programming pulses.

semiconductor parameter analyzer. The condition of V_G pulse can be optimized considering the characteristic of IGZO synaptic TFT, and in our case, the P/D pulse of 15 V/−5 V and the readout pulse of 1 V are used, as seen in Fig. 3(a). The I_{mem} is measured during the readout pulse.

Synaptic weight update characteristics of I_{mem} flowing through the stand-alone Pd/IGZO/SiO_2/p^+-Si memristor (1M) and that through 1T1M block are comparatively shown in Fig. 4(a), where 50 potentiation pulses followed by 50 depression pulses are applied as denoted by Fig. 3(b).

As shown in Fig. 4(a), the large current of the single memristor was initially increased by the first few pulses, and the current quickly saturated (see the "black" curve), resulting in non-linear synaptic behavior. In addition, during the depression, the current was found to be decreased abruptly as soon as a negative pulse was applied. The non-linear response of the current has been described by the lower pulse amplitude required to change the current in the memristor during the identical pulse. The switching mechanism of the memristor has been explained by interfacial barrier modulation. Therefore, the amount of vacancies needs to be increased as a function of applied pulse. However, as the resistance of the IGZO memristor was decreased, less voltage drop occurred and the pulses became ineffective at generating more vacancies. This caused current changes to saturate, making the synaptic response non-linear and asymmetric. These results imply that an incremental pulse scheme is preferred to achieve the desired synaptic behavior.

To mitigate this challenge, the synaptic TFT was additionally introduced to transfer progressively larger (or smaller) voltages to the memristor during potentiation (or depression), respectively. In this 1T1M configuration, where two elements are connected in series, the V_{pulse} is applied to the synaptic TFT first. When the synaptic TFT is turned on, most of the V_{pulse} is sent to the memristor. Note that the V_T of the synaptic TFT is adjusted to lower values, as the V_{pulse} is applied, as shown in Fig. 2d. In the next pulse cycle, the voltage drop across the synaptic TFT becomes smaller, which means that the magnitude of the voltage delivered to the memristor steadily increases. This resulted in improved linearity of the synaptic behavior (see the "red" curve), as shown in Fig. 4(a).

To numerically analyze this improvement in 1T1M configuration, the drain voltage (V_D) of synaptic TFT and the voltage across the memristor (V_{mem}) are monitored during the consecutive 50 P/D pulses, as shown in Fig. 4(b) and (c). In the 1T1M block, V_D can be calculated as follows:

$$V_D = \frac{R_{TFT}}{R_{mem} + R_{TFT}} \times V_{pulse} = \frac{1}{(R_{mem}/R_{TFT}) + 1} \times V_{pulse} \quad (1)$$

where R_{TFT} and R_{mem} are the resistances of TFT and memristor.

When the potentiation pulse is applied to the 1T1M block, both R_{TFT} and R_{mem} decrease by ΔR_{TFT} and ΔR_{mem}, respectively, with the increase in the number of potentiation pulses. At this time, V_D decreases and V_{mem} increases due to $\Delta R_{TFT} > \Delta R_{mem}$, as shown in Fig. 4(b). In contrast, when the depression pulse is applied, both R_{TFT} and R_{mem} increase by ΔR_{TFT} and ΔR_{mem}. Then, V_D increases, and V_{mem} decreases with the increase in the number of depression pulses, as shown in Fig. 4(c), due to $\Delta R_{TFT} < \Delta R_{mem}$. Insets of Fig. 4(b) and (c) illustrate the pattern of changes of V_{mem} and V_D with the increase in the number of P/D pulses. Therefore, the symmetry and linearity of 1T1M improve since the amplitude of V_{mem} increases during P/D programming. These results indicate that achieving a progressively tuned V_{mem} plays an important role in enhancing the synaptic behavior, which is why the synaptic TFT exhibiting tunable V_T was used in this study. Meanwhile, since the memristive characteristics were obtained by pulses with a width

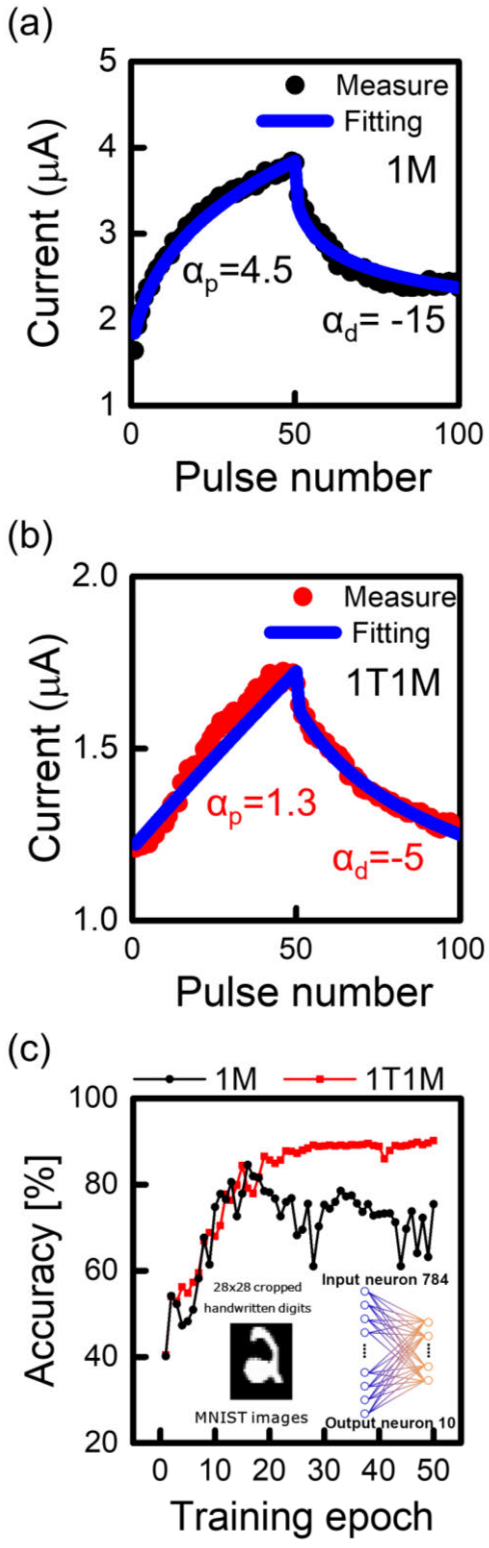

FIGURE 5. Synaptic weight update characteristics of (a) 1 M and (b) 1T1M blocks. (c) Comparison between 1M and 1T1M of MNIST pattern recognition accuracy.

of several tens of μs, improved synaptic behavior can be achieved by further reducing the duration of the P/D pulses to 20 μs in the 1T1M block. In this work, measurements were performed by external wiring connections between 1T and 1M, so unwanted voltage losses due to parasitic components may be involved. We thus used the relatively long pulse width (∼20 ms) to characterize 1T1M block to clarify the impact of the introduced 1T on the weight update. Direct integration is expected to eliminate this side effect, thereby allowing linearly controlled weight update driven by shorter pulses.

The symmetry and linearity of synaptic weight update characteristic of conductance G can be quantified as [24]:

$$G = \left\{\left(G_{\max}^{\alpha} - G_{\min}^{\alpha}\right) \times w + G_{\min}^{\alpha}\right\}^{1/\alpha} \quad (2)$$

where $G_{\max}$ and $G_{\min}$ are maximum and minimum conductance values, respectively, α is a nonlinearity factor that controls P/D, and w is the internal variable which ranges from 0 to 1.

Normalized synaptic weight update characteristics of 1M and 1T1M blocks are shown in Fig. 5(a) and (b). The α in potentiation (α_p) and that in depression operation (α_d) are 3 and −4.5 in 1M, while they are 1.3 and −1.6 in 1T1M block.

Furthermore, the simulation of pattern recognition is performed using hand-written digit images (MNIST) consisting of 28 × 28 pixels to evaluate the training behaviors of 1T1M and 1M. For the input images, 784 input neurons were connected to 10 output neurons to extract answers from 0 to 9. Thus, the neural network consists of 784 × 10 single-layer fully connected by synapses. The achieved synaptic behaviors of 1T1M and 1M were used, and each weight was updated through a back propagation algorithm. Then, the 10,000 datasets were inferred through forward propagation after training of 50,000 datasets. Pattern recognition training is conducted with obtained weight values (Fig. 4a) for P/D pulses. As shown in Fig. 5(c), it is found that the asymmetry and nonlinearity of 1M affect not only the recognition accuracy but also the convergence rate in training. When an error occurs during the inference stage, the weight values begin to be tuned during the back propagation to extract the correct answer. Thus, assuming that the weights obtained from the 1M are mapped to the neural networks, it is difficult to update the weights to the target value, degrading accuracy. On the other hand, the linearly modulated weight indicates that the degree of the change in the weight as a function of pulse becomes constant. This problem is solved by predictably controlled weights in 1T1M block, and a pattern recognition accuracy of 88% is achieved after 50 epochs. Here, although the dynamic range of the current was limited, improved linearity ensured high recognition accuracy, which was good agreement with many simulation studies [11]. This means that obtaining constantly tunable weights to reduce the errors plays a crucial role in neural network training.

IV. CONCLUSION

Our result suggests that the a-IGZO memristor combined with the a-IGZO synaptic TFT is a potentially promising 1T1M block for the two-terminal circuit burden-free analog RS device with high symmetry and good linearity of synapse weight update.

ACKNOWLEDGMENT

(Tae Jun Yang and Jung Rae Cho contributed equally to this work.)

REFERENCES

[1] K. Nomura, H. Ohta, A. Takagi, T. Kamiya, M. Hirano, and H. Hosono, "Room-temperature fabrication of transparent flexible thin-film transistors using amorphous oxide semiconductors," *Nature*, vol. 432, no. 7016, pp. 488–492, Nov. 2004, doi: 10.1038/nature03090.

[2] H. Hosono, K. Nomura, Y. Ogo, T. Uruga, and T. Kamiya, "Factors controlling electron transport properties in transparent amorphous oxide semiconductors," *J. Non-Crystalline Solids*, vol. 354, nos. 19–25, pp. 2796–2800, May 2008, doi: 10.1016/j.jnoncrysol.2007.10.071.

[3] A. Olziersky, P. Barquinha, A. Vilà, C. Magaña, E. Fortunato, J. R. Morante, and R. Martins, "Role of Ga_2O_3–In_2O_3–ZnO channel composition on the electrical performance of thin-film transistors," *Mater. Chem. Phys.*, vol. 131, nos. 1–2, pp. 512–518, Dec. 2011, doi: 10.1016/j.matchemphys.2011.10.013.

[4] M. Oota, Y. Ando, K. Tsuda, T. Koshida, S. Oshita, A. Suzuki, K. Fukushima, S. Nagatsuka, T. Onuki, R. Hodo, T. Ikeda, and S. Yamazaki, "3D-stacked CAAC-In-Ga-Zn oxide FETs with gate length of 72nm," in *IEDM Tech. Dig.*, Dec. 2019, pp. 321–324, doi: 10.1109/IEDM19573.2019.8993506.

[5] Z. Q. Wang, H. Y. Xu, X. H. Li, H. Yu, Y. C. Liu, and X. J. Zhu, "Synaptic learning and memory functions achieved using oxygen ion migration/diffusion in an amorphous InGaZnO memristor," *Adv. Funct. Mater.*, vol. 22, no. 13, pp. 2759–2765, Jul. 2012, doi: 10.1002/adfm.201103148.

[6] L. Hu, J. Yang, J. Wang, P. Cheng, L. O. Chua, and F. Zhuge, "All-Optically controlled memristor for optoelectronic neuromorphic computing," *Adv. Funct. Mater.*, vol. 31, no. 4, Jan. 2021, Art. no. 2005582, doi: 10.1002/adfm.202005582.

[7] M. Pereira, J. Deuermeier, R. Nogueira, P. A. Carvalho, R. Martins, E. Fortunato, and A. Kiazadeh, "Noble-metal-free memristive devices based on IGZO for neuromorphic applications," *Adv. Electron. Mater.*, vol. 6, no. 10, pp. 1–9, Oct. 2020, doi: 10.1002/aelm.202000242.

[8] Y. Xi, B. Gao, J. Tang, A. Chen, M.-F. Chang, X. S. Hu, J. V. D. Spiegel, H. Qian, and H. Wu, "In-memory learning with analog resistive switching memory: A review and perspective," *Proc. IEEE*, vol. 109, no. 1, pp. 14–42, Jan. 2021, doi: 10.1109/JPROC.2020.3004543.

[9] W. Haensch, T. Gokmen, and R. Puri, "The next generation of deep learning hardware: Analog computing," *Proc. IEEE*, vol. 107, no. 1, pp. 108–122, Jan. 2019, doi: 10.1109/JPROC.2018.2871057.

[10] I. Chakraborty, M. Ali, A. Ankit, S. Jain, S. Roy, S. Sridharan, A. Agrawal, A. Raghunathan, and K. Roy, "Resistive crossbars as approximate hardware building blocks for machine learning: Opportunities and challenges," *Proc. IEEE*, vol. 108, no. 12, pp. 2276–2310, Dec. 2020, doi: 10.1109/JPROC.2020.3003007.

[11] J. Woo, K. Moon, J. Song, S. Lee, M. Kwak, J. Park, and H. Hwang, "Improved synaptic behavior under identical pulses using AlO_x/HfO_2 bilayer RRAM array for neuromorphic systems," *IEEE Electron Device Lett.*, vol. 37, no. 8, pp. 994–997, Aug. 2016, doi: 10.1109/LED.2016.2582859.

[12] I.-T. Wang, C.-C. Chang, L.-W. Chiu, T. Chou, and T.-H. Hou, "3D Ta/TaO_x/TiO_2/Ti synaptic array and linearity tuning of weight update for hardware neural network applications," *Nanotechnology*, vol. 27, no. 36, Sep. 2016, Art. no. 365204, doi: 10.1088/0957-4484/27/36/365204.

[13] J. Woo, K. Moon, J. Song, M. Kwak, J. Park, and H. Hwang, "Optimized programming scheme enabling linear potentiation in filamentary HfO_2 RRAM synapse for neuromorphic systems," *IEEE Trans. Electron Devices*, vol. 63, no. 12, pp. 5064–5067, Dec. 2016, doi: 10.1109/TED.2016.2615648.

[14] P.-Y. Chen, B. Lin, I.-T. Wang, T.-H. Hou, J. Ye, S. Vrudhula, J.-S. Seo, Y. Cao, and S. Yu, "Mitigating effects of non-ideal synaptic device characteristics for on-chip learning," in *Proc. IEEE/ACM Int. Conf. Comput.-Aided Design (ICCAD)*, Nov. 2015, pp. 194–199, doi: 10.1109/ICCAD.2015.7372570.

[15] Z.-Y. Shao, H.-M. Huang, and X. Guo, "Optimizing linearity of weight updating in TaO_x-based memristors by depression pulse scheme for neuromorphic computing," *Solid State Ionics*, vol. 370, Nov. 2021, Art. no. 115746, doi: 10.1016/j.ssi.2021.115746.

[16] S. Park, A. Sheri, J. Kim, J. Noh, J. Jang, M. Jeon, B. Lee, B. R. Lee, B. H. Lee, and H. Hwang, "Neuromorphic speech systems using advanced ReRAM-based synapse," in *IEDM Tech. Dig.*, Dec. 2013, pp. 2561–2564, doi: 10.1109/IEDM.2013.6724692.

[17] S. Yu, "Neuro-inspired computing with emerging nonvolatile memorys," *Proc. IEEE*, vol. 106, no. 2, pp. 260–285, Feb. 2018, doi: 10.1109/JPROC.2018.2790840.

[18] J.-M. Choi, E.-J. Park, J.-J. Woo, and K.-W. Kwon, "A highly linear neuromorphic synaptic device based on regulated charge trap/detrap," *IEEE Electron Device Lett.*, vol. 40, no. 11, pp. 1848–1851, Nov. 2019, doi: 10.1109/LED.2019.2943113.

[19] J. Park, M. Kwak, K. Moon, J. Woo, D. Lee, and H. Hwang, "TiO_x-based RRAM synapse with 64-levels of conductance and symmetric conductance change by adopting a hybrid pulse scheme for neuromorphic computing," *IEEE Electron Device Lett.*, vol. 37, no. 12, pp. 1559–1562, Dec. 2016, doi: 10.1109/LED.2016.2622716.

[20] C. Li, D. Belkin, Y. Li, P. Yan, M. Hu, N. Ge, H. Jiang, E. Montgomery, P. Lin, Z. Wang, W. Song, J. P. Strachan, M. Barnell, Q. Wu, R. S. Williams, J. J. Yang, and Q. Xia, "Efficient and self-adaptive in-situ learning in multilayer memristor neural networks," *Nature Commun.*, vol. 9, no. 1, pp. 7–14, Jun. 2018, doi: 10.1038/s41467-018-04484-2.

[21] S. J. Yun, K.-H. Lee, J. Skarp, H.-R. Kim, and K.-S. Nam, "Dependence of atomic layer-deposited Al_2O_3 films characteristics on growth temperature and al precursors of $Al(CH_3)_3$ and $AlCl_3$," *J. Vac. Sci. Technol. A: Vac., Surf., Films*, vol. 15, no. 6, pp. 2993–2997, Nov. 1997, doi: 10.1116/1.580895.

[22] S. Park, J. T. Jang, Y. Hwang, H. Lee, W. S. Choi, D. Kang, C. Kim, H. Kim, and D. H. Kim, "Effect of the gate dielectric layer of flexible InGaZnO synaptic thin-film transistors on learning behavior," *ACS Appl. Electron. Mater.*, vol. 3, no. 9, pp. 3972–3979, Sep. 2021, doi: 10.1021/acsaelm.1c00517.

[23] S. Park, J. T. Jang, S.-J. Choi, D. M. Kim, and D. Hwan Kim, "Synaptic behavior of flexible IGZO TFTs with Al_2O_3 gate insulator by low temperature ALD," in *Proc. IEEE 19th Int. Conf. Nanotechnol. (IEEE-NANO)*, Jul. 2019, pp. 517–520, doi: 10.1109/NANO46743.2019.8993883.

[24] J.-W. Jang, S. Park, G. W. Burr, H. Hwang, and Y.-H. Jeong, "Optimization of conductance change in $Pr_{1-x}CaxMnO_3$-based synaptic devices for neuromorphic systems," *IEEE Electron Device Lett.*, vol. 36, no. 5, pp. 457–459, May 2015, doi: 10.1109/LED.2015.2418342.

TAE JUN YANG received the B.S. and M.S. degrees in electrical engineering from Kookmin University, Seoul, South Korea, in 2021 and 2023, respectively.

JUNG RAE CHO recieved the B.S. degree in electrical engineering from Kookmin University, Seoul, South Korea, in 2023, where he is currently pursuing the M.S. degree with the School of Electrical Engineering.

HYUNKYU LEE received the B.S. and M.S. degrees in electrical engineering from Kookmin University, Seoul, South Korea, in 2021 and 2023, respectively.

HEE JUN LEE received the B.S. degree in electrical engineering from Kookmin University, Seoul, South Korea, in 2021, where he is currently pursuing the M.S. degree with the School of Electrical Engineering.

SEUNG JOO MYOUNG received the B.S. degree in electrical engineering from Kookmin University, Seoul, South Korea, in 2022, where he is currently pursuing the M.S. degree with the School of Electrical Engineering.

DA YEON LEE received the B.S. degree in electrical engineering from Kookmin University, Seoul, South Korea, in 2022, where she is currently pursuing the M.S. degree with the School of Electrical Engineering.

SUNG-JIN CHOI received the M.S. and Ph.D. degrees in electrical engineering from Korea Advanced Institute of Science and Technology, Daejeon, South Korea, in 2012. He is currently an Associate Professor with the School of Electrical Engineering, Kookmin University, Seoul, South Korea.

JONG-HO BAE (Member, IEEE) received the B.S. degree in electrical engineering from Pohang University of Science and Technology, South Korea, in 2011, and the Ph.D. degree from the Department of Electrical and Computer Engineering, Seoul National University, Seoul, South Korea, in 2018. He is currently an Assistant Professor with the School of Electrical Engineering, Kookmin University, Seoul.

DONG MYONG KIM (Member, IEEE) received the B.S. (magna cum laude) and M.S. degrees in electronics engineering from Seoul National University, Seoul, South Korea, in 1986 and 1988, respectively, and the Ph.D. degree in electrical engineering from the University of Minnesota, Minneapolis, MN, USA, in 1993. Since 1993, he has been a Professor with the School of Electrical Engineering, Kookmin University, Seoul. His research interest includes modeling and characterization of semiconductor devices.

CHANGWOOK KIM received the B.S. and M.S. degrees from the Department of Chemistry, Sogang University, Seoul, South Korea, in 1993 and 1995, respectively, and the Ph.D. degree from the Department of Chemistry, Korea Advanced Institute of Science and Technology, Daejeon, South Korea, in 2003. Since 2016, he has been a Research Professor with the Circadian ICT Research Center, Kookmin University, Seoul. His research interests include circadian rhythm, color science, and computational chemistry.

JIYONG WOO (Associate Member, IEEE) received the Ph.D. degree in materials science and engineering from Pohang University of Science and Technology, Pohang, South Korea, in 2017. He is currently an Assistant Professor of electronic and electrical engineering with Kyungpook National University, Daegu, Republic of Korea.

DAE HWAN KIM (Senior Member, IEEE) received the B.S., M.S., and Ph.D. degrees in electrical engineering from Seoul National University, Seoul, South Korea, in 1996, 1998, and 2002, respectively. He is currently a Professor with the School of Electrical Engineering, Kookmin University, Seoul. His current research interests include nano CMOS, oxide and organic thin-film transistors, biosensors, and neuromorphic devices.