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RESEARCH ARTICLE

Design and Analysis of Novel High-Gain Boost Converter for Renewable Energy Systems (RES)

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ABSTRACT High-gain DC-DC converters are becoming increasingly popular in renewable energy applications and solar PV systems. This article introduces a non-isolated non-coupled inductor-based high-gain DC-DC boost converter with the desirable features of low voltage stress on controlled power switches and high voltage gain at lower duty ratios. The proposed converter is well suited for boosting the low-input DC voltage obtained from distributed generation units like photovoltaic (PV) or fuel cells to substantially higher DC voltage. The converter comprises only two switches, and a single PWM signal governs its operation. These characteristics result in a topology that is more compact, less costly, lighter weight, and easier to control. The proposed converter is compared with some previously developed topologies of high-gain boost converters across various performance parameters. This comparison illustrates that the proposed model surpasses them in every aspect. A 300 W hardware prototype of a proposed model is developed and tested in a laboratory environment to confirm the theoretical assertions of a proposed model. The proposed topology offers a promising solution and enables a high gain of approximately 12 times the input voltage at a smaller duty ratio, specifically 11.25 at a duty of 0.6 and 17.77 at a duty of 0.7. The efficiency of a proposed converter ranges between 92.5% to 94.5% making it appropriate for numerous medium-high power applications. The uniqueness of the suggested system is its simple design and greater efficiency, which provides a more considerable gain and higher output voltages for sustainable energy systems.

INDEX TERMS Renewable energy system (RES), high gain, boost converter, dc–dc converter.

I. INTRODUCTION

The high-gain DC-DC boost converters are essential in converting small input direct current (DC) voltage ranging from a few volts to substantially higher DC voltage levels [1]. These DC-DC converters must have a constant input current and step-up capabilities. Such converters are used in various applications like solar photovoltaic (PV) systems, robotics, high-voltage DC systems, and electric vehicles [2], [3]. The energy produced by sources like fuel cells or solar photovoltaic is quite low and the required output voltage is relatively high for various household and industrial applications. These pressing concerns enable the researchers to focus more on the development of high-step-up DC-DC converters. DC-DC converters consist of various arrangements of inductors, capacitors, diodes, and switches. These components are interconnected to enable energy exchange between inductors and capacitors. The process begins with

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the exchange of stored energy in the inductors. Subsequently, this stored energy is transferred to the capacitors, resulting in the achievement of a higher voltage level [4]. Figure 1 illustrates the schematic of a DC energy system. In a DC microgrid, a high-gain DC-DC converter regulates the DC voltage to a specified level. Modern DC microgrids employ a combination of supercapacitors and a high-gain DC-DC converter. In the islanded mode operation of a DC microgrid, it is common practice to pair an inverter with a high-gain DC-DC converter to supply alternating current (AC) loads. High-gain DC-DC converters have increasingly become a popular alternative to traditional boost converters and their derivatives [5]. The conventional DC-DC boost converter has some drawbacks. These include high voltage stress, upswing electromagnetic interference (EMI), intolerable input current ripples, and low efficiency at light load conditions and therefore it is unsuitable in practical applications where the duty ratio exceeds a predetermined threshold value.

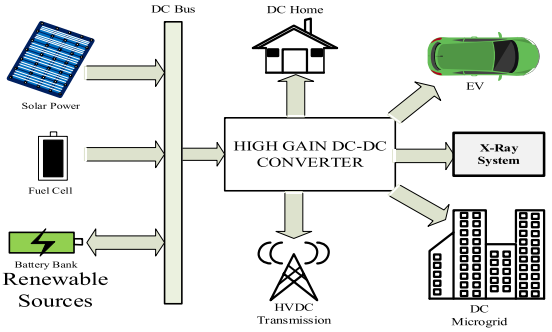

FIGURE 1. DC energy system.

DC-DC converters serve as a bridge between the source and the load. These converters are generally categorized into isolated and non-isolated types. Conventional boost converters as shown in Figure 2 (a) must operate at higher duty ratio values when integrated with microgrids. This results in a significant amount of current and voltage stress on the converter. As the duty ratio increases, the parasitic resistance (ESR) of the capacitor and inductor experiences a substantial rise, resulting in a significant loss in voltage gain and efficiency of the boost converter.

Non-isolated converters are further classified as coupled inductor and noncoupled inductor-based configurations. An isolated converter creates electrical isolation between the input power supply and load. It effectively divides the circuit into two distinct sections to prevent the direct flow of current by incorporating a high-frequency transformer. However, it leads to an increase in both the size and expense [6], [7], [8], [9] of the converter. Isolated configurations are preferred in high-power applications that require a shared ground between the source and load. The coupled inductor configurations can achieve notably high voltage gain at a lower duty ratio but at a higher duty, it causes issues like switch voltage stress, conduction loss, low efficiency, and leakage inductance [10]. This research article exclusively looks at

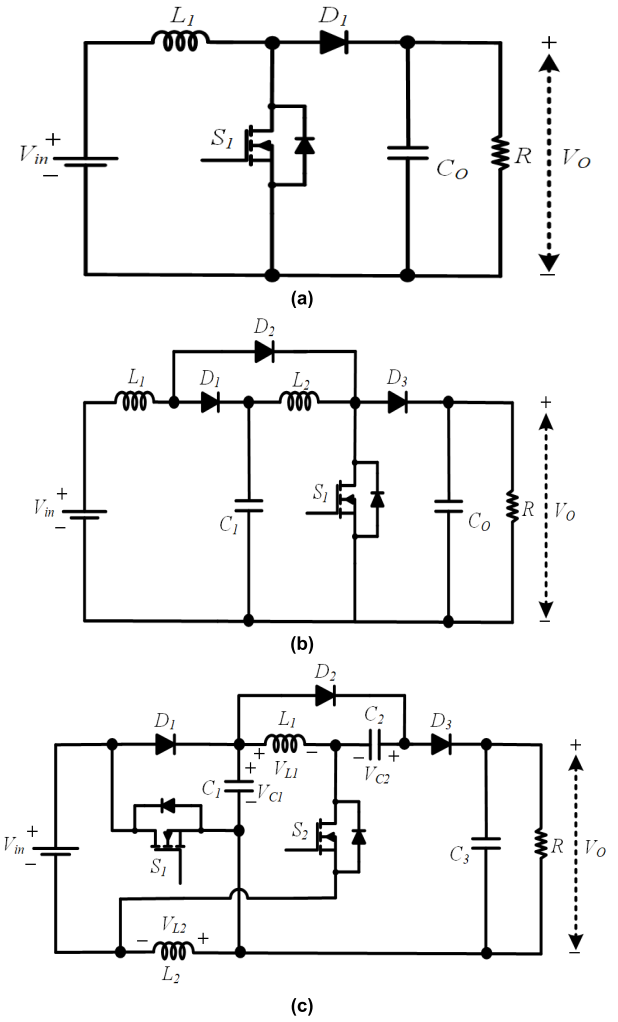

FIGURE 2. (a) Conventional boost converter (b) Conventional quadratic boost converter (c) Proposed high gain boost converter.

non-isolated non-coupled inductor topologies. Non-isolated converters are preferred when there is no need for isolating the input from the output.

To solve these challenges, various DC-DC converter topologies have been proposed in this article. The study proposed in [11] shows a comparative review of several non-isolated high step-up DC-DC converters. Several topologies of quadratic boost converter (QBC) have been introduced in [12], [13], and [14]. These topologies are designed to produce significantly high voltage at lower duty cycles by effectively minimizing the stress on the switching devices, but at a higher duty ratio, the inductor core is more likely to saturate. A novel quadratic boost converter shown in [15] is designed to minimize the inductor current ripples and reduce the stress on the switches. The study proposed in [16] and [17] shows a quasi-z-source converter. This converter replaces the inductor with an impedance network belonging to the high-gain boost converter topology but they operate within a constrained duty cycle range. An interleaved boost converter

presented in [18] enhances both output voltage and efficiency with fewer switches. A study proposed in [19] shows an interleaved high-gain boost converter carried out by combining two boost converters. The converter requires a large number of capacitors and diodes to achieve a higher voltage conversion ratio. A multiphase interleaved converter combined with a z-source network to achieve a high gain with a low input current ripple and eliminates the need for an input filter [20]. However, a voltage boost circuit is required at the end of the converter to further enhance the converter gain. A quadratic boost converter is introduced in [21] by implementing the voltage lift technique. A high-gain hybrid converter uses a voltage multiplier cell and switched capacitor cells to mitigate the issues related to the stress on the power device [22]. The study proposed in [23] shows a converter with different voltage stress levels on two switches. It employs both the diode voltage capacitor multiplier and switched inductor voltage multiplier techniques to attain high gain. The study proposed in [24] shows a non-isolated coupled inductor-based high step-up DC-DC converter with ultra-high voltage gain facilitated by an active switched inductor. The three-winding coupled inductor ensures a wide output voltage range for various applications. Its broad voltage gain range offers versatility, low semiconductor spikes to enhance reliability, and a simple gate driver control system to make it user-friendly.

This research article presents a novel topology of a non-isolated non-coupled high gain boost converter. The appealing characteristics of the proposed converter include:

- The proposed converter offers advantages including high gain, increased output voltage, and continuous current mode (CCM) operation. These qualities make it an attractive option for medium to high-power applications.
- The proposed converter offers a promising solution and achieves a high gain of approximately 17.77 at a duty cycle of 0.7 and 11.25 at a duty of 0.6.
- The proposed converter has an efficiency of approximately 92.5% to 94.5%, making it appropriate for several medium to high-power applications.
- The converter employs only two switches and the voltage stress on these power switches is lower than the output voltage. Despite having two switches it requires a single PWM signal for its operation which makes it easier to control and reduces the requirement for a gate driver.
- The absence of a coupled inductor eliminates the issue associated with leakage inductance and switch stress at a higher duty ratio.

The rest of the paper is systematized subsequently: Section II describes how a proposed converter works. Section III compares a proposed high-gain boost converter with previously developed topologies. The simulation results are described in Section IV. The hardware results are described in Section V. The conclusion is delivered in Section VI.

II. PROPOSED CONVERTER AND OPERATIONAL MODE

The schematic of a proposed high-gain boost converter is shown in Figure 2 (c). The converter consists of two inductors (L_1 and L_2), three diodes (D_1, D_2 and D_3), three capacitors ($C_1, C_2,$ *and* C_3), and two switches (S_1 and S_2). The same PWM signal controls the operation of both switches. This facilitates easier control of the converter and reduces the requirement for gate driver circuitry. The proposed converter provides a promising solution to achieve high gain and high efficiency. These desirable features make it suitable for numerous medium-high power applications. The CCM and DCM modes of operation of a proposed converter are explained in the following section:

A. CONTINUOUS CONDUCTION MODE

Based on a switching signal there are two modes of operation (switch on mode and switch off mode). For the proper functioning of a converter both the switch (S_1 and S_2) must be turned on and turned off simultaneously. When the CCM mode of operation is considered, the current must flow regularly through both inductors (cap L sub 1,, and, cap L sub 2) Furthermore, the energy is transferred from a source to both inductors, increasing the current across the inductor. Figure 3 depicts related waveforms for inductor current and capacitor voltage in a CCM mode.

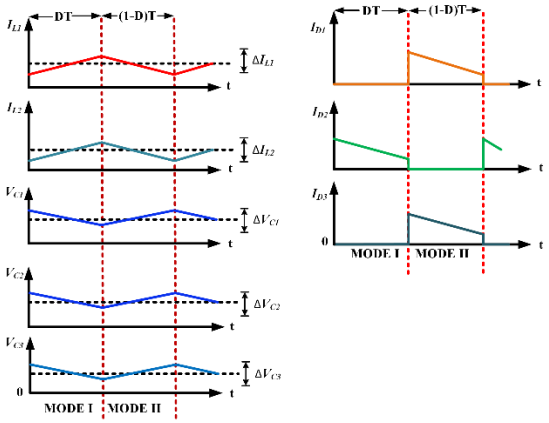

FIGURE 3. Related waveform in CCM mode.

1) Mode-1 ($0 \leq t \leq DT$)

In mode-1 when both the switches (S_1 and S_2) are turned on, the diode (D_1 and D_3) becomes reverse biased while the diode D_2 becomes forward biased. Figure 4 shows an analogous circuit diagram for a converter's first mode of functioning. The switch-on mode equations in CCM (continuous conduction mode) were found by applying Kirchhoff's voltage law (KVL) to an equivalent circuit shown below:

$$V_{L1} = V_{in} + V_{C1} = V_{C2} \tag{1}$$

$$V_{L2} = V_{in} \tag{2}$$

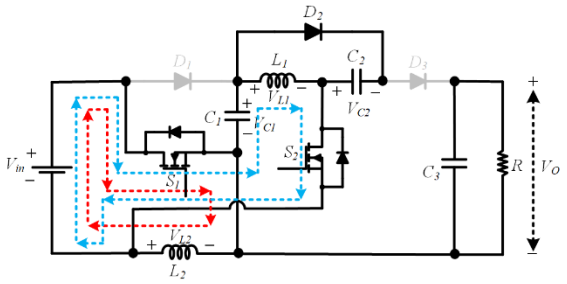

FIGURE 4. Equivalent circuit for switch-on mode of operation.

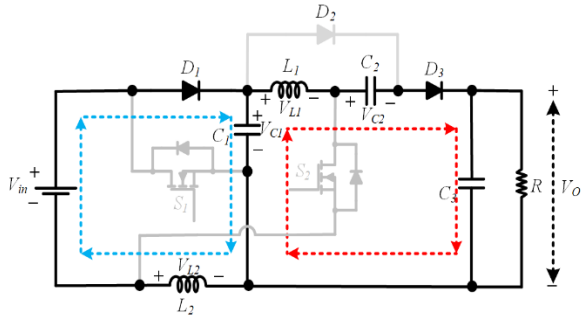

FIGURE 5. Equivalent circuit for switch-off mode of operation.

2) Mode-2 (DT ≤ t ≤ T)

The equivalent circuit shown in Figure 5 illustrates the converter switch-off mode operation. In mode 2, when switches (S_1 and S_2) are turned off, the diode (D_1 and D_3) will conduct while the diode D_2 will becomes reverse biased and energy stored in passive components of the converter is transmitted to the load. The equation for the second mode of operation can be obtained by applying KVL to an equivalent circuit.

$$V_{C1} - V_{L1} + V_{C2} - V_O = 0 \tag{3}$$
$$-V_{L1} = V_O - V_{C1} - V_{C2} \tag{4}$$
$$-V_{L1} = V_O - V_{C1} - (V_{in} + V_{C1}) \tag{5}$$
$$V_{L1} = V_{in} + 2V_{C1} - V_O \tag{6}$$
$$V_{L2} = V_{in} - V_{C1} \tag{7}$$

By applying volt-inductor balance across an inductor L_2.

$$V_{in}D + (V_{in} - V_{C1})(1 - D) = 0 \tag{8}$$
$$V_{C1} = \frac{V_{in}}{1 - D} \tag{9}$$

where:

V_{C1} is the capacitor (C_1) voltage of the converter.

V_{in} is the input voltage of the converter.

D is the duty ratio of the pulse-width modulation (PWM) gating signal.

Apply the voltage inductor balance at the inductor L_1.

$$(V_{in} + V_{C1})D + (2V_{C1} + V_{in} - V_o)(1 - D) = 0 \tag{10}$$
$$2V_{C1} - V_{C1}D + V_{in} - V_o(1 - D) = 0 \tag{11}$$
$$V_{C1}(2 - D) - V_o(1 - D) + V_{in} = 0 \tag{12}$$
$$-V_o(1 - D) + \frac{V_{in}(2 - D)}{(1 - D)} + V_{in} = 0 \tag{13}$$
$$V_o(1 - D) = \frac{2V_{in} - V_{in}D + V_{in} - V_{in}D}{(1 - D)} \tag{14}$$
$$V_o(1 - D) = \frac{3V_{in} - 2V_{in}D}{1 - D} \tag{15}$$
$$\frac{V_o}{V_{in}} = \frac{(3 - 2D)}{(1 - D)^2} \tag{16}$$

where:

V_0 is the output voltage of the converter.

V_{in} is the input voltage of the converter.

B. DISCONTINUOUS CONDUCTION MODE

Figure 6 illustrates two conditions for a discontinuous conduction mode. Any discontinuity in any one of the inductor currents causes the converter to switch to discontinuous conduction mode (DCM). A generalized DCM equations of proposed a high gain converter can be computed as stated below:

$$V_{in}D_1 + (V_{in} - V_{C1})D_2 = 0 \tag{17}$$
$$V_{in}D_1 + V_{in}D_2 = V_{C1}D_2 \tag{18}$$
$$V_{C1} = \frac{V_{in}D_1 + V_{in}D_2}{D_2} \tag{19}$$
$$(V_{in} + V_{C1})D_1 + 2(V_{C1} + V_{in} - V_O)D_3 = 0 \tag{20}$$
$$(V_{in}D_1 + V_{C1}D_1 + 2_{V_{C1}D_3} + 2\_V_{in}D_3 = 2V_OD_3 \tag{21}$$
$$(V_{in}D_1 + \left(\frac{V_{in}D_1 + V_{in}D_2}{D_2}\right)D_1 + 2\left(\frac{V_{in}D_1 + V_{in}D_2}{D_2}\right)D_3 + 2V_{in}D_3 = 2\frac{V_oD_3}{V_{in}} \tag{22}$$
$$\left(\frac{V_O}{V_{in}}\right)_{DCM} = \left(\frac{2D_1^2 + 4(D_1D_2 + D_1D_3 + D_2D_3)}{D_2D_3}\right) \tag{23}$$

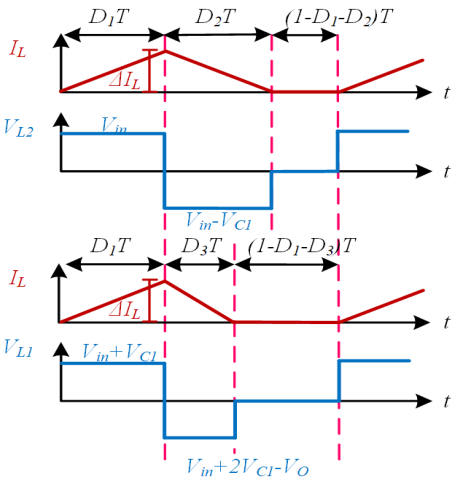

FIGURE 6. Equivalent circuit for switch-off mode of operation.

C. DESIGNING OF PASSIVE COMPONENTS

This section details the design and calculation of passive elements. A diligent design of the inductor and capacitor is required for the effective operation of the suggested converter in CCM mode. The size of the passive components is influenced by several factors such as the switching frequency, output load, and duty ratio. Higher switching frequencies lead to smaller component sizes.

1) DETERMINING THE INDUCTANCE VALUE

The main goal of designing an inductor is to operate the converter in CCM. Equation (30) specifies the minimum required inductance for L_1 in CCM mode.

$$L_1\frac{dI_{L1}}{dt} = V_{in} + V_{C1} \tag{24}$$

$$L_1\frac{dI_{L1}}{dt} = V_{in} + \frac{V_{in}}{1-D} \tag{25}$$

$$L_1\frac{dI_{L1}}{dt} = \frac{V_{in} - V_{in}D + V_{in}}{1-D} \tag{26}$$

$$L_1\frac{\Delta I_{L1}}{DT} = \frac{2V_{in} - V_{in}D}{1-D} \tag{27}$$

$$\frac{V_o}{R}L_1 \geq \frac{V_{in}\,(2-D)\,DT}{2} \tag{28}$$

$$V_oL_1 \geq \frac{RV_{in}\,(2-D)\,DT}{2} \tag{29}$$

$$L_1 \geq \frac{R\,(1-D)^2\,(2-D)\,D}{2(3-2D)f_s} \tag{30}$$

where R is the load value, the duty ratio is signified by D, and f_s indicated switching frequency. L is the required inductance of the inductor (L_1 & L_2).

Similarly for inductor L_2:

$$L_2 \geq \frac{R\,(1-D)^4\,D^2}{2_{fs}\,(3-2D)\,(1+D-D^2)} \tag{31}$$

2) SELECTING THE CAPACITANCE VALUE

The choice of a capacitor depends on a maximum allowable voltage ripple as well as a voltage across the capacitor itself. While making the selection of a capacitor and preventing it from bursting, its value should be chosen

Sufficiently high to withstand any potential high voltage that may be applied across the capacitor. The value of the capacitor can be computed using equation (37).

$$I_{c1}\Delta T = C_1\Delta V_{C_1} \tag{32}$$

$$I_{C1}DT = C_1\Delta V_{C_1} \tag{33}$$

$$\frac{V_O}{R(1-D)} = C_1\Delta V_{C_1} \tag{34}$$

$$C_1 = \frac{V_O}{R\,(1-D)f_s\Delta V_{C1}} \tag{35}$$

$$V_{C1} = \frac{V_{in}(3-2D)}{(1-D)^2\,R\,(1-D)f_s\Delta V_{C1}} \tag{36}$$

$$C_1 = \frac{V_{in}(3-2D)}{R\,(1-D)^3\,f_s\Delta V_{C1}} \tag{37}$$

Similarly for capacitor C_2 and C_3:

$$C_2 = \frac{V_{in}(3-2D)}{R\,(1-D)^2\,f_s\Delta V_{C2}} \tag{38}$$

$$C_3 = \frac{V_{in}(3-2D)}{R\,(1-D)^2\,f_s\Delta V_{C3}} \tag{39}$$

where:

V_{in} is the converter input voltage.
f_s is the switching frequency.
ΔV_C is the permissible ripple in the capacitor voltage.
C is the required capacitance of capacitor (C_1, C_2 & C_3).
R is the load value.

D. REAL VOLTAGE GAIN

The parasitic parameters such as on-state resistance of switches, diodes and ESR of inductors and capacitors affects the efficiency drastically. The equation for calculating the real voltage gain considering inductor ESR of the converter is shown in Equation (43). Figure 7 shows the ideal and real gain curve of a proposed topology.

$$V_{in}\frac{V_O(3-2D)}{R\,(1-D)^2} = \frac{V_O^2}{R} + \frac{V_O^2}{R^2\,(1+D)^2}r_{L1} + \frac{V_O^2\left(1+D-D^2\right)^2}{R^2D^2\,(1-D)^4}r_{L2} \tag{40}$$

$$\frac{V_{in}(3-2D)}{(1-D)^2} = V_O(1 + \frac{r_{L1}}{R\,(1-D)^2} + \frac{\left(1+D-D^2\right)^2 r_{L2}}{RD^2\,(1-D)^4}) \tag{41}$$

$$\frac{V_{in}(3-2D)}{(1-D)^2} = V_O(\frac{RD^2\,(1-D)^4 + r_{L1}D^2\,(1-D)^2 + r_{L2}\left(1+D-D^2\right)^2}{RD^2\,(1-D)^2}) \tag{42}$$

$$V_O = \frac{V_{in}\,(3-2D)\,RD^2\,(1-D)^2}{RD^2\,(1-D)^4 + D^2\,(1-D)^2\,r_{L1} + \left(1+D-D^2\right)^2\,r_{L2}} \tag{43}$$

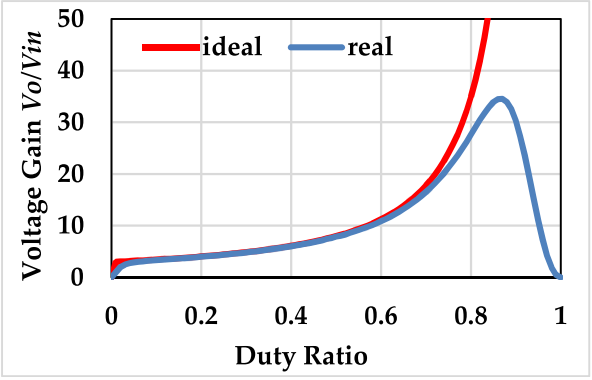

FIGURE 7. Ideal Vs real gain curve of a proposed topology.

TABLE 1. Comparison with other recent topologies.

Topology	Number of Components					Voltage Gain ($\frac{V_o}{V_{in}}$)	Switch voltage Stress
	Switch (N_S)	*Diode* (N_D)	*Inductor* (N_L)	*Capacitor* (N_C)	Total		
[12]	2	7	4	3	16	$\frac{3+D}{(1-D)}$	$S_1 = \frac{2V_O}{(3+D)}$. $S_2 = \frac{(1+D)V_O}{(3+D)}$
[15]	2	6	2	4	14	$\frac{3-3D+D^2}{(1-D)^2}$	$S_{1,2} = \frac{2V_O}{(3-D+D^2)}$
[25]	2	7	4	1	8	$\frac{1+3D}{1-3D}$	$S_{1,2} = \frac{V_O}{1+D}$
[26]	2	3	2	2	9	$\frac{2D}{(1-D)^2}$	$S_1 = \frac{(1-D)V_O}{2D}$ $S_2 = \frac{(1+D)V_O}{2D}$
[27]	2	6	2	4	14	$\frac{3}{1-D}$	$\frac{V_O}{1-D}$
[28]	1	4	1	4	10	$\frac{3-D}{1-D}$	$\frac{V_O}{3-D}$
[29]	2	3	2	3	10	$\frac{D^2-3D+3}{(1-D)^2}$	$S_1 = \frac{V_O(1-D)^3}{D^2-3D+3}$ $S_2 = \frac{V_O(1-D)^2}{D^2-3D+3}$
[30]	2	3	2	3	10	$\frac{D^2-3D+3}{(1-D)^2}$	$S_1 = \frac{V_O(1-D)^3}{D^2-3D+3}$ $S_2 = \frac{V_O(1-D)^2}{D^2-3D+3}$
CBC	1	1	1	1	4	$\frac{1}{(1-D)}$	1
CQBC	1	3	2	2	8	$\frac{1}{(1-D)^2}$	1
[Proposed]	2	3	2	3	10	$\frac{(3-2D)}{(1-D)^2}$	$S_1 = \frac{V_O(1-D)^3}{(3-2D)}$ $S_2 = \frac{V_o - 2V_OD(1-D)^2}{(3-2D)}$

III. COMPARISION WITH OTHER RECENT TOPOLOGIES

A detailed analysis of the proposed converter with similar topologies is performed in this section. The comparison is done on the basis of components required, voltage gain, and voltage stress across the power switches as shown in TABLE 1. Figure 8 shows the voltage gain curve versus duty ratio of a proposed converter. The graph indicates that the suggested converter outperforms all other topologies in terms of gain. Generally, non-isolated boost converters are not employed with duty ratios exceeding the limit of 0.8. Beyond this limit, there is a reduction in gain due to increased conduction losses. The proposed converter introduced in [12] incorporates higher components count when compared to other suggested topologies. Furthermore, the incorporation of multiple diodes and inductors contributes to a bulkier and larger size of circuit. The components utilized in a proposed converter are lower than a converter presented in [12], [15], and [27]. In comparison to previously developed topologies outlined in the curve, the gain of the suggested converter notably increases when the duty cycle exceeds 0.1. Despite having four inductors as discussed in [12], the gain of a converter is significantly lesser than a proposed converter. Similarly, the converter proposed in [27] employs two inductors, but its gain limits at a higher duty ratio. The voltage gain of converter [29] and [30] are much higher than the other proposed topologies with lesser component count. It employs only two inductor such as CQBC, which reduces the size and weight of a converter as compared to converter presented in [12] and [15]. Figure 9 depicts the voltage stress versus voltage gain curve. It can be observed from the graph

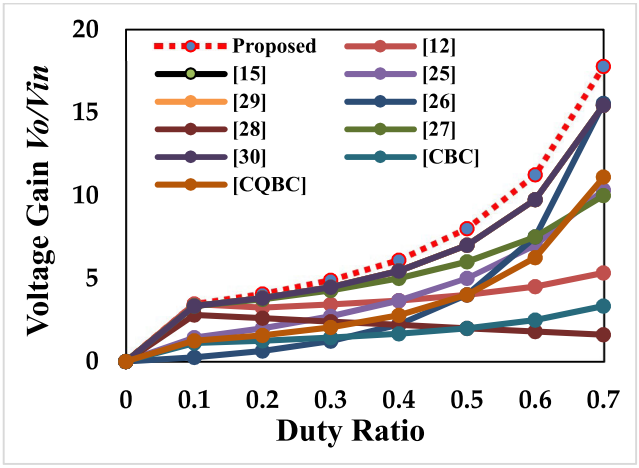

FIGURE 8. Voltage gain vs duty ratio.

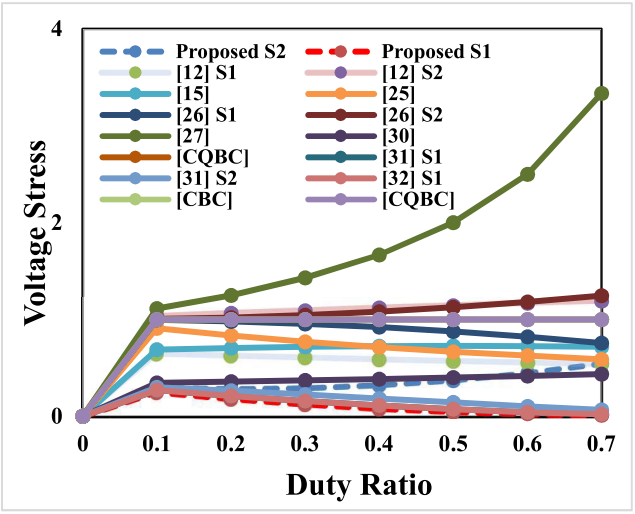

FIGURE 9. Voltage stress vs Duty ratio.

that the switch S_1 of a proposed converter experiences the least amount of stress when compared to other topologies mentioned in [12], [15], and [27]. Furthermore, switch S_2 undergoes a higher voltage stress for high voltage gain compared to switch S_1. However, it remains lower than the stress observed in the converters [12], [27], and [28].

The proposed converter lacks a common ground configuration which makes the design of the control difficult. However, there are several methods available to mitigate common-ground and leakage current issues in the proposed converter for PV applications:

- In future work we will implement transformer isolation for galvanic separation.
- Utilize floating ground design or isolated power supplies on the PV side.
- Introduce capacitive coupling for AC transfer and DC blocking.
- Consider optical isolation for control signal transmission.
- Use active common-mode control to regulate and minimize common-mode voltage.
- Carefully design grounding schemes to minimize ground loops.

IV. SIMULATION RESULTS

To evaluate the performance of a proposed high-gain boost converter the simulation results in open loop and closed loop were taken using MATLAB R2021b software.

A. OPEN-LOOP PERFORMANCE

TABLE 2 shows a simulation designed parameters of a proposed converter. The simulation results of a proposed converter at different duty ratio values are discussed in this section.

TABLE 2. Simulation design parameters.

Parameters	Specifications
Input voltage	V_{in} = 24V ~ 36V
R_L Load	R = 500 Ω
Frequency	200 kHz
Inductors L_1 & L_2	L_1 = 24.5 µH, L_2 = 1 mH
Capacitors C_1, C_2 & C_3	C_1 = 33 µF, C_2 = 220 µF, C_3 = 220 µF
Duty Ratio	0.4, 0.6 and 0.7

Figure 10 (a) shows the simulation result of the proposed converter at 24 V input. The duty ratio is set at 0.4 with a load resistance of 500 ohms. The measured output voltage is determined to be 140 V. Furthermore, the voltage of across capacitors (C_1 and C_2) is measured to be 40 V and 60 V respectively. Figure 10 (b) shows a simulation outcome at a duty ratio of 0.6 with the same load resistance and input voltage. The measured output voltage is determined to be 140 V respectively. Subsequently, the voltages across capacitors (C_1 and C_2) are found to be 58 V and 80 V respectively. Figure 10 (c) shows the simulation outcome at 36 V input. The duty ratio is set at 0.7 with a load resistance of 500 ohms. The measured output voltage is determined to be 610 V. The measured capacitor voltage (C_1) is approximately 110 V, while capacitor (C_2) has a voltage of 140 V respectively. Figure 11 (a) shows the simulation result of capacitor current waveform (C_1, C_2, and C_3). The diode current (I_{D1}, I_{D2}, and I_{D3}) and switch current (I_{SW1}, and I_{SW2}) simulation waveforms are shown in Figure 11 (b) and Figure 11 (c) respectively.

B. CLOSED-LOOP PERFORMANCE

Figure 12 shows a schematic diagram of the circuit used to regulate the suggested circuit output voltage. Figure 13 and Figure 14 illustrate the closed-loop simulation performance of the proposed converter. When the input voltage ranges from 24 to 30 volts, the output voltage (Vo) is effectively controlled at 400 volts. Similarly, when the load resistance

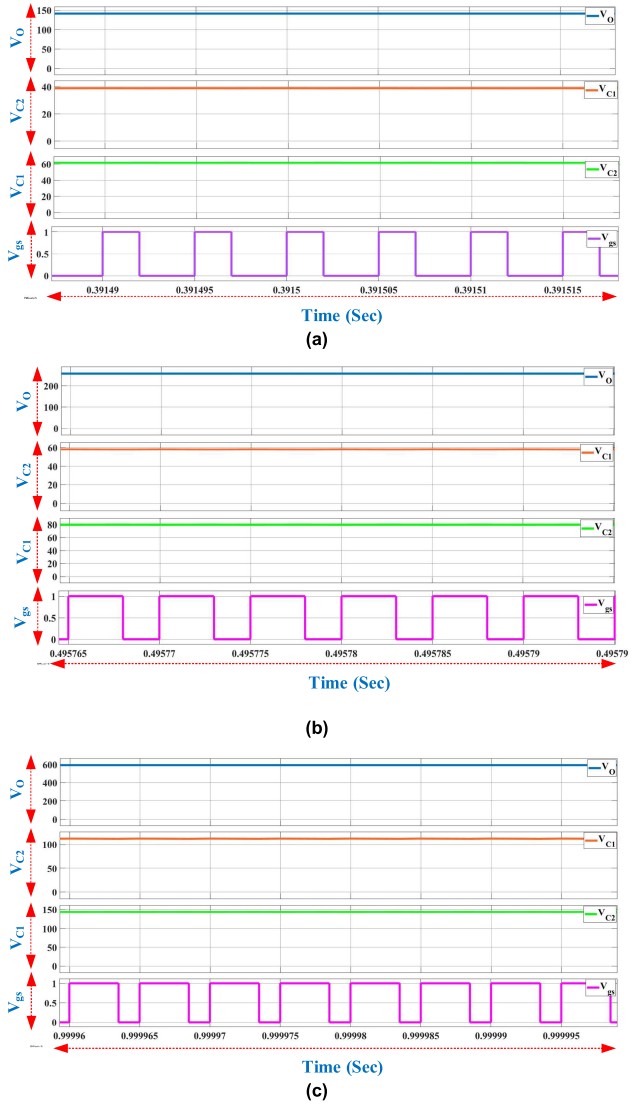

FIGURE 10. Simulation waveforms (V_O,V_{C1} *and* V_{C2}) of a proposed converter at a duty ratio of (a) 0.4, (b) 0.6, and (d) 0.7.

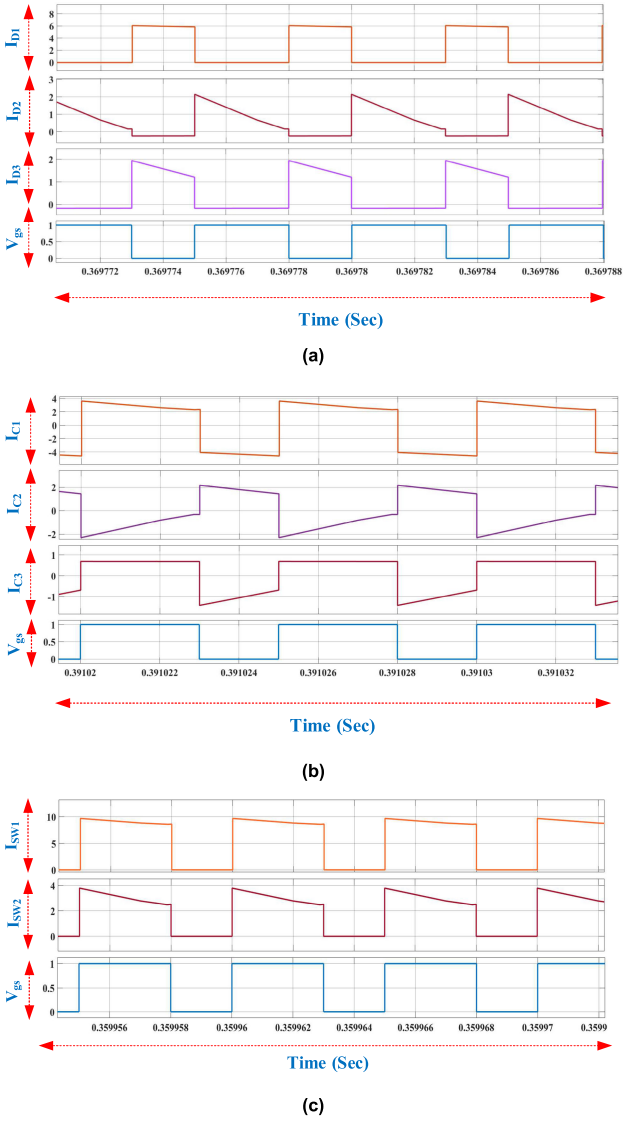

FIGURE 11. Current waveforms (a) Diode, (b) Capacitor, and (c) Switch.

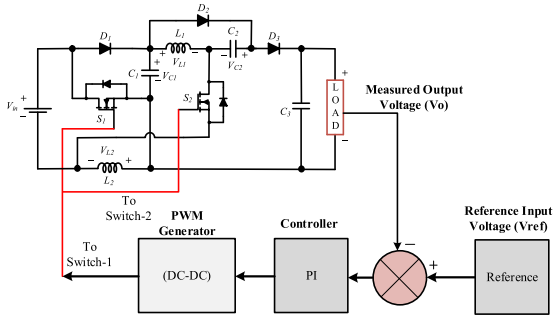

FIGURE 12. A schematic diagram of the closed loop control circuit.

is varied, the PI controller maintains a consistent output voltage. Despite changes in the load, the output voltage remains constant at 400 V, indicating the proper functioning of the PI controller. For the PI controller, specific values are assigned to the proportional constant (K_p) and integral constant (K_i). In this case, K_p is set to 0.05, and K_i is set to 0.02.

V. HARDWARE RESULTS

A 300 W hardware prototype of a proposed high gain boost converter is shown in Figure 15. The proposed converter is devised and examined in a controlled laboratory environment to determine its performance. A schematic architecture of the experimental setup is shown in Figure 16. TABLE 3 lists the converter parameters and their specifications for experimental analysis. To analyze the assembled hardware in an open loop a PWM pulse of desired duty ratio is produced and targeted to the gate driver circuit using a microcontroller (STM32G474).

The converter switches are powered by same DC power source with two isolated voltage regulator ICs (MCWI03-48S15). The Tektronix (MDO3024) oscilloscope is used to

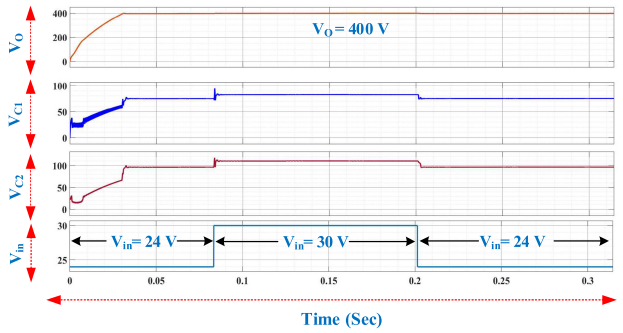

FIGURE 13. Simulation waveforms of output voltage with change in input voltage from 24 V to 30 V.

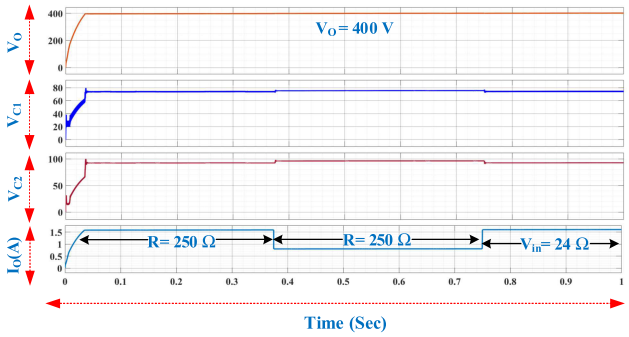

FIGURE 14. Simulation waveforms of output voltage with change in load resistance from 250 Ω to 500 Ω.

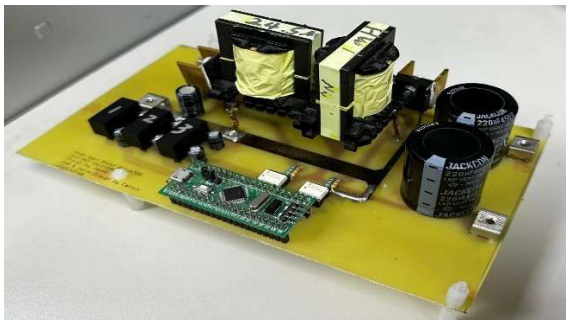

FIGURE 15. Developed hardware prototype.

record the outcomes of a proposed a converter performance under open loop control.

Figure 17 shows the experimental waveforms of a proposed high-gain boost converter. Figure 17 (a) displays the waveforms of voltage stress across switch ($V_{ds1} and V_{ds2}$) and output voltage (V_O) of the converter. The output voltage at $D = 0.6$ and $V_{in} = 24$ V is determined to be 280 V, which is in accordance with the calculated voltage gain. According to captured waveform the voltage stress across switches S_1 and S_2 is determined to be 70 V and 180 V respectively which is significantly lower as compared to the output voltage V_O. The key advantage of a suggested model is its high gain of approximately 12 times of input at a smaller duty ratio. Figure 17 (b) depicts the waveform of diode voltage

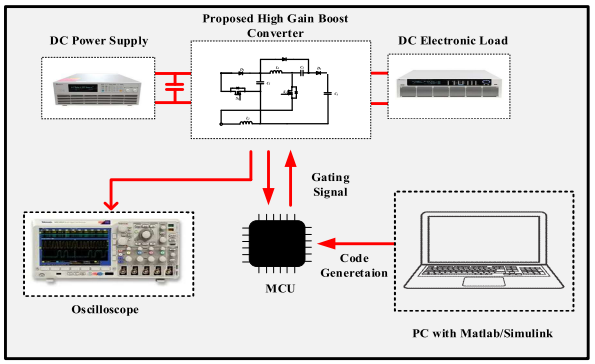

FIGURE 16. A Schematic of experimental prototype.

TABLE 3. Hardware design parameters.

Parameters	Specifications
Input voltage	V_{in} = 24V ~ 36V
Maximum power	P_{max} = 300 W
R_L Load	R = 500 Ω
Frequency	200 kHz
Inductors L_1 & L_2	L_1 = 24.5 µH, L_2 = 1 mH
Capacitors C_1, C_2 & C_3	C_1 = 33 µF, C_2 = 220 µF, C_3 = 220 µF
Power MOSFET (S_1, S_2)	SPW52N50C3, 560 V, 52 A, 0.07 Ω
Diode (D_1-D_3)	CMPFCD86-600V, I_F = 8 A, V_F = 1.5 V
Microcontroller	STM32G474
Gate driver IC	TLP250H
Voltage regulator IC	MCWI03-48S15
DC power supply	Chroma, 62100H-600S

(V_{D1}, V_{D2}, and V_{D3}) of a proposed converter and Figure 17 (c) exhibits the experimental waveforms of inductor current (I_{L1} and I_{L2}) and capacitor voltage (V_{C1} and V_{C2}). It is evident from the waveforms that capacitor voltages of C_1 and C_2 are significantly lower than the output voltage V_O of a proposed converter, which states that all the capacitors excluding C_3, are subject to minimal voltage stress. Figure 18 shows the related experimental waveforms of output voltage V_O at $V_{in} = 36$ V and D = 0.7. Output voltage (V_O) is found to be 636 V, which is also in accordance with the theoretically calculated gain value and simulated results of a proposed converter.

Figure 19 illustrates the experimental waveforms of a PV module's output in relation to a high-gain boost used for maximum power point tracking (MPPT). The experimental waveforms include output voltage (V_{pv}), output current (I_{pv}), and output power (P_{pv}). The experiment begins by configuring the PV simulator (Chroma/62020H-150S) to generate a maximum power output (P_{mpp}) of 300 W. The setting includes a maximum power voltage (V_{mpp}) of 30 V, maximum power current (I_{mpp}) of 10 A, an open-circuit voltage (V_{oc}) of 36 V, and a short-circuit current (I_{sc}) of 11 A. These conditions were established under an irradiance level

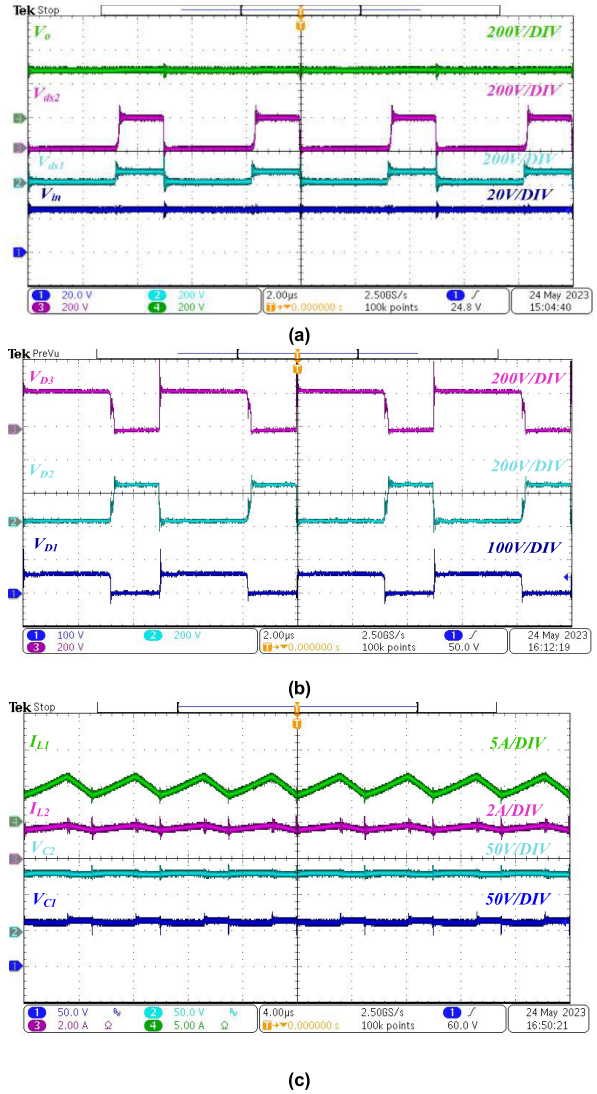

FIGURE 17. Experimental waveforms of high gain boost $D = 0.6$, $V_{in} = 24$ V and $V_O = 280$ V (a) Output voltage (V_O) and switch voltage stress ($Vds1$ *and* $Vds2$) (b) Voltage across the diode (V_{D1},V_{D2}, and V_{D3}), and (c) Capacitor voltage (V_{C1} and V_{C2}). and inductor current (I_{L1} and I_{L2}).

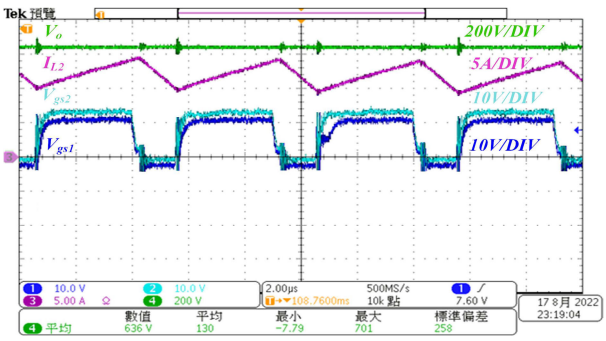

FIGURE 18. Experimental waveforms (V_O, I_{L2}, V_{gs1}, V_{gs2}) of high gain boost at $D = 0.7$, $V_{in} = 36$ V, $V_{out} = 636$ V.

of 1000 W/m^2 and a temperature of 25 degrees Celsius. Subsequently, the MPPT algorithm utilizes the well-known perturb and observe (P&O) method [31]. It is combined with

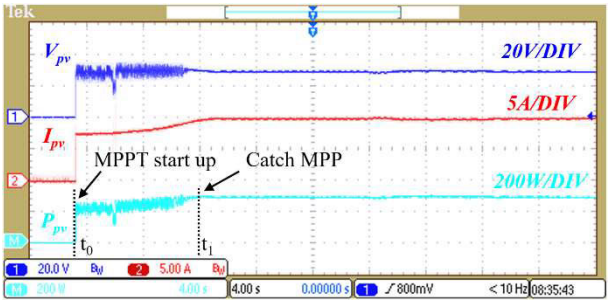

FIGURE 19. Experimental waveforms V_{pv}, I_{pv}, and P_{pv} associated with the high-gain boost in MPPT.

the proposed converter to effectively identify the maximum power point (MPP) at 300 W to ensures optimal system performance.

The graph depicted in Figure 20 illustrates how efficiency changes with output power while maintaining a constant load resistance. The efficiency of a proposed converter ranges in between 92.5 % to 94.5 %.

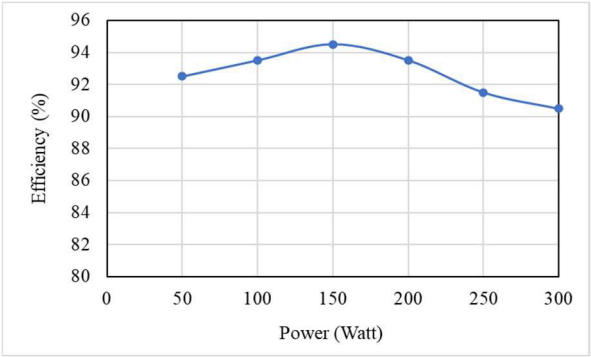

FIGURE 20. Efficiency curve.

VI. CONCLUSION

The proposed converter can generate a voltage gain of more than 12 times at a duty ratio of 0.6. The converter does not incorporate a coupled inductor, which minimizes the probability of electromagnetic interference, reduces losses, and leads to a more lightweight converter. This design features a simple structure and high efficiency of around 94.5 % at 24 V input voltage. These characteristics make it suitable for a variety of medium-high power applications. Following a comprehensive steady-state analysis, a hardware prototype of the proposed model was constructed, including the proper design of all components and PCB layout. The high-gain boost converter is crucial for renewable energy systems by efficiently increases the voltage level from renewable sources. This enhancement facilitates the effective storage and utilization of the generated energy. This elevated voltage is essential for grid integration or battery storage systems to ensure a stable energy supply. The proposed converter can be integrated into renewable systems to optimize energy usage and serve as a cornerstone for sustainable power generation. The proposed model outperforms previously presented boost topologies regarding the number of required components,

voltage gain, and switch voltage stress over a wide range of duty cycles. Future research will improve the system's performance by integrating the suggested high-gain converter with various optimal control algorithms.

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