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RESEARCH ARTICLE

Novel Control Scheme of Three-Phase Six-Level Hybrid Flying-Capacitor Inverters With Self-Balancing Capability

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ABSTRACT In this paper, a novel control scheme is proposed for the recently developed six-level hybrid flying-capacitor inverter. In the conventional scheme, an auxiliary balancing circuit is required to regulate the voltages of split DC-link capacitors. This results in the increased device count and converter volume, and thus diminishes the competitiveness of this topology. In order to eliminate these auxiliary components, a novel control scheme is proposed based on zero-sequence voltage (ZSV) injection to the phase-shifted modulation voltages. This method has enabled a simultaneous control of all split DC-link and flying capacitor voltages through the regulation of closely-linked key parameters affecting these voltages, resulting in the self-balancing capability with low voltage ripples (lower than 10 % of the references). The proposed technique has been verified with simulation and experimental results.

INDEX TERMS Capacitor voltage balancing, high-power converter, multilevel converter, six-level hybrid-clamped inverter, zero-sequence voltage injection.

I. INTRODUCTION

Over the past few decades, the advancement of various medium-voltage (MV) and high-voltage (HV) applications such as motor drives, photovoltaic inverters, and grid-connected converters has been significantly supported by high-power multilevel converters [1], [2], [3], [4], [5], [6], [7], [8], [9]. Since these converters possess inherent benefits of improved power quality, lower voltage stress at switching device, and alleviated electromagnetic interference, numerous researches have been conducted to reduce the device count [10], [11], [12]. For instance, the widely-recognized five-level hybrid active neutral-point-clamped (5L-ANPC) inverter was developed based on the predecessor three-level active neutral-point-clamped (3L-ANPC) and three-level flying-capacitor (3L-FC) inverters. This hybrid ANPC structure requires significantly less components compared to the 5L-P2 inverter and the generalized 5L-ANPC, which is also known as multilevel active-clamped (5L-MAC) inverter [13], [14], [15], [16]. Other topology which stems from the NPC and offers competitive device count is the five-level nested neutral-point-clamped (5L-NNPC) inverter [17]. This structure requires less number of active switches as a tradeoff for the higher amount of flying capacitors compared to the 5L-ANPC type.

One of the most recent topologies recently emerging due to the extensibilities to higher number of level is the (HC) hybrid-clamped inverter. This structure has been developed for four-level (4L-HC), five-level (5L-HC), and six-level (6L-HC) inverters [18], [19], [20], [21]. These HC inverters provide competitive number of switches compared to the aforementioned 5L-ANPC, each of which sustains the same blocking voltage. Moreover, unlike the hybrid ANPC structure which is only extensible to odd number of level, this topology can be extended to any higher number of level by adding the FC units at each phase leg.

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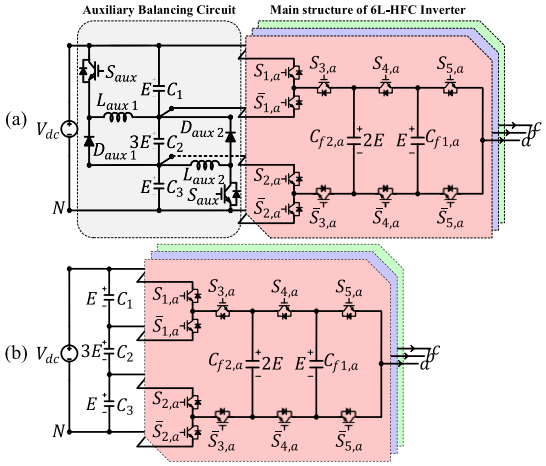

FIGURE 1. Structures of three-phase 6L-HFC inverters. (a) With auxiliary balancing circuit. (b) Without auxiliary balancing circuit.

One of the topologies that stems from the HC structure is the six-level flying capacitor based (6L-FCB) inverter, where the 4L-HC inverter has been modified and hybridized with the nested-multilevel characteristic to generate six-level output voltages [22]. This combination is particularly beneficial for circumventing the complexity of voltage regulation caused by the multiple split DC-link capacitors.

Another topology, which also resembles the structure of HC inverter, is the hybrid flying-capacitor (HFC) inverter. Since the earliest development stage, the five-level (5L-HFC) inverter has emerged as a preferable solution for high-power medium-voltage applications, particularly in industrial variable-speed drive (VSD) systems. Subsequently, the six-level (6L-HFC) inverter was proposed to improve power quality compared to the five-level counterpart, address the absence of even-level inverters in the ANPC framework, and offer an alternative with a reduced device count compared to the HC structure [23], [24]. While the 6L-HC inverter necessitates three non-uniform (FC) units per phase leg, the alternative 6L-HFC inverter stands out by requiring only two such units per phase leg. However, the 6L-HFC inverter heavily relies on an external circuit dedicated to regulating the voltages of the split DC-link capacitors (SC) during operation. This additional balancing circuit diminishes the competitiveness of this topology, leading to a significantly higher device count and larger physical size needed to achieve the same number of levels.

In this paper, a novel operating technique is proposed based on the injection of zero-sequence voltage (ZSV) to the PS-PWM modulation voltage references. This control scheme is constructed by taking into consideration the key components affecting the voltage fluctuation at each of the split DC-link capacitors (SC) and flying capacitors (FC). With this technique, the inverter possesses the inherent capability to control all of the aforementioned voltages simultaneously, and thus eliminates the requirement of any auxiliary balancing circuit. The effectiveness of this proposed technique is verified under various conditions through simulation results and validated with a downscaled 6L-HFC inverter prototype.

TABLE 1. Comparison of three-phase six-level inverters with uniform and non-uniform voltage ratings of devices.

Topology	Component (Uniform | Non-Uniform)							
	SW		CD		SC		FC	
6L-NPC	30	30	60	24	5	5	0	0
6L-FC	30	30	0	0	5	1	30	12
6L-P2 ^{AUX}	90	90	0	0	5	5	30	30
6L-MAC ^{AUX}	90	90	0	0	5	5	0	0
6L-NNPC	30	30	2	2	5	1	27	4
6L-FCB	36	30	0	0	5	1	12	12
6L-HC	36	36	0	0	5	3	18	9
6L-HFC ^{AUX}	36	30	0	0	5	3	9	6

- *SW* : Active switches.
- *CD* : Clamped diodes.
- *SC* : Split DC-link capacitors.
- *FC* : Flying capacitors.
- *AUX* : Requiring auxiliary balancing circuit.

TABLE 2. Available switching states for 6L-HFC inverter.

Switching States					v_{xN}	V_{kl}	SC/FC Currents				
$S_{1,x}$	$S_{2,x}$	$S_{3,x}$	$S_{4,x}$	$S_{5,x}$			a	b	c	d	e
0	0	0	0	0	0	$V_{01}{}^{*}$	∘	∘	∘	∘	∘
1	0	0	0	0	0	V_{02}	∘	∘	∘	∘	∘
0	0	0	0	1	E	$V_{11}{}^{*}$	∘	∘	∘	∘	↑
0	0	0	1	0	E	$V_{12}{}^{*}$	∘	∘	∘	↑	↓
0	1	0	0	0	E	$V_{13}{}^{*}$	∘	∘	↑	∘	∘
1	0	0	0	1	E	V_{14}	∘	∘	∘	∘	↑
1	0	0	1	0	E	V_{15}	∘	∘	∘	↑	↓
1	1	0	0	0	E	V_{16}	∘	∘	↑	∘	∘
0	0	0	1	1	$2E$	$V_{21}{}^{*}$	∘	∘	∘	↑	∘
0	0	1	0	0	$2E$	V_{22}	∘	↑	↑	↓	∘
0	1	0	0	1	$2E$	$V_{23}{}^{*}$	∘	∘	↑	∘	↑
0	1	0	1	0	$2E$	$V_{24}{}^{*}$	∘	∘	↑	↑	↓
0	1	1	0	0	$2E$	$V_{25}{}^{*}$	∘	↑	↑	↓	∘
1	0	0	1	1	$2E$	V_{26}	∘	∘	∘	↑	∘
1	1	0	0	1	$2E$	V_{27}	∘	∘	↑	∘	↑
1	1	0	1	0	$2E$	V_{28}	∘	∘	↑	↑	↓
0	0	1	0	1	$3E$	V_{31}	∘	↑	↑	↓	↑
0	0	1	1	0	$3E$	V_{32}	∘	↑	↑	∘	↓
0	1	0	1	1	$3E$	$V_{33}{}^{*}$	∘	∘	↑	↑	∘
0	1	1	0	1	$3E$	$V_{34}{}^{*}$	∘	↑	↑	↓	↑
0	1	1	1	0	$3E$	$V_{35}{}^{*}$	∘	↑	↑	∘	↓
1	0	1	0	0	$3E$	V_{36}	↑	↑	↑	↓	∘
1	1	0	1	1	$3E$	V_{37}	∘	∘	↑	↑	∘
1	1	1	0	0	$3E$	$V_{38}{}^{*}$	↑	↑	↑	↓	∘
0	0	1	1	1	$4E$	V_{41}	∘	↑	↑	∘	∘
0	1	1	1	1	$4E$	$V_{42}{}^{*}$	∘	↑	↑	∘	∘
1	0	1	0	1	$4E$	V_{43}	↑	↑	↑	↓	↑
1	0	1	1	0	$4E$	V_{44}	↑	↑	↑	∘	↓
1	1	1	0	1	$4E$	$V_{45}{}^{*}$	↑	↑	↑	↓	↑
1	1	1	1	0	$4E$	$V_{46}{}^{*}$	↑	↑	↑	∘	↓
1	0	1	1	1	$5E$	V_{51}	↑	↑	↑	∘	∘
1	1	1	1	1	$5E$	$V_{52}{}^{*}$	↑	↑	↑	∘	∘

0/1 : Switch is turned-off / turned-on.
$*$: Switching state is utilized in PD scheme.
∘ : No current flows through the capacitor ($i_x > 0$).
↑/↓ : Current discharges/charges the capacitor ($i_x > 0$).
$a/b/c/d/e$: $i_{C1,x}/i_{C2,x}/i_{C3,x}/i_{f2,x}/i_{f1,x}$.

II. OPERATING PRINCIPLE OF 6L-HFC INVERTERS

A. CIRCUIT CONFIGURATION

The conventional structure of three-phase 6L-HFC inverter is illustrated in Fig. 1(a). In this topology, each phase leg shares the same three split DC-link capacitor (SC) voltages, namely C_1, C_2, and C_3. If the base voltage is $E = V_{dc}/5$, the

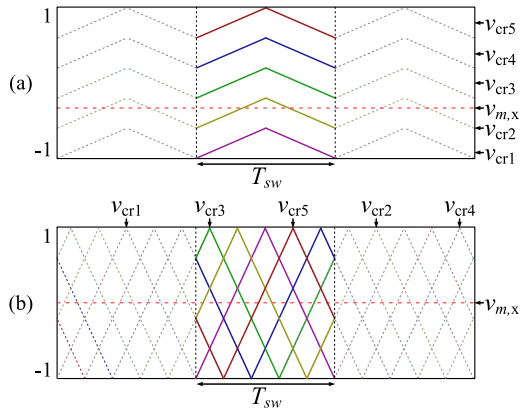

FIGURE 2. Modulation schemes for 6L-HFC inverter. (a) Conventional PD-PWM scheme. (b) Ideal PS-PWM scheme.

aforementioned capacitors should be controlled at E, $3E$, and E, respectively. Meanwhile, two flying capacitors (FC) are placed at each phase, namely $C_{f1,x}$ and $C_{f2,x}$, each of which is controlled at E and $2E$, respectively. The main inverter structure is comprised by five pairs of complementary active switches, most of which have the blocking voltages of E, whereas those of S_{3x} and $\bar{S}_{3x}$ are $2E$. With these features, this topology is considered as one of the six-level inverters with the least number of devices. The comparison of various six-level inverters in three-phase configuration, including the 6L-NPC, 6L-FC, 6L-P2, 6L-MAC, 6L-NNPC, 6L-HC, and the 6L-HFC inverters, is summarized in Table 1 based on the device count and the necessity of using external balancing circuit for regulating the SC voltages [25], [26], [27], [28], [29], [30]. The voltage rating of each device has also been taken into account by comparing both the uniform and non-uniform scenarios.

While the FC voltages of the 6L-HFC inverter are controlled through the redundancy of switching states, the regulation of SC voltages still requires an auxiliary balancing circuit which is comprised of two active switches, two diodes, and two inductors, resulting in higher device count and increased system volume.

B. ESTABLISHED PD-PWM OPERATING SCHEME

In the conventional structure, the 6L-HFC inverter is controlled with phase-disposition PWM (PD-PWM) scheme [23], [31]. Suppose that a modulation voltage denoted by $v_{m,x}$ is defined as follows:

$$\begin{cases} v_{m,x} = m_a \cos\left(r_f \omega_0 t + \delta_x\right) \\ m_a = \hat{V}_{m,x} \big/ \hat{V}_{cr} \\ r_f = f_{m,x} \big/ f_0, \end{cases} \tag{1}$$

where the amplitude modulation index, frequency ratio, fundamental angular operating frequency, and the initial phase angle are denoted by m_a, r_f, ω_0, and δ_x, respectively. Note that m_a is determined by the peak values of the actual modulating signal ($\hat{V}_{m,x}$) and carrier waves ($\hat{V}_{cr}$), whereas r_f is the ratio between the actual operating frequency ($f_{m,x}$) and the rated operating frequency (f_0). Both m_a and r_f should be kept within the linear range from 0 to 1. In this scheme, $v_{m,x}$ is compared with five carriers, namely v_{cr1}, v_{cr2}, v_{cr3}, v_{cr4}, and v_{cr5}, to determine the switching status of each device, as shown in Fig. 2(a).

TABLE 3. Redundant switching states pair in PD-PWM scheme.

Conditions			Pair
$v_{m,x}$	$Sig_{f1,x}$	$Sig_{f2,x}$	
$-1 \le v_{m,x} < -0.6$	1	~	$V_{01} \leftrightarrow V_{11}$
	-1	1	$V_{01} \leftrightarrow V_{12}$
	Other conditions		$V_{01} \leftrightarrow V_{13}$
$-0.6 \le v_{m,x} < -0.2$	1	~	$V_{11} \leftrightarrow V_{23}$
	-1	1	$V_{12} \leftrightarrow V_{24}$
	~	1	$V_{13} \leftrightarrow V_{21}$
	~	-1	$V_{13} \leftrightarrow V_{25}$
$-0.2 \le v_{m,x} < 0.2$	1	-1	$V_{23} \leftrightarrow V_{34}$
	-1	1	$V_{24} \leftrightarrow V_{35}$
	~	1	$V_{21} \leftrightarrow V_{33}$
	~	-1	$V_{25} \leftrightarrow V_{38}$
$0.2 \le v_{m,x} < 0.6$	1	-1	$V_{34} \leftrightarrow V_{45}$
	-1	~	$V_{35} \leftrightarrow V_{46}$
	~	1	$V_{33} \leftrightarrow V_{42}$
	~	-1	$V_{38} \leftrightarrow V_{42}$
$0.6 \le v_{m,x} \le 1$	1	-1	$V_{45} \leftrightarrow V_{51}$
	-1	~	$V_{46} \leftrightarrow V_{51}$
	Other conditions		$V_{42} \leftrightarrow V_{51}$

~ : Undefined condition.

Among the 32 available switching states (V_{kl}) listed in Table 2, only 16 switching states are used in order to minimize the voltage stress of each device and lower the amount switching transitions. When the inverter is operated with the conventional PD-PWM scheme, the instantaneous output voltage at each phase leg, namely v_{xN}, is determined by the device switching status, as follows:

$$v_{xN} = \left(S_{1,x} + S_{2,x} + S_{3,x} + S_{4,x} + S_{5,x}\right) \frac{V_{dc}}{5} = \sum_{i=1}^{5} S_{i,x} E. \tag{2}$$

Eq. (2) shows that v_{xN} is affected by the summation of the main switching states.

C. VOLTAGE CONTROL SCHEME FOR SPLIT DC-LINK CAPACITORS (SC) AND FLYING CAPACITORS (FC)

Since the PD-PWM carriers are elevated in the same phase, the switch duty ratios exhibit various values within one switching period (T_{sw}) [32], [33]. Due to the wide difference between the duty ratios, regulating the neutral-point currents, which affect the SC voltages, becomes a more difficult task.

Unlike the FC voltages, which can be more flexibly controlled through the redundant switching states, the SC voltages are controlled with an auxiliary balancing circuit due to the lack of switching redundancy for these capacitors. This external circuit consists of active switches, diodes, and inductors, as illustrated in Fig. 1(a), each of which contributes to the increased device count and volume of the inverter compared to the other multilevel counterparts [23].

Generally, the ripple of each capacitor voltage should be regulated within ±10 % of the reference [34], [35]. The

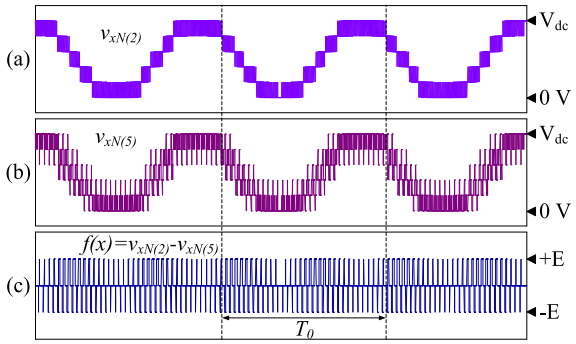

FIGURE 3. Output voltages. (a) Conventional PD-PWM scheme. (b) PS-PWM scheme. (c) Mismatch between both schemes.

regulation of FC voltages is realized by using the *signum* function of capacitor voltages, and output currents to determine the proper switching states, as follows:

$$Sig_{f1,x} = \text{sgn}\left[\left(v_{f1,x} - 0.2V_{dc}\right) i_x\right], \tag{3}$$
$$Sig_{f2,x} = \text{sgn}\left[\left(v_{f2x} - 0.4V_{dc}\right) i_x\right], \tag{4}$$

where the *signum* functions $Sig_{f1,x}$ and $Sig_{f2,x}$ signify the balance state of both the outermost and innermost capacitors at each phase leg, whereas i_x, $v_{f1,x}$, and $v_{f2,x}$ denote the output currents and corresponding FC voltages. With these parameters, the proper switching states can be assigned to counter the voltage deviation.

Due to the numerous possible scenarios of FC voltage imbalance, the balancing scheme is simplified by matching the switching states with most resembling effects. Therefore, 18 unique scenarios have been selected based on the aforementioned *signum* functions as listed in Table 3.

III. PROPOSED SELF-BALANCING CONTROL SCHEME

As mentioned in the previous section, the 6L-HFC inverter relies on the auxiliary balancing circuit to maintain each of the SC voltages. In order to eliminate this circuit, a novel operating scheme is herein proposed based on the injection of zero-sequence voltage (ZSV) to the phase-shifted PWM (PS-PWM) modulation voltage, and hence it is called the ZSV-injection-based PS-PWM (ZSVPS-PWM).

A. PROPOSED OPERATING SCHEME (ZSVPS-PWM)

The phase-shifted carrier waves for the six-level inverter operation are illustrated in Fig. 2(b). Each carrier is shifted by 72° from the other. During normal operation, when all capacitor voltages are assumed to be constant, the modulation voltage, $v_{m,x}$, is compared with each carrier to determine the switching status of each switch [36], [37], [38].

In the proposed scheme, all of the 32 switching states, as listed in Table 2, are fully utilized. As a result, the instantaneous output voltage at each phase leg should be redefined as follows:

$$v_{xN} = \left[\left(S_{1,x} - S_{2,x} + 2\right)\left(S_{3,x}\right) + \left(S_{2,x} + S_{4,x} + S_{5,x}\right)\right] E. \tag{5}$$

This consequently leads to the increased voltage stress at $S_{3,x}$ and $\bar{S}_{3,x}$ from $2E$ to $3E$, whereas those of the other switch pairs are kept at E.

If all SC and FC voltages are assumed to be constant and the switching frequency (f_{sw}) is significantly higher than the fundamental operating frequency (f_0), the modulation voltage reference can be seen a constant linear wave within a carrier period. If the normalized modulation reference is denoted by $v^*_{m,x}$, the duty ratio of each switch can be expressed as follows:

$$v^*_{m,x} = 0.5\left(v_{m,x} + 1\right), \tag{6}$$
$$d_{1,x} = d_{2x} = d_{3x} = d_{4x} = d_{5x} = v^*_{m,x}. \tag{7}$$

The average output voltage at each phase over a carrier cycle can be approximated based on (2) as follows:

$$u_x = \left(d_{1,x} + d_{2,x} + d_{3,x} + d_{4,x} + d_{5,x}\right) E = v^*_{m,x} V_{dc}, \tag{8}$$

where u_x denotes the average output voltage at each phase leg. Note that such an approximation is not identical to that of the PS-PWM in (5), resulting in the presence of output voltage spikes. Switching states in Table 2 which do not comply with (2) generate errors at v_{xN}. For instance, some switching states generate one level higher, i.e., V_{02}, V_{14}, V_{15}, V_{16}, V_{26}, V_{27}, and V_{28}, while the others generate one level lower, i.e., V_{22}, V_{31}, V_{32}, V_{36}, V_{41}, V_{43}, V_{44}, and V_{51}. This phenomenon is illustrated in Fig. 3, where the mismatch between both v_{xN} values is shown to vary among E, 0, and $-E$. These voltage spikes are generated by the deviance at either $S_{1,x}$ or $S_{2,x}$, resulting in similar current patterns at SC and FC with those of the corresponding counterparts, e.g., V_{23} and V_{27}. Moreover, the amount of those with one-level higher voltage step is equal to those with one-level lower voltage step, which merely contributes to the average value of output voltage. Therefore, applying PS-PWM scheme with (5) as the modulation voltage reference does not affect the controllability of SC and FC voltages despite the increased harmonic distortion at output voltages.

B. CONTROL OF SC AND FC VOLTAGES

Regulating the switches surrounding the FCs is the key to controlling the FC voltages since it affects the current flowing out of $C_{f1,x}$ and $C_{f2,x}$, namely $i_{f1,x}$ and $i_{f2,x}$, respectively. The instantaneous values of these currents can be expressed as follows:

$$i_{f1,x} = \left(S_{5,x} - S_{4,x}\right) i_x, \tag{9}$$
$$i_{f2,x} = \left(S_{4,x} - S_{3,x}\right) i_x. \tag{10}$$

From (9) and (10), the average FC currents during one carrier cycle, namely $\bar{i}_{f1,x}$ and $\bar{i}_{f2,x}$, can be obtained as follows:

$$\bar{i}_{f1,x} = \left(d_{5,x} - d_{4,x}\right) i_x, \tag{11}$$
$$\bar{i}_{f2,x} = \left(d_{4,x} - d_{3,x}\right) i_x. \tag{12}$$

Note that under ideal condition, the duty ratios of these surrounding switches are equal to the common normalized

modulation reference, as expressed in (7). However, (11) and (12) show how the direction and magnitude of these FC currents can be controlled by varying the corresponding duty ratios. Meanwhile, the voltage ripple of each FC in one carrier cycle (T_{sw}), namely $\Delta u_{f1,x}$ and $\Delta u_{f2,x}$, can be approximated as follows:

$$\Delta u_{f1,x} = -\frac{\bar{i}_{f1,x} T_{sw}}{C_{f1,x}} = -\frac{T_{sw}}{C_{f1,x}} \left(d_{5,x} - d_{4,x}\right) i_x, \tag{13}$$

$$\Delta u_{f2,x} = -\frac{\bar{i}_{f2x} T_{sw}}{C_{f2,x}} = -\frac{T_{sw}}{C_{f2,x}} \left(d_{4,x} - d_{3,x}\right) i_x. \tag{14}$$

Therefore, in order to maintain the FC voltages at the reference values, the aforementioned duty ratios should be adjusted according to the magnitude of the voltage ripple and the direction of the output current at each phase leg. For instance, when $\Delta u_{f1,x} > 0$ and $i_x > 0$, a positive offset should be applied as a countermeasure to the overcharged capacitor voltage. This adjustment can be applied by increasing the duty ratio of $S_{5,x}$ by $\Delta d_{f1,x}$. In order to alleviate the effect of this action on the output voltage, the duty ratio at each of the other main switches should be evenly decreased by $\Delta d_{f1,x}/4$. As a result, the new duty ratios denoted by $d_{1f1,x}$–$d_{5f1,x}$ are set as follows:

$$\begin{bmatrix} d_{1f1,x} \\ d_{2f1,x} \\ d_{3f1,x} \\ d_{4f1,x} \\ d_{5f1,x} \end{bmatrix} = \begin{bmatrix} d_{1,x} - \Delta d_{f1,x}/4 \\ d_{2,x} - \Delta d_{f1,x}/4 \\ d_{3,x} - \Delta d_{f1,x}/4 \\ d_{4,x} - \Delta d_{f1,x}/4 \\ d_{5,x} + \Delta d_{f1,x} \end{bmatrix}. \tag{15}$$

Meanwhile, when $\Delta u_{f2,x} > 0$ and $i_x > 0$, a positive offset of $\Delta d_{f2,x}/2$ is added to each of the duty ratios of $S_{4,x}$ and $S_{5,x}$, whereas those of the other switches are evenly decreased by $\Delta d_{f2,x}/3$, resulting in the new duty ratios denoted by $d_{1f2,x}$–$d_{5f2,x}$ as follows:

$$\begin{bmatrix} d_{1f2,x} \\ d_{2f2,x} \\ d_{3f2,x} \\ d_{4f2,x} \\ d_{5f2,x} \end{bmatrix} = \begin{bmatrix} d_{1,x} - \Delta d_{f2,x}/3 \\ d_{2,x} - \Delta d_{f2,x}/3 \\ d_{3,x} - \Delta d_{f2,x}/3 \\ d_{4,x} + \Delta d_{f2,x}/2 \\ d_{5,x} + \Delta d_{f2,x}/2 \end{bmatrix}. \tag{16}$$

Similar approach is also applied to maintain each of the SC voltages. In this case, the objective is to control the key components that directly affect the SC currents. The currents flowing out of the top, middle, and bottom SCs, namely i_{C1}, i_{C2}, and i_{C3}, are assessed distinctively according to the contributions of all phase legs, which are denoted by $i_{C1,x}$, $i_{C2,x}$, and $i_{C3,x}$, respectively. For instance, $i_{C2,x}$ is closely linked to the top and bottom SC neutral-point currents at each phase leg, namely $i_{nu,x}$ and $i_{nl,x}$, respectively. The former current relies on the switching of $\bar{S}_{1,x}$ and $S_{3,x}$, whereas the latter one is controlled by $S_{2,x}$ and $\bar{S}_{3,x}$, as expressed in the following equation:

$$\begin{cases} i_{nu,x} = \left(1 - S_{1,x}\right)\left(S_{3,x}\right) i_x, \\ i_{nl,x} = \left(S_{2,x}\right)\left(1 - S_{3,x}\right) i_x. \end{cases} \tag{17}$$

Therefore, $i_{C2,x}$ can be regarded as the difference between $i_{nu,x}$ and $i_{nl,x}$, as follows:

$$i_{C2,x} = \left[\left(1 - S_{1,x}\right)\left(S_{3,x}\right) - \left(S_{2,x}\right)\left(1 - S_{3,x}\right)\right] i_x. \tag{18}$$

Meanwhile, the contribution of each phase leg to the middle SC voltage ripple, namely $\Delta u_{C2,x}$, can be written as follows:

$$\Delta u_{C2,x} = -\frac{\bar{i}_{C2,x} T_{sw}}{C_2}, \tag{19}$$

where $\bar{i}_{C2,x}$ is the average middle SC current during one carrier cycle. From (18) and (19), the value of $i_{C2,x}$ during positive output current tends to increase when the duty ratios of $S_{1,x}$ and $S_{2,x}$ are decreased while that of $S_{3,x}$ is increased. Therefore, when $\Delta u_{C2,x} > 0$ and $i_x > 0$, the duty ratios of the main switches can be controlled to counter the deviation and restore the middle SC voltage balance, as follows:

$$\begin{bmatrix} d_{1C2,x} \\ d_{2C2,x} \\ d_{3C2,x} \\ d_{4C2,x} \\ d_{5C2,x} \end{bmatrix} = \begin{bmatrix} d_{1,x} - \Delta d_{C2,x}/2 \\ d_{2,x} - \Delta d_{C2,x}/2 \\ d_{3,x} + \Delta d_{C2,x}/3 \\ d_{4,x} + \Delta d_{C2,x}/3 \\ d_{5,x} + \Delta d_{C2,x}/3 \end{bmatrix}, \tag{20}$$

where $d_{1C2,x}$–$d_{5C2,x}$ are the new duty ratios with respect to the addition or subtraction of the offset $\Delta d_{C2,x}$. Note that the duty ratios of $S_{4,x}$ and $S_{5,x}$ are also increased accordingly to maintain the zero sum of all voltage adjustments, and thus keep the output voltage intact.

When the middle SC voltage is maintained at the reference value, the average middle SC current can be considered as zero ($i_{C2,x} \approx 0$). As a result, the middle SC can be seen as a super node, out of which the neutral-point current (i_N) flows. The contribution of each phase leg to this current, namely $i_{N,x}$, can be expressed as follows:

$$i_{N,x} = i_{nu,x} + i_{nl,x} = i_{C3,x} - i_{C1,x}. \tag{21}$$

The contribution of each phase leg to the voltage ripple at each of the top and bottom SCs, namely $\Delta u_{C1,x}$ and $\Delta u_{C3,x}$, can be written as follows:

$$\begin{bmatrix} \Delta u_{C1,x} \\ \Delta u_{C3,x} \end{bmatrix} = \begin{bmatrix} -\bar{i}_{C1,x} T_{sw}/C_1 \\ -\bar{i}_{C3,x} T_{sw}/C_3 \end{bmatrix}, \tag{22}$$

where $\bar{i}_{C1,x}$ and $\bar{i}_{C3,x}$ denote the average value of top and bottom SC currents during one carrier cycle, respectively. Therefore, the average value of neutral-point current at each phase leg, which is denoted by $\bar{i}_{N,x}$, is obtained as follows:

$$\bar{i}_{N,x} = \left(\bar{i}_{C3,x} - \bar{i}_{C1,x}\right) = \frac{C_{eq}}{T_{sw}} \left(\Delta u_{C1,x} - \Delta u_{C3,x}\right), \tag{23}$$

where C_{eq} is equal to C_1, C_3, and $C_{f1,x}$. Note that the capacitances of middle SC and innermost FCs are set inversely proportional to the voltages, where $C_2 = C_{eq}/3$ and $C_{f2,x} = C_{eq}/2$.

When the bottom SC voltage exceeds that of the top SC ($v_{C3} > v_{C1}$) during positive output current, the value of $\bar{i}_{N,x}$ should be increased to enlarge the gap between $\Delta u_{C1,x}$ and $\Delta u_{C3,x}$, and thus restore the voltage balance between

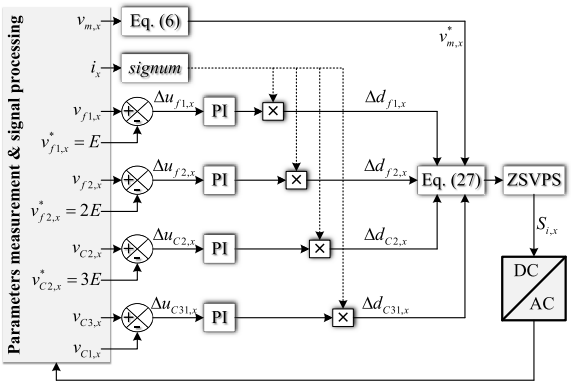

FIGURE 4. Control block diagram of the ZSVPS-PWM scheme.

these SC voltages. From (17), (18), and (21), the switching of $S_{3,x}$ and $\bar{S}_{3,x}$ is particularly reserved for regulating the middle SC voltage. Therefore, $\bar{i}_{N,x}$ can be increased more straightforwardly by injecting an offset voltage to $d_{2,x}$ and simultaneously reducing $d_{1,x}$ by the same value, as expressed in the following equation:

$$\begin{bmatrix} d_{1C31,x} \\ d_{2C31,x} \\ d_{3C31,x} \\ d_{4C31,x} \\ d_{5C31,x} \end{bmatrix} = \begin{bmatrix} d_{1,x} \\ d_{2,x} \\ d_{3,x} \\ d_{4,x} \\ d_{5,x} \end{bmatrix} + \begin{bmatrix} -\Delta d_{C31,x} \\ \Delta d_{C31,x} \\ 0 \\ 0 \\ 0 \end{bmatrix}, \tag{24}$$

where $d_{1C31,x}$–$d_{5C31,x}$ are the updated duty ratios with regard to the injection of the offset voltage, $\Delta d_{C31,x}$.

From the aforementioned discussion, it can be concluded that some offset voltages need to be injected in order to maintain the balance at all SC and FC voltages while keeping the output voltage intact, as illustrated previously in Fig. 3(b). Each of the updated duty ratios comprises the initial value, which is equal to the normalized modulation voltage, and the corresponding offset voltages. For simplification, the updated duty ratios can be summarized as follows:

$$d^*_{i,x} = d_{i,x} + \Delta d_{i,x} = v^*_{m,x} + \Delta d_{i,x} (i = 1, \ldots, 5), \tag{25}$$

where $d_{i,x}$, $\Delta d_{i,x}$, $d^*_{i,x}$ denote the initial duty ratio, the offset voltage, and the updated duty ratio of switch $S_{i,x}$, respectively, which embody the parameters expressed in (15)–(16), (20), and (24). The value of $\Delta d_{i,x}$ for each switch $S_{i,x}$ can be expressed as follows:

$$\begin{bmatrix} \Delta d_{1,x} \\ \Delta d_{2,x} \\ \Delta d_{3,x} \\ \Delta d_{4,x} \\ \Delta d_{5,x} \end{bmatrix} = \begin{bmatrix} -\Delta d_{f1,x}/4 - \Delta d_{f2,x}/3 - \Delta d_{C2,x}/2 - \Delta d_{C31,x} \\ -\Delta d_{f1,x}/4 - \Delta d_{f2,x}/3 - \Delta d_{C2,x}/2 + \Delta d_{C31,x} \\ -\Delta d_{f1,x}/4 - \Delta d_{f2,x}/3 + \Delta d_{C2,x}/3 \\ -\Delta d_{f1,x}/4 + \Delta d_{f2,x}/2 + \Delta d_{C2,x}/3 \\ \Delta d_{f1,x} + \Delta d_{f2,x}/2 + \Delta d_{C2,x}/3 \end{bmatrix}. \tag{26}$$

TABLE 4. Simulation parameters.

Parameters	Value
DC-bus voltage	$V_{dc} = 7000$ V
DC-link capacitors	$C_1 = C_3 = 2.5$ mF, $C_2 = 0.83$ mF
Flying capacitors	$C_{f1,x} = 2.5$ mF, $C_{f2,x} = 1.25$ mF
Fundamental frequency	$f_0 = 60$ Hz
Carrier frequency	$f_{sw} = 2000$ Hz
Dead time	$T_d = 4$ µs
Auxiliary inductors	$L_{aux1} = L_{aux2} = 0.5$ mH
RL-load	$R_{load} = 10\ \Omega$, $L_{load} = 6$ mH

As a result, an updated approximate value of the average output voltage over a carrier cycle, which is denoted by u'_x, can be expressed as follows:

$$\begin{cases} u'_x = \sum_{i=1}^{5} d^*_i E = v^*_{m,x} V_{dc} + \sum_{i=1}^{5} \Delta d_{i,x} E, \\ \sum_{i=1}^{5} \Delta d_{i,x} = 0. \end{cases} \tag{27}$$

In (27), the value of u'_x is kept intact as that of u_x in (8) due to the zero sum of all offset voltages. The control block diagram of the proposed ZSVPS-PWM scheme is illustrated in Fig. 4.

IV. SIMULATION RESULTS

In this section, the performance of a three-phase 6L-HFC inverter under the proposed scheme is verified through a number of simulations. The parameters used in the simulations are listed in Table 4.

Firstly, the steady-state performance of the 6L-HFC inverter under both the conventional PD-PWM and the proposed ZSVPS-PWM techniques are investigated. Fig. 5 shows the operation at unity modulation index and frequency ratio ($m_a = r_f = 1$) under the conventional PD-PWM scheme with an auxiliary balancing circuit, where the inductors are set at $L_{aux1} = L_{aux2} = 0.5$ mH. Each of the pole voltage, line-to-line voltage, and output currents reaches the maximum number of level and amplitude, as shown in Fig. 5(a)–(c). The THD values of these waveforms are 22.47 %, 14.10 %, and 1.25 %, respectively. Meanwhile, all of the SC and FC voltages are controlled with low ripples, each of which is controlled within the allowable range (20 % of the corresponding reference). In this case, the peak-to-peak voltage ripples of v_{C1}, v_{C2}, and v_{C3} are 14.52 %, 3.32 %, and 11.73 % of the corresponding references, respectively. Meanwhile, those of $v_{f1,x}$ and $v_{f2,x}$ are 2.13 % and 1.55 % of the corresponding references, respectively.

Fig. 6 shows the inverter performance when it is operated under the proposed scheme, where the balancing circuit is eliminated. In this case, the THD of pole voltage, line-to-line voltage, and output currents are 40.48 %, 27.90 %, and 4.38 %, respectively. Note that the pole voltage spikes shown in Fig. 6(a), which have been discussed earlier in section III-A, are acknowledged as a tradeoff for the elimination of the auxiliary circuit. Moreover, this scheme manages to regulate the SC and FC voltages with

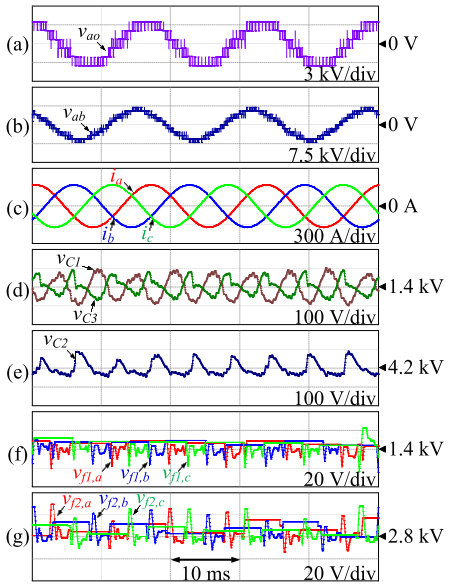

FIGURE 5. Steady-state performance under the conventional scheme. (a) Pole voltage. (b) Line-to-line voltage. (c) Output currents. (d) Top and bottom SC voltages. (e) Middle SC voltage. (f) Outermost FC voltages. (g) Innermost FC voltages.

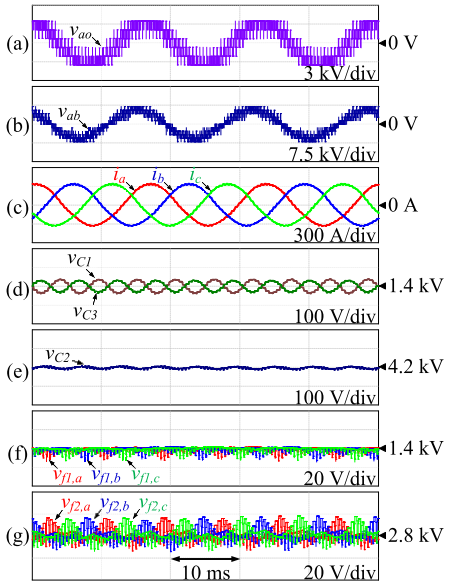

FIGURE 6. Steady-state performance under the proposed ZSVPS-PWM scheme. (a) Pole voltage. (b) Line-to-line voltage. (c) Output currents. (d) Top and bottom SC voltages. (e) Middle SC voltage. (f) Outermost FC voltages. (g) Innermost FC voltages.

lower fluctuations compared to the conventional technique, as shown in Fig. 6(d)–(g). The peak-to-peak voltage ripples of v_{C1}, v_{C2}, and v_{C3} are 5.67 %, 0.55 %, and 4.93 % of the corresponding references, respectively. Meanwhile, those of $v_{f1,x}$ and $v_{f2,x}$ are 1.12 % and 1.13 % of the corresponding references, respectively. As a result, this technique manages to keep the output voltage at each phase intact and indistinguishable from that of the ideal one, as shown previously in Fig. 3(b).

The harmonic spectra of the output voltages at unity modulation index under both schemes are shown in Fig. 7.

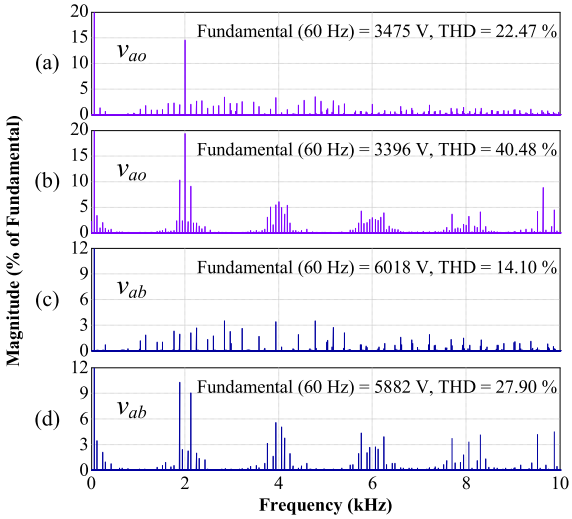

FIGURE 7. Harmonic spectra of output voltages at unity modulation index under the conventional PD-PWM scheme (PD) and the proposed ZSVPS-PWM scheme (PS). (a) Pole voltage (PD). (b) Pole voltage (PS). (c) Line voltage (PD). (d) Line voltage (PS).

The magnitude of the switching-frequency component under the conventional scheme is 14.58 % of the fundamental-frequency component. Meanwhile, that of the proposed scheme is 19.48 % of the fundamental-frequency component.

Fig. 8 shows the operation of this inverter at various modulation indices and frequency ratios under the conventional scheme. In this scenario, both m_a and m_f are gradationally increased from 0.1 to 1. The number of level at each of pole and line-to-line voltages increases accordingly, resulting in the increased amplitude of output currents, as shown in Fig. 8(a)–(c). Due to the increasing output current, the peak-to-peak ripple at each of SC and FC voltages also increases slightly, as shown in Fig. 8(d)–(g). For each stage, the voltage ripple is kept within ±10 % of the corresponding reference. For instance, the peak-to-peak ripples of v_{C1}, v_{C2}, and v_{C3} at $m_a = r_f = 1$ are 15.85 %, 4.43 %, and 16.18 % of the references, respectively. Meanwhile, those of $v_{f1,x}$ and $v_{f2,x}$ are 2.93 % and 1.52 % of the references, respectively.

Fig. 9 exhibits the performance of the inverter when the same scenario is conducted under the proposed ZSVPS-PWM scheme without auxiliary balancing circuit. In this case, each of the SC and FC voltages exhibits lower ripple compared to those of the conventional technique. The peak-to-peak ripples of v_{C1}, v_{C2}, and v_{C3} at $m_a = r_f = 1$ are 6.20 %, 0.72 %, and 5.53 % of the references, respectively. Meanwhile, those of $v_{f1,x}$ and $v_{f2,x}$ are 1.25 % and 1.21 % of the references, respectively.

Another scenario that is herein investigated is the inverter operation during sudden load change. In this case, the output power is stepped-up from approximately 10 % of the rated power ($R_{load} = 100\ \Omega$ and $p_o \approx 175$ kW) up to the rated power ($R_{load} = 10\ \Omega$ and $p_o = 1.65$ MW) before it is stepped-down to the initial condition. Fig. 10 shows the performance of this inverter under the conventional scheme. During power step-up, the amplitude of each output

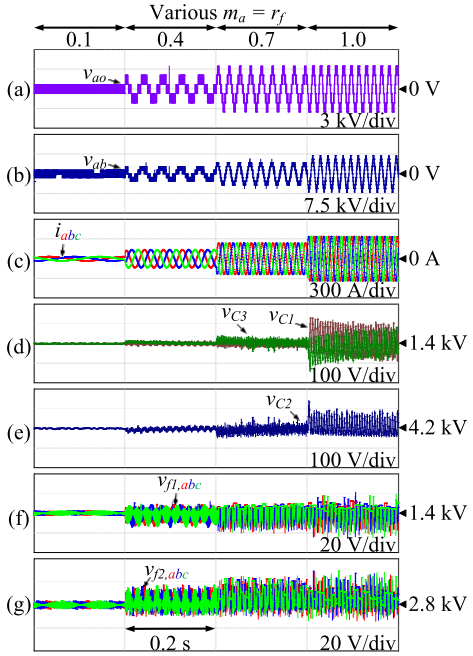

FIGURE 8. Control performance at various modulation indices and frequency ratios under the conventional scheme. (a) Pole voltage. (b) Line-to-line voltage. (c) Output currents. (d) Top and bottom SC voltages. (e) Middle SC voltage. (f) Outermost FC voltages. (g) Innermost FC voltages.

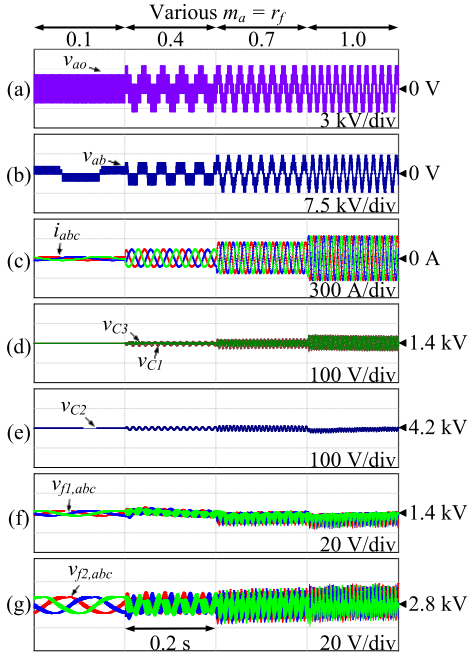

FIGURE 9. Control performance at various modulation indices and frequency ratios under the proposed ZSVPS-PWM scheme. (a) Pole voltage. (b) Line-to-line voltage. (c) Output currents. (d) Top and bottom SC voltages. (e) Middle SC voltage. (f) Outermost FC voltages. (g) Innermost FC voltages.

current increases significantly, as shown in Fig. 10(a). As a result, the SC and FC voltages exhibit more fluctuations although the ripples are still controlled within the allowable range. The highest peak-to-peak ripples of v_{C1}, v_{C2}, and v_{C3} are 16.33 %, 3.78 %, and 14.49 % of the references,

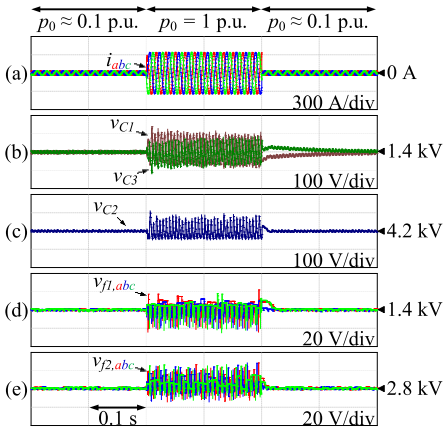

FIGURE 10. Performance during sudden load change under the conventional scheme. (a) Output currents. (b) Top and bottom SC voltages. (c) Middle SC voltage. (d) Outermost FC voltages. (e) Innermost FC voltages.

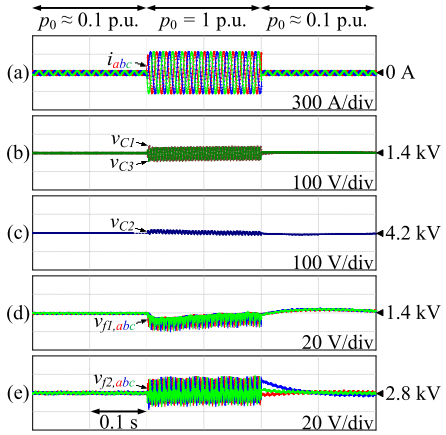

FIGURE 11. Performance during sudden load change under the proposed scheme. (a) Output currents. (b) Top and bottom SC voltages. (c) Middle SC voltage. (d) Outermost FC voltages. (e) Innermost FC voltages.

respectively, whereas those of $v_{f1,x}$ and $v_{f2,x}$ are 3.30 % and 1.51 % of the references, respectively.

When the same scenario is applied to the inverter under the proposed scheme, the controller manages to regulate the voltages with low ripples, as shown in Fig. 11. In this case, the peak-to-peak ripples of v_{C1}, v_{C2}, and v_{C3} are 6.24 %, 0.76 %, and 5.49 % of the references, respectively. Meanwhile, those of $v_{f1,x}$ and $v_{f2,x}$ are 1.71 % and 1.15 % of the references, respectively.

In order to assess the total converter volume for each of the conventional and proposed schemes, a simplified comparison based on the most fundamental components has been provided in Table 5. In this case, only the switches, gate drivers, capacitors, and inductors are considered, whereas the other supporting devices are neglected for simplicity. The auxiliary balancing circuit requires a huge space that is equal to 25.49 % of the total volume of the conventional structure. Among these auxiliary components, 88.37 % of the space is taken by the inductors. The volume ratio between the proposed and conventional structures is 74.37 %, which

TABLE 5. Volume comparison for different operating schemes.

Devices	Part Name	Rated Value	Volume / Device (mm^3)
S_{1x}, $\bar{S}_{1x}$, S_{2x}, $\bar{S}_{2x}$, S_{4x}, $\bar{S}_{4x}$, S_{5x}, $\bar{S}_{5x}$	DIM600DCM17-A000	1700 V / 600 A	691,600
S_{3x}, $\bar{S}_{3x}$ (PD)	DIM800ECM33-F000	3300 V / 800 A	1,010,800
S_{3x}, $\bar{S}_{3x}$ (PS)	5SNA 0650J450300	4500 V / 650 A	873,600
S_{aux1}, S_{aux2} (PD)	5SNA 1000G650300	6500 V / 1000 A	1,276,800
D_{aux1}, D_{aux2} [1] (PS)	DD750S65K3	6500 V / 750 A	873,600
L_{aux1}, L_{aux2} [2] (PS)	HCS-601M-500AG RB1	500 A (600 μH)	23,587
C_1, C_2, C_3, $C_{f1,x}$, $C_{f2,x}$	C44USGT-7113M33K	1500 V (1130 μF)	4,125,590
	C44USGT-7140M35K	1500 V (1400 μF)	5,069,827
Gate Driver (all)	2SC0108T	1700 V	24,696
(PD)	2SC0535T	3300 V	117,749
(PS)	1SC0450	4500 V	148,500
Total volume under PD-PWM (three-phase)			204,066,216
Total volume under ZSVPS-PWM (three-phase)			151,763,184

[1] Two diodes are set in parallel for each of D_{aux1} and D_{aux2}.
[2] Four inductors are utilized for each of L_{aux1} and L_{aux2}.

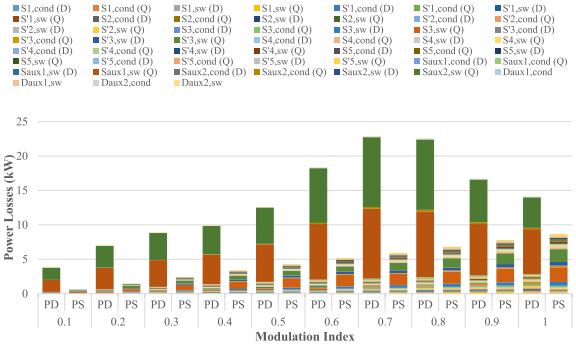

FIGURE 12. Switching and conduction losses under the conventional and proposed schemes at various modulation indices.

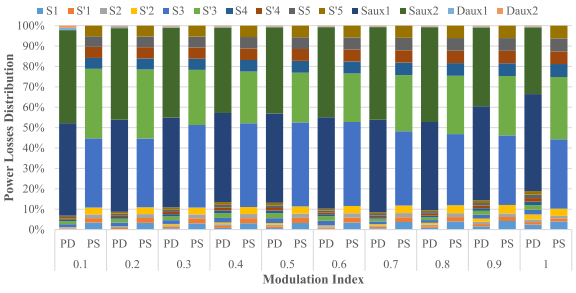

FIGURE 13. Distribution of power losses across the switches of the main inverter and the auxiliary balancing circuit.

suggests that the proposed technique offers space savings up to 25.63 %.

Fig. 12 shows the power loss comparison between both conventional and proposed schemes. The summation of switching ('sw') and conduction ('cond') losses at each of the main transistors ('Q') and anti-parallel diodes ('D') is shown for various modulation indices. The conventional scheme dissipates higher power losses at all cases due to the high switching losses at the auxiliary balancing circuit, as also

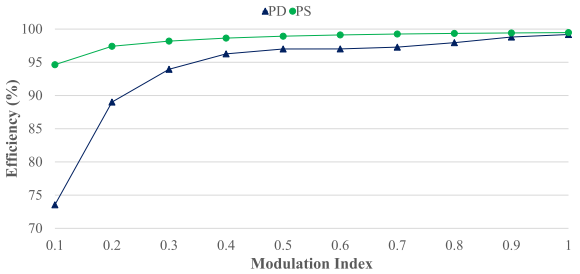

FIGURE 14. Efficiency of the inverter under the conventional and proposed schemes at various modulation indices.

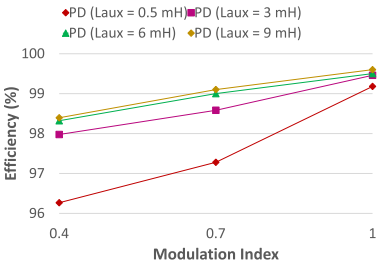

FIGURE 15. Efficiency of the inverter under the conventional scheme with various auxiliary inductor values.

exhibited in Fig. 13. The total power dissipated from the auxiliary balancing circuit ranges from 81.10 % to 93.17 % of the total power losses. As a result, the efficiency of the proposed scheme is higher than that of the conventional scheme at most of the modulation indices, as shown in Fig. 14. Note that the efficiency of the conventional scheme can be improved by significantly increasing the inductances at the auxiliary balancing circuit, as shown in Fig. 15, where each of L_{aux1} and L_{aux2} is increased from 0.5 mH to 9 mH. Due to this significant change, the current surges and fluctuation at each inductor are reduced, and thus lower the power losses dissipated in the auxiliary balancing circuit. However, this technique should be avoided since it translates into bulkier inductor size and increases the system volume.

V. EXPERIMENTAL RESULTS

In order to further validate the effectiveness of this ZSVPS-PWM scheme, an experiment has been conducted with a down-scaled parameters summarized in Table 6. Fig. 16 shows the experimental prototype of this inverter which is equipped with the detachable auxiliary balancing circuit (L_{aux} = 0.67mH). This inverter is controlled with a DSP chip (TMS320F28335) and FPGA (Xilinx XC3S400). It is noteworthy that the prototype system utilized in this experiment was not designed with a primary focus on optimizing power density since the principal objective was to validate the effectiveness of the proposed control technique. Nonetheless, the tangible benefits are clearly evident, where the removal of the auxiliary balancing circuit is approximately equivalent to reclaiming 25 % of the initially utilized space.

Firstly, the performance of the inverter prototype during steady-state condition is investigated. Fig. 17 shows the inverter operation under the conventional scheme. Note that for this particular case, the inverter is operated at slightly

TABLE 6. Experimental parameters.

Parameters	Value
DC-bus voltage	$V_{dc} = 200$ V
DC-link capacitors	$C_1 = C_3 = 2.7$ mF, $C_2 = 0.9$ mF
Flying capacitors	$C_{f1,x} = 2.7$ mF, $C_{f2,x} = 1.35$ mF
Fundamental frequency	$f_0 = 60$ Hz
Carrier frequency	$f_{sw} = 2000$ Hz
Dead time	$T_d = 4$ µs
Auxiliary inductors	$L_{aux1} = L_{aux2} = 0.67$ mH
RL-load	$R_{load} = 9.1\ \Omega$, $L_{load} = 3$ mH

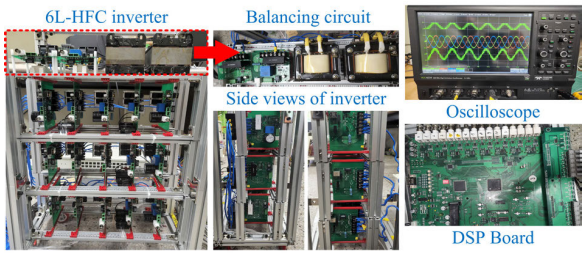

FIGURE 16. Experimental prototype of a three-phase 6L-HFC inverter with detachable auxiliary balancing circuit.

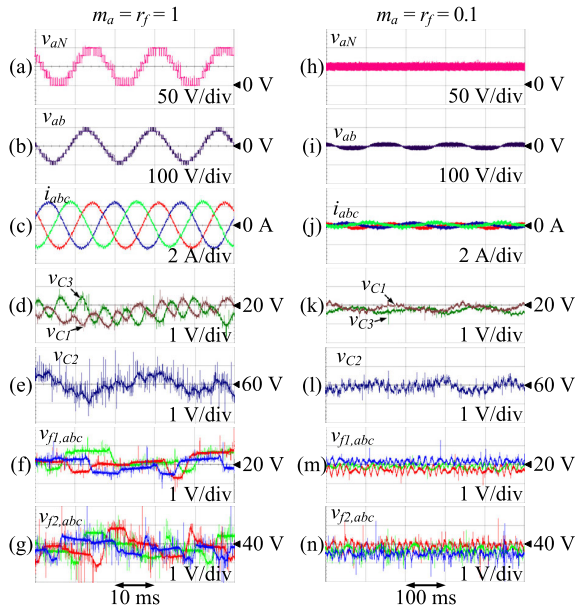

FIGURE 17. Steady-state operation of 6L-HFC inverter prototype under the conventional scheme ($m_a = r_f = k$). (a) Pole voltage ($k = 1$). (b) Line-to-line voltage ($k = 1$). (c) Output currents ($k = 1$). (d) Top and bottom SC voltages ($k = 1$). (e) Middle SC voltage ($k = 1$). (f) Outermost FC voltages ($k = 1$). (g) Innermost FC voltages ($k = 1$). (h) Pole voltage ($k = 0.1$). (i) Line-to-line voltage ($k = 0.1$). (j) Output currents ($k = 0.1$). (k) Top and bottom SC voltages ($k = 0.1$). (l) Middle SC voltage ($k = 0.1$). (m) Outermost FC voltages ($k = 0.1$). (n) Innermost FC voltages ($k = 0.1$).

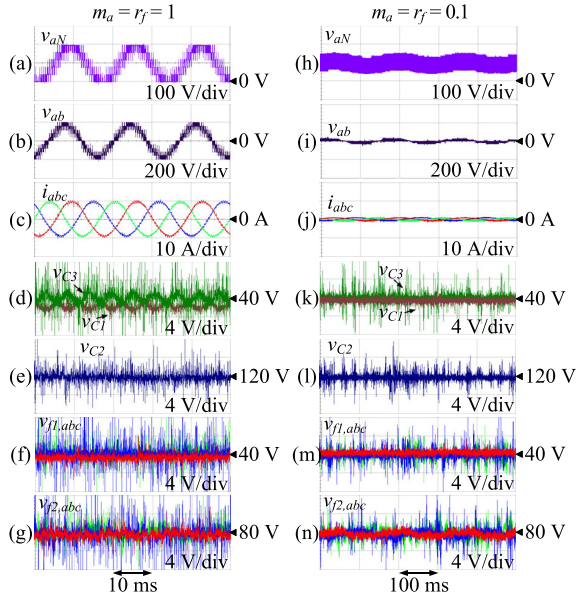

FIGURE 18. Steady-state operation of inverter prototype under the proposed ZSVPS-PWM scheme ($m_a = r_f = k$). (a) Pole voltage ($k = 1$). (b) Line-to-line voltage ($k = 1$). (c) Output currents ($k = 1$). (d) Top and bottom SC voltages ($k = 1$). (e) Middle SC voltage ($k = 1$). (f) Outermost FC voltages ($k = 1$). (g) Innermost FC voltages ($k = 1$). (h) Pole voltage ($k = 0.1$). (i) Line-to-line voltage ($k = 0.1$). (j) Output currents ($k = 0.1$). (k) Top and bottom SC voltages ($k = 0.1$). (l) Middle SC voltage ($k = 0.1$). (m) Outermost FC voltages ($k = 0.1$). (n) Innermost FC voltages ($k = 0.1$).

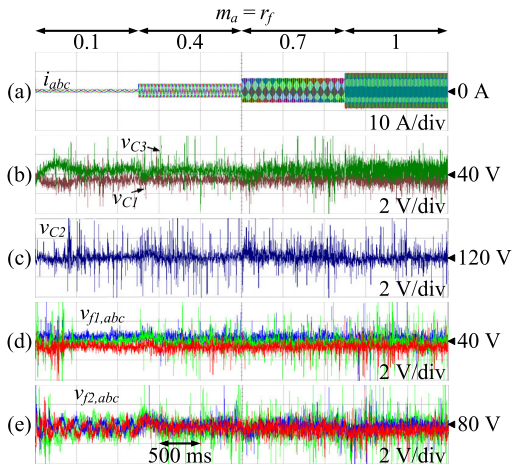

FIGURE 19. Performance of inverter prototype at various modulation indices and frequency ratios under the proposed ZSVPS-PWM scheme. (a) Output currents. (b) Top and bottom SC voltages. (c) Middle SC voltage. (d) Outermost FC voltages. (e) Innermost FC voltages.

different setup, where the V_{dc} is set at 100 V and the three-phase *RL*-load is set with $R_{load} = 20\ \Omega$, resulting in lower output power compared to the remaining experimental scenarios. When the inverter is operated at high modulation index and frequency ratio ($m_a = r_f = 1$), the output voltages and currents reach the highest amplitudes, as shown in Fig. 17(a)–(c). In this case, each of SC and FC voltages manage to be controlled at the reference values, as exhibited in Fig. 17(d)–(g). Meanwhile, when the modulation index and frequency ratio are set low ($m_a = r_f = 0.1$), the inverter generates lower output voltages and current, as shown in Fig. 17(h)(j). All of SC and FC voltages are also kept at the corresponding references, as shown in Fig. 17(k)–(n).

Fig. 18 shows the performance of the inverter under the proposed ZSVPS-PWM scheme during steady-state condition. In this case, the output voltages and currents resemble those of the simulation results in Fig. 6. Each of the SC and FC voltages manages to be controlled at the corresponding reference at both high ($m_a = r_f = 1$) and low ($m_a = r_f = 0.1$) modulation indices and frequency ratios, as shown in Fig. 18(d)–(g) and (k)–(n).

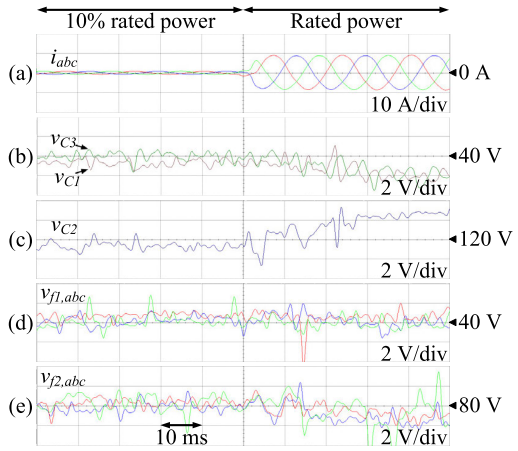

FIGURE 20. Performance of inverter prototype under the proposed ZSVPS-PWM scheme during sudden load change (step-up). (a) Output currents. (b) Top and bottom SC voltages. (c) Middle SC voltage. (d) Outermost FC voltages. (e) Innermost FC voltages.

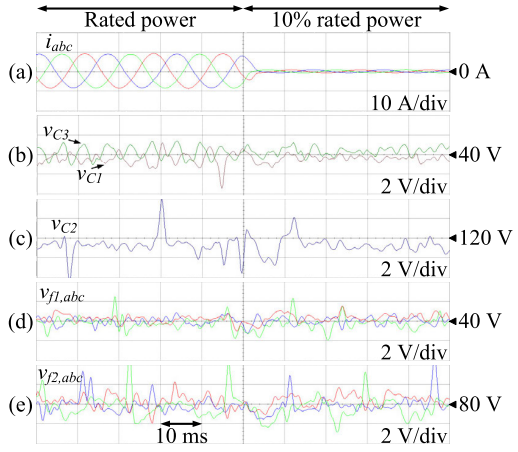

FIGURE 21. Performance of inverter prototype under the proposed ZSVPS-PWM scheme during sudden load change (step-down). (a) Output currents. (b) Top and bottom SC voltages. (c) Middle SC voltage. (d) Outermost FC voltages. (e) Innermost FC voltages.

Fig. 19 shows the inverter operation at various modulation indices and frequency ratios. In this scenario, both m_a and r_f are gradationally and simultaneously increased with the same increment from 0.1 to 1. As a result, both the amplitude and frequency of the phase currents also increase along with the output voltages. Fig. 19(b)–(e) show the SC and FC voltages, each of which is controlled at the corresponding reference within the allowable range.

Another scenario investigated herein is the performance of the inverter during sudden load change. Fig. 20 shows the output currents, SC voltages, and FC voltages at $m_a = r_f = 1$ when the output power is increased from 10 % of the rated load ($R_{load} = 100\ \Omega$) up to the rated load ($R_{load} = (100 \parallel 10)\ \Omega \approx 9.1\ \Omega, p_o = 1.378$ kW). Fig. 20(b)–(e) show how each of the SC and FC voltages manages to be kept at the corresponding reference with low ripple which is within the allowable range.

When the scenario is reversed, the inverter also exhibits similar performance under the proposed control scheme, as shown in Fig. 21. In this case, the output power is decreased from the rated load to 10 % of the rated load. Although the output currents are reduced significantly, each of the SC and FC voltages manages to be controlled at the corresponding value within the allowable range, as shown in Fig. 21(b)–(e).

VI. CONCLUSION

In this article, a novel control scheme has been proposed for the six-level hybrid flying-capacitor (6L-HFC) inverter to regulate the voltages split DC-link and flying capacitors simultaneously without requiring auxiliary balancing circuit. In this method, the key parameters affecting the balance state of each capacitor voltage have been analyzed to synthesize the proper counter measure. The current flowing through each capacitor is controlled by injecting a zero-sequence voltage (ZSV) to the modulation voltage reference at each phase leg and adjust the duty ratio of each device to keep the output voltages intact. The elimination of auxiliary balancing circuit under the proposed scheme offers space savings up to 25.63 % and enhances system efficiency by 0.29 % to 21.09 %, contingent on the modulation index. The effectiveness of the proposed control scheme in regulating the capacitor voltages with low ripple (lower than 10 % of the reference) has been verified through various simulation and experimental results.

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